ER-OLEDM1602-4

OLED Display User Manual

EastRising Technology Co., Limited

REV	DESCRIPTION	RELEASE DATE
1.0	Preliminary Release	Jun-17-2010
2.0	Preliminary Release	Jul-02-2011

Contents

1.Module Basic Specification

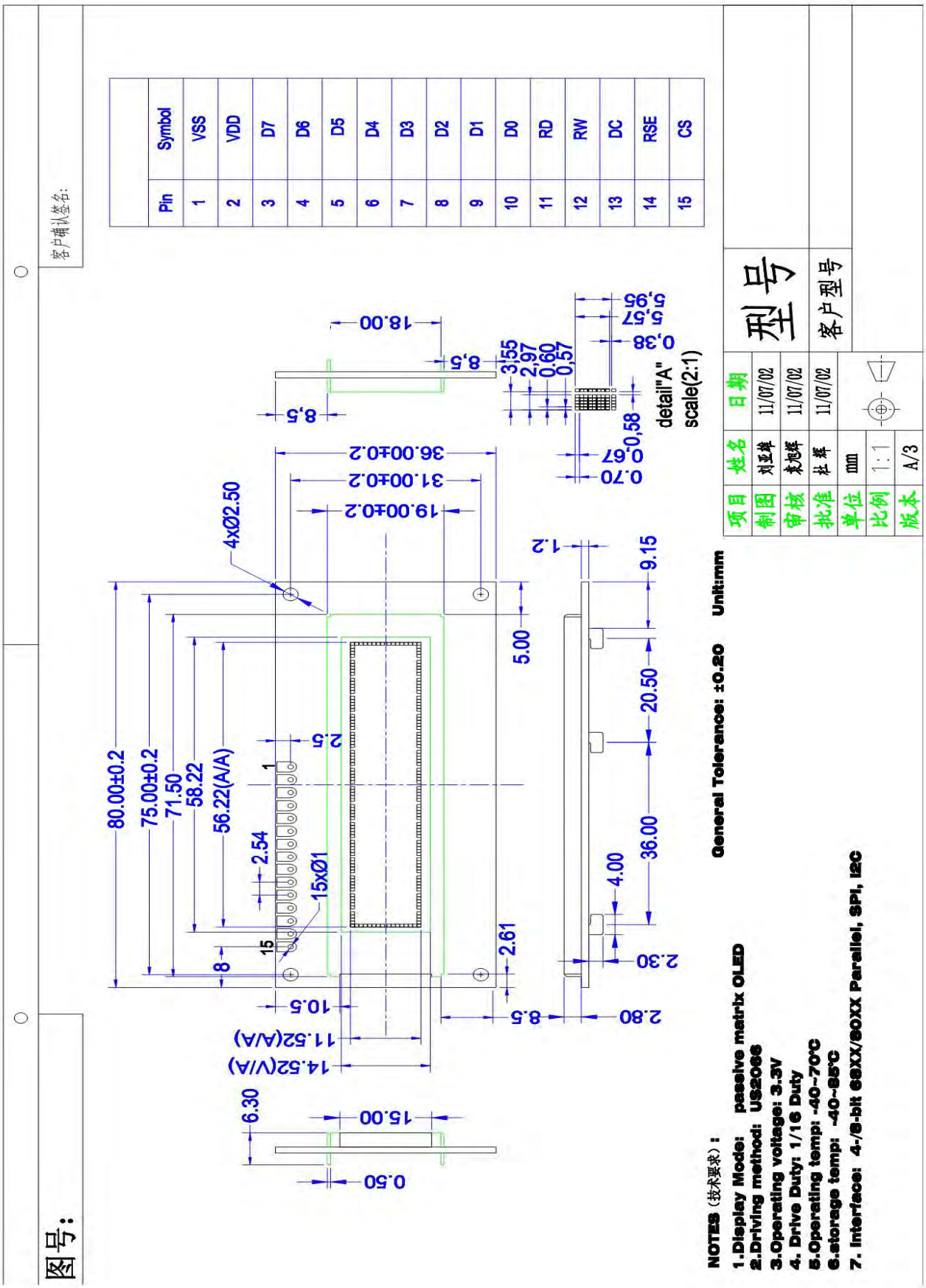
1.1 Display Specifications

1) Display Mode: Passive Matrix OLED
2) Display Color: Yellow(monochrome)
3) Drive Duty: 1/16 Duty
4) Controller Driver:US2066

1.2 Module Features

Items	Specification	Unit
Diagonal A/A Size	2.26	Inch
Number of dots	16 Characters (5 X 8 dots) X 2 Lines	dot
Module size	80 X 36 X 4	mm
Active Area	56.22 X 11.52	mm
viewing Area	57 X 14.52	mm
Character Pitch	3.55 X 5.95	mm
Character Size	2.97 X 5.57	mm
Dot Pitch	0.60 X 0.70	mm
Dot Size	0.57 X 0.67	mm
General Tolerance	± 0.20	mm

2.Mechanical Drawing



3.Pin Definition

3.1 JP1:

Pin number	Symbol	Type	Function
1	VSS	P	Power supply ground
2	VDD	P	3.3V power supply
3~10	D7~D0	I/O	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.
11	RD	I	When interface to a 6800-series microprocessor, this pin will be used as the Enable(E) signal, When interface to an 8080-microprocessor, this pin receives the Read(RD#)signal.
12	RW	I	This is read/write control input pin connecting to the MCU interface. When interface to a 6800-series microprocessor, Read mode will be carried out when this pin is pulled HIGH and write mode when low .When interface to an 8080-microprocessor, this pin will be the data Write input. When serial interface is selected, this pin must be connected to Vss
13	DC	I	This is DATA/COMMAND control pin. When it is pulled HIGH, the data at D[0~7] is treated as data. When it is pulled LOW, the data at D[0~7] will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
14	RSE	I	This pin is reset signal input (active LOW)
15	CS	I	This pin is chip select input (active LOW)

3.2 Jump

BS0 /BS1 /BS2:MUC bus interface selection pin.

BS2	BS1	BS0	Interface
0	0	0	Serial Interface
0	0	1	Invalid
0	1	0	I2C
0	1	1	Invalid
1	0	0	8-bit 6800 parallel
1	0	1	4-bit 6800 parallel
1	1	0	8-bit 8080 parallel
1	1	1	4-bit 8080 parallel

Notes: "0"connection GND and "1"connection VDD.

4.Absolute Maximum Ratings.

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for logic	VDD	-0.3	5.5	V	1,2
Supply Voltage for display	VCC	0	13	V	1,2
Operating Temperature	TOP	-40	70	℃	-
Storage Temperature	TSTG	-40	85	℃	-
Life time (100cd/m2)		50000	-	hour	3

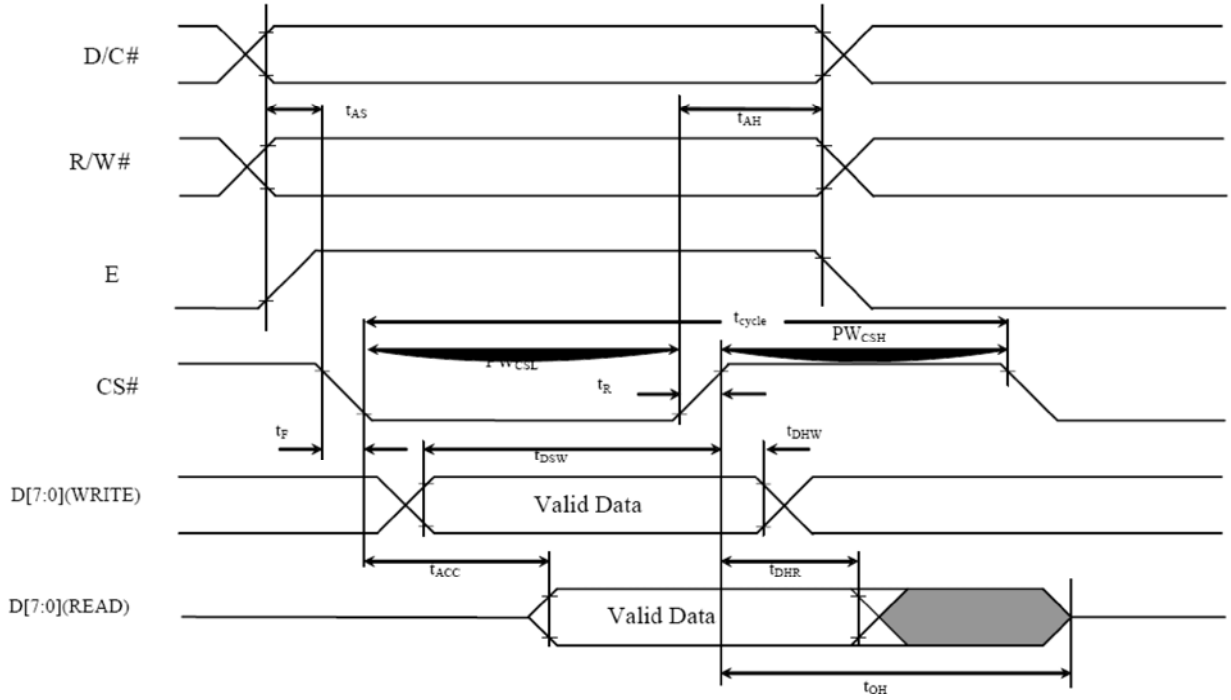
Notes1:
All the above voltages are on the basis of "Vss =0V "
Notes2:
When this module is used beyond the above absolute maximum ratings,permanent breakage of the module may occur , also for normal operations, it is desirable to use this module under the conditions according to Section 3."Optics and Electrical Characteristics "If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.
Notes3:
VCC = 7.25V, Ta = 25 ° C, 50% Checkerboard.
Software configuration follows Section 6.4 Initialization. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.Timing Characteristics

5.1 68XX-Series MPU Parallel Interface Timing Characteristics:

(TA=25°C,V_{DD} -V_{SS}=1.65V to 3.3V)

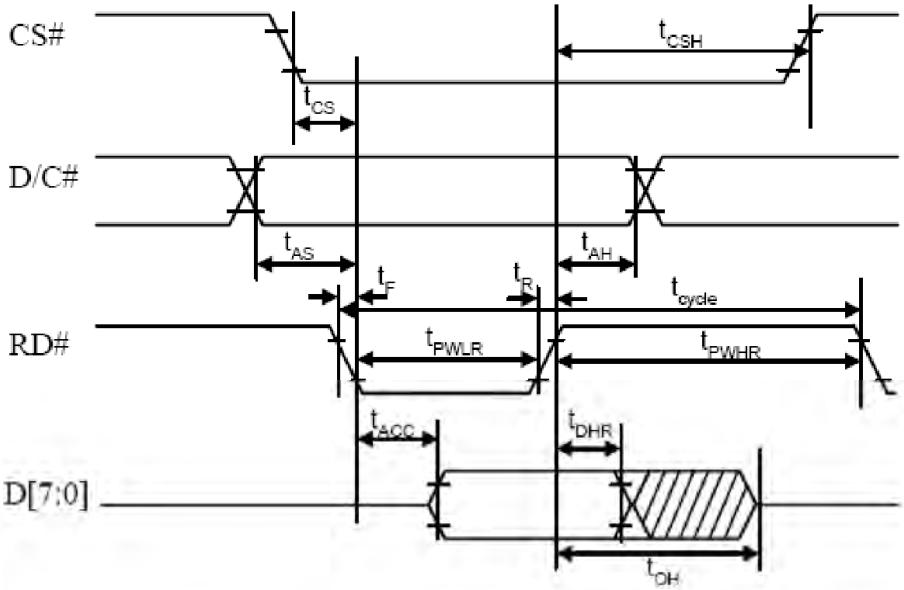
Symbol	parameter	Min	Type	Max	Unit
tcycle	Clock Cycle Time (write cycle)	400	-	-	ns
tAS	Address Setup time	13	-	-	ns
tAH	Address Hold time	17	-	-	ns
tDSW	Write Data Setup Time	35	-	-	ns
tDHW	Write Data Hold time	18	-	-	ns
tDHR	Read Data Hold Time	13	-	-	ns
tOH	Output Disable Time	10	-	90	ns
tACC	Access Time (RAM) Access Time (command)	-	-	125	ns
PWCSL	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PWCSH	Chip select High Pulse Width (read) Chip Select High Pulse Width (write)	155 55	- -	- -	ns ns
tR	Rise Time	-	-	15	ns
tF	Fall Time	-	-	15	ns



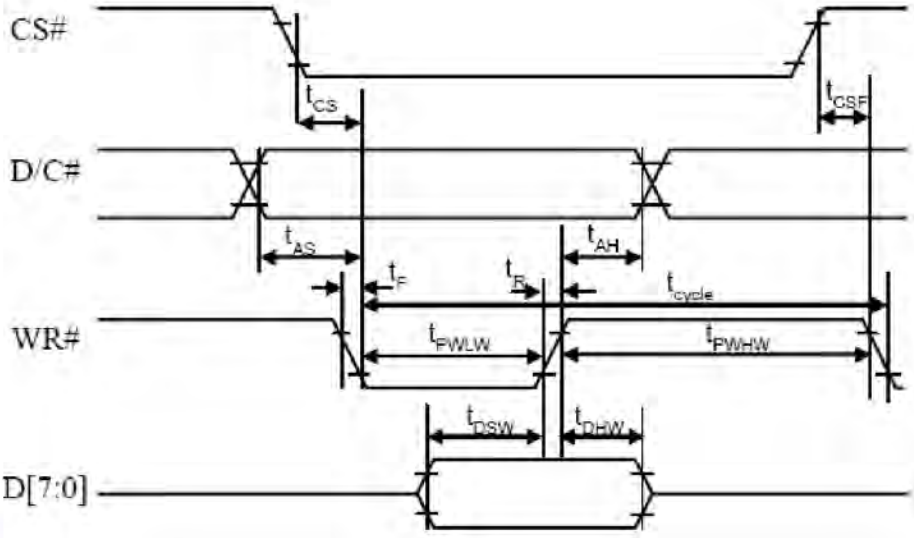
5.2 80XX-Series MPU Parallel Interface Timing Characteristics:

(TA=25°C, V_{DD} -V_{SS}=1.65V to 3.3V)

Symbol	parameter	Min	Type	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup time	13	-	-	ns
t_{AH}	Address Hold time	17	-	-	ns
t_{CS}	Chip Select time	0	-	-	ns
t_{CSH}	Chip select Hold Time To read signal	0	-	-	ns
t_{CSF}	Chip select hold time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	10	-	90	ns
t_{ACC}	Access Time	-	-	125	ns
t_{PWLR}	Read Low time	250	-	-	ns
t_{PWLW}	Write Low time	50	-	-	ns
t_{PWHR}	Read High time	155	-	-	ns
t_{PWHW}	Write High time	55	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

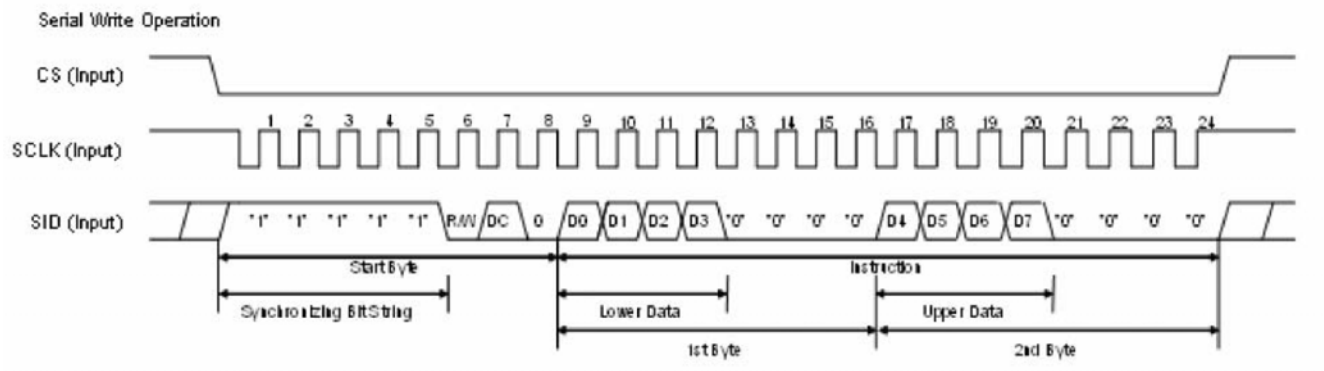


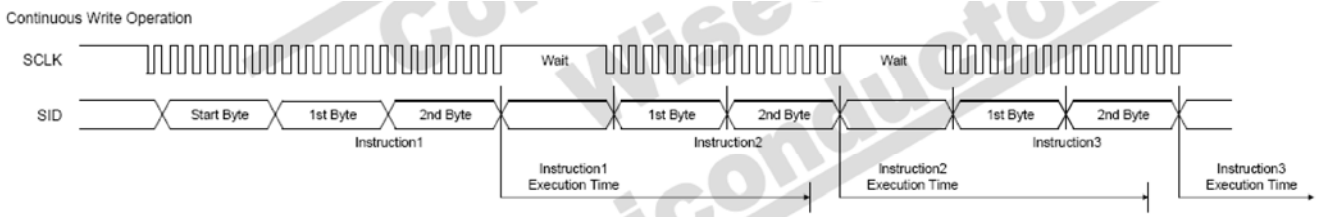
(Read Timing)



(Write Timing)

5.3 Serial Interface Timing Characteristics:





6.Reference Sequence

6.1 Commands

Refer to the Technical Manual for the US2066

6.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

6.2.1 Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VCC
6. Delay 100ms (When VCC is stable)
7. Send Display on command

6.2.2 Power down Sequence:

1. Send Display off command
2. Power down VCC
3. Delay 100ms (When VCC is reach 0 and panel is completely discharges)
4. Power down VDD

Note :

1) Since an ESD protection circuit is connected between VDD and VCC inside the driver IC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF.
2) VCC should be kept float (disable) when it is OFF.
3) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.
4) VDD should not be power down before VCC power down.

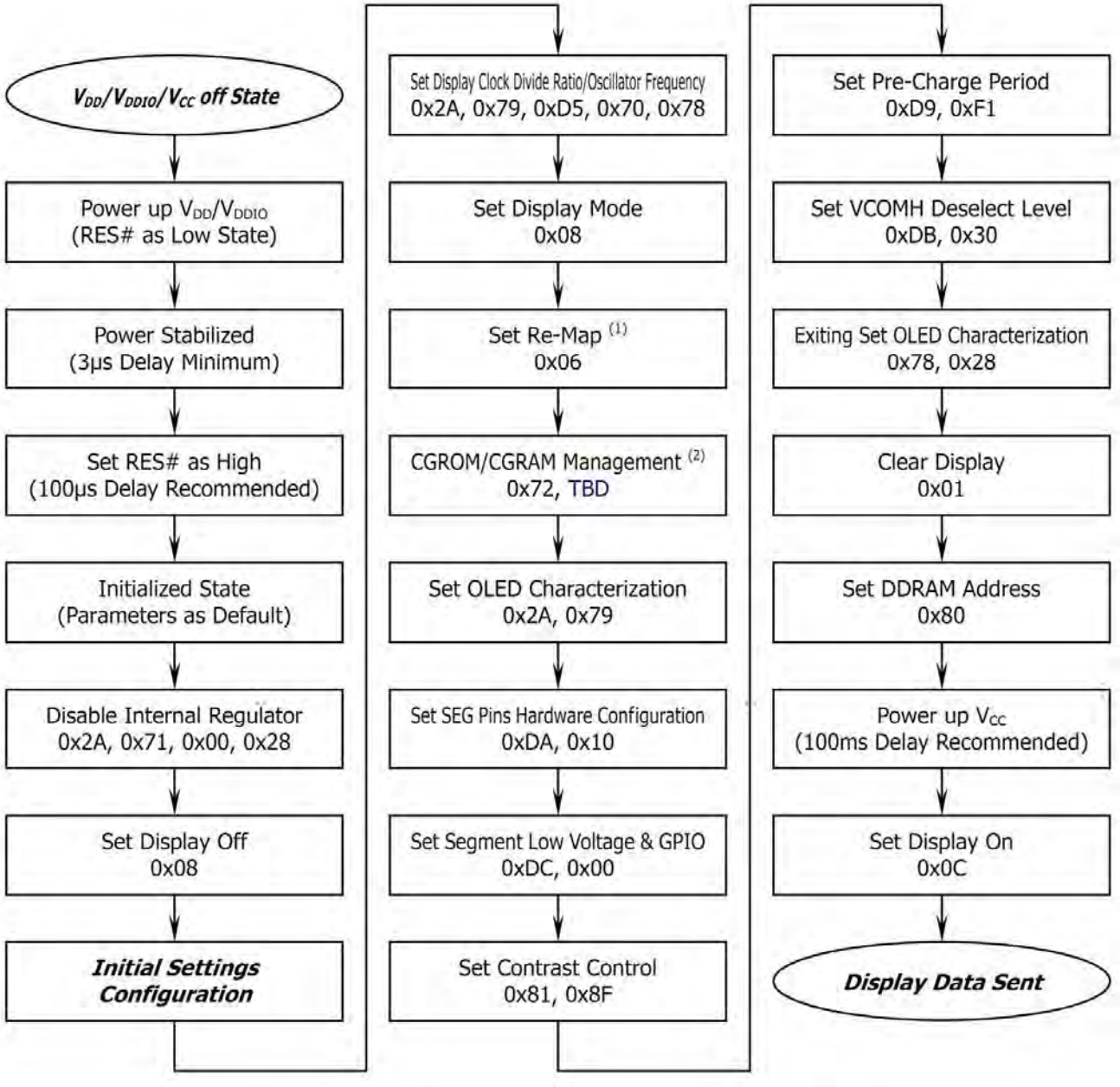
6.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display off, Cursor off, Blink off.
2. Power Down off.
3. 5-dot font is default.
4. Display Shift Disable.
5. CGRAM address is 00h. SEGRAM address is 00h.
6. DDRAM address is 00h.
7. Display start line is set at display RAM address 0
8. Column address counter is set at 0
9. Normal scan direction of the COM outputs
10. Contrast control register is set at 7Fh

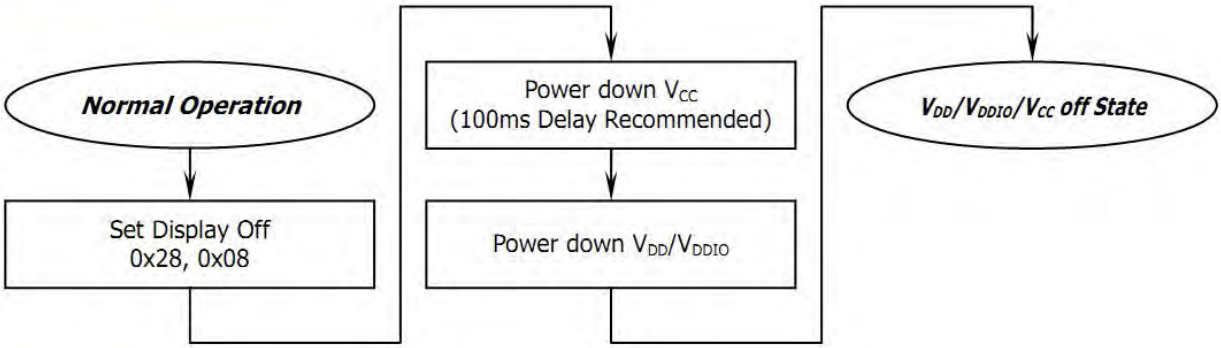
6.4: 3.3V I/O Application

<Power up Sequence>

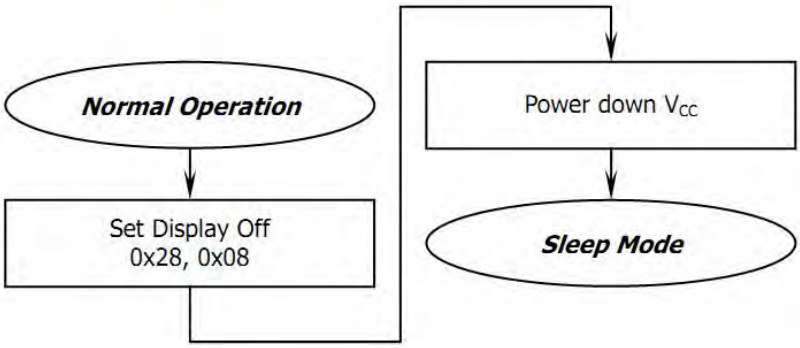


(1) This command could be programmable or defined by pin configuration.
(2) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from Section Built-in CGROM (Character Generator ROM) and Self-Defined CGRAM (Character Generator RAM)
If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

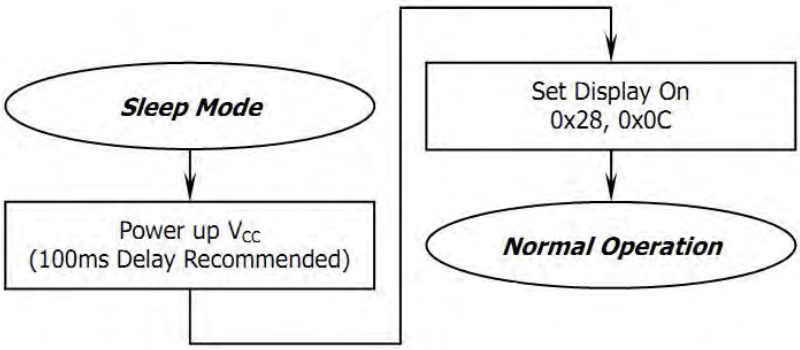
<Power down Sequence>



<Entering Sleep Mode>

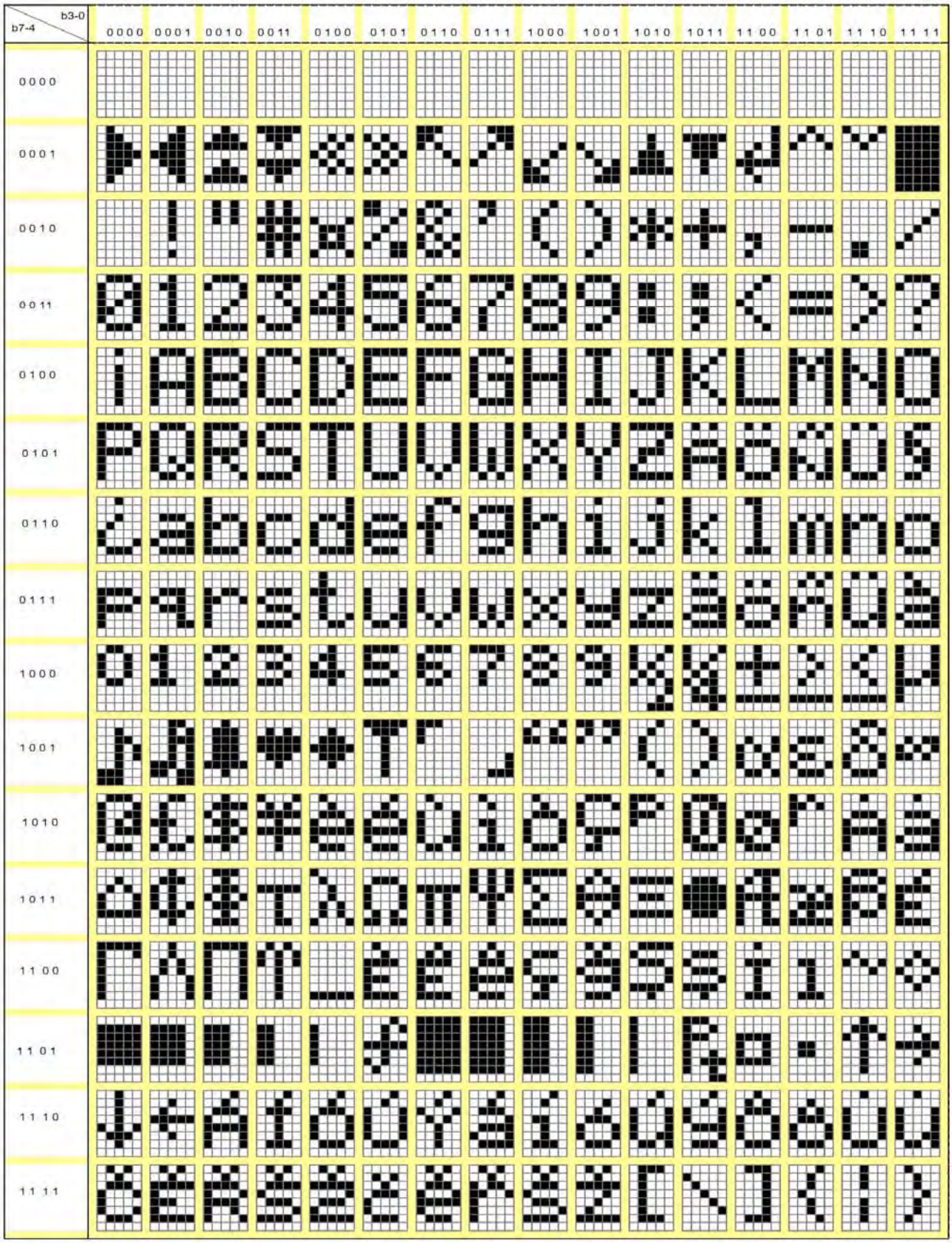


<Exiting Sleep Mode>

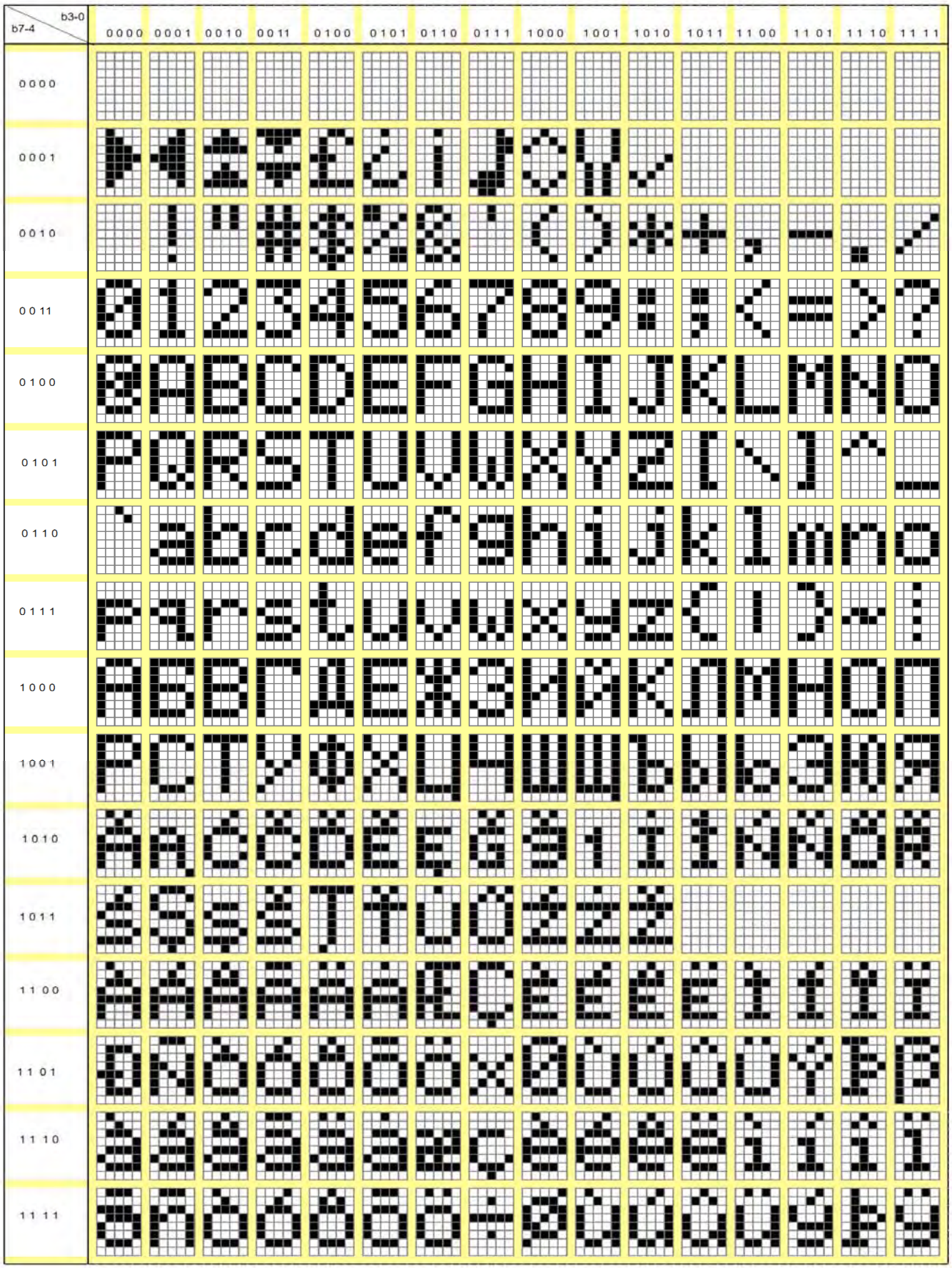


6.5 US2066 CGROM Character Code

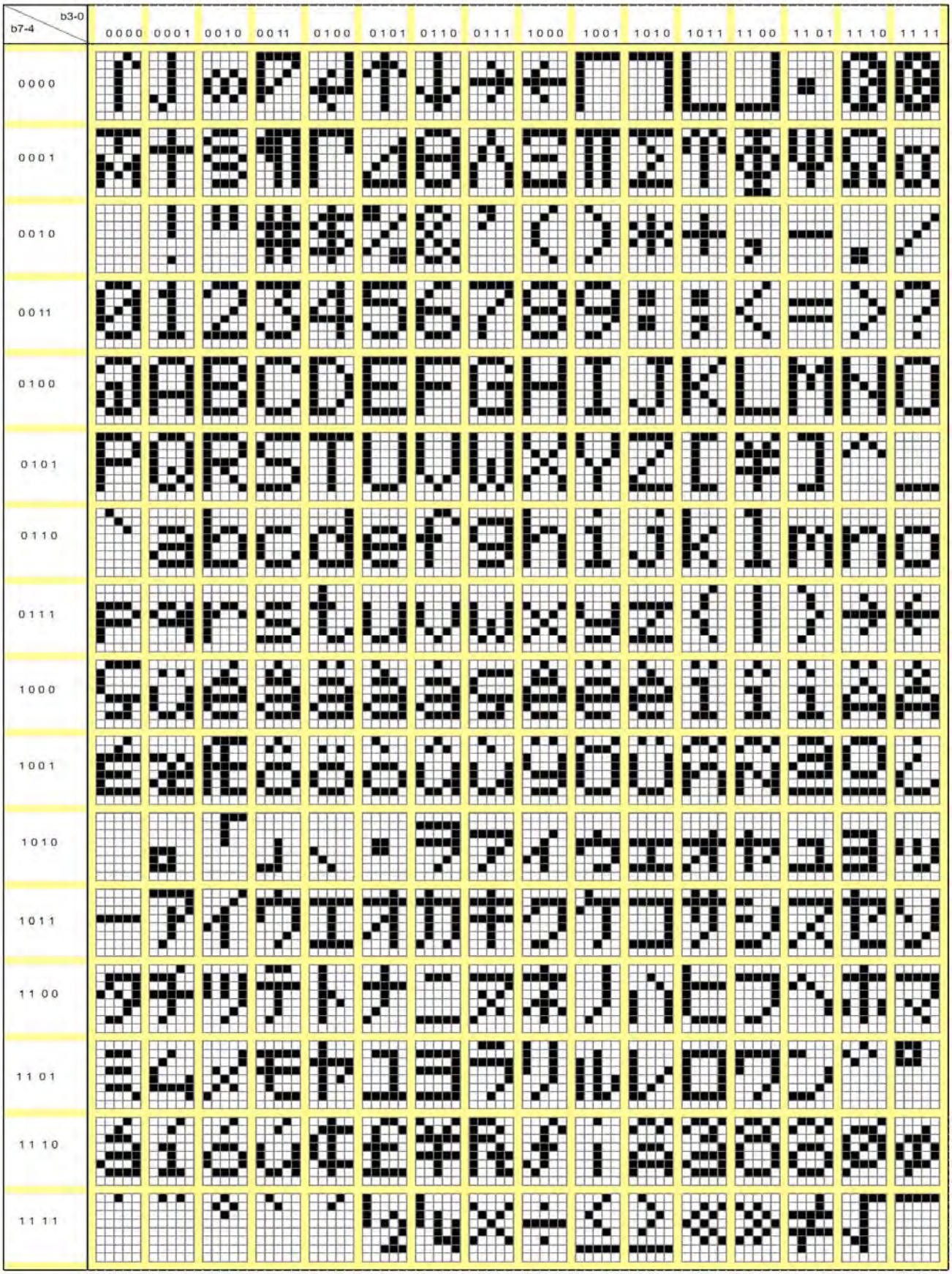
5.5.1 ROMA



6.5.2 RMOB


b3-0
b7-4
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

6.5.3 ROMC


b3-0
b7-4
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111