EK79030

Rev. 0.2

PRELIMINARY DATA SHEET

1200CH Source Driver with TCON MIPI/LVDS Interface

fitipower integrated technology Inc.

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Single Chip 1200 Channel Source Driver with Timing Controller for TFT LCD

1. GENERAL DESCRIPTION

The EK79030 is a highly integrated solution for small size to middle size α-Si TFT-LCD panels. This chip integrates 1200ch source driver with MIPI/LVDS input interface.

2. FEATURES

- Integrate 1200 channel source driver and timing controller
- Display Resolution :
  - 400 x RGB x (1280, (8 x SLN))
- Full color mode:
  - 16.7M colors (24-bit per pixel, R:G:B = 8:8:8)

  Reduced color mode:
  - 262K colors (18-bit per pixel, R:G:B = 6:6:6)
  - 65K colors (16-bit per pixel, R:G:B = 5:6:5)

- System Interfaces:
  - MIPI DSI (3/4 data lane): MIPI DSI(DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01)
  - LVDS interface(DE mode only)

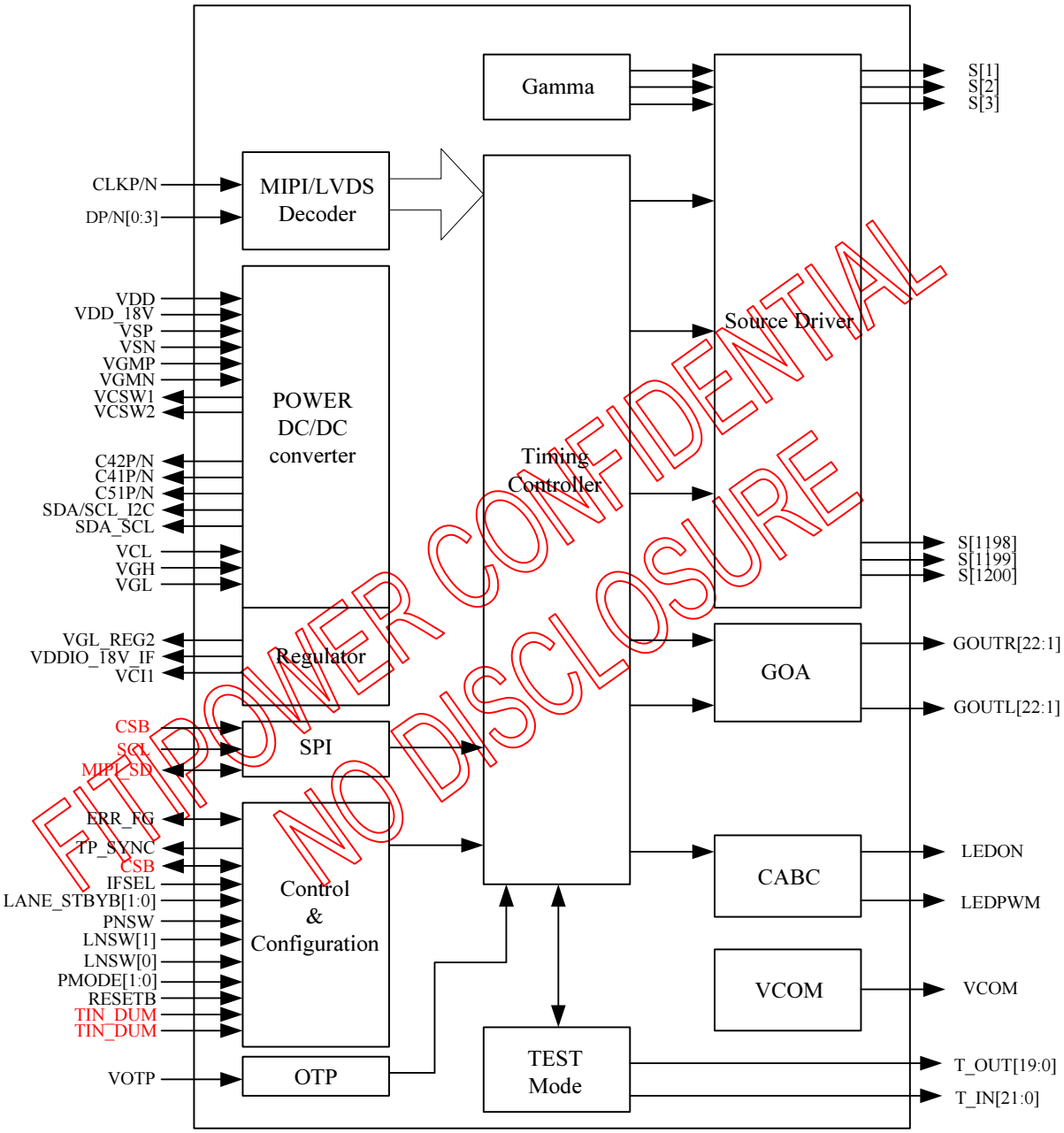
- Integrate 1200 channel source driver and timing controller
- Gate driver control signals for GIP
- Internal level shifter for Gate driver control
- Support SPI/I2C interface
- Supports 1-dot / 2-dot / 4-dot / Column inversion
- Gamma correction (1 preset gamma curve)
- GAS function for preventing image sticking when abnormal power off
- Support DC COM driving
- Built-In Charge pump for VGH / VGL , and VCOM generator
- Built-In Enhanced BIST pattern
- Support for Programming Gamma correction
- Support Dither Function
- OTP memory to store initialization register settings
- Built-In OTP (4 Times) to store VCOM calibration
- Built-In OTP (1 Times) to store gamma, panel timing, and analog power setting
- COG package

- Input voltage ranges:
  - I/O and interface power supply (VDDIO): 2.3V to 5.5V
  - High speed interface power supply (VDDIO_IF): 2.3V to 5.5V
  - Analog power supply (VDD): 2.5V to 6.0V
  - DC/DC set-up supply (VDDP): 2.5V to 6.0V
  - OTP programming voltage (VOTP): 7.5V+/- 0.2V
  - Analog voltage range for VSP to VSSP: 4.5V to 6.0V
  - Analog voltage range for VSN to VSSP: -4.5V to -6.0V
  - Analog voltage range for VGH to VSSP: 9.0V to 20V
  - Analog voltage range for VGL to VSSP: -9V to -18V
  - VGH,VGL: VGH-VGL<32V

- Output voltage ranges:
  - Analog voltage range for VSP to VSSP: 4.5V to 6.0V
  - Analog voltage range for VSN to VSSP: -4.5V to -6.0V
  - Analog voltage range for VCL to VSSP: -3.0V

- Positive source output voltage level: VGMP= 3.5V to 5.8V
- Negative source output voltage level: VGMN= -3.5V to -5.8V
- Positive gate driver output voltage level: VGH= 9.0V to 20V
- Positive gate driver output voltage level: VGH_REG= 9.0V to 19V
- Negative gate driver output voltage level: VGL= -9V to -18V
- Negative gate driver output voltage level: VGL_REG= -6V to -15V
- VCOM= -3.5V to -0.2V, a step=12mV
- VGH,VGL: VGH-VGL<32V

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

4.1 Pin define

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td colspan="3">Interface and Control</td></tr>
<tr><td>DP[0]/DN[0]
DP[1]/DN[1]
DP[2]/DN[2]
DP[3]/DN[3]</td><td>Input</td><td>MIPI or LVDS data Input. Select by “IFSEL” pin.</td></tr>
<tr><td>CKP/CKN</td><td>Input</td><td>MIPI or LVDS clock Input. Select by “IFSEL” pin.</td></tr>
<tr><td>IFSEL</td><td>Input</td><td>“0” : LVDS interface
“1” : MIPI interface (default)</td></tr>
<tr><td>LNSW[1:0]
(VDDIO)</td><td>Input</td><td>MIPI data lane swapping selection pins.
<table>
<tr><th rowspan="2">LNSW[1:0]</th><th colspan="5">MIPI Lane Mapping</th></tr>
<tr><th>D0(PAD)</th><th>D1(PAD)</th><th>CLK(PAD)</th><th>D2(PAD)</th><th>D3(PAD)</th></tr>
<tr><td>00</td><td>D3</td><td>D2</td><td>CLK</td><td>D1</td><td>D0</td></tr>
<tr><td>01</td><td>D3</td><td>D0</td><td>CLK</td><td>D1</td><td>D2</td></tr>
<tr><td>10</td><td>D0</td><td>D1</td><td>CLK</td><td>D2</td><td>D3</td></tr>
<tr><td>11</td><td>D2</td><td>D1</td><td>CLK</td><td>D0</td><td>D3</td></tr>
</table>
Note: MIPI data lane sequence are unused when IFSEL=”0”
LVDS data/clk lane swapping selection pins.
<table>
<tr><th rowspan="2">LNSW[1:0]</th><th colspan="5">LVDS Lane Mapping</th></tr>
<tr><th>D0(PAD)</th><th>D1(PAD)</th><th>CLK(PAD)</th><th>D2(PAD)</th><th>D3(PAD)</th></tr>
<tr><td>00</td><td>D3</td><td>D2</td><td>CLK</td><td>D1</td><td>D0</td></tr>
<tr><td>01</td><td>D3</td><td>CLK</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>10</td><td>D0</td><td>D1</td><td>CLK</td><td>D2</td><td>D3</td></tr>
<tr><td>11</td><td>D0</td><td>D1</td><td>D2</td><td>CLK</td><td>D3</td></tr>
</table>
Note: LVDS data lane sequence are unused when IFSEL=”1”
Detail LVDS lane swapping please refer section 8.4.2</td></tr>
<tr><td>PNSW
(VDDIO)</td><td>Input</td><td>MIPI/LVDS polarity selection pins.
<table>
<tr><th rowspan="2">PNSW</th><th colspan="5">MIPI/LVDS Lane Mapping</th></tr>
<tr><th>D0P/N</th><th>D1P/N</th><th>CLKP/N</th><th>D2P/N</th><th>D3P/N</th></tr>
<tr><td>0</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>1</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
</table></td></tr>
<tr><td>PMODE[1:0]
(VDDIO)</td><td>Input</td><td>Power mode selection. Normally pull high.
<table>
<tr><th>PMODE[1:0]</th><th>VSP</th><th>VSN</th><th>VGH</th><th>VGL</th></tr>
<tr><td>00</td><td>JD5001/2</td><td>JD5001/2</td><td>External</td><td>External</td></tr>
<tr><td>01</td><td>External</td><td>External</td><td>Charge pump</td><td>Charge pump</td></tr>
<tr><td>10</td><td>JD5001/2</td><td>JD5001/2</td><td>Charge pump</td><td>Charge pump</td></tr>
<tr><td>11</td><td>External</td><td>External</td><td>External</td><td>External</td></tr>
</table></td></tr>
<tr><td>RES[2:0]
(VDDIO)</td><td>Input</td><td>Panel resolution setting selection.
<table>
<tr><th colspan="3">RESOL[2:0]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>400RGB x 1280</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>LVBIT
(VDDIO)</td><td>Input</td><td>6-bit / 8-bit input select for LVDS mode. Normally pull high.
(only for LVDS, MIPI Mode = Dummy)
LVBIT = L, 6-bit.
LVBIT = H, 8-bit. (Default)</td></tr>
<tr><td>LVFMT
(VDDIO)</td><td>Input</td><td>8-bit input format select for LVDS mode. Normally pull high.
(only for LVDS, MIPI Mode = Dummy)
LVFMT = L, JEIDA format.
LVFMT = H, VESA format. (Default)</td></tr>
<tr><td>RESETB
(VDDIO)</td><td>Input</td><td>Global reset pin. Normally pull high.
RESETB = L, The controller is in reset state.
RESETB = H, Normal operation.(Default)
Suggest to connecting with an RC reset circuit for stability.</td></tr>
<tr><td>LANE[1]_STBYB
(VDDIO)</td><td>Input</td><td>MIPI mode(IFSEL=1) : MIPI LANE number control pin
LVDS mode(IFSEL=0) : Standby mode signal (low :standby mode)
LANE[1]_STBYB default pull hi
<table>
<tr><th>LANE[1]_STBYB</th><th>LANE[0]_BISTB</th><th>Interface mode</th></tr>
<tr><td>0</td><td>0</td><td>Not used</td></tr>
<tr><td>0</td><td>1</td><td>Not used</td></tr>
<tr><td>1</td><td>0</td><td>3 Lanes</td></tr>
<tr><td>1</td><td>1</td><td>4 Lanes (default)</td></tr>
</table></td></tr>
<tr><td>LANE[0]_BISTB
(VDDIO)</td><td>Input</td><td>MIPI mode(IFSEL=1) : MIPI LANE number control pin
LVDS mode(IFSEL=0) : BIST mode signal (low :BIST mode)
LANE[0]_BISTB default pull hi</td></tr>
<tr><td>LEDPWM
(VDDIO)</td><td>Output</td><td>This pin is connected to the external LED driver.
PWM type control signal for brightness of the LED backlight.
If not used, please float this pin.</td></tr>
<tr><td>LEDON
(VDDIO)</td><td>Output</td><td>Back-light enable signal.</td></tr>
<tr><td>CMD_SEL
(VDDIO)</td><td>Input</td><td>Command interface selection. Normally pull high.
<table>
<tr><th>CMD_SEL</th><th>Function</th></tr>
<tr><td>0</td><td>3-Wire (Default)</td></tr>
<tr><td>1</td><td>I2C</td></tr>
</table>MIPI and 3-wire/I2C command can’t receive at the same time.</td></tr>
<tr><td>CSB
(VDDIO)</td><td>Input</td><td>Serial communication enables. Normally pull high</td></tr>
<tr><td>SDA
(VDDIO)</td><td>I/O</td><td>Serial communication data input.</td></tr>
<tr><td>SCL
(VDDIO)</td><td>Input</td><td>Serial communication clock input.</td></tr>
</table>

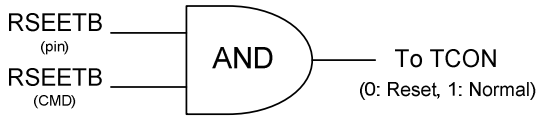
Pin Name	Pin Type	Description
SDA_I2C (VDDIO)	I/O	Serial communication data input.
SCL_I2C (VDDIO)	Input	Serial communication clock input.
Panel driver output		
S[1200:1]	Output	Source Driver output signals. Source output mapping with different resolution. **Resolution** / **Source channel**: 400RGB / S[1200:1]
SDUMY[3:0]	Output	Source dummy output.
GOUTL[1]~ GOUTL[22]	Output	These pins are used for Panel gate control signals. If not used, let it open.
GOUTR[1]~ GOUTR[22]	Output	These pins are used for Panel gate control signals. If not used, let it open.
Power supply pins		
VDDIO	PI	A power supply for the I/O circuit. VDDIO=2.3V to 5.5V When VDDIO=1.8V, connect VDDIO to VDD_18V.
VDD	PI	A power supply for DC/DC circuit. VDD=2.5V to 6.0V VCI input level should be same as VCIP input level to avoid the level-mismatching at internal level shifter circuit.
VDDP	PI	A power supply for DC/DC circuit. VDD=2.5V to 6.0V VCIP input level should be same as VCI input level to avoid the level-mismatching at internal level shifter circuit.
VDDIO_IF	PI	Interface and I/O power supply for the MIPI power regulator circuits. VDDIO=2.3V to 5.5V. When VDDIO_IF=1.8V, connect VDDIO_IF to VDD_18V_IF.
VDD_18V	Output	Internal power supply for logic circuits. Connect to a stabilizing capacitor.
VDD_18V_IF	Output	Internal power supply for MIPI circuits. Connect to a stabilizing capacitor.
VSSA	PI	Analog ground. VSS=0V. When using the COG method, connect to VSS on the FPC to prevent noise.
VSS	PI	GND for the internal logic. VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VSSP	PI	GND for the DC/DC circuit. VSSP=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VSS_IF	PI	Ground for interface.
VOTP	PI	External high voltage pin used in OTP mode and operates at 7.5V. If not used, let it open.
VSP	PI	Input voltage from the set-up circuit (4.5V to 6.0V). It is generated from VDDP.
VSN	PI	Input voltage from the set-up circuit (-4.5V to -6.0V). It is generated from VSN. Place a schottkey barrier diode between VSN and VGL.
VCL	PO	Input voltage from the set-up circuit (~-3.0V). It is generated from VSN.
VGH	PO	Output voltage from the step-up circuit Connect to stabilizing capacitor between VSSA and VGH.

Pin Name	Pin Type	Description
VGL	PO	Output voltage from the step-up circuit Connect to stabilizing capacitor between VSSA and VGL. Place a schottkey barrier diode between VSSA and VGL.
VCI1	PO	Reference voltage from internal band gap circuit. The tolerance of VCI1 voltage is +/- 3% .
VGMP	PO	Positive regulated voltage output (3.5V to 5.8V)
VGMN	PO	Negative regulated voltage output (-3.5V to -5.8V)
VGH_REG	PO	Regulator output voltage generated from VGH. Connect to a stabilizing capacitor between VSSA and VGH_REG. If not used, please open.
VGL_REG	PO	Regulator output voltage generated from VGL. Connect to a stabilizing capacitor between VSSA and VGL_REG. If not used, please open.
VCOM	PO	The power supply of common voltage in DC com driving. The voltage range is set between -3.5V to -0.2V. It must connected a stabilizing capacitor 2.2u to VSS.
DC/DC pumping		
C41P, C41N C42P, C42N	C	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH voltage. If not used, let them open.
C51P, C51N C11P_VGL, C11N_VGL	C	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGL voltage. If not used, let them open.
VCSW1, VCSW2	PO	**In external power IC mode:** VCSW1 and VCSW2 connect to external power IC. **If not used, Please open these pin.**
Other pins		
TP_SYNC (VDDIO)	Output	Touch sync signal. Float these pins for normal operation.
T_IRX	T	Test pin. Float these pins for normal operation.
T_VREF	T	Test pin. Float these pins for normal operation.
T_IBIAS	T	Test pin. Float these pins for normal operation.
TOUT[15:0]	T	Test pin. Float these pins for normal operation.
T_CSB_DUM	T	Test pin. Float these pins for normal operation.
TEST_EN	T	Test pin. Float these pins for normal operation.
TIN[19:0]	T	Test pin. Float these pins for normal operation.
T_SCL_DUM	T	Test pin. Float these pins for normal operation.
T_SDA_DUM	T	Test pin. Float these pins for normal operation.
TEST_IO[2:0]	T	Test pin. Float these pins for normal operation.
TIN_DUM[10:0]	T	Test pin. Float these pins for normal operation.
T_OTP_RLOAD	T	Test pin. Float these pins for normal operation.
T_VDDN15	T	Test pin. Float these pins for normal operation.
T_VDDN3	T	Test pin. Float these pins for normal operation.
T_EXT_VCOMI	T	Test pin. Float these pins for normal operation.
C13P_DUM	T	Test pin. Float these pins for normal operation.
C12N_DUM	T	Test pin. Float these pins for normal operation.
C12P_DUM	T	Test pin. Float these pins for normal operation.

Note: P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, PS: Power Setting, C: Capacitor pin.

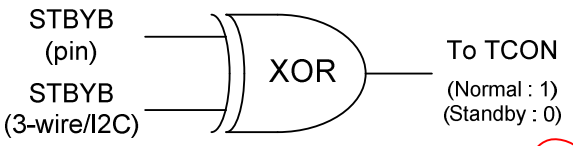
4.2 The relationship between Pin and Register

4.2.1 RESETB PIN/CMD control

Combination Logic	Truth Table
	

RESETB(pin)	GRB(CMD)	TCON
0	0	0
0	1	0
1	0	0
1	1	1

4.2.2 STBYB PIN/CMD control

Combination Logic	Truth Table
For LVDS Register Command interface in use 	

PIN	Register(3wire/I2C)	TCON
0	0	0
0	1	1
1	0	1
1	1	0

4.2.3 Function PIN/CMD control

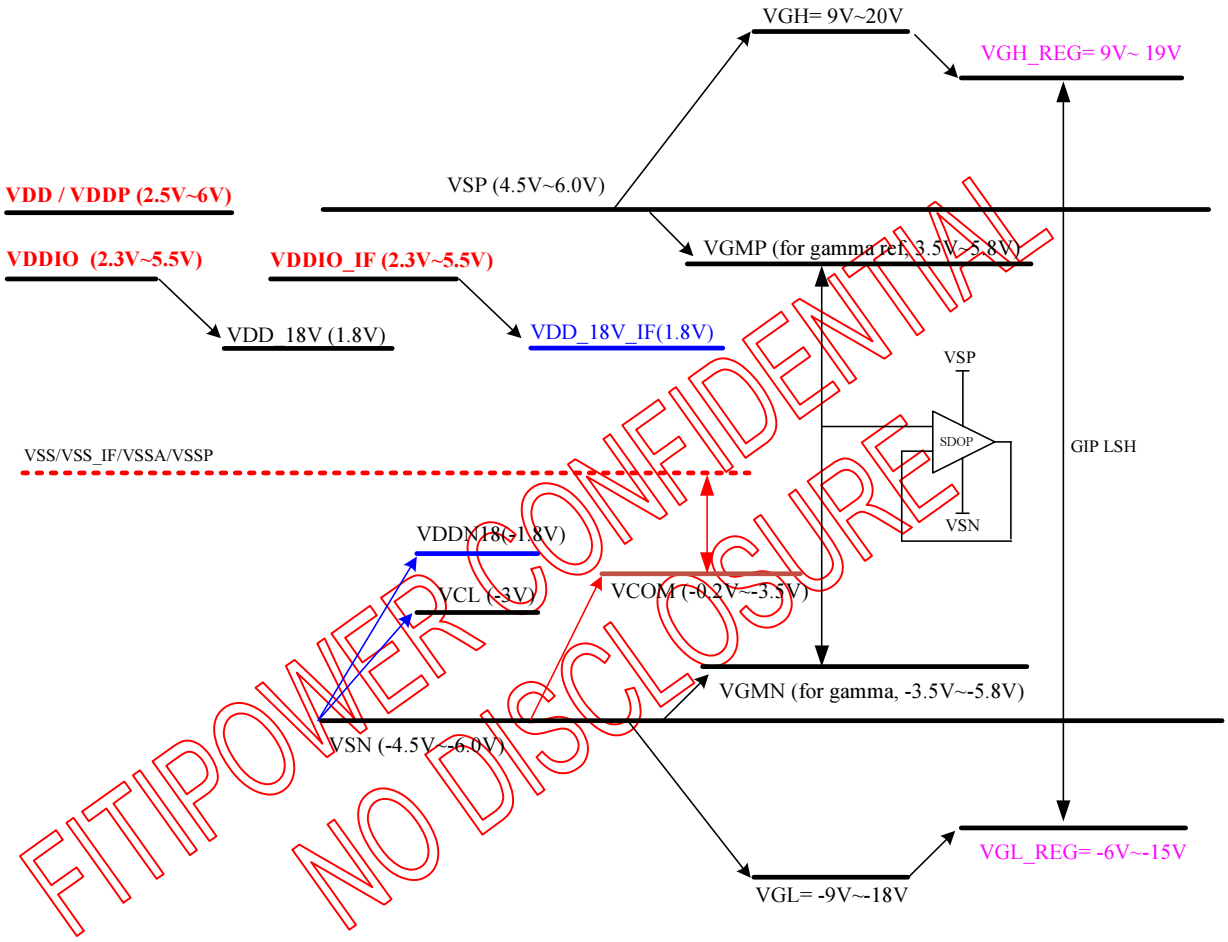
Combination Logic	Truth Table
	

PIN	Register	TCON
0	0	0
0	1	1
1	0	1
1	1	0

Combination with XNOR
CMD is the function register; include MIPI, 3-wire and I2C command.
Pin the function control pin.
Function list:
IFSEL, LNSW[1:0], PNSW, PMODE[1:0], RES[2:0], LVBIT, LVFMT, LANE[1]_STBYB, LANE[0]_BISTB, CMD_SEL.

5. APPLICATION POWER CIRCUIT

5.1 Power Generation



5.2 Power Supply Configution

Four power structures for different applications controlled by PMODE[1:0] pins, like the following table.

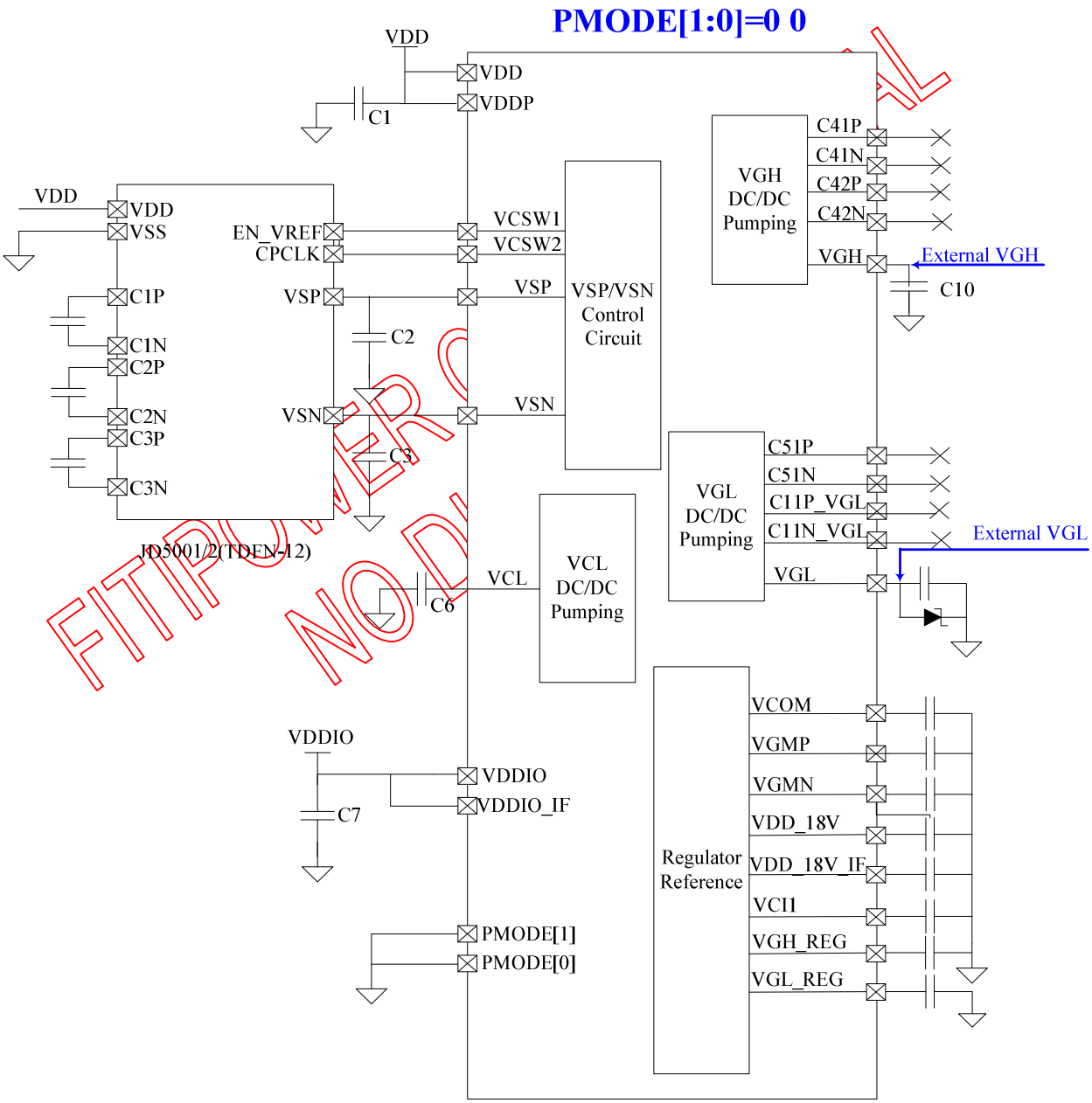
PMODE[1:0]	VSP	VSN	VGH	VGL
00	JD5001/2	JD5001/2	External	External
01	External	External	Charge pump	Charge pump
10	JD5001/2	JD5001/2	Charge pump	Charge pump
11	External	External	External	External

5.3. DC/DC converter circuit

5.3.1 DC/DC power mode 1

VSP/VSN with JD5001/2 controlled by driver IC
External power input: VDDIO(VDDIO_IF), VDD(VDDP), VGH, VGL

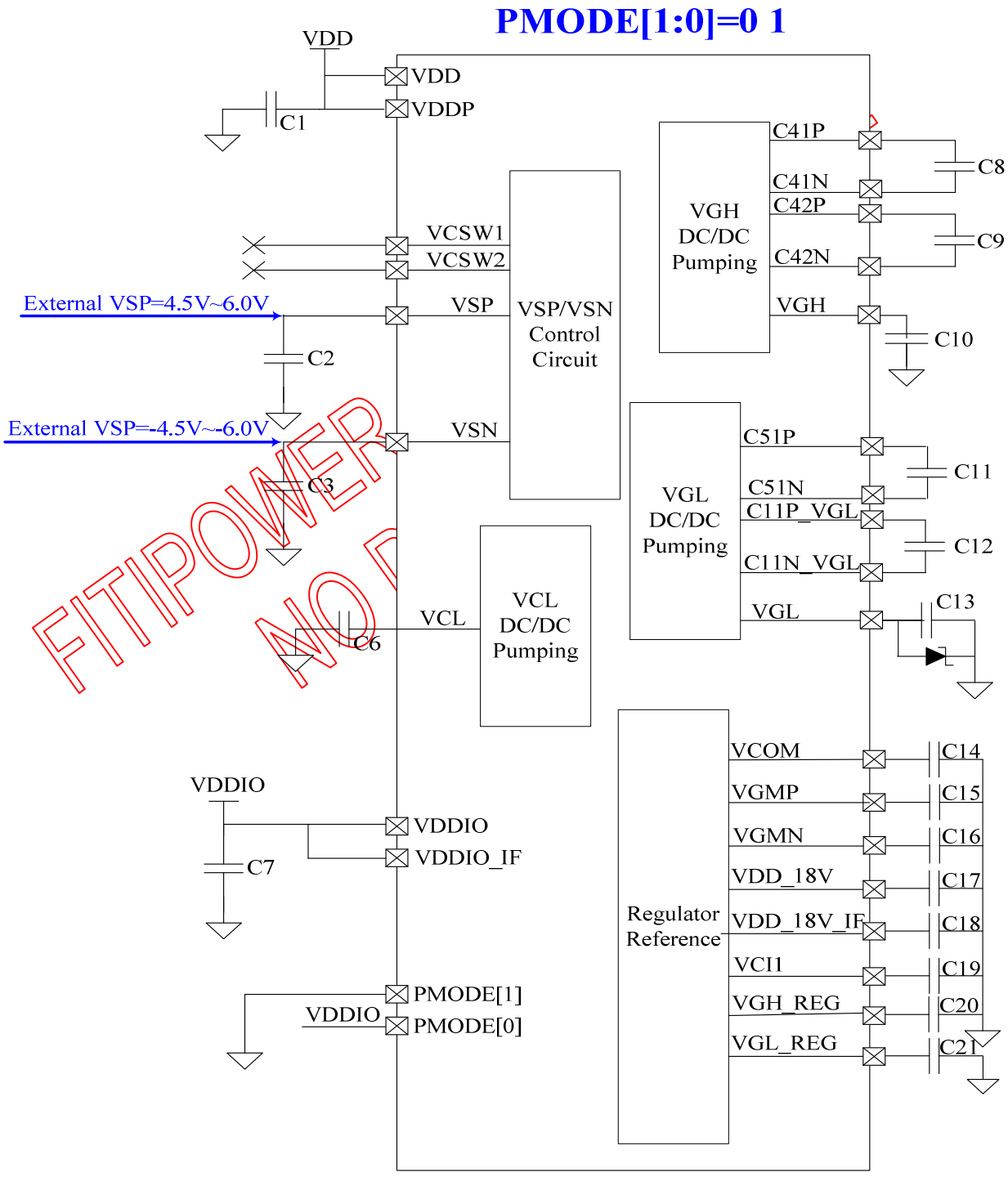
VDDIO=VDDIO_IF=2.3~5.5V, VDD=VDDP=2.5~4.8V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



5.3.2 DC/DC power mode 2

Charge Pump: VGH, VGL
External power input: VDDIO(VDDIO_IF), VDD(VDDP), VSP, VSN

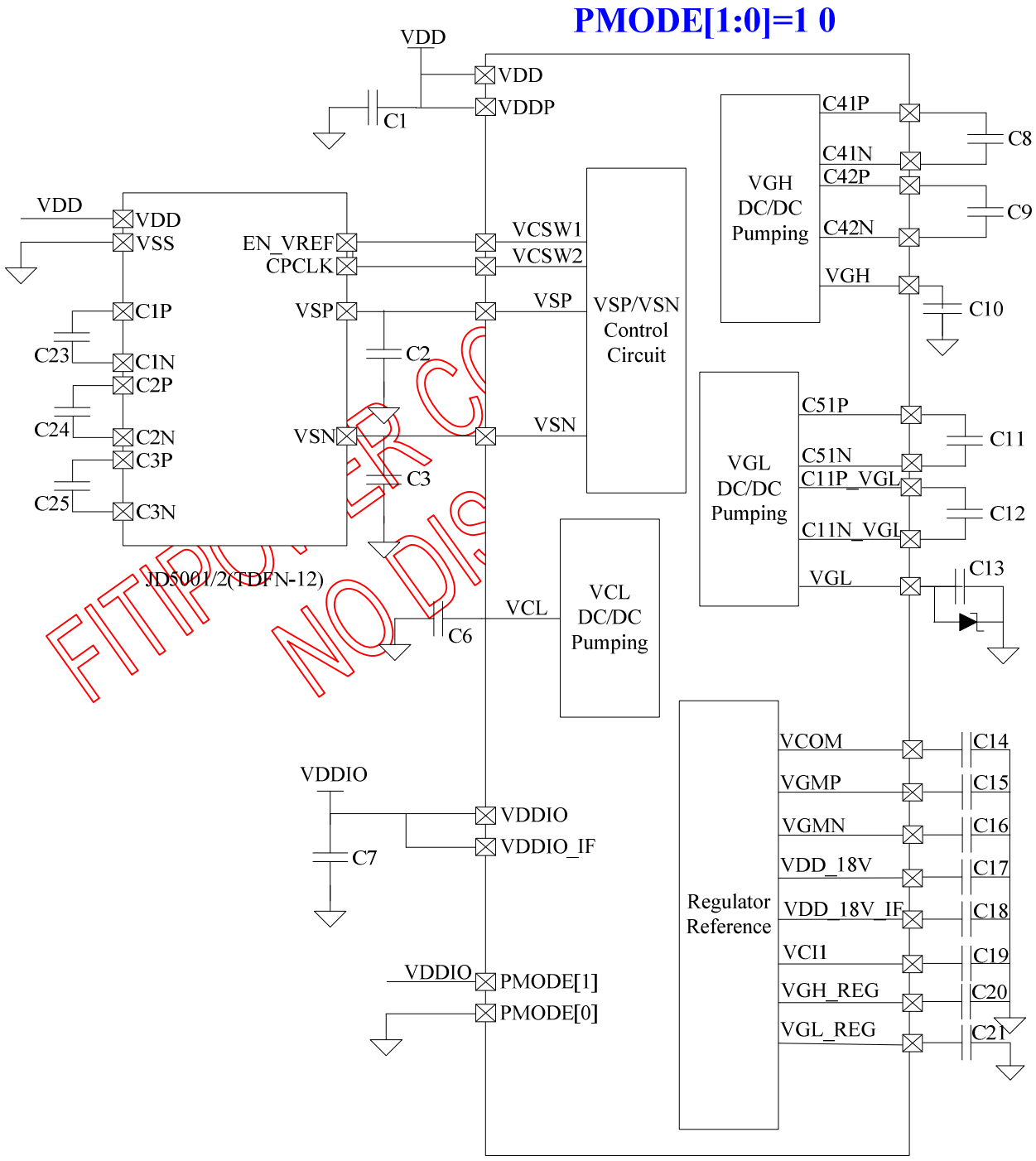
VDDIO=VDDIO_IF=2.3~5.5V, VDD=VDDP=2.5~6.0V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



5.3.3 DC/DC power mode 3

VSP/VSN with JD5001/2 controlled by driver IC; Charge Pump: VGH, VGL
External power input: VDDIO(VDDIO_IF), VDD(VDDP)

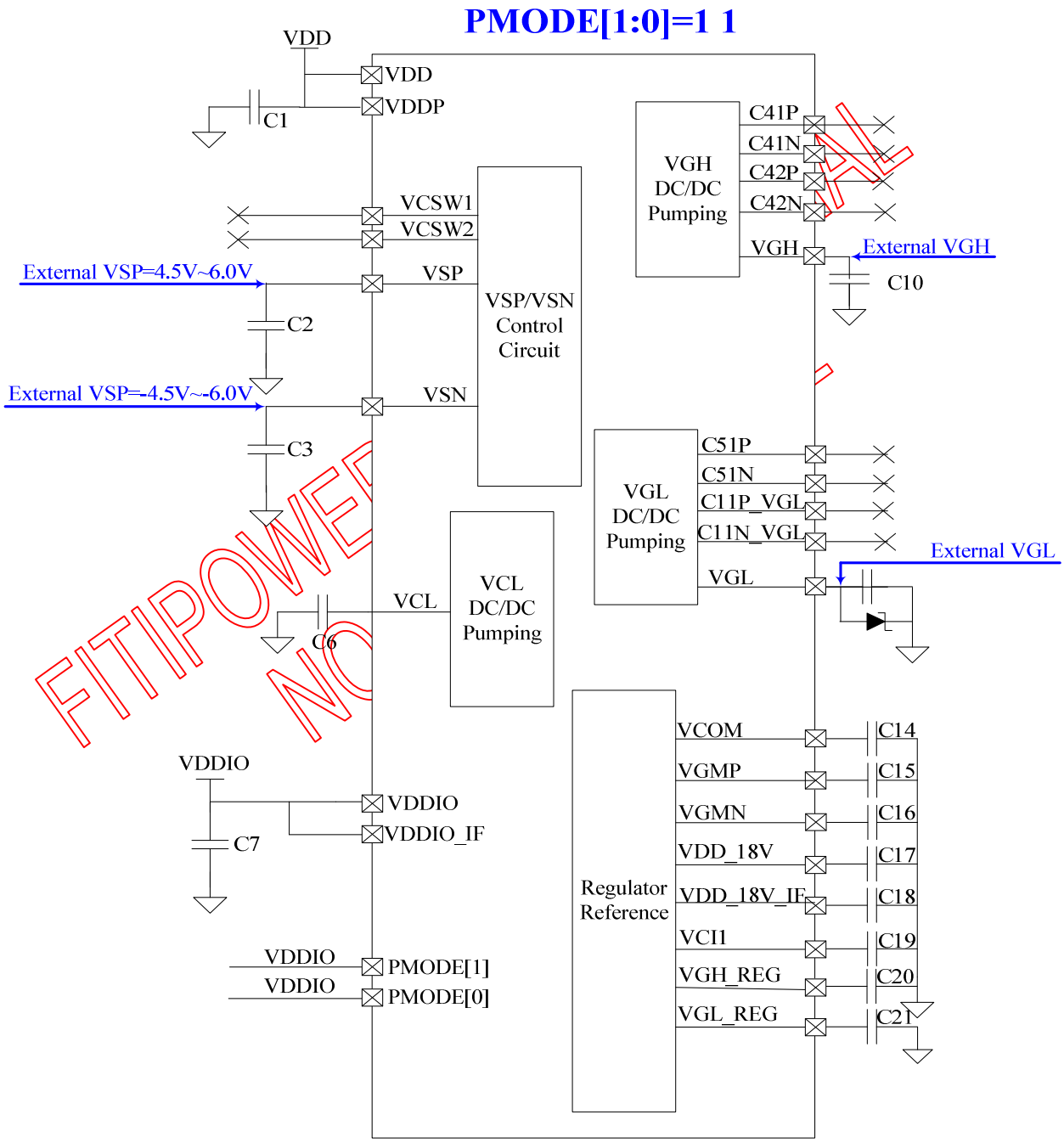
VDDIO=VDDIO_IF=2.3~5.5V, VDD=VDDP=2.5~4.8V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



5.3.4 DC/DC power mode 4

External power input: VDDIO(VDDIO_IF), VDD(VDDP), VSP, VSN, VGH, VGL

VDDIO=VDDIO_IF=2.3~5.5V, VDD=VDDP=2.5~6.0V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



5.4. Power on/off sequence

5.4.1 Power on sequence PMODE[1:0]=00b

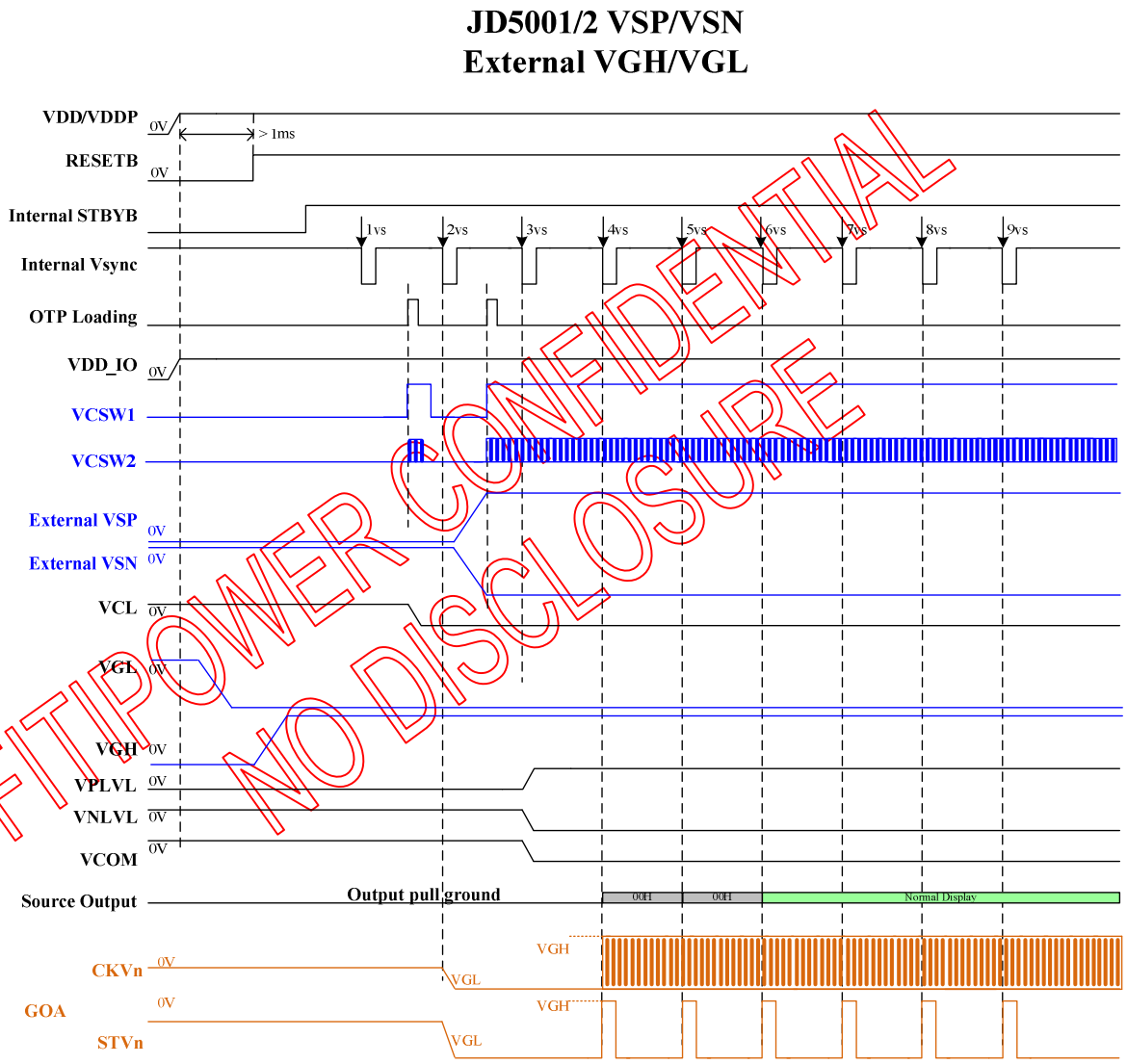


Figure 5.1: Power on sequence with PMODE[1:0]=00b

5.4.2 Power off sequence PMODE[1:0]=00b

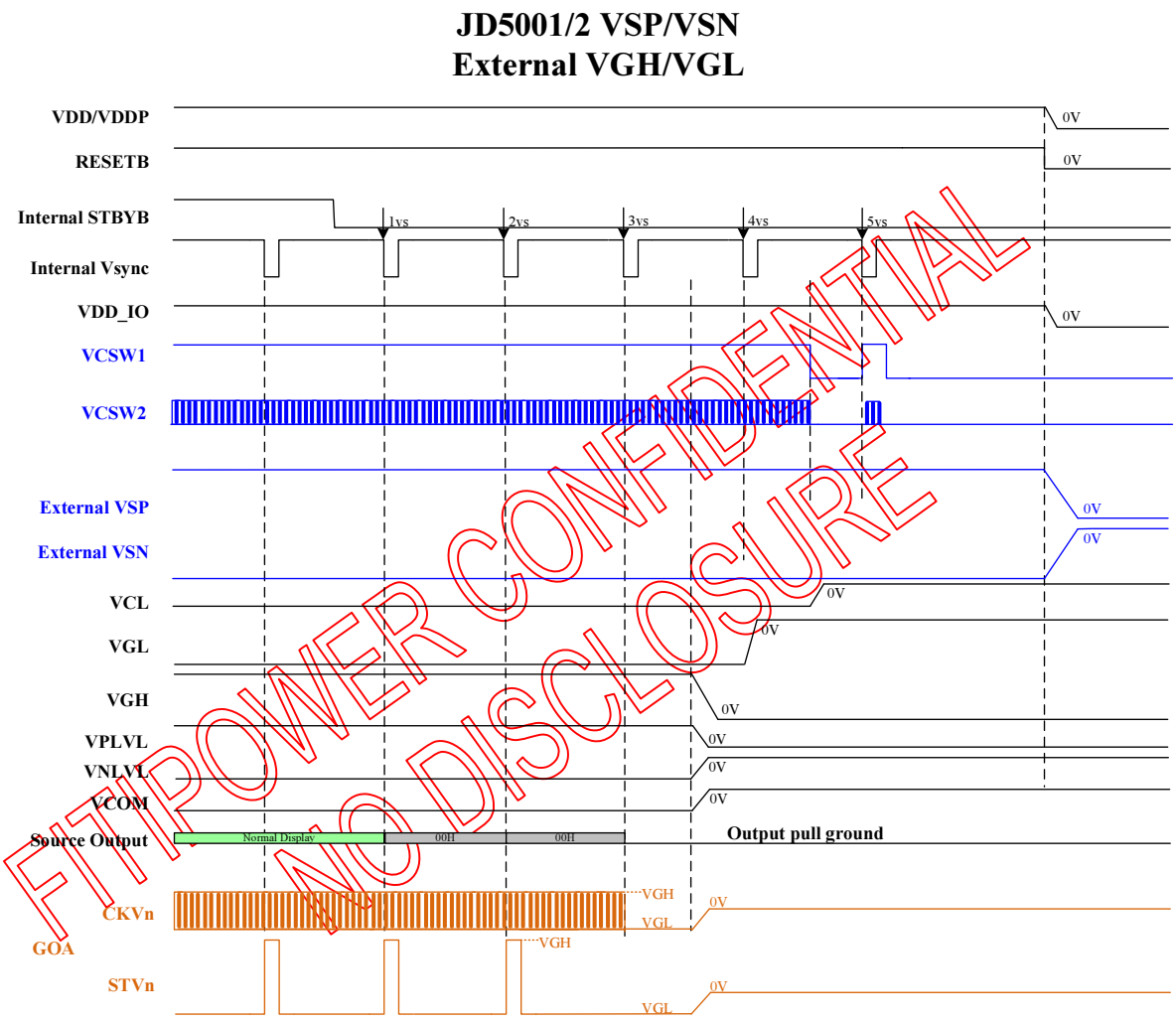


Figure 5.2: Power off sequence with PMODE[1:0]=00b

5.4.3 Power on sequence PMODE[1:0]=01b

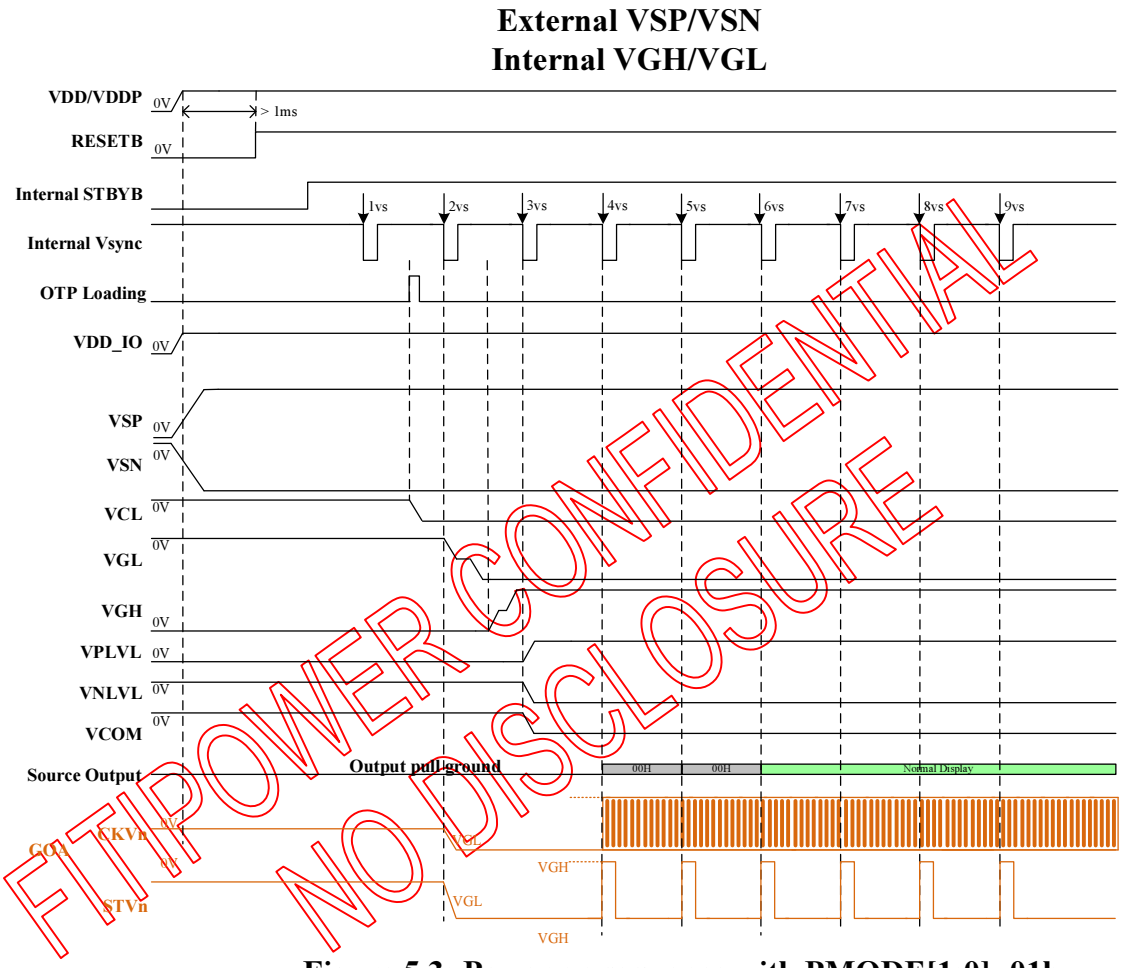


Figure 5.3: Power on sequence with PMODE[1:0]=01b

5.4.4 Power off sequence PMODE[1:0]=01b

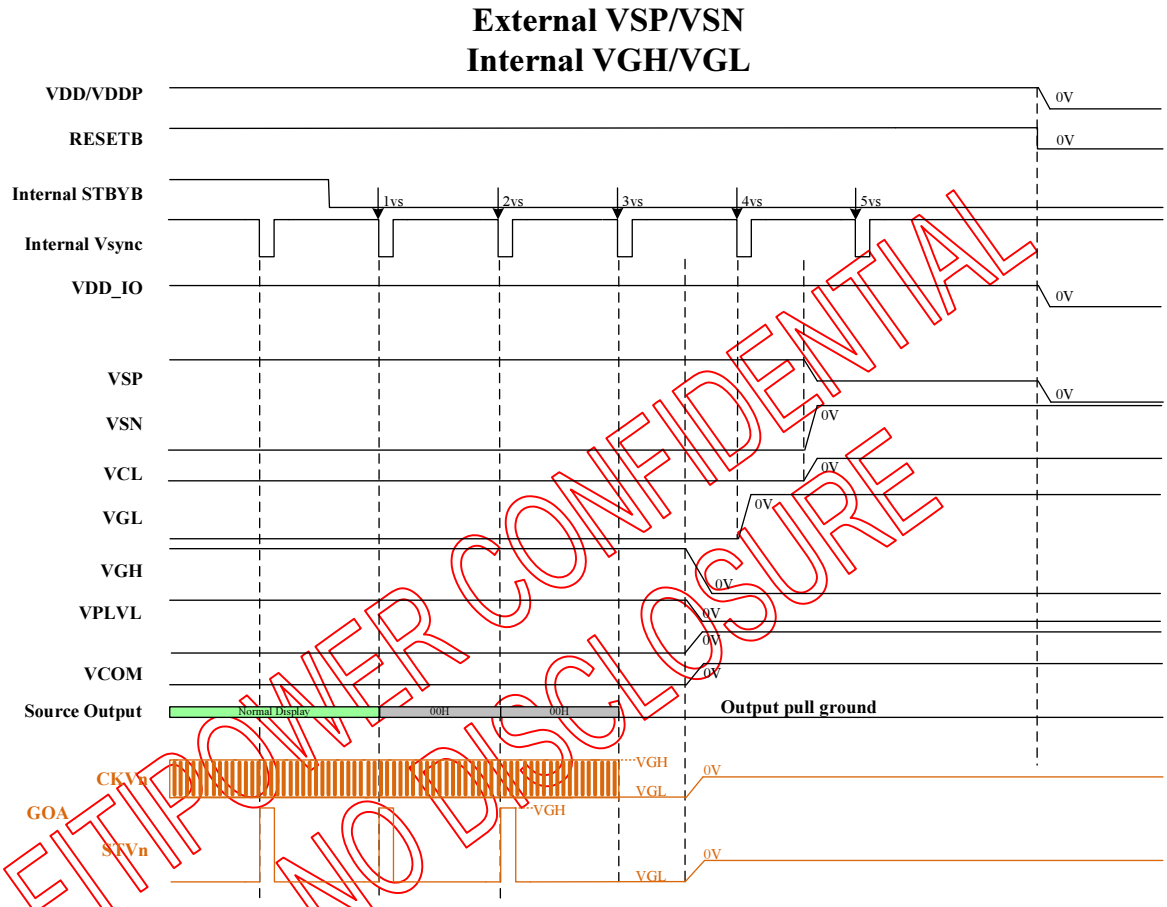


Figure 5.4: Power off sequence with PMODE[1:0]=01b

5.4.5 Power on sequence PMODE[1:0]=10b

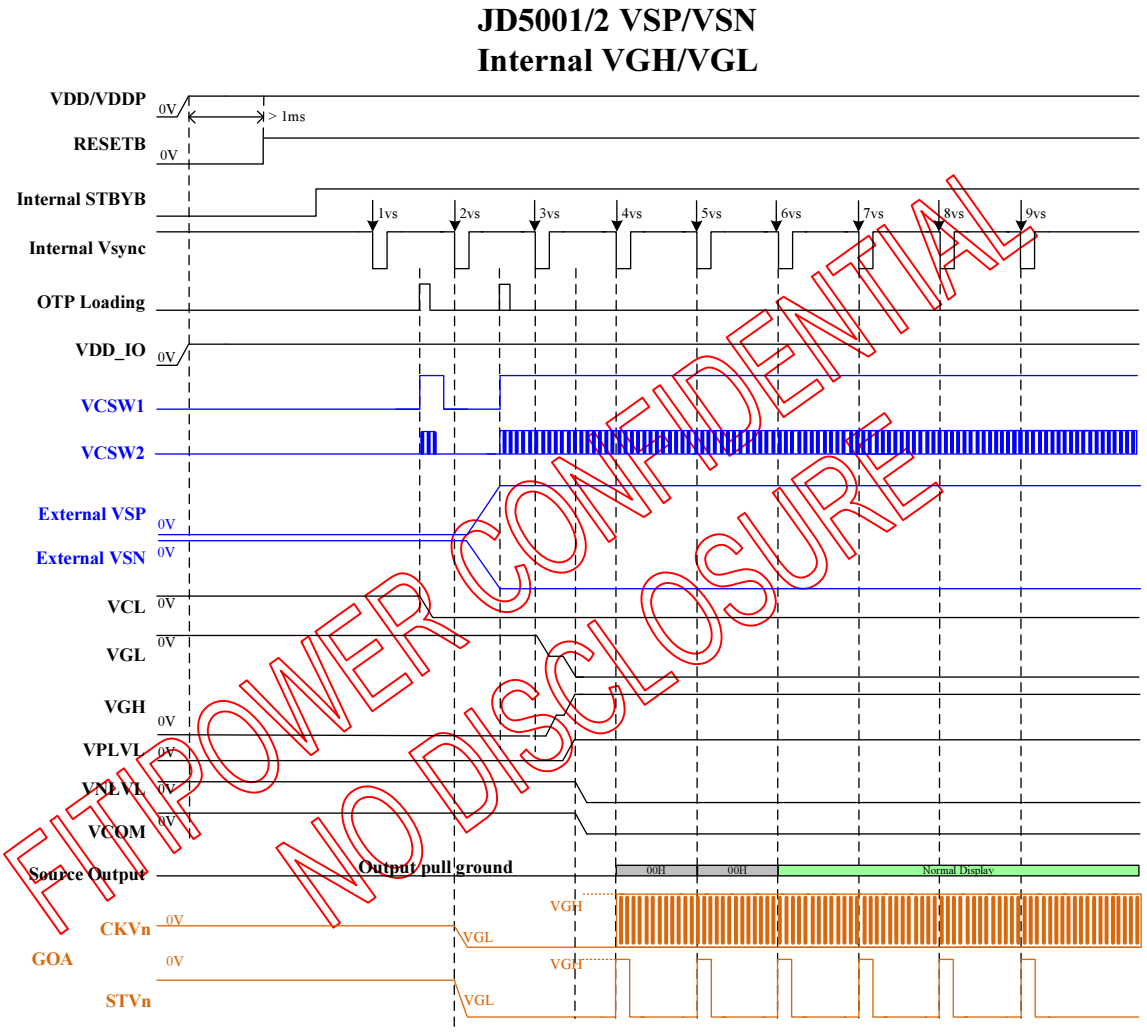


Figure 5.5: Power on sequence with PMODE[1:0]=10b

5.4.6 Power off sequence PMODE[1:0]=10b

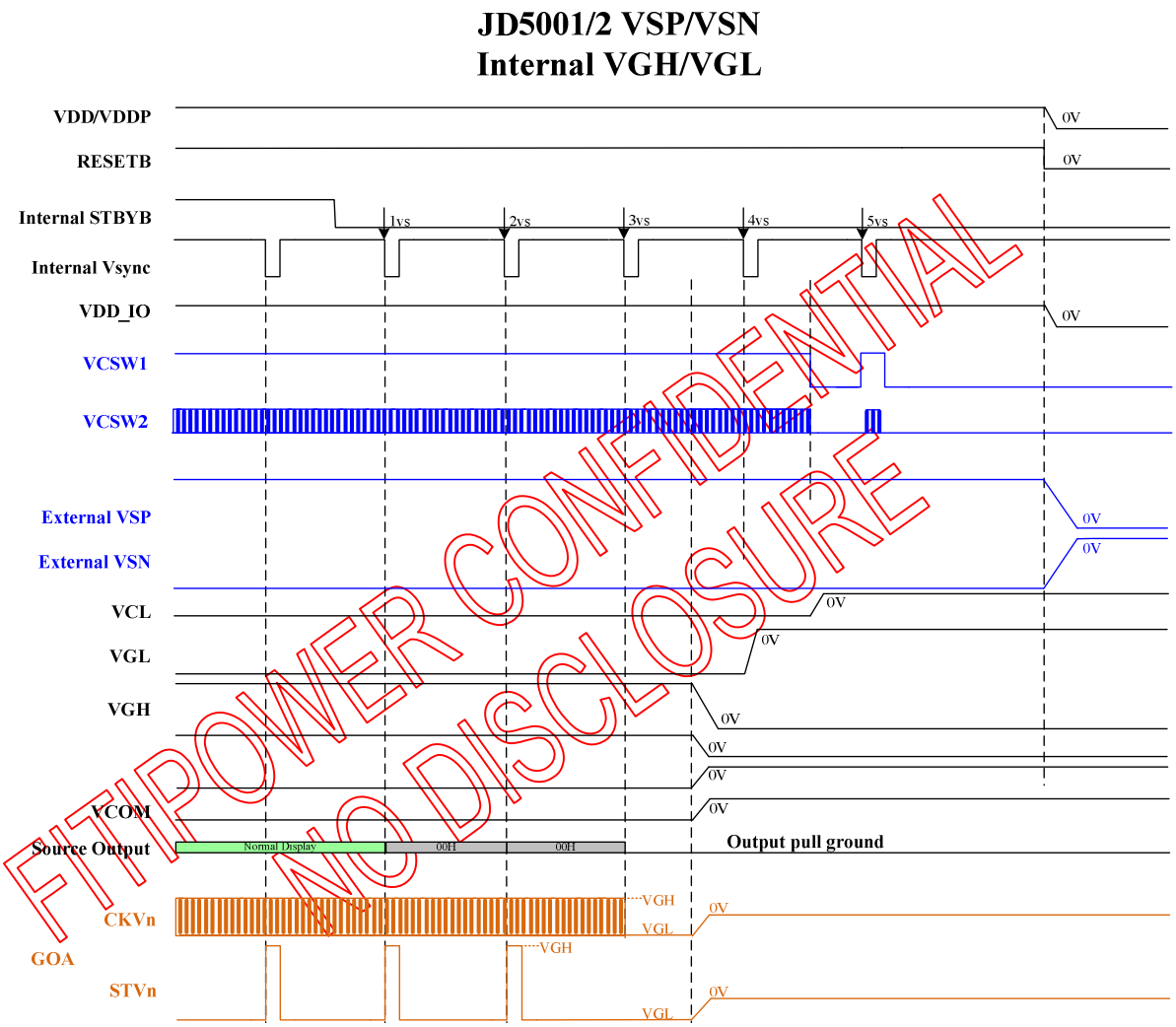


Figure 5.6: Power off sequence with PMODE[1:0]=10b

5.4.7 Power on sequence PMODE[1:0]=11b

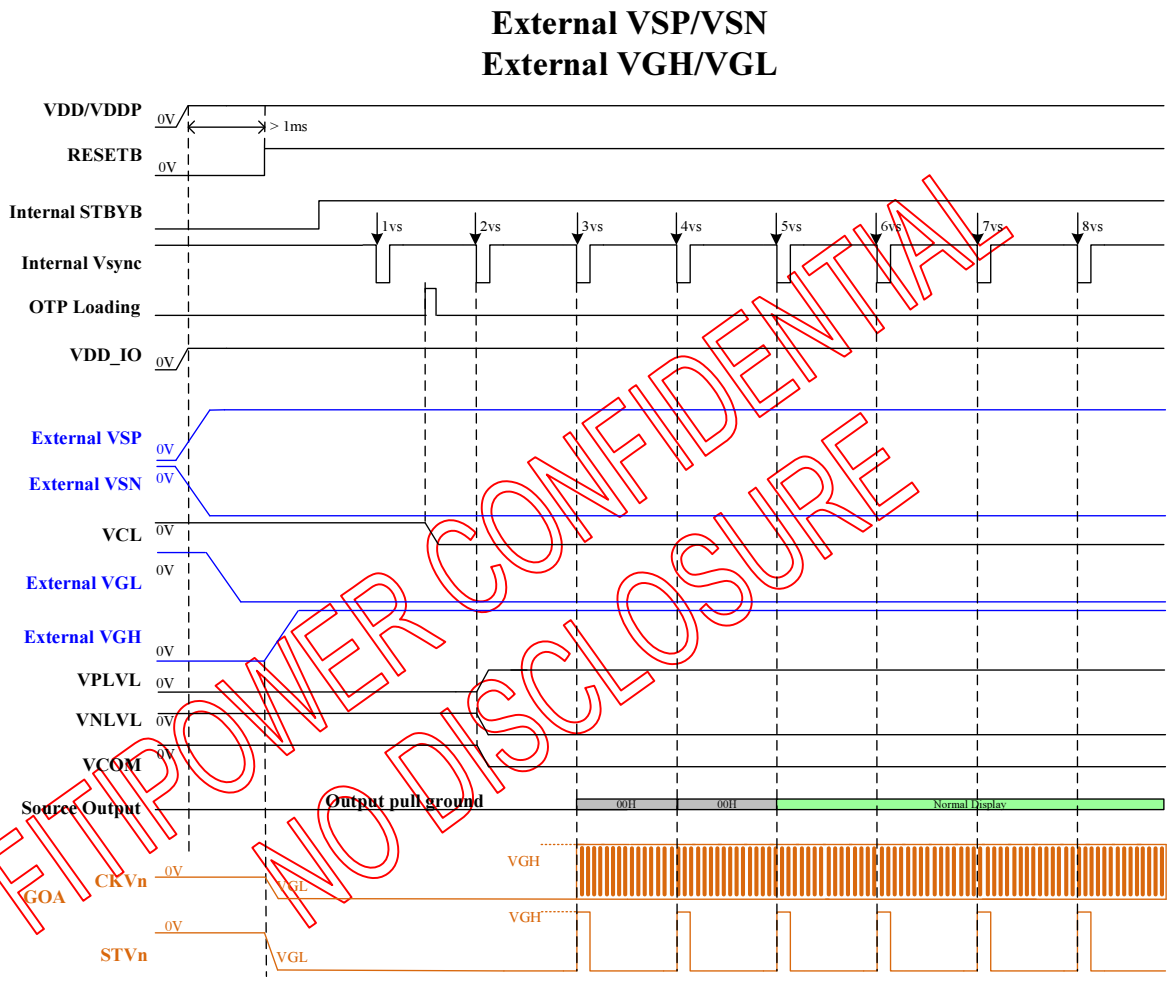


Figure 5.7: Power on sequence with PMODE[1:0]=11b

5.4.8 Power off sequence PMODE[1:0]=11b

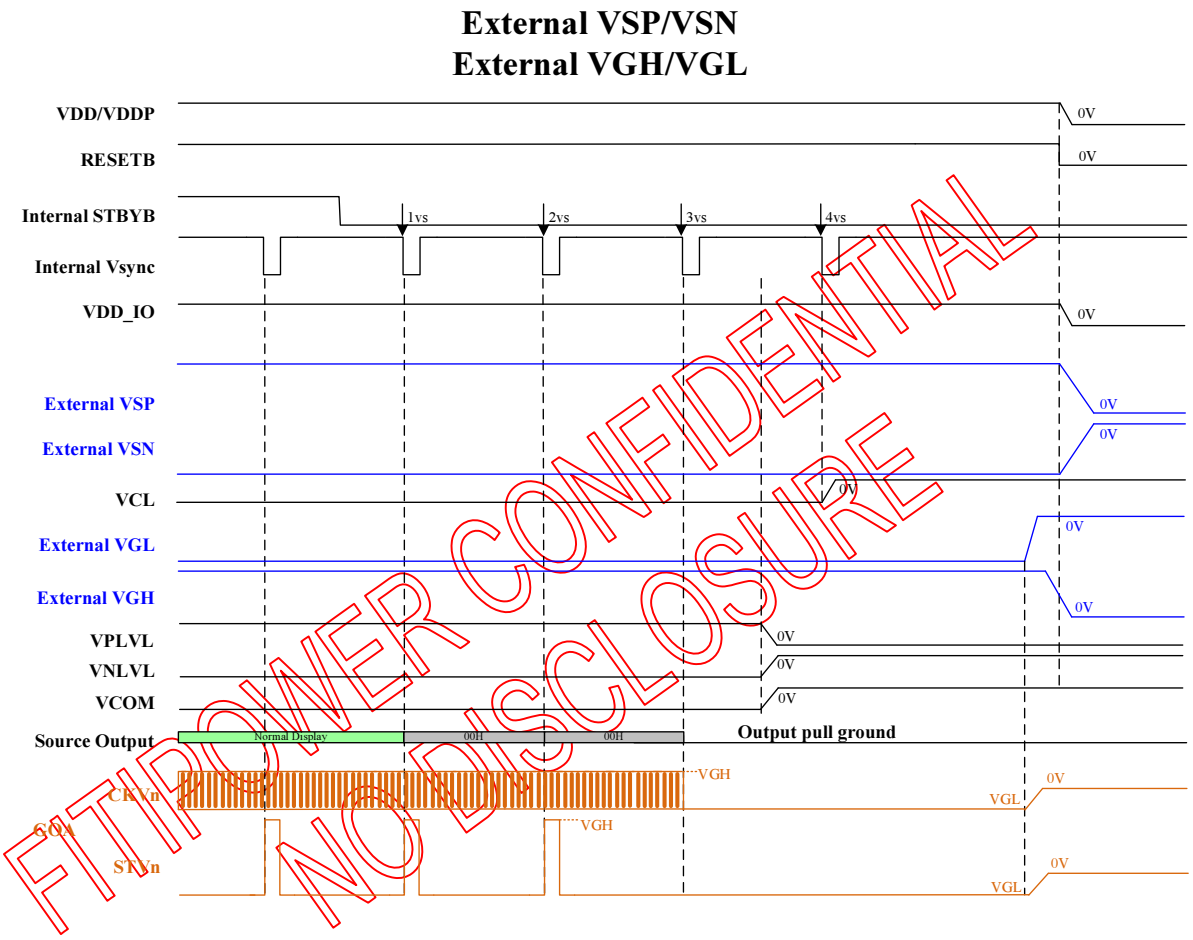


Figure 5.8: Power off sequence with PMODE[1:0]=11b

6. RECOMMEND VALUE OF WIRING RESISTANCE AND CAPACITORS

Recommended specification of wiring resistance and capacitors

Pad Name	Pin Definition	Maximum series resistance(ohm)
VDDIO,VDDIO_IF	Power supply	5
VDD,VDDP	Power supply	5
VSS,VSSA,VSS_IF,VSSP	Power supply	5
VOTP	OTP Power supply	10
RESETB,CSB,SCL,SDA,SCL_I2C,SDA_I2C	Input	100
PMODE[1:0],LANE1_STBYB,LANE0_BISTB,LNSW[1:0],RES[2:0],PNSW	Input	100
VCSW1,VCSW2,LEDPWM,LEDON,ERR_FG	Output	100
DP[0],DN[0]	Input+Output	5
DP[1],DN[1],DP[2],DN[2],DP[3],DN[3],CKP,CKN	Input	5
VCOM	Output,Capacitor connection	5
VDD_18V,VDD_18V_IF	Output,Capacitor connection	5
VSP,VSN,VCL	Output,Capacitor connection	10
VGMP,VGMN,VREF	Output,Capacitor connection	10
VGH,VGH_REG,VGL,VGL_REG	Output,Capacitor connection	10
C41P,C41N,C42P,C42N,C51P,C51N,C11P_VGL,C11N_VGL	Capacitor connection	5
GOUTL[22:1],GOUTR[22:1]	Output	50

Pad Name	Withstanding voltage (V)	CAP (uF)
VGH	25	1
VGL	25	1
VGH_REG	25	1
VGL_REG	25	1
VSP	10	1
VSN	10	1
VGMP	10	1
VGMN	10	1
VCOM	6.3	2.2
VDD/VDDP	6.3	2.2
VDDIO/VDDIO_IF	6.3	2.2
VDD_18V	6.3	1
VDD_18V_IF	6.3	1
VCL	6.3	1
VCI1	6.3	1
C41P/C41N	25	1
C42P/C42N	25	1
C51P/C51N	25	1

7. PANEL APPLICATION

The EK79030 supports the resolution of 400RGBx1280.

The TCON also can generate gate controller timing. These signals can support for general gate driver or GOA (Gate driver on Array).

7.1 GOA connection

The EK79030 can support GOA/GIP (Gate driver on array) function.

GOA output pin define can set by register. A multiplexer is built in GOA function that selects one of several GOA signals. GOA function showed as below. The detail GOA output signal setting please refer application note.

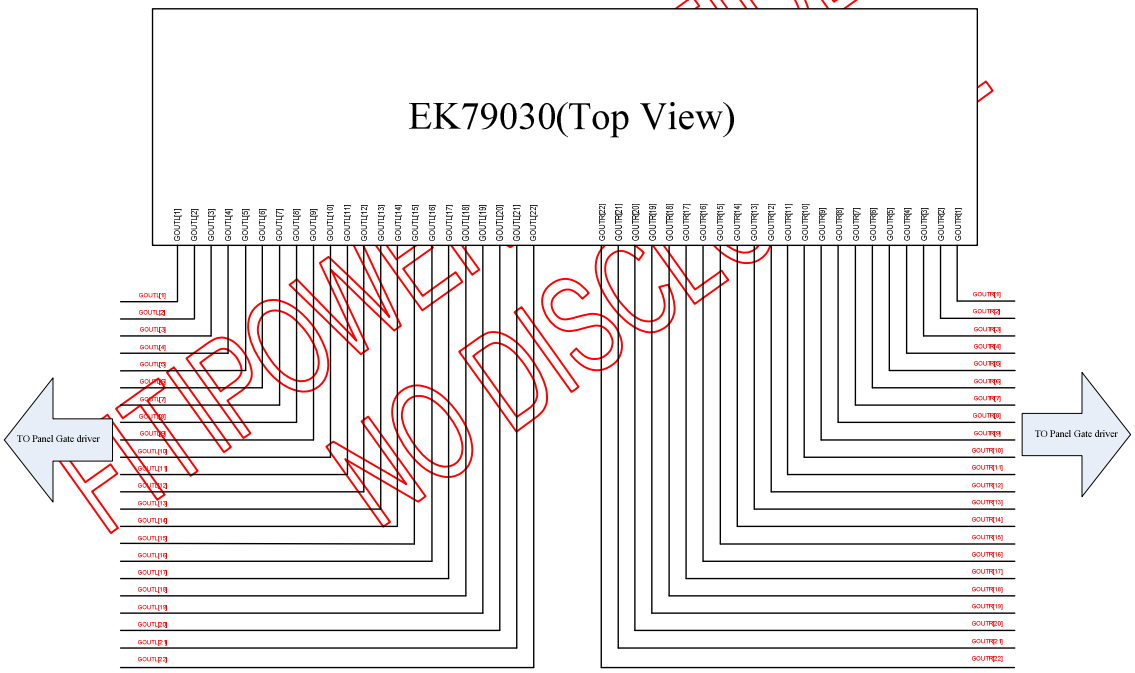


Figure 6.1 : GOA wire example

7.2 Panel Structure

7.2.1. Driving method for panel structure

EK79030 only support stripe panel type as following Figure:

7.2.1.1. Stripe driving method for panel structure

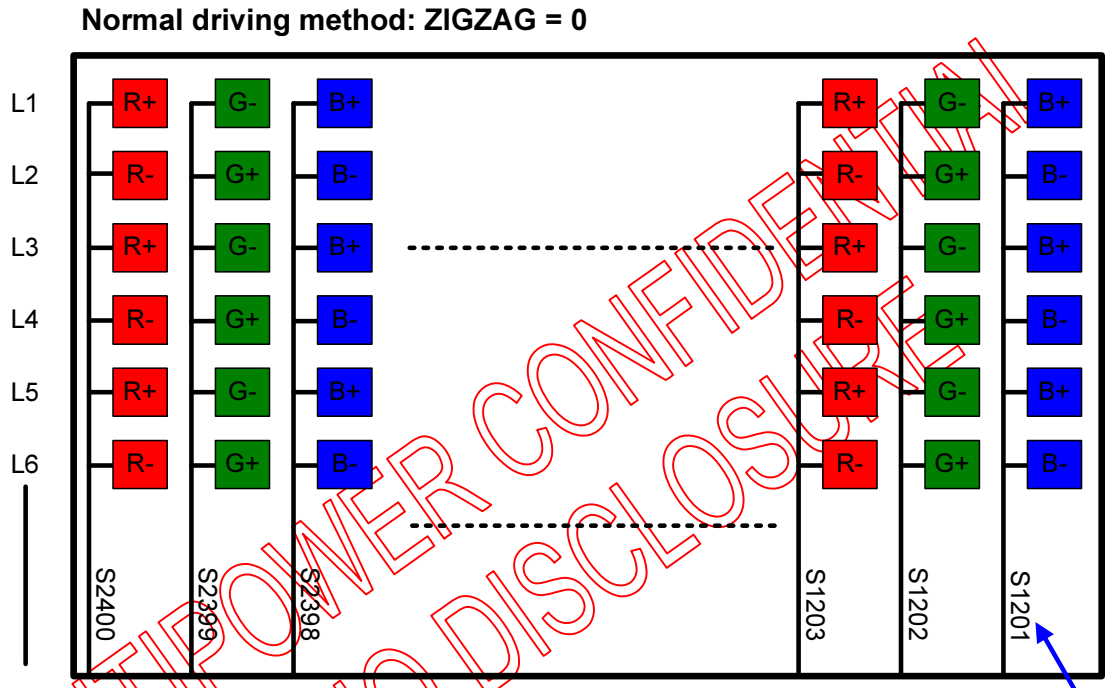
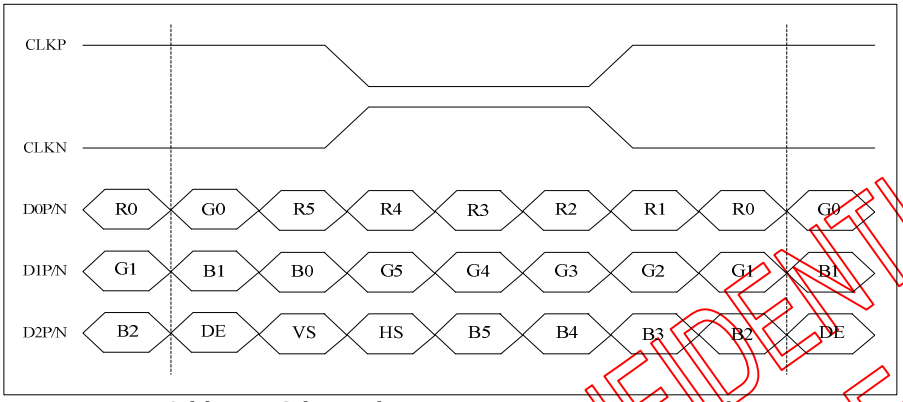


Figure 6.2 : Stripe driving method

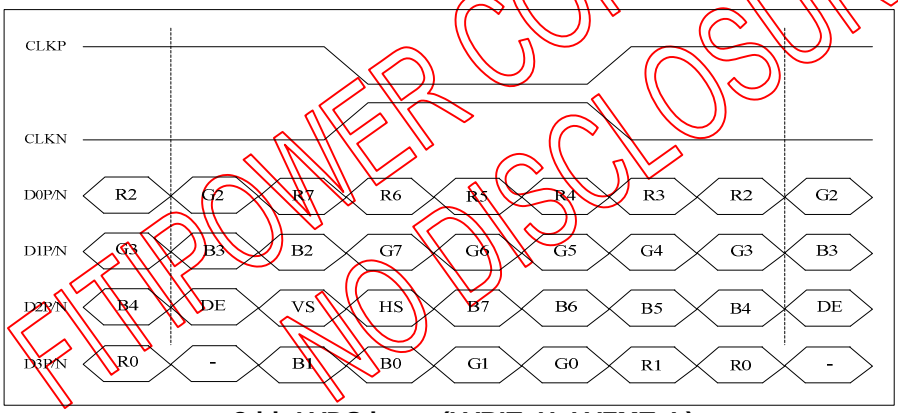
8. INTERFACE

8.1 LVDS interface

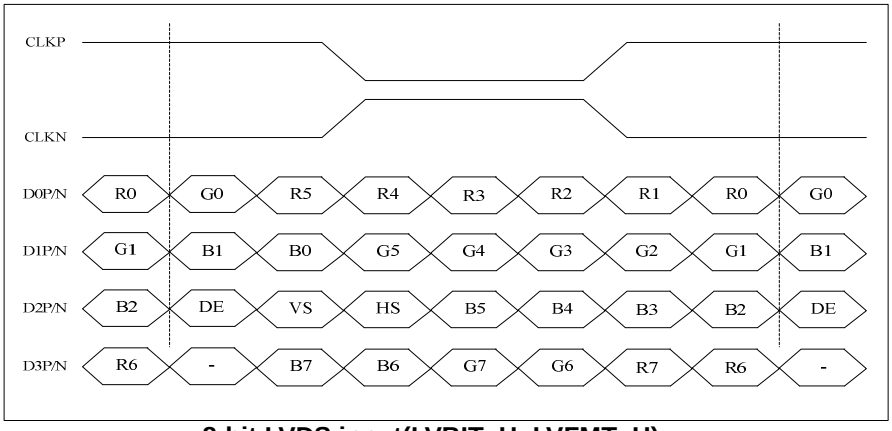
8.1.1 Data input format for LVDS



6-bit LVDS input (LVBIT=L, LVFMT=Don't care)



8-bit LVDS input (LVBIT=H, LVFMT=L)



8-bit LVDS input(LVBIT=H, LVFMT=H)

8.2 MIPI interface

8.2.1 DSI protocol

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. These terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode(saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scanline during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero.

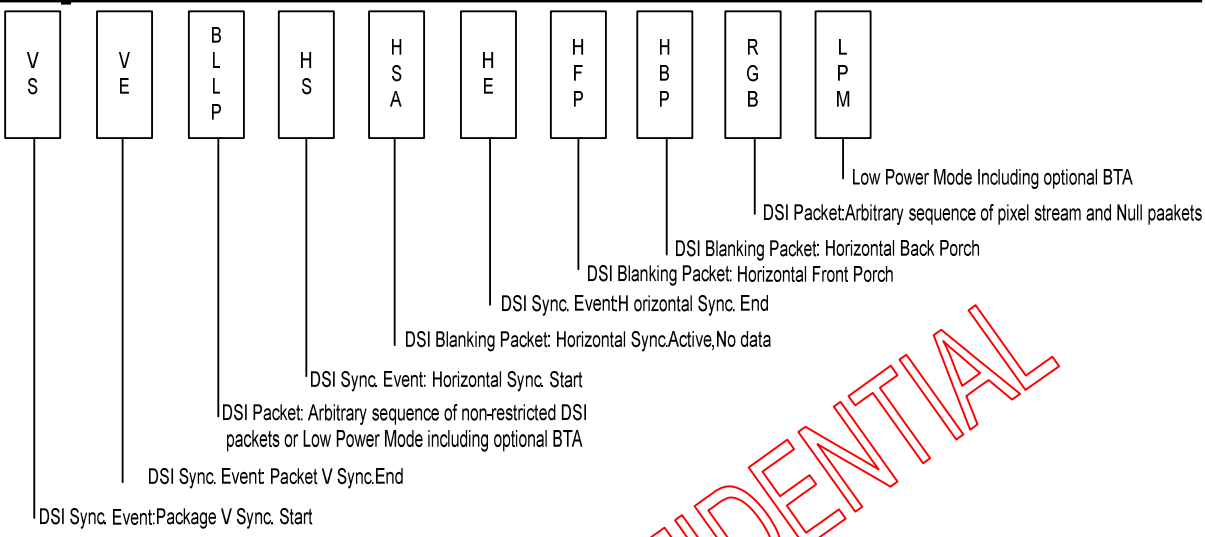
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode.
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. Individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

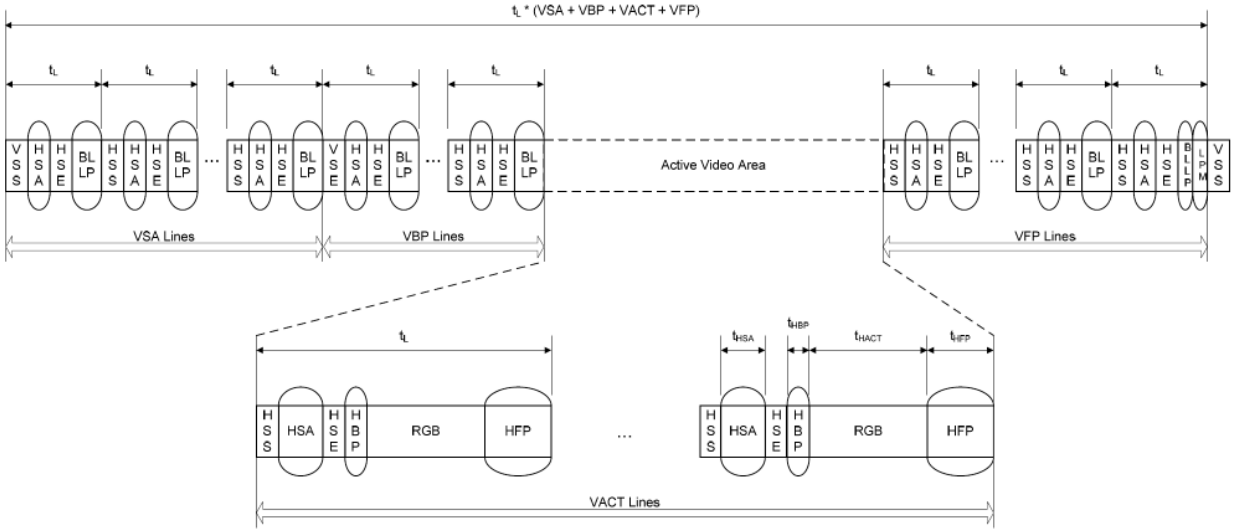
If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

Clock Requirements

A DSI host processor shall support continuous clock on the Clock Lane for display module that require it, so the host processor needs to keep the HS serial clock running.

●Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

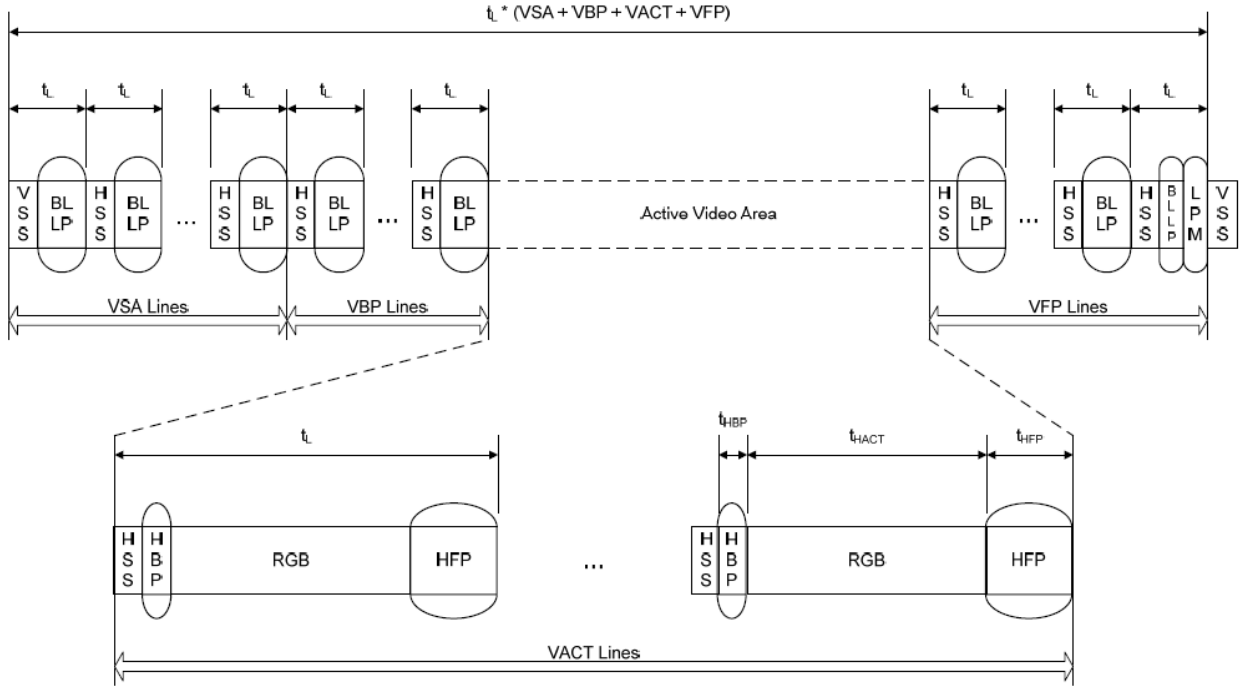


Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP

mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

●Non-Burst Mode with Sync Events

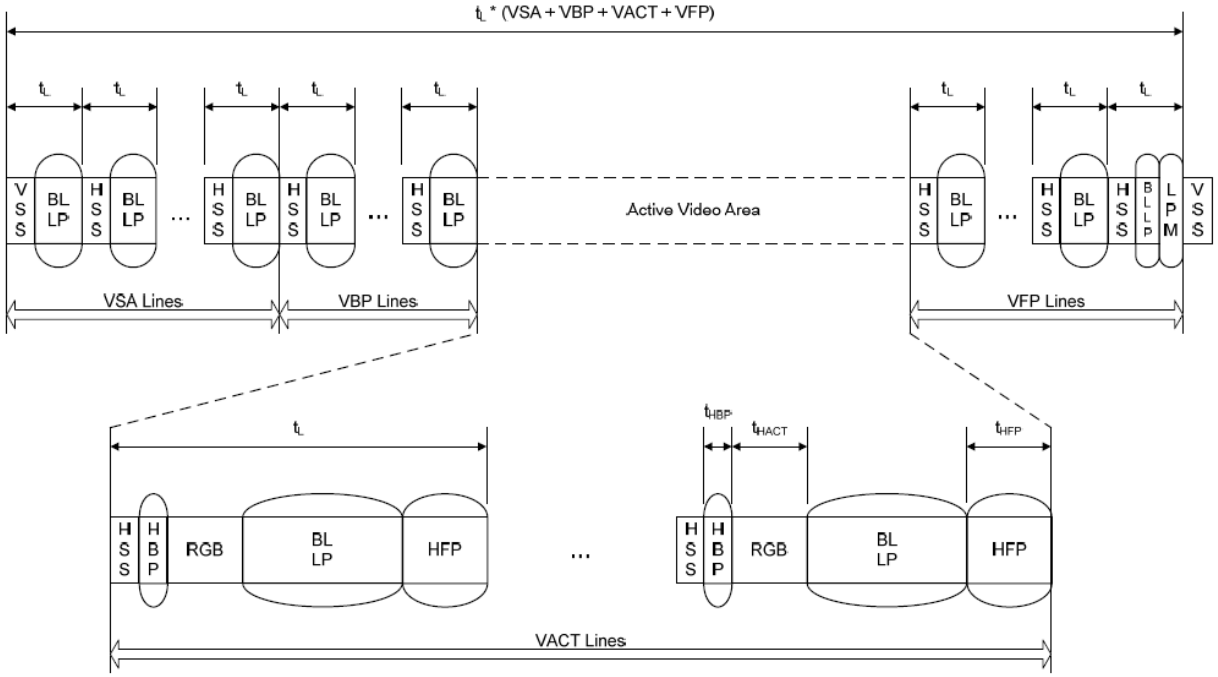
This mode is a simplification of the format described in section “Non-Burst Mode with Sync Pulse” .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.



As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

● Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.3 LVDS/MIPI Input Timing Table

For 400RGBx1280

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
MIPI (4 Lane) @Frame rate=60Hz			349		Mbps
MIPI (3 Lane) @Frame rate=60Hz			465		Mbps
DCLK frequency @Frame rate=60Hz	F_{DCLK}		58.2		MHz
HSYNC period time	T_H		744		DCLK
Horizontal display area	T_{HD}		400		DCLK
HSYNC pulse width	T_{HPW}		24	-	DCLK
HSYNC back porch	T_{HBP}		160	-	DCLK
HSYNC front porch	T_{FBP}		160	-	DCLK
VSYNC period time	T_V		1304		H
Vertical display area	T_{VD}		1280		H
VSYNC pulse width	T_{VPW}		2	-	H
VSYNC back porch	T_{VBP}		10	-	H
VSYNC front porch	T_{VFP}		12	-	H

MIPI Frequency = (Frame rate) x TH x TV x 24bits.

9. REGISTER TABLE

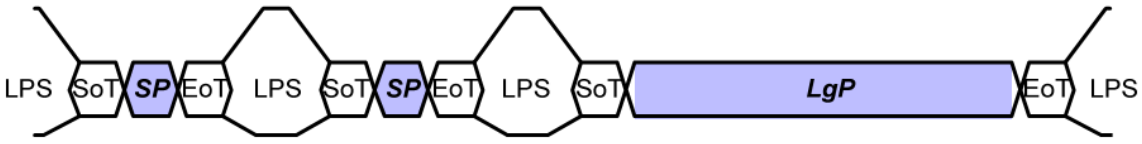
The EK79030 supports set internal register by MIPI interface, SPI interface and I2C interface. MIPI and SPI/I2C interface use different register address. The MSB bit [7] of address is only for MIPI interface. The SPI and I2C must be ignored its. “MIPI address” and “SPI/I2C address” showed in register table.

9.1 MIPI command mode control register

In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the overhead of frequent switching between LPS and High-Speed Mode will severely limit bandwidth if packets are sent separately, e.g. one packet per transmission.

The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup. The diagram illustrates as multiple packets being sent separately, and as concatenated packets in a single HS transmission.

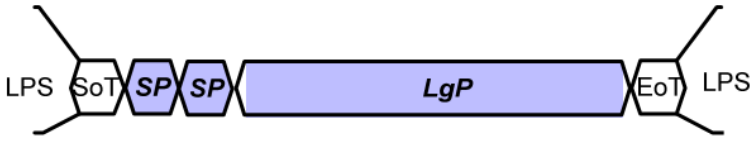
In HS Mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT between packets. This constraint does not apply to LP transmissions



Separate Transmissions

KEY:

LPS – Low Power State	SP – Short Packet
SoT – Start of Transmission	LgP – Long Packet
EoT – End of Transmission	



Single Transmission

9.2 SPI format

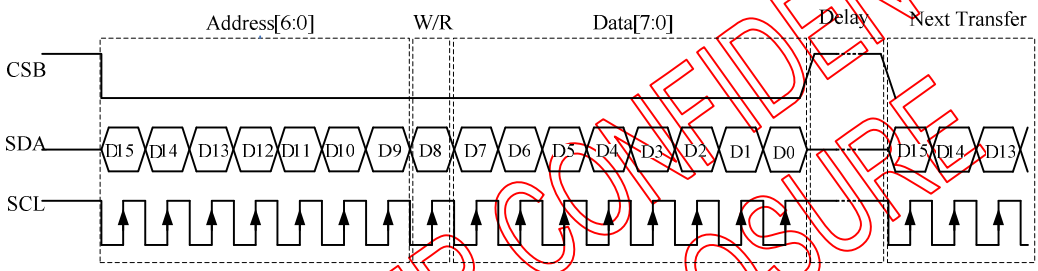
EK79030 use the 3-wire serial port as communication interface for all the function and command setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK79030 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of “3-Wire Timing. Because the 3-wire only can read/write one address. So we put the “parameter index” at the address 0x2F. When 3-wire command sends, it will refer to the address 0x2F[4:0] as the parameter index value.



3-Wire Command Format:

Bit	Description
D15-D9	Register Address [6:0]
D8	W/R control bit. “0” for Write; “1” for Read
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							0	Data (Issue by external controller)							

3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							1	Data (Issue by 3-Wire engine)							

9.3 I2C format

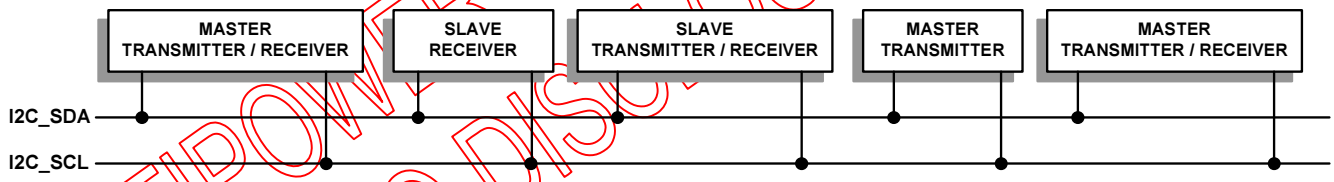
The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I²C_SDA) and the Serial Clock Line (I²C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I²C-Bus Protocol:

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

(b) Definitions:

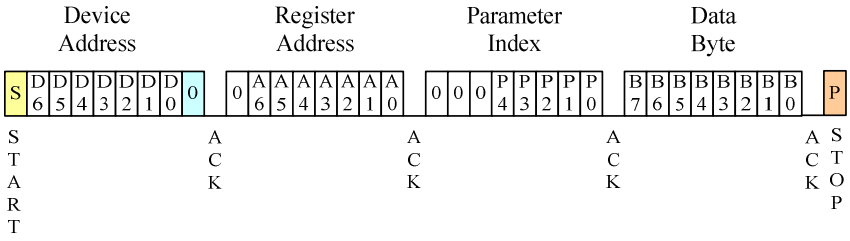
- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



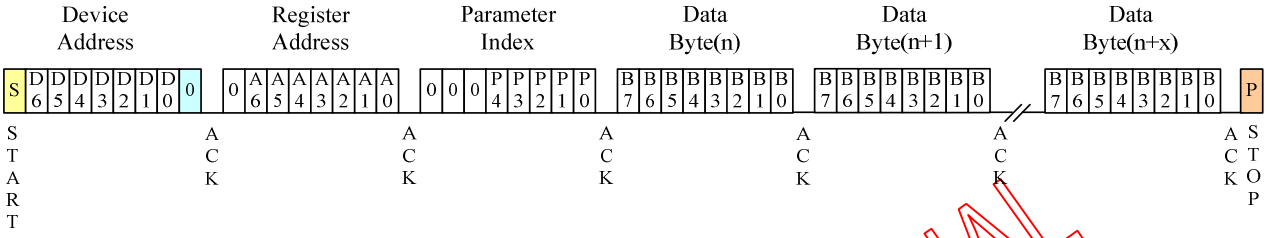
9.3.1 Register Write Sequence of I²C Interface

EK79030 supports register write sequence via I²C-bus transfer. The register writing support single register write mode and multi-register write mode. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in below.
(2) After the START condition (S), a slave address is sent. R/W bit is setting to "0" for WRITE.
(3) The slave issues an ACK to master.
(4) 8 bits register address transfer first then transfer the register data parameter.
(5) A data transfer is always terminated by a STOP condition.
(6) EK79030 DA[6:0]=110_1000



Single Register Writing Timing

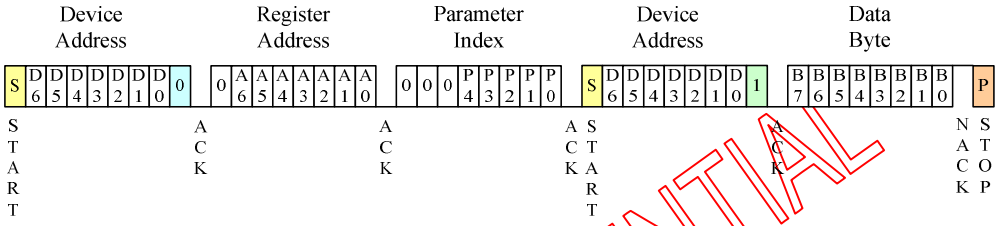


Multi Register Writing Timing

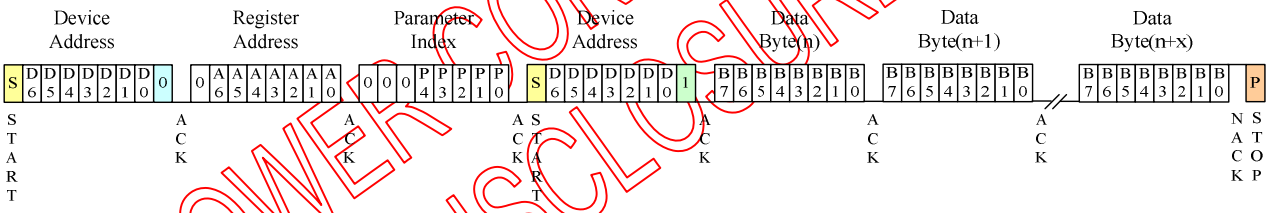
9.3.2 Register Read Sequence of I2C Interface

EK79030 supports register read sequence via I^{2}C-bus transfer. The register reading only support single register read mode.

Register data reading transfers follow the format and is shown in below.



Single Register Reading Timing



Multi Register Reading Timing

9.4 User Define Command List and Description (For MIPI command mode, SPI mode, and I2C mode)

9.4.1 User Define Command List Table

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)	Function
0xCD	1	R/W	FITI_CMD[7:0]								00	Enter FITI_CMD
0x4D	1	R/W	FITI_CMD[7:0]								00	Exit FITI_CMD
0x04	1	R	core_state[8]	-	-	-	-	-	-	-		Core_state
0x06	1	R	core_state[7:0]									
0X1B	1	R/W	-	-	-	-	-	otp_pwr_rdy	otp_prog_reg	-	00	OTP setting
0x27	1	R/W	-	-	-	-	-	otp_lock	-	-	00	
0x28	1	R/W	-	-	-	-	-	eco_pclk_ledon_sel	-	-	11	Power enable setting
0x29	1	R/W	-	-	-	-	-	-	-	res_400	10	Panel control
0x2D	1	R/W	-	-	-	VGL_REG_SEL[4:0]					11	VGL_REG voltage
0x2E	1	R/W	-	-	-	-	PWRIC_CLK1[3:0]				0E	JD5001/2 pump clock
0x2F	1	R/W	-	-	-	parameter_index[4:0]					00	parameter_index
0x30	1	R/W	LNSW[7:4]				VRES_FIX	RES[2:0]			00	Panel control
0x31	1	R/W	VRES[7:0]								9F	
0x32	1	R/W	-	STBYB	UPDNB	SHLR	-	-	NBW	BIST	00	
0x33	1	R/W	-	-	PMODE[5:4]		ZIGZAG	Z_LEFT	Z_SCAN	Z_TYPE	21	
0x34	1	R/W	-	HFRC	DITHER	LED_EN	LEDPWPOL	LEDONPOL			FC	
0x35	1	R/W	PNSW	SWDIV	RTREM_EN	LVFMT	LVBIT	MODE	INVSEL[1:0]		24	
0x36	1	R/W	-	-	-	-	BLK_SW	GOA_MODE[2:0]			41	GOA
0x39	1	R/W	-	-	-	pwm_to_pwr_sel	-	-	-	-	11	JD5001/2 pump clk
0x3A	1	R/W	-	-	goa_sel[5:4]		dummy_sel[3:0]				00	GOA
0x3D	1	R/W	-	-	-	VCOM_SET_1	-	-	-	programmed	1F	OTP setting
0x3F	1	R/W	-	-	cmd_sel	-	-	-	-	if_sel	1A	OTP/IFSEL setting
0x41	1	R/W	VCOM_SEL[7:0]								5E	VCOM voltage
0x44	1	R/W	TRIM_VDD18[7:5]			-	-	-	-	-	A8	Logic circuit power supply

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0x47	1	R/W	-	-	-	VGH_S[4:0]					14	VGH voltage
0x48	1	R/W	-	-	-	VGL_S[4:0]					66	VGL voltage
0x4E	1	R/W	-	VNLVLH_SEL[6:0]							4F	GAML voltage
0x4F	1	R/W	-	VPLVLH_SEL[6:0]							50	GAMH voltage
0x53	1	R/W	-	-	-	GP_00[4:0]					1F	Gamma positive voltage
	2	R/W	-	-	-	GP_01[4:0]					1B	
	3	R/W	-	-	-	GP_02[4:0]					19	
	4	R/W	-	-	-	GP_03[4:0]					15	
	5	R/W	-	-	-	GP_04[4:0]					15	
	6	R/W	-	-	-	GP_05[4:0]					15	
	7	R/W	-	-	-	GP_06[4:0]					17	
	8	R/W	-	-	-	GP_07[4:0]					19	
	9	R/W	-	-	-	GP_08[4:0]					19	
	10	R/W	-	-	-	GP_09[4:0]					14	
	11	R/W	-	-	-	GP_10[4:0]					11	
	12	R/W	-	-	-	GP_11[4:0]					0F	
	13	R/W	-	-	-	GP_12[4:0]					0F	
	14	R/W	-	-	-	GP_13[4:0]					0F	
	15	R/W	-	-	-	GP_14[4:0]					0C	
	16	R/W	-	-	-	GP_15[4:0]					0A	
	17	R/W	-	-	-	GP_16[4:0]					07	
	18	R/W	-	-	-	GP_17[4:0]					03	
	19	R/W	-	-	-	GP_18[4:0]					01	
0x54	1	R/W	-	-	-	GN_00[4:0]					1F	Gamma negative voltage
	2	R/W	-	-	-	GN_01[4:0]					1A	

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0x54	3	R/W	-	-	-	GN_02[4:0]					18	Gamma negative voltage
	4	R/W	-	-	-	GN_03[4:0]					14	
	5	R/W	-	-	-	GN_04[4:0]					14	
	6	R/W	-	-	-	GN_05[4:0]					14	
	7	R/W	-	-	-	GN_06[4:0]					16	
	8	R/W	-	-	-	GN_07[4:0]					18	
	9	R/W	-	-	-	GN_08[4:0]					19	
	10	R/W	-	-	-	GN_09[4:0]					15	
	11	R/W	-	-	-	GN_10[4:0]					12	
	12	R/W	-	-	-	GN_11[4:0]					0F	
	13	R/W	-	-	-	GN_12[4:0]					0E	
	14	R/W	-	-	-	GN_13[4:0]					0E	
	15	R/W	-	-	-	GN_14[4:0]					0B	
	16	R/W	-	-	-	GN_15[4:0]					09	
	17	R/W	-	-	-	GN_16[4:0]					06	
	18	R/W	-	-	-	GN_17[4:0]					03	
	19	R/W	-	-	-	GN_18[4:0]					01	
0x55	1	R/W	-	-	gstv1_rise[5:0]						00	GOA STV
	2	R/W	-	-	gstv1_fall[5:0]						0F	
	3	R/W	-	-	gstv2_rise[5:0]						00	
	4	R/W	-	-	gstv2_fall[5:0]						0F	
	5	R/W	-	-	gstv3_rise[5:0]						00	
	6	R/W	-	-	gstv3_fall[5:0]						0F	
	7	R/W	-	-	gstv4_rise[5:0]						00	
	8	R/W	-	-	gstv4_fall[5:0]						0F	

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0x56	1	R/W	-	-	gckv1_rise[5:0]						00	GOA CLK
	2	R/W	-	-	gckv1_fall[5:0]						0F	
	3	R/W	-	-	gckv2_rise[5:0]						00	
	4	R/W	-	-	gckv2_fall[5:0]						0F	
	5	R/W	-	-	gckv3_rise[5:0]						00	
	6	R/W	-	-	gckv3_fall[5:0]						0F	
	7	R/W	-	-	gckv4_rise[5:0]						00	
	8	R/W	-	-	gckv4_fall[5:0]						0F	
	9	R/W	-	-	gckv5_rise[5:0]						00	
	10	R/W	-	-	gckv5_fall[5:0]						0F	
	11	R/W	-	-	gckv6_rise[5:0]						00	
	12	R/W	-	-	gckv6_fall[5:0]						0F	
	13	R/W	-	-	gckv7_rise[5:0]						00	
	14	R/W	-	-	gckv7_fall[5:0]						0F	
	15	R/W	-	-	gckv8_rise[5:0]						00	
	16	R/W	-	-	gckv8_fall[5:0]						0F	
0x57	1	R/W	-	-	grst1_rise[5:0]						00	GOA RESET
	2	R/W	-	-	grst1_fall[5:0]						16	
	3	R/W	-	-	grst2_rise[5:0]						00	
	4	R/W	-	-	grst2_fall[5:0]						16	
	5	R/W	-	-	grst3_rise[5:0]						00	
	6	R/W	-	-	grst3_fall[5:0]						16	
	7	R/W	-	-	grst4_rise[5:0]						00	
	8	R/W	-	-	grst4_fall[5:0]						16	
0x58	1	R/W	GFLC[7:0]								08	flc toggle frequency select

Address	Parameter	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0X5E	1	R/W	-	nchg_cs_en	-	-	-	-	-	-	03	Source EQ
0X60	1	R/W	TRIM_VDD18F[7:5]			-	-	-	-	-	B0	Receiver circuit power supply
0x63	1	R/W	-	lan_sel[6:5]		-	-	-	-	-	06	MIPI lane number selection
0x65	1	R/W	-	-	-	-	goa_updn	-	-	-	08	GOA
0X67	1	R/W	phase[7:4]				ckv_width[3:0]				82	
0X68	1	R/W	ckv_blksw_revl[7:4]				flc_trans_stvsp_dis[3:0]				16	
0X69	1	R/W	stv_width[7:4]				flc_stag_trans_stvsp_dis[3:0]				27	
0X6A	1	R/W	ckv_blkpulse_stv_rise_dis[7:4]				ckv_blkpulse_stv_fall_dis[3:0]				C3	
0x6B	1	R/W	eq_fall				eq_rise				00	GOA clock EQ
0X6C	1	R/W	dummy_en	flc_stag_en	ckv_blkpulse_stagger_sel[5:4]		ckv_blkpulse_phase_sel	ckv_blkpulse_en	ckv_blksw_logic	stv_ckv_select	08	GOA
0X6D	1	R/W	-	-	-	sft_goe_scale	-	sft_goe_drct[2:1]		stv_ckv_sft	01	
0x73	1	R/W	-	-	hv_learn	de_edge_sel	-	-	-	-	30	Panel control
0x74	1	R/W	-	-	-	mipi_glp_hss_sel	-	-	-	-	10	
0x77	1	R/W	-	-	-	-	CLK_SEL_VGL[3:2]		-	-	00	VGL pump clock
0X78	1	R/W	-	-	-	VGH_REG_SEL[4:0]					47	VGH_REG voltage
0X7B	1	R/W	-	-	-	-	-	-	-	GRB	01	Global reset bit
0XFA	1	R	VENDER_id[7:0]								29	Vender ID

MIPI Address : 0xCD

Address	Bit							
0xCD	D7	D6	D5	D4	D3	D2	D1	D0
Name	FITI_CMD							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	FITI_CMD	CD=”AA” → Enter fiti command.

MIPI Address : 0x4D

Address	Bit							
0xCD	D7	D6	D5	D4	D3	D2	D1	D0
Name	FITI_CMD							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	FITI_CMD	4D=”00” → Exit fiti command.

MIPI Address : 0x04

Address	Bit							
0x04	D7	D6	D5	D4	D3	D2	D1	D0
Name	core_state[8]	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7	core_state[8]	Core state description: 04=”80” → Standby status.

MIPI Address : 0x06

Address	Bit							
0x06	D7	D6	D5	D4	D3	D2	D1	D0
Name	core_state[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:0	core_state[8]	Core state description: **core_state[8:0]** / **status** **[0,0,0,0,0,0,0,0,1]** / **Idle** **[0,0,0,0,0,0,1,0,0]** / **FreeRun** **[0,0,0,0,1,0,0,0,0]** / **MIPI vedio mode** **[0,1,0,0,0,0,0,0,0]** / **BIST**

MIPI Address : 0x1B

Address	Bit							
0x1B	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	otp_pwr_rdy	otp_prog_reg	-
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
1	otp_prog_reg	1B=”02” → OTP function enable. 1B=”00” → OTP function disable.
2	otp_pwr_rdy	1B=”06” → Enable OTP power, and blow the e-fuse. 1B=”00” → Disable OTP power.

MIPI Address : 0x27

Address	Bit							
0x27	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	otp_lock	-	-
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
1	otp_lock	27=”04” → Unlock OTP register. 27=”00” → Lock OTP register.

MIPI Address : 0x28

Address	Bit							
0x28	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	eco_pclk_ledon_sel	-	-
Default	0	0	0	1	0	0	0	1

Bit	Name	Description
2	eco_pclk_ledon_sel	28=”31” → LEDON pin output power enable signal. 28=”35” → LEDON pin output JD5001 pump clock signal.

MIPI Address : 0x29

Address	Bit							
0x29	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	res_400
Default	0	0	0	1	0	0	0	0

Bit	Name	Description
0	res_400	29=”01” → Only for 400RGBx1280 resolution. 29=”00” → Other resolution.

MIPI Address : 0x2D

Address	Bit							
0x2D	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	VGL_REG_SEL				
Default	0	0	0	1	0	0	0	1

Bit	Name	Description
4:0	VGL_REG_SEL	VGL_REG voltage selection. | VGL_REG|=|VGL|-1.

[0,0,0,0,0]	-6.000V
[0,0,0,0,1]	-6.283V
[0,0,0,1,0]	-6.579V
[0,0,0,1,1]	-6.875V
[0,0,1,0,0]	-7.178V
[0,0,1,0,1]	-7.470V
[0,0,1,1,0]	-7.760V
[0,0,1,1,1]	-8.075V
[0,1,0,0,0]	-8.347V
[0,1,0,0,1]	-8.637V
[0,1,0,1,0]	-8.947V
[0,1,0,1,1]	-9.23V
[0,1,1,0,0]	-9.55V
[0,1,1,0,1]	-9.83V
[0,1,1,1,0]	-10.13V
[0,1,1,1,1]	-10.40V
[1,0,0,0,0]	-10.74V
[1,0,0,0,1]	-11.04V
[1,0,0,1,0]	-11.29V
[1,0,0,1,1]	-11.62V
[1,0,1,0,0]	-11.90V
[1,0,1,0,1]	-12.19V
[1,0,1,1,0]	-12.52V
[1,0,1,1,1]	-12.92V
[1,1,0,0,0]	-13.18V
[1,1,0,0,1]	-13.44V
[1,1,0,1,0]	-13.44V
[1,1,0,1,1]	-13.44V
[1,1,1,0,0]	-13.44V
[1,1,1,0,1]	-13.44V
[1,1,1,1,0]	-13.44V
[1,1,1,1,1]	-13.44V

MIPI Address : 0x2E

Address	Bit							
0x2D	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	PWRIC_CLK1			
Default	0	0	0	0	1	1	1	0

Bit	Name	Description
3:0	PWRIC_CLK1	JD5001/2 pump clock [0,0,0,0] 3.69 kHz [0,0,0,1] 7.41 kHz [0,0,1,0] 14.85 kHz [0,0,1,1] 29.66 kHz [0,1,0,0] 59.49 kHz [0,1,0,1] 118.25 kHz [0,1,1,0] 177.4 kHz [0,1,1,1] 236.53 kHz [1,0,0,0] 299.73 kHz [1,0,0,1] 355.85 kHz [1,0,1,0] 408.08 kHz [1,0,1,1] 475.72 kHz [1,1,0,0] 541.23 kHz [1,1,0,1] 598.44 kHz [1,1,1,0] 632.04 kHz [1,1,1,1] 711.13 kHz

MIPI Address : 0x2F

Address	Bit							
0x2F	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	parameter_index				
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
2	parameter_index	TCON will read/write the particular parameter according to this data.

MIPI Address : 0x30

Address	Bit							
0X30	D7	D6	D5	D4	D3	D2	D1	D0
Name	LNSW				VRES_FIX	RES		
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
2:0	RES	Display resolution selection. It do XOR operation with Pin setting.
3	VRES_FIX	Display vertical Line decided by 1:VRES[7:0] 0:RES[2:0]
7:4	LNSW	MIPI lane swap. (to pin RES do XOR operation) It do XOR operation with Pin setting. LVDS lane swap. (to pin RES do XOR operation) It do XOR operation with Pin setting.

MIPI Address : 0x31

Address	Bit							
0xB1	D7	D6	D5	D4	D3	D2	D1	D0
Name	VRES							
Default	1	0	0	1	1	1	1	1

Bit	Name	Description
7:0	VRES	Vertical Resolution selection=(VRES+1)*8, range=0~255.

MIPI Address : 0x32

Address	Bit							
0x32	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	STBYB	UPDNB	SHLR	-	-	NBW	BIST
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
0	BIST	Normal Operaton / Bist pattern selection. It do XOR operation with Pin setting. (Only LVDS)
1	NBW	Normally black or normally white setting.
4	SHLR	Source Right/Left sequence control.
5	UPDNB	Gate up or Down scan control.
6	STBYB	STBYB mode selection. Timing control, Driver and DC-DC converter are off. It do XOR operation with Pin setting. (Only LVDS)

MIPI Address : 0X33

Address	Bit							
0XB3	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	PWRMD		ZIGZAG	Z_LEFT	Z_SCAN	Z_TYPE
Default	0	0	1	0	0	0	0	1

Bit	Name	Description
0	Z_TYPE	Zig-Zag driving method selection.
1	Z_SCAN	Zig-Zag panel, Source Right/Left selection.
2	Z_LEFT	Zig-Zag panel layout type selection.
3	ZIGZAG	Panel type selection.
5:4	PWRMD	Power mode selection. It do XOR operation with Pin setting.

MIPI Address : 0X34

Address	Bit							
0xB4	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	HFRC	DITHER	LED_EN	LEDPWPOL	LEDONPOL	-	-
Default	1	1	1	1	1	1	0	0

Bit	Name	Description
2	LEDONPOL	Set the enable active polarity for external LED driver control.
3	LEDPWPOL	Set the PWM active polarity for external LED driver control.
4	LED_EN	The output of LEDON / LEDPWM signal on/off control. LED_EN = 0, Disable LEDON / LEDPWM signal. LED_EN = 1, Enable LEDON / LEDPWM signal.
5	DITHER	Dithering function enable control. Dither = 0, Dither disable. Dither = 1, Dither enable.
6	HFRC	H-FRC selection. HFRC = 0, FRC enable. HFRC = 1, H-FRC enable. If DITHER = “1” and HFRC = “0”, only FRC dithering function is enabled. If DITHER = “0”, disable dithering function, H-FRC and FRC are both disabled.

MIPI Address : 0X35

Address	Bit							
0xB5	D7	D6	D5	D4	D3	D2	D1	D0
Name	PNSW	SWDIV	RTERM_EN	LVFMT	LVBIT	MODE	INVSEL	
Default	0	0	1	0	0	1	0	0

Bit	Name	Description
1:0	INVSEL	Inversion method selection. INVSEL[1:0] = “00”, 1 line inversion. INVSEL[1:0] = “01”, 2 line one dot inversion. INVSEL[1:0] = “10”, 4 line one dot inversion. INVSEL[1:0] = “11”, Column inversion.
2	MODE	DE / HV mode select for LVDS mode. MODE = 0, HV mode. MODE = 1, DE mode.
3	LVBIT	6-bit / 8-bit input select for LVDS mode. It do XOR operation with Pin setting.
4	LVFMT	8-bit input format select for LVDS mode. It do XOR operation with Pin setting.
5	RTREM_EN	Terminal resistor disenable/enable selection. (only for LVDS)
7	PNSW	MIPI Lane polarity swap. It do XOR operation with Pin setting.

MIPI Address : 0X36

Address	Bit							
0x36	D7	D6	D5	D4	D3	D2	D1	D0
Name				-	BLK_SW	GOA_MODE		
Default	0	1	0	0	0	0	0	1

Bit	Name	Description
3	BLK_SW	ckv switch at blanking 0 : ckv stops at blanking 1 : ckv keeps toggling at blanking
2:0	GOA_MODE	differenct goa timing defined by vendor

MIPI Address : 0X39

Address	Bit							
0x39	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	pwm_to_pwr_sel	-	-	-	-
Default	0	0	0	1	0	0	0	1

Bit	Name	Description
4	pwm_to_pwr_sel	JD5001/2 pump clock 0 : LEDPWM output 1 : VCSW2 output

MIPI Address : 0X3A

Address	Bit							
0x3A	D7	D6	D5	D4	D3	D2	D1	D0
Name			goa_sel		dummy_sel			
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
5:4	goa_sel	goa vendor select
3:0	dummy_sel	ckv pre-dummy select dummy_sel[0000] :all dummy_sel[0001] :1 clk dummy_sel[0010] :2 clk … dummy_sel[0010] :15 clk

MIPI Address : 0X3D

Address	Bit							
0XB3	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-		VCOM_SET_1	-	-	-	programmed
Default	0	0	0	1	1	1	1	1

Bit	Name	Description
0	programmed	programmed=1, OTP Vender_id password.
4	VCOM_SET_1	VCOM_SET_1=1, OTP VCOM password.

MIPI Address : 0X3F

Address	Bit							
0XB3	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	cmd_sel	-	-	-	-	if_sel
Default	0	0	0	1	1	0	1	0

Bit	Name	Description
0	if_sel	MIPI/LVDS I/F selection. It do XOR operation with Pin setting. if_sel = 1, MIPI I/F. if_sel = 0, LVDS I/F.
5	cmd_sel	3-wire/I2C selection. It do XOR operation with Pin setting. cmd_sel = 0, 3-wire. cmd_sel = 1, I2C.

MIPI Address : 0X41

Address	Bit							
0x44	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOM_SEL[7:0]							
Default	0	1	0	1	1	1	1	0

Bit	Name	Description
7:0	VCOM_SEL	The register is defines vender id for customer. [0,0,0,0,0,0,0,0] -0.205V [0,0,0,0,0,0,0,1] -0.217V [0,0,0,0,0,0,1,0] -0.230V [0,0,0,0,0,0,1,1] -0.243V [0,0,0,0,0,1,0,0] -0.256V : -13mv/step [0,1,0,1,1,1,0,0] -1.400V [0,1,0,1,1,1,0,1] -1.413V [0,1,0,1,1,1,1,0] -1.426V [0,1,0,1,1,1,1,1] -1.439V : -13mv/step [1,1,1,1,1,1,1,0] -3.492V [1,1,1,1,1,1,1,1] -3.505V

MIPI Address : 0X44

Address	Bit							
0x44	D7	D6	D5	D4	D3	D2	D1	D0
Name	TRIM_VDD18[7:5]			-	-	-	-	-
Default	1	0	1	0	1	0	0	0

Bit	Name	Description
7:5	TRIM_VDD18	Internal power supply for logic circuits. [0,0,0] 1.768V [0,0,1] 1.693V [0,1,0] 1.615V [0,1,1] 1.536V [1,0,0] 1.842V [1,0,1] 1.917V [1,1,0] 1.989V [1,1,1] 2.062V

MIPI Address : 0x47

Address	Bit							
0x47	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	VGH_S[4:0]				
Default	0	0	0	1	0	1	0	0

Bit	Name	Description
4:0	VGH_S	VGH voltage selection.

[0,0,0,0,0]	**7.559V**
[0,0,0,0,1]	**8.061V**
[0,0,0,1,0]	**8.657V**
[0,0,0,1,1]	**9.054V**
[0,0,1,0,0]	**9.350V**
[0,0,1,0,1]	**9.647V**
[0,0,1,1,0]	**9.946V**
[0,0,1,1,1]	**10.241V**
[0,1,0,0,0]	**10.837V**
[0,1,0,0,1]	**11.43V**
[0,1,0,1,0]	**12.02V**
[0,1,0,1,1]	**12.62V**
[0,1,1,0,0]	**12.91V**
[0,1,1,0,1]	**13.21V**
[0,1,1,1,0]	**13.50V**
[0,1,1,1,1]	**13.79V**
[1,0,0,0,0]	**14.09V**
[1,0,0,0,1]	**14.26V**
[1,0,0,1,0]	**14.26V**
[1,0,0,1,1]	**14.26V**
[1,0,1,0,0]	**14.26V**
[1,0,1,0,1]	**14.26V**
[1,0,1,1,0]	**14.26V**
[1,0,1,1,1]	**14.26V**
[1,1,0,0,0]	**14.26V**
[1,1,0,0,1]	**14.26V**
[1,1,0,1,0]	**14.26V**
[1,1,0,1,1]	**14.26V**
[1,1,1,0,0]	**14.26V**
[1,1,1,0,1]	**14.26V**
[1,1,1,1,0]	**14.26V**
[1,1,1,1,1]	**14.26V**

MIPI Address : 0x48

Address	Bit							
0x48	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	VGL_S[4:0]				
Default	0	1	1	0	0	1	1	0

Bit	Name	Description
4:0	VGL_S	VGL voltage selection.

[0,0,0,0,0]	-9.28V
[0,0,0,0,1]	-9.61V
[0,0,0,1,0]	-9.94V
[0,0,0,1,1]	-10.26V
[0,0,1,0,0]	-10.59V
[0,0,1,0,1]	-10.92V
[0,0,1,1,0]	-11.24V
[0,0,1,1,1]	-11.57V
[0,1,0,0,0]	-11.89V
[0,1,0,0,1]	-12.22V
[0,1,0,1,0]	-12.54V
[0,1,0,1,1]	-12.87V
[0,1,1,0,0]	-13.20V
[0,1,1,0,1]	-13.52V
[0,1,1,1,0]	-13.83V
[0,1,1,1,1]	-14.00V
[1,0,0,0,0]	-14.00V
[1,0,0,0,1]	-14.00V
[1,0,0,1,0]	-14.00V
[1,0,0,1,1]	-14.00V
[1,0,1,0,0]	-14.00V
[1,0,1,0,1]	-14.00V
[1,0,1,1,0]	-14.00V
[1,0,1,1,1]	-14.00V
[1,1,0,0,0]	-14.00V
[1,1,0,0,1]	-14.00V
[1,1,0,1,0]	-14.00V
[1,1,0,1,1]	-14.00V
[1,1,1,0,0]	-14.00V
[1,1,1,0,1]	-14.00V
[1,1,1,1,0]	-14.00V
[1,1,1,1,1]	-14.00V

MIPI Address : 0x4E

Address	Bit							
0x4E	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	VNLVLH_SEL[6:0]						
Default	0	1	0	0	1	1	1	1

Bit	Name	Description
6:0	VNLVLH_SEL	GAML voltage selection.

[0,0,0,0,0,0,0]	4.997V
[0,0,0,0,0,0,1]	4.997V
:	4.997V
[0,1,0,1,0,0,1]	4.997V
[0,1,0,1,0,0,1]	4.979V
[0,1,0,1,0,1,1]	4.961V
[0,1,0,1,1,0,0]	4.943V
[0,1,0,1,1,0,1]	4.925V
[0,1,0,1,1,1,0]	4.907V
[0,1,0,1,1,1,1]	4.899V
:	-18mv/step
[1,0,0,1,0,0,0]	4.455V
[1,0,0,1,0,0,1]	4.437V
[1,0,0,1,0,1,0]	4.419V
[1,0,0,1,0,1,1]	4.401V
:	-18mv/step
[1,1,1,1,1,1,1]	3.488V
[1,1,1,1,1,1,1]	3.470V

MIPI Address : 0x4F

Address	Bit							
0x4F	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	VPLVLH_SEL[6:0]						
Default	0	1	0	1	0	0	0	0

Bit	Name	Description
6:0	VPLVLH_SEL	GAMH voltage selection.

[0,0,0,0,0,0,0]	-4.997V
[0,0,0,0,0,0,1]	-4.997V
:	-4.997V
[0,1,0,1,0,0,1]	-4.997V
[0,1,0,1,0,0,1]	-4.989V
[0,1,0,1,0,1,1]	-4.971V
[0,1,0,1,1,0,0]	-4.953V
[0,1,0,1,1,0,1]	-4.935V
[0,1,0,1,1,1,0]	-4.917V
[0,1,0,1,1,1,1]	-4.899V
:	-18mv/step
[1,0,0,1,0,0,0]	-4.498V
[1,0,0,1,0,0,1]	-4.480V
[1,0,0,1,0,1,0]	-4.462V
[1,0,0,1,0,1,1]	-4.444V
:	-18mv/step
[1,1,1,1,1,1,1]	-3.508V
[1,1,1,1,1,1,1]	-3.490V

MIPI Address : 0X53

Address	Bit							
0x53	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	Positive gamma correction				
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
4:0	Positive gamma correction	For normal black type. 1. GP_00: Setting gamma positive voltage for level 255 . 2. GP_01: Setting gamma positive voltage for level 253 . 3. GP_02: Setting gamma positive voltage for level 250 . 4. GP_03: Setting gamma positive voltage for level 246 . 5. GP_04: Setting gamma positive voltage for level 240 . 6. GP_05: Setting gamma positive voltage for level 232 . 7. GP_06: Setting gamma positive voltage for level 224 . 8. GP_07: Setting gamma positive voltage for level 208 . 9. GP_08: Setting gamma positive voltage for level 176 . 10. GP_09: Setting gamma positive voltage for level 128 . 11. GP_10: Setting gamma positive voltage for level 80 . 12. GP_11: Setting gamma positive voltage for level 48 . 13. GP_12: Setting gamma positive voltage for level 30 . 14. GP_13: Setting gamma positive voltage for level 22 . 15. GP_14: Setting gamma positive voltage for level 14 . 16. GP_15: Setting gamma positive voltage for level 8 . 17. GP_16: Setting gamma positive voltage for level 4 . 18. GP_17: Setting gamma positive voltage for level 2 . 19. GP_18: Setting gamma positive voltage for level 0 . Example: GAMH=4.3V GP_00 voltage is defined as follows

[0,0,0,0,0]	**2.819V**
[0,0,0,0,1]	**2.867V**
[0,0,0,1,0]	**2.914V**
[0,0,0,1,1]	**2.962V**
[0,0,1,0,0]	**3.010V**
:	
[1,1,0,1,1]	**4.109V**
[1,1,1,0,0]	**4.157V**
[1,1,1,0,1]	**4.204V**
[1,1,1,1,0]	**4.252V**
[1,1,1,1,1]	**4.300V**

MIPI Address : 0X54

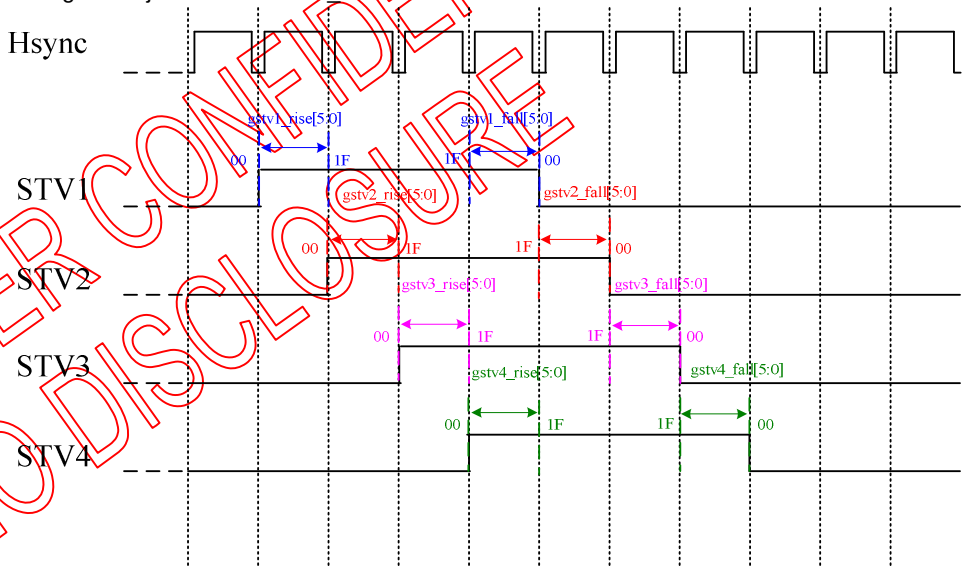
Address	Bit							
0x54	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	Negative gamma correction				
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
4:0	Negative gamma correction	For normal black type. 1. GN_00: Setting gamma negative voltage for level 255 . 2. GN_01: Setting gamma negative voltage for level 253 . 3. GN_02: Setting gamma negative voltage for level 250 . 4. GN_03: Setting gamma negative voltage for level 246 . 5. GN_04: Setting gamma negative voltage for level 240 . 6. GN_05: Setting gamma negative voltage for level 232 . 7. GN_06: Setting gamma negative voltage for level 224 . 8. GN_07: Setting gamma negative voltage for level 208 . 9. GN_08: Setting gamma negative voltage for level 176 . 10. GN_09: Setting gamma negative voltage for level 128 . 11. GN_10: Setting gamma negative voltage for level 80 . 12. GN_11: Setting gamma negative voltage for level 48 . 13. GN_12: Setting gamma negative voltage for level 30 . 14. GN_13: Setting gamma negative voltage for level 22 . 15. GN_14: Setting gamma negative voltage for level 14 . 16. GN_15: Setting gamma negative voltage for level 8 . 17. GN_16: Setting gamma negative voltage for level 4 . 18. GN_17: Setting gamma negative voltage for level 2 . 19. GN_18: Setting gamma negative voltage for level 0 . Example: GAML=-4.3V GN_00 voltage is defined as follows

[0,0,0,0,0]	**-2.819V**
[0,0,0,0,1]	**-2.867V**
[0,0,0,1,0]	**-2.914V**
[0,0,0,1,1]	**-2.962V**
[0,0,1,0,0]	**-3.010V**
:	
[1,1,0,1,1]	**-4.109V**
[1,1,1,0,0]	**-4.157V**
[1,1,1,0,1]	**-4.204V**
[1,1,1,1,0]	**-4.252V**
[1,1,1,1,1]	**-4.300V**

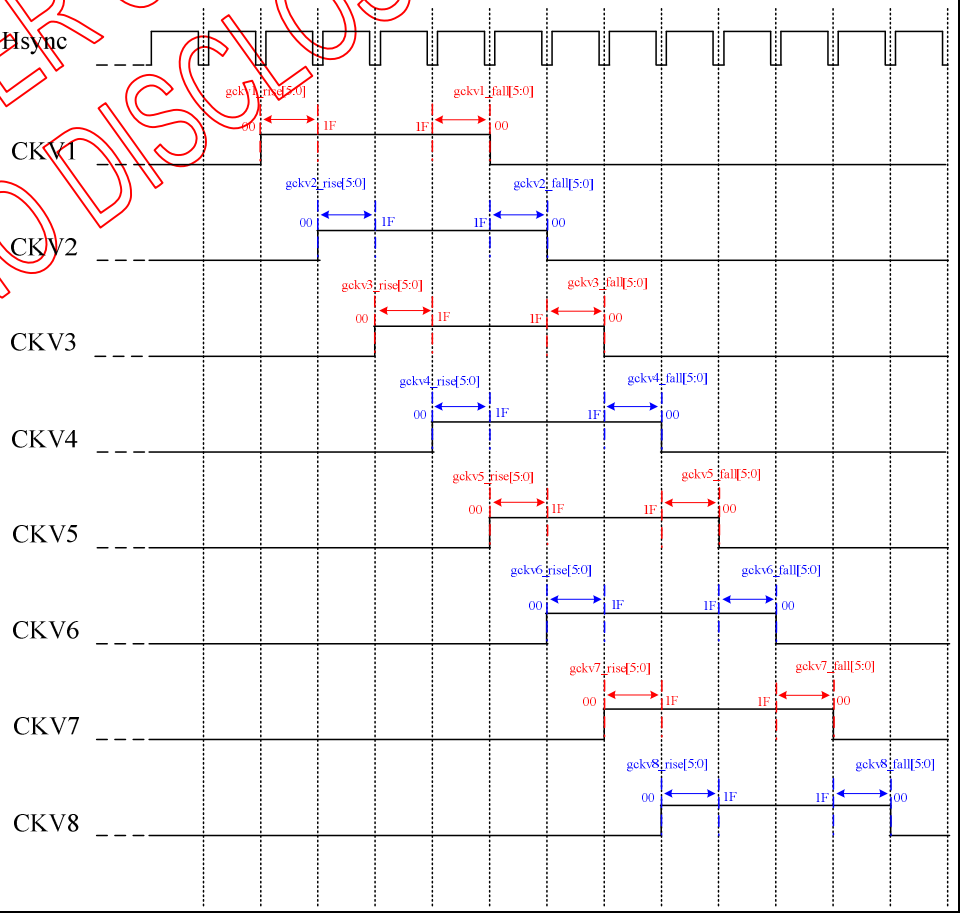
MIPI Address : 0X55

Address	Bit							
0x55	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		gstv					
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
5:0	gstv	1. gstv1_rise: Setting time between Hsync and GIP STV1 rising. 2. gstv1_fall : Setting time between Hsync and GIP STV1 falling. 3. gstv2_rise: Setting time between Hsync and GIP STV2 rising. 4. gstv2_fall : Setting time between Hsync and GIP STV2 falling. 5. gstv3_rise: Setting time between Hsync and GIP STV3 rising. 6. gstv3_fall : Setting time between Hsync and GIP STV3 falling. 7. gstv4_rise: Setting time between Hsync and GIP STV4 rising. 8. gstv4_fall : Setting time between Hsync and GIP STV4 falling. Note : range of adjustment 0~31*sft_scale 

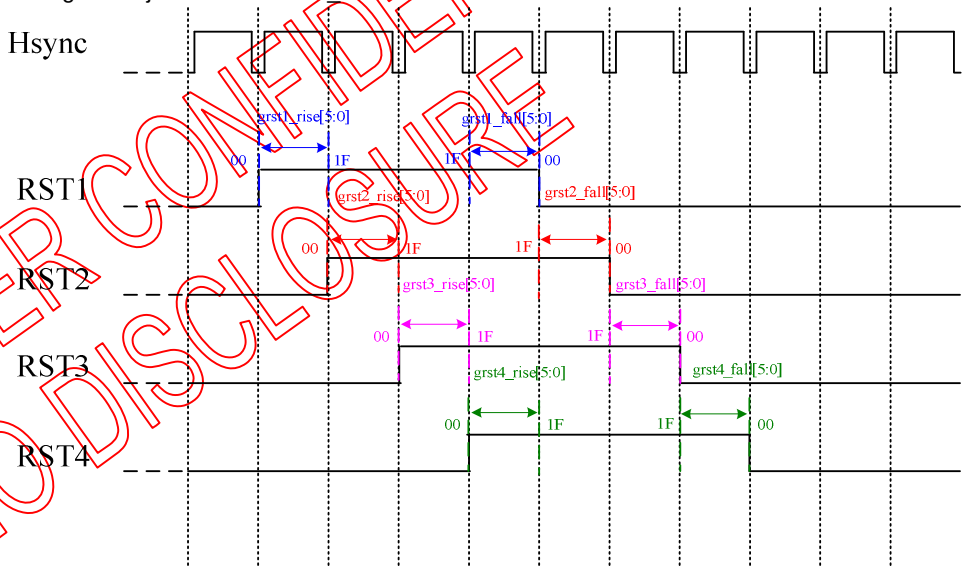
MIPI Address : 0X56

Address	Bit							
0x56	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		gckv					
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
5:0	gckv	1. gckv1_rise: Setting time between Hsync and GIP CKV1 rising. 2. gckv1_fall : Setting time between Hsync and GIP CKV1 falling. 3. gckv2_rise: Setting time between Hsync and GIP CKV2 rising. 4. gckv2_fall : Setting time between Hsync and GIP CKV2 falling. 5. gckv3_rise: Setting time between Hsync and GIP CKV3 rising. 6. gckv3_fall : Setting time between Hsync and GIP CKV3 falling. 7. gckv4_rise: Setting time between Hsync and GIP CKV4 rising. 8. gckv4_fall : Setting time between Hsync and GIP CKV4 falling. 9. gckv5_rise: Setting time between Hsync and GIP CKV5 rising. 10. gckv5_fall : Setting time between Hsync and GIP CKV5 falling. 11. gckv6_rise: Setting time between Hsync and GIP CKV6 rising. 12. gckv6_fall : Setting time between Hsync and GIP CKV6 falling. 13. gckv7_rise: Setting time between Hsync and GIP CKV7 rising. 14. gckv7_fall : Setting time between Hsync and GIP CKV7 falling. 15. gckv8_rise: Setting time between Hsync and GIP CKV8 rising. 16. gckv8_fall : Setting time between Hsync and GIP CKV8 falling. Note : range of adjustment 0~31*stf_scale 

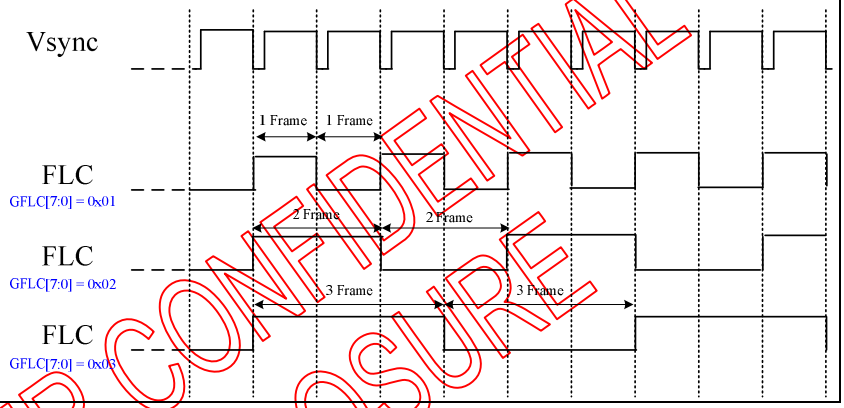
MIPI Address : 0X57

Address	Bit							
0x57	D7	D6	D5	D4	D3	D2	D1	D0
Name	-		grst					
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
5:0	grst	1. grst1_rise : Setting time between Hsync and GIP RST1 rising. 2. grst1_fall : Setting time between Hsync and GIP RST1 falling. 3. grst2_rise: Setting time between Hsync and GIP RST2 rising. 4. grst2_fall : Setting time between Hsync and GIP RST2 falling. 5. grst3_rise: Setting time between Hsync and GIP RST3 rising. 6. grst3_fall : Setting time between Hsync and GIP RST3 falling. 7. grst4_rise: Setting time between Hsync and GIP RST4 rising. 8. grst4_fall : Setting time between Hsync and GIP RST4 falling. Note : range of adjustment 0~31*sft_scale 

MIPI Address : 0X58

Address	Bit							
0x58	D7	D6	D5	D4	D3	D2	D1	D0
Name	GFLC							
Default	0	0	0	0	1	0	0	0

Bit	Name	Description
7:0	GFLC	GFLC : flc toggle frequency select Note : range of adjustment 1~255 Frame , 0 is diable 

MIPI Address : 0X5E

Address	Bit							
0x5E	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	nchg_cs_en	-	-	-	-	-	-
Default	0	0	0	0	0	0	1	1

Bit	Name	Description
6	nchg_cs_en	Source EQ 0 : Disable 1 : Enable

MIPI Address : 0X60

Address	Bit							
0x60	D7	D6	D5	D4	D3	D2	D1	D0
Name	TRIM_VDD18F[7:5]							
Default	1	0	1	1	0	0	0	0

Bit	Name	Description
7:5	TRIM_VDD18F	Internal power supply for MIPI/LVDS circuits.

[0,0,0]	**1.763V**
[0,0,1]	**1.690V**
[0,1,0]	**1.615V**
[0,1,1]	**1.539V**
[1,0,0]	**1.834V**
[1,0,1]	**1.905V**
[1,1,0]	**1.976V**
[1,1,1]	**2.046V**

MIPI Address : 0X63

Address	Bit							
0x65	D7	D6	D5	D4	D3	D2	D1	D0
Name		lan_sel			-		-	
Default	0	0	0	0	0	1	1	0

Bit	Name	Description
6:5	lan_sel	MIPI lane number selection It do XOR operation with Pin setting.

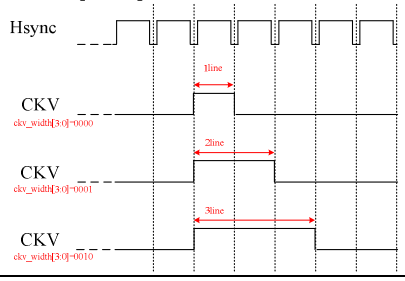
MIPI Address : 0X65

Address	Bit							
0x65	D7	D6	D5	D4	D3	D2	D1	D0
Name	-				goa_updn		-	
Default	0	0	0	0	1	0	0	0

Bit	Name	Description
3	goa_updn	GIP signal Scan direction 1: Forward 0: Backward

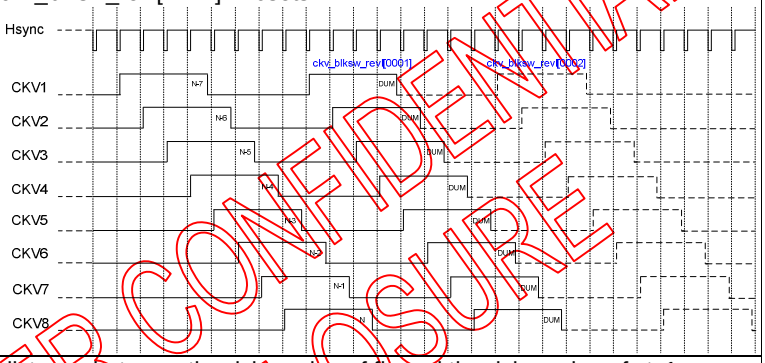
MIPI Address : 0X67

Address	Bit							
0x67	D7	D6	D5	D4	D3	D2	D1	D0
Name	phase				ckv_width			
Default	1	0	0	0	0	0	1	0

Bit	Name	Description
7:4	phase	ckv phase select. phase[0000] : 2phase phase[0001] : 2phase phase[0010] : 2phase phase[0011] : 3phase phase[0100] : 4phase phase[0101] : 5phase … phase[1111] : 12phase
3:0	ckv_width	ckv width ckv width[0000] : 1line ckv width[0001] : 2line ckv width[0010] : 3line … ckv width[1111] : 16line 

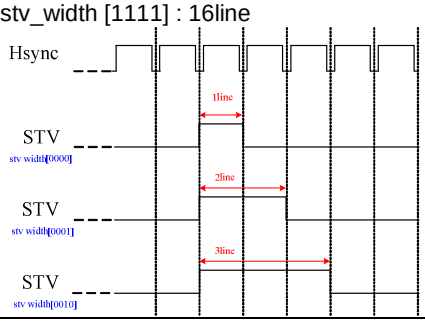
MIPI Address : 0X68

Address	Bit							
0x68	D7	D6	D5	D4	D3	D2	D1	D0
Name	ckv_blksw_revl				flc_trans_stvsp_dis			
Default	0	0	0	1	0	1	1	0

Bit	Name	Description
7:4	ckv_blksw_revl	when ckv keeps toggling at blanking, the quantity of sets of ckv. ckv_blksw_revl[0000] : 1sets ckv_blksw_revl[0001] : 2sets ckv_blksw_revl[0010] : 3sets … ckv_blksw_revl[1111] : 16sets 
3:0	flc_trans_stvsp_dis	distance between the rising edge of flc and the rising edge of stv1 flc_trans_stvsp_dis[0000] : 0line flc_trans_stvsp_dis[0001] : 1line … flc_trans_stvsp_dis[1111] : 15line

MIPI Address : 0X69

Address	Bit							
0x69	D7	D6	D5	D4	D3	D2	D1	D0
Name	stv_width				flc_stag_trans_stvsp_dis			
Default	0	0	1	0	0	1	1	1

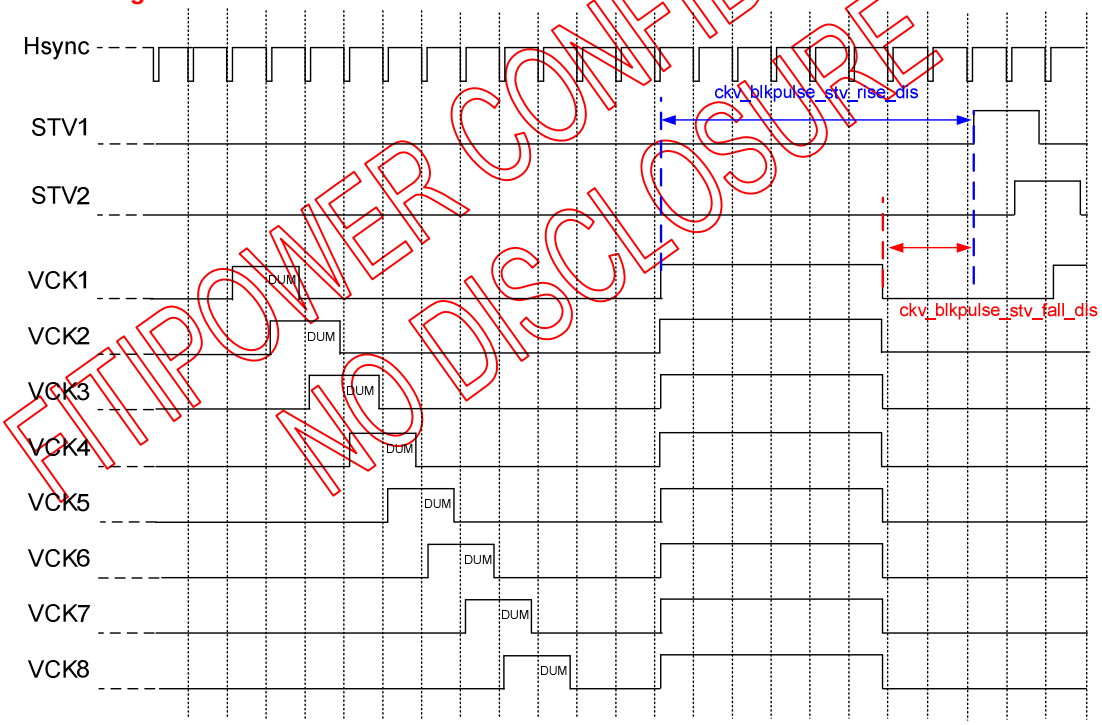
Bit	Name	Description
7:4	stv_width	stv width. stv_width [0000] : 1line stv_width [0001] : 2line … stv_width [1111] : 16line 
3:0	flc_stag_trans_stvsp_dis	distance between the falling edge of flc and the rising edge of stv1 flc_stag_trans_stvsp_dis[0000] : 0lime flc_stag_trans_stvsp_dis[0001] : 1lime … flc_stag_trans_stvsp_dis[1111] : 1lime

MIPI Address : 0X6A

Address	Bit							
0x6A	D7	D6	D5	D4	D3	D2	D1	D0
Name	ckv_blkpulse_stv_rise_dis				ckv_blkpulse_stv_fall_dis			
Default	1	0	1	0	0	0	1	0

Bit	Name	Description
7:4	ckv_blkpulse_stv_rise_dis	distance between the rising edge of ckv xon and the rising edge of stv1. ckv_blkpulse_stv_rise_dis[0000] : 0line ckv_blkpulse_stv_rise_dis[0001] : 1line … ckv_blkpulse_stv_rise_dis[1111] : 15line
3:0	ckv_blkpulse_stv_fall_dis	distance between the falling edge of ckv xon and the rising edge of stv1 ckv_blkpulse_stv_fall_dis[0000] : 0line ckv_blkpulse_stv_fall_dis[0001] : 1line … ckv_blkpulse_stv_fall_dis[1111] : 15line

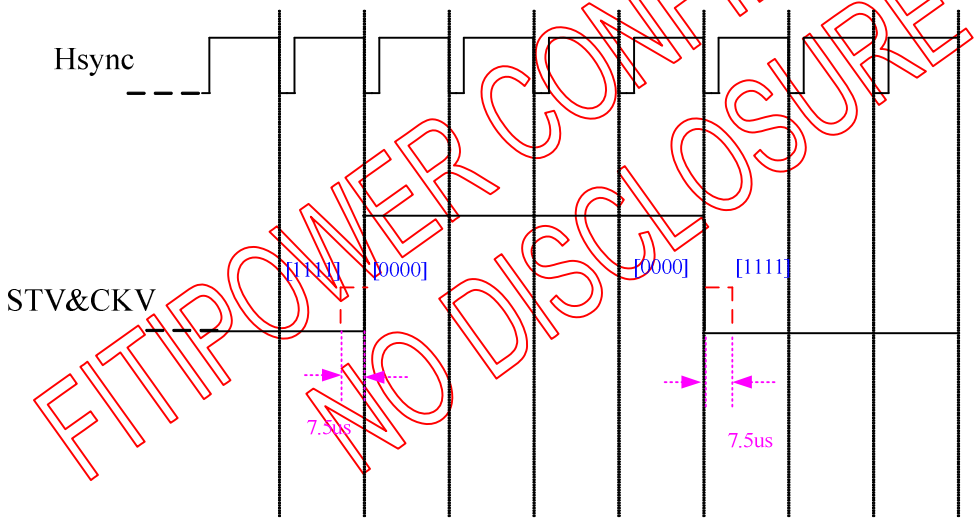
GIP timing



MIPI Address : 0X6B

Address	Bit							
0x6B	D7	D6	D5	D4	D3	D2	D1	D0
Name	eq_fall				eq_rise			
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
7:4	eq_fall	eq time select for falling edge [0000] : disable [0001] : 0.5us [0010] : 1us … [1111] : 7.5us
3:0	eq_rise	eq time select for rising edge [0000] : disable [0001] : 0.5us [0010] : 1us … [1111] : 7.5us



MIPI Address : 0X6C

Address	Bit							
0x6C	D7	D6	D5	D4	D3	D2	D1	D0
Name	dummy_en	flc_stag_en	ckv_blkpulse_stagger_sel		ckv_blkpulse_phase_sel	ckv_blkpulse_en	ckv_blksw_logic	stv_ckv_select
Default	0	0	0	0	1	0	0	0

Bit	Name	Description
7	dummy_en	ckv pre-dummy
6	flc_stag_en	the relation between flc1 and flc2 0 : not stagger 1 : stagger
5:4	ckv_blkpulse_stagger_sel	stagger time select for ckv blanking xon [00] : disable [01] : 0.5u [10] : 1u [11] : 1.5u
3	ckv_blkpulse_phase_sel	stagger phase select for ckv blanking xon 0 : 2 phase 1 : 4 phase
2	ckv_blkpulse_en	when ckv stops at blanking, ckv xon at blanking 0 : disable 1 : enable
1	ckv_blksw_logic	ckv logic when ckv stops at blanking 0 : logic 0 1 : logic 1
0	stv_ckv_select	the relation between stv and ckv 0 : overlap 1 : stagger

MIPI Address : 0X6D

Address	Bit							
0x6D	D7	D6	D5	D4	D3	D2	D1	D0
Name		-		sft_goe_scale	-	sft_goe_drct		stv_ckv_sft
Default	0	0	0	0	0	0	0	1

Bit	Name	Description
4	sft_goe_scale	sft_dat scale 0 : 8*osc_clk 1 : 24*osc_clk
2:1	sft_goe_drct	sft_goe_drct rising forward, falling backward (default)
0	stv_ckv_sft	the shift between stv and ckv when overlap 0 : 1 line 1 : 2line

MIPI Address : 0X73

Address	Bit							
0x73	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	hv_learn	de_edge_sel	-	-	-	-
Default	0	0	1	1	0	0	0	1

Bit	Name	Description
4	de_edge_sel	set Gate clock falling location depend on DE rising or DE falling in MIPI mode. 0 : Rising 1 : Falling
5	hv_learn	learning H line length and V line numbers from TX, not reference RES setting value. 0:Non-Learning 1: Learning

MIPI Address : 0X74

Address	Bit							
0x74	D7	D6	D5	D4	D3	D2	D1	D0
Name	-			mipi_gip_hss_sel				
Default	0	0	0	1	0	0	0	0

Bit	Name	Description
4	mipi_gip_hss_sel	GIP reference H sync / V sync pulse from TX in MIPI mode. 0 : Disable 1 : Enable

MIPI Address : 0X77

Address	Bit							
0x77	D7	D6	D5	D4	D3	D2	D1	D0
Name	-			-	CLK_SEL_VGL		-	-
Default	0	0	0	1	0	0	0	0

Bit	Name	Description
4	CLK_SEL_VGL	VGL pump clock frequency selection.

MIPI Address : 0x78

Address	Bit							
0x78	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	VGH_REG_SEL[4:0]				
Default	0	1	0	0	0	1	1	1

Bit	Name	Description
4:0	VGH_REG_SEL	VGH_REG voltage selection.

[0,0,0,0,0]	14.17V
[0,0,0,0,1]	14.17V
[0,0,0,1,0]	14.17V
[0,0,0,1,1]	14.17V
[0,0,1,0,0]	14.17V
[0,0,1,0,1]	14.17V
[0,0,1,1,0]	14.17V
[0,0,1,1,1]	14.17V
[0,1,0,0,0]	14.17V
[0,1,0,0,1]	14.17V
[0,1,0,1,0]	14.17V
[0,1,0,1,1]	14.10V
[0,1,1,0,0]	13.86V
[0,1,1,0,1]	13.62V
[0,1,1,1,0]	13.29V
[0,1,1,1,1]	13.07V
[1,0,0,0,0]	12.85V
[1,0,0,0,1]	12.54V
[1,0,0,1,0]	12.25V
[1,0,0,1,1]	12.07V
[1,0,1,0,0]	11.80V
[1,0,1,0,1]	11.54V
[1,0,1,1,0]	11.29V
[1,0,1,1,1]	11.06V
[1,1,0,0,0]	10.76V
[1,1,0,0,1]	10.57V
[1,1,0,1,0]	10.28V
[1,1,0,1,1]	10.03V
[1,1,1,0,0]	9.78V
[1,1,1,0,1]	9.54V
[1,1,1,1,0]	9.27V
[1,1,1,1,1]	9.06V

MIPI Address : 0X7B

Address	Bit							
0x7B	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	GRB
Default	0	0	0	0	0	0	0	1

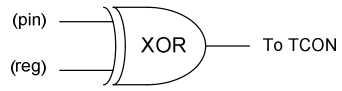
Bit	Name	Description
0	GRB	7B=”00” → Reset status. 7B=”01” → Normal display.

MIPI Address : 0XFA

Address	Bit							
0xFA	D7	D6	D5	D4	D3	D2	D1	D0
Name	Vender ID							
Default	0	0	1	0	1	0	0	1

Bit	Name	Description
7:0	Vender ID	The register is defines vender id for customer.

9.4.2 Function truth table

Combination Logic	Truth table		
	PIN	REG	To Tcon
	0	0	0
	0	1	1
	1	0	1
	1	1	0

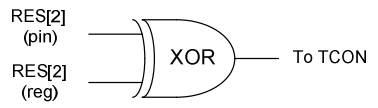
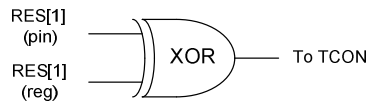
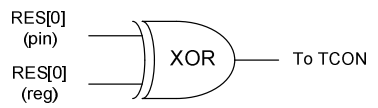
LNSW[1:0] do XOR operation.(MIPI I/F)

To Tcon		MIPI Lane Mapping				
LNSW[1]	LNSW[0]	D0(PAD)	D1(PAD)	CLK(PAD)	D2(PAD)	D3(PAD)
0	0	D3	D2	CLK	D1	D0
0	1	D3	D0	CLK	D1	D2
1	0	D0	D1	CLK	D2	D3
1	1	D2	D1	CLK	D0	D3

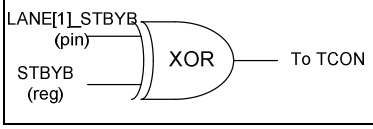
LNSW[1:0] do XOR operation.(LVDS I/F)

To Tcon				LVDS Lane Mapping				
LNSW[3] (OTP)	LNSW[2] (OTP)	LNSW[1]	LNSW[0]	D0(PAD)	D1(PAD)	CLK(PAD)	D2(PAD)	D3(PAD)
0	0	0	0	D3	D2	CLK	D1	D0
0	0	0	1	D3	CLK	D2	D1	D0
0	0	1	0	D0	D1	CLK	D2	D3
0	0	1	1	D0	D1	D2	CLK	D3
0	1	0	0	CLK	D0	D1	D2	D3
0	1	0	1	CLK	D3	D2	D1	D0
0	1	1	0	D3	D2	D1	D0	CLK
0	1	1	1	D0	D1	D2	D3	CLK
1	0	0	0	D3	D0	CLK	D1	D2
1	0	0	1	D2	D1	CLK	D0	D3

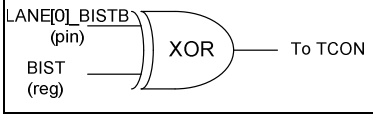
RES[2:0] do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	
	0	0	0	Display resolution selection. RES[2:0] = 000, 400RGBx1280.
	0	1	1	
	1	0	1	
	1	1	0	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	

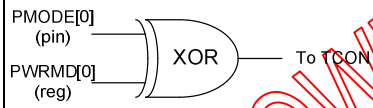
STBYB do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	STBYB mode selection. STBYB = 0, STBYB mode. STBYB = 1, Normal Display mode.
	0	1	1	
	1	0	1	
	1	1	0	

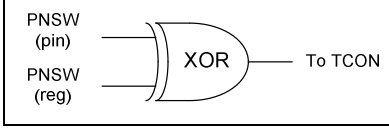
BIST do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	Normal Operation / BIST pattern select. BIST_EN = 0, BIST. BIST_EN = 1, Normal Operation.
	0	1	1	
	1	0	1	
	1	1	0	

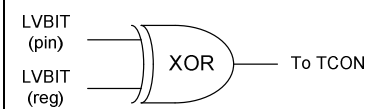
PWRMD do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	Power mode selection. PWRMD[1:0] = 00, VSP/VSN: JD5001/2. VGH/VGL: External. PWRMD[1:0] = 01, VSP/VSN: External. VGH/VGL: Charge pump. PWRMD[1:0] = 10, VSP/VSN: JD5001/2. VGH/VGL: Charge pump. PWRMD[1:0] = 11, VSP/VSN: External. VGH/VGL: External.
	0	1	1	
	1	0	1	
	1	1	0	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	

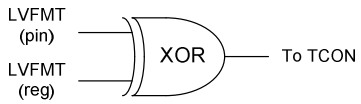
PNSW do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	MIPI Lane polarity swap. PNSW = 0, P/N polarity swap. PNSW = 1, Normal.
	0	1	1	
	1	0	1	
	1	1	0	

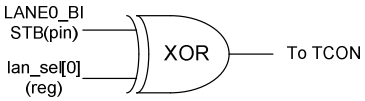
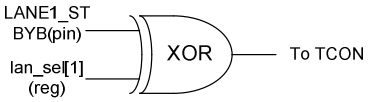
LVBIT do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	6-bit / 8-bit input select for LVDS mode. LVBIT = 0, 6-bit. LVBIT = 1, 8-bit.
	0	1	1	
	1	0	1	
	1	1	0	

LVFMT do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	8-bit input format select for LVDS mode. LVFMT = 0, JEIDA format. LVFMT = 1, VESA format.
	0	1	1	
	1	0	1	
	1	1	0	

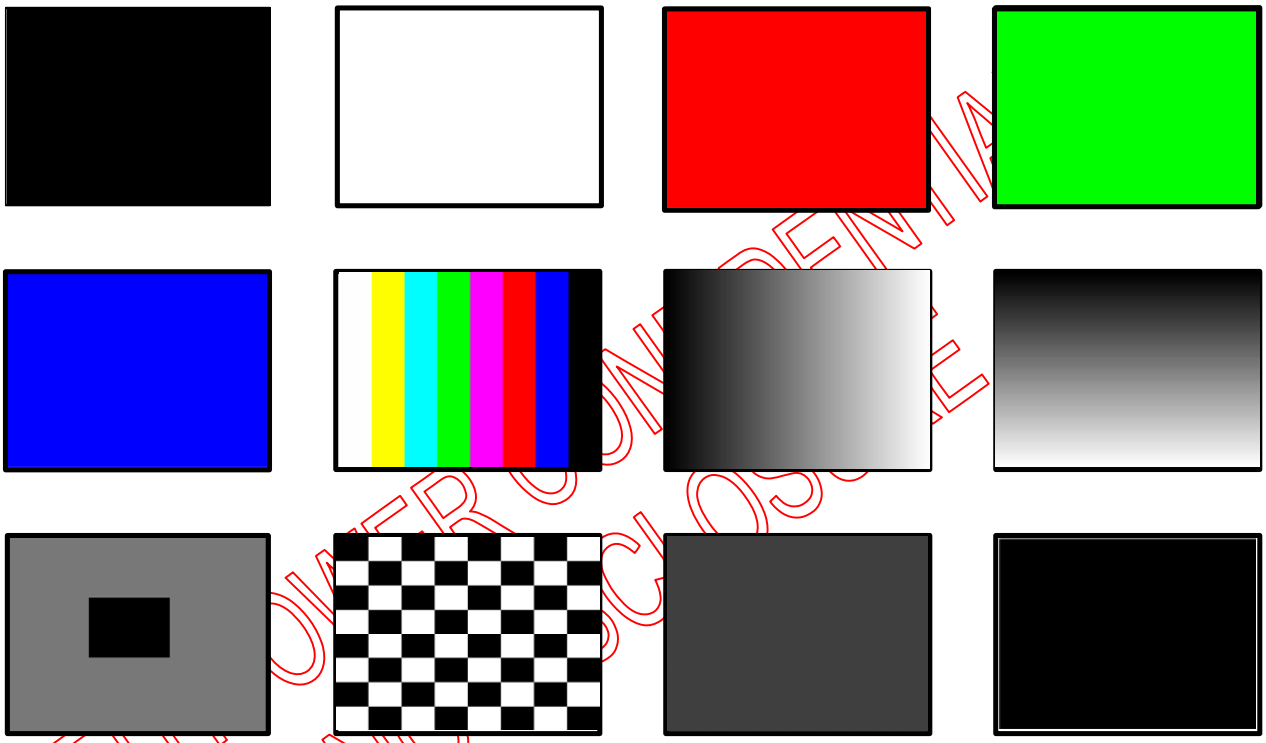
lan_sel do XOR operation.

Combination Logic	Truth table			To Tcon
	PIN	REG	To Tcon	
	0	0	0	MIPI lane number selection . lan_sel[1:0] = 10, MIPI 3 lane. lan_sel[1:0] = 11, MIPI 4 lane.
	0	1	1	
	1	0	1	
	1	1	0	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	

10. FUNCTION DESCRIPTION

10.1 BIST pattern

We support the BIST mode to test panel and debug. It can stop pattern at any time while LANE[0]_BISTB set to high. The pattern sequence is listed below.



Black→White→R→G→B→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern→Chess board (L255/L0)→Flicker pattern→Black background with white out frame

10.2 XON function

When power is removed from an electronic device during display, the image still keeps on the LCD panel for a long time. XON function can speed the process that image disappears.

The XON function is a voltage detector. By XON circuit, EK79030 can detect low voltage of power and send control signal to discharge residual potential in LCD panel and remove image.

In the following case, the chip will entry XON function.

1. VDD is lower than 1.7V.

XON function:

1. Source output pull to VSSA.
2. All GOA signals will be set to VGH voltage level.
3. Stop charge pump function.
4. VCOM output pull to VSSA.

The XON function has debounce protection circuit. EX: If duration of voltage drop on VDD is less than 20us (**EX: induced by ESD pulse**), the XON function will not be active even the VDD voltage level is less than 1.7V.

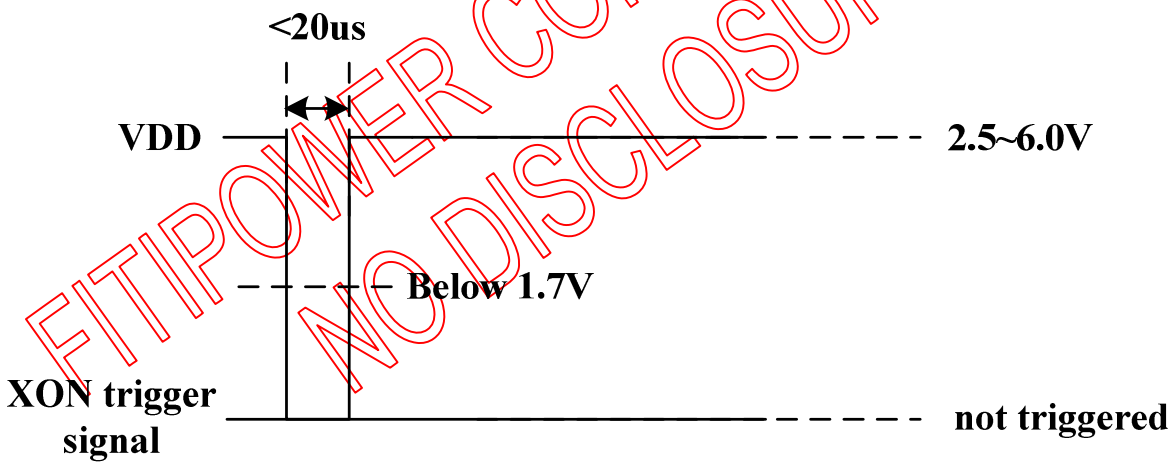
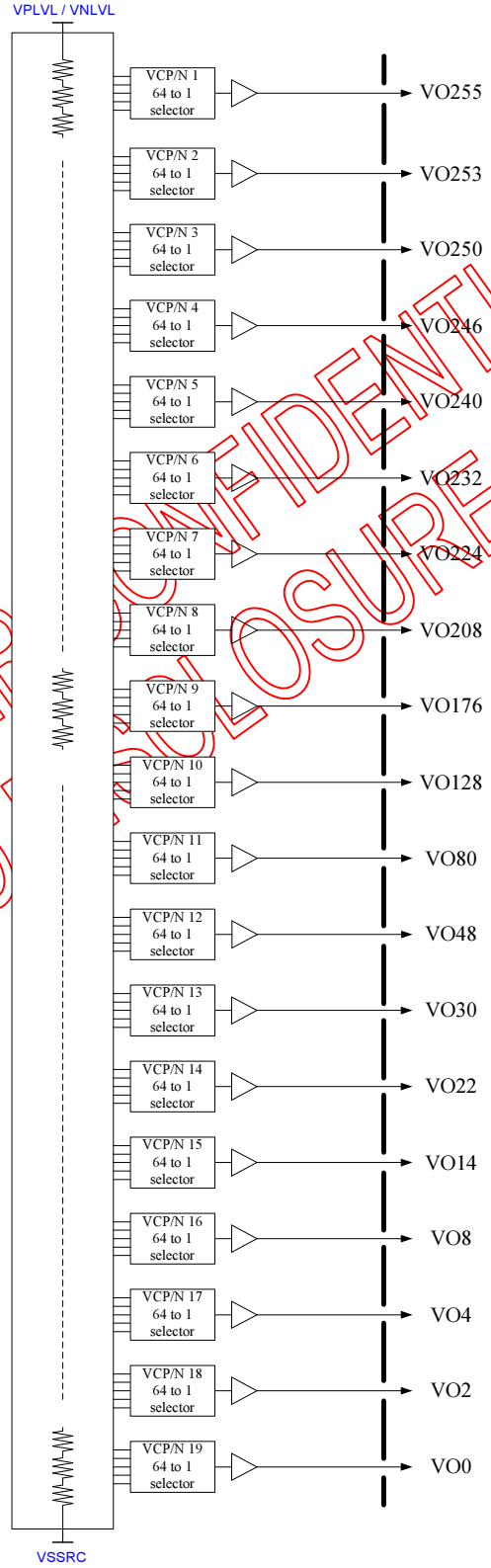


Figure 9.1: XON function vs. VDD

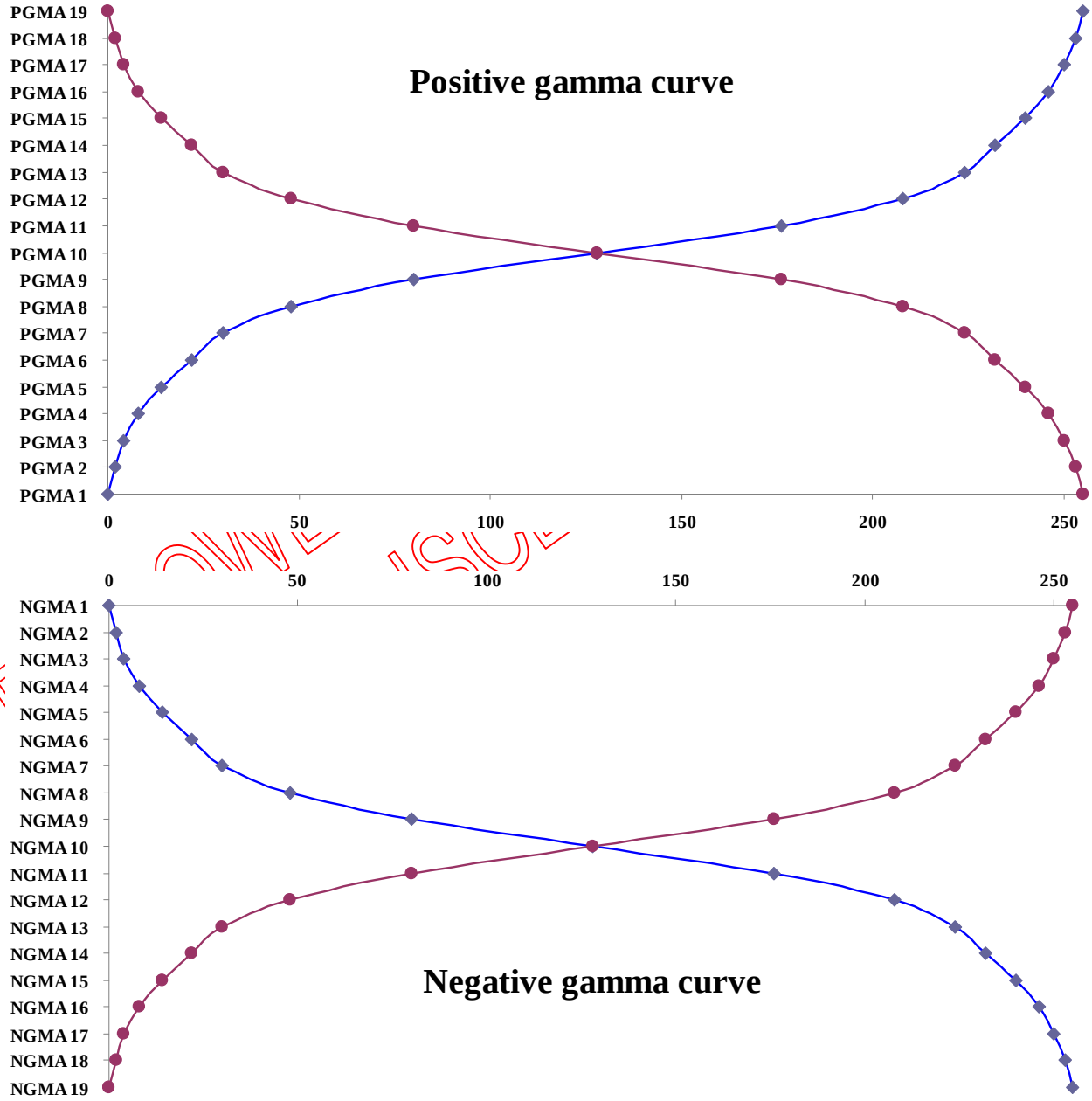
11. GAMMA CORRECTION CIRCUIT

We use the gamma resistor stream and 64-to-1 selector to adjust voltage



11.1 Gamma Architecture

The gamma correction are done by 18-segment piecewise linear interpolation. The 18 segments are defined with 19 register values for level 0, 2, 4, 8, 14, 22, 30, 48, 80, 128, 176, 208, 224, 232, 240, 246, 250, 253 and 255. These total 19 register values defined the positive and negative gamma curve.



The blue line is for normal black type, the red line is for normal white type.

12. DC CHARACTERISTICS

12.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
I/O voltage	VDDIO_IF	1.8	-	3.6	V	
	VDDIO					
Power input	VDD	2.5	-	3.6	V	
VSP voltage	VSP	4.5	-	6	V	
VSN voltage	VSN	-4.5	-	-6	V	
VOTP power	VOTP	-	7.5	-	V	
Operating Temperature		-20	-	85	℃	(1)

Note :(1) Do not let condensation for low temperature

Table 12.1: Absolute maximum rating

12.2 Typical operating condition

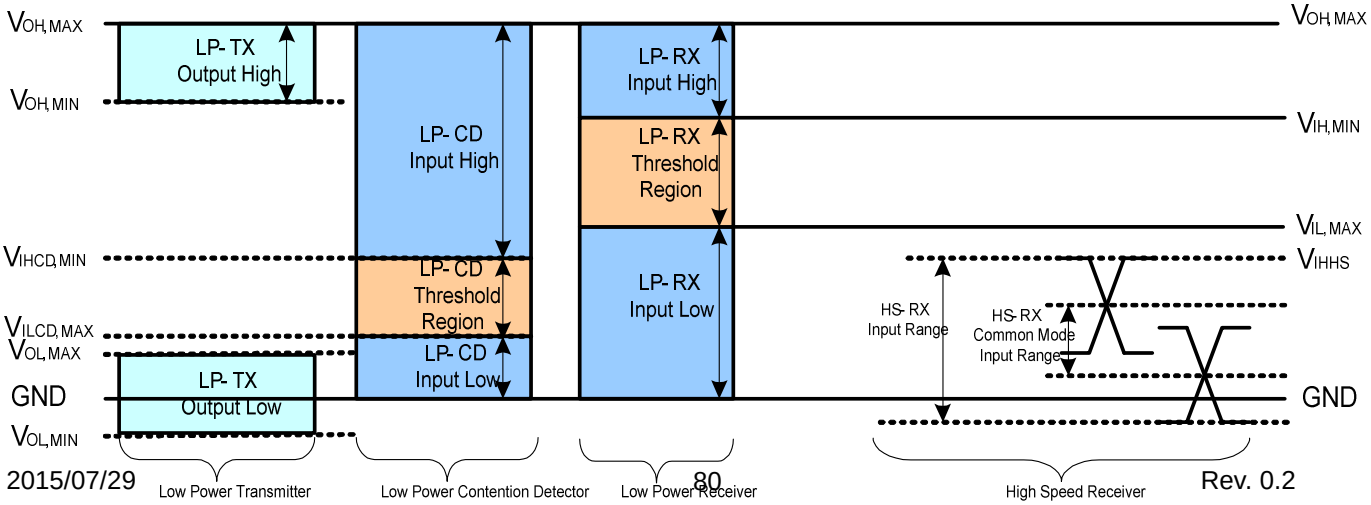
Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
VDD voltage	VDD	-	3.3	-	V	Digital supply voltage
VDDP voltage	VDDP	-	3.3	-	V	Analog supply voltage
VDDIO voltage	VDDIO	-	3.3	-	V	I/O Power supply voltage
VOTP voltage	VOTP	-	7.5	-	V	Programming voltage
VSP voltage	VSP	4.5	5.0	6	V	VSP voltage
VSN voltage	VSN	-4.5	-5.0	-6	V	VSN voltage
VGH voltage	VGH	9.3	-	18	V	VGH voltage
VGL voltage	VGL	-16	-	-6.7	V	VGL voltage

Table 12.2 : Typical operating conditions

12.3 DC electrical characteristics

(Test condition: VCI=1.6~3.6V, TA=-20℃~+85℃,VSS=VSSA=0V)

Parameter		Symbol	Spec.			Unit	Note
			Min.	Typ.	Max.		
VDDIO Input high level voltage		VIH	0.8 x VDDIO		VDDIO	V	
VDDIO input low level voltage		VIL	VSS		0.2 x VDDIO	V	
Input Leakage Current		Ileak	(-1)		(+1)	μA	
VGL_REG2 output voltage		VGL_REG2		TBD		V	
VGMP output voltage		VGMP		TBD		V	
VGMN output voltage		VGMN		TBD		V	
VCI1 output voltage		VCI1		TBD		V	
VGL output voltage		VGL_O	-16		-6	V	
VGH output voltage		VGH_O	8		19	V	
VCL output voltage		VCL	-2.1	-2.4	-3	V	
VOM output voltage		VCOM	-2.75	-1.48	-0.2	V	
Input terminal resistance		ZID		100		ohm	
Source output level deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255			TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240			TBD		mV	
	Graycode = 32 ~ 207			TBD		mV	
Source output offset deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255	-		TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240	-		TBD		mV	
	Graycode = 32 ~ 207	-		TBD		mV	
Current consumption	Analog Operating	IAOP		TBD		mA	
	Analog Stand-by	IAST		TBD		mA	
Rush current		Ivddpeak		TBD		mA	
VOTP operation current		Ivpp		TBD		mA	



13. AC CHARACTERISTICS

13.1 MIPI AC characteristics

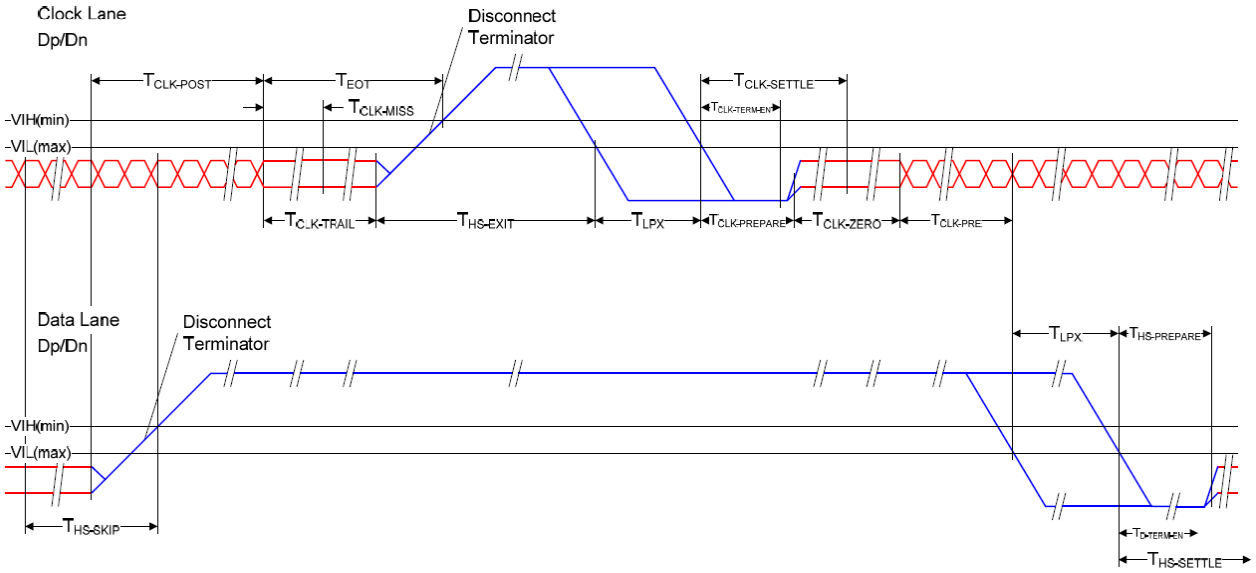


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

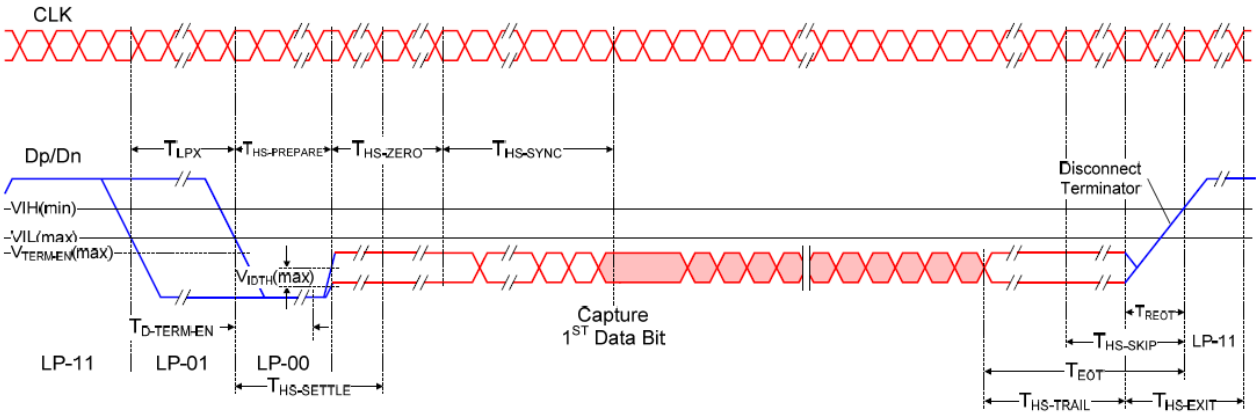


Figure 13.2: Timing of high-speed data transmission in bursts

13.2 MIPI data-clock timing specification

Parameter	Descript	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI (For DCS)	-		ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-		ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI	-	145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$ (1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

13.3 LVDS mode AC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	R_{xFCLK}	30	-	TBD	MHz	Refer to input timing table for each display resolution
Input data skew margin	T_{RSKM}	500	-	-	ps	|VID| = 200mV RxVCM = 1.2V RxFCLK = 81MHz
Clock high time	T_{LVCH}	-	4/(7* R_{xFCLK})	-	ns	
Clock low time	T_{LVCL}	-	3/(7* R_{xFCLK})	-	ns	
PLL wake-up time	T_{enPLL}	-	-	150	us	

Table 13.1: LVDS mode AC electrical characteristics

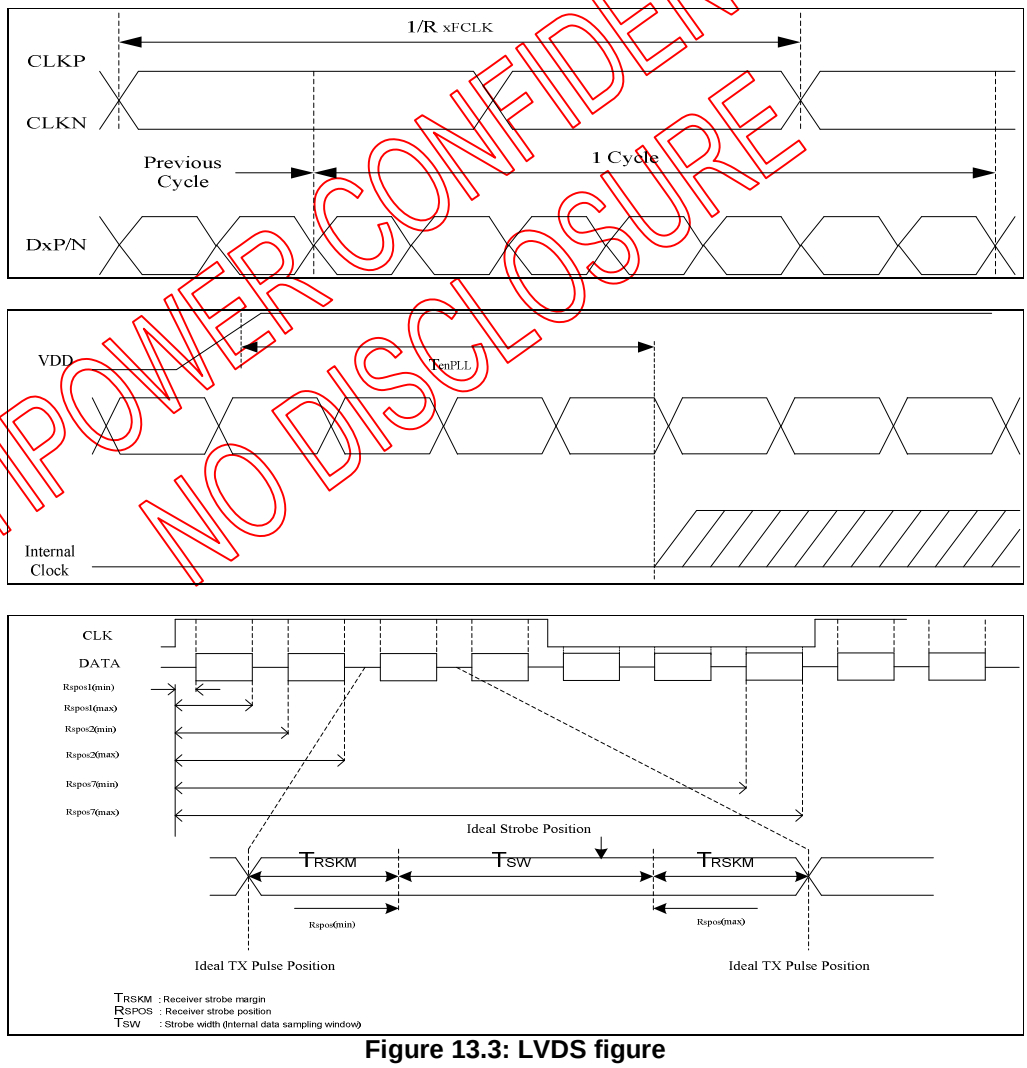
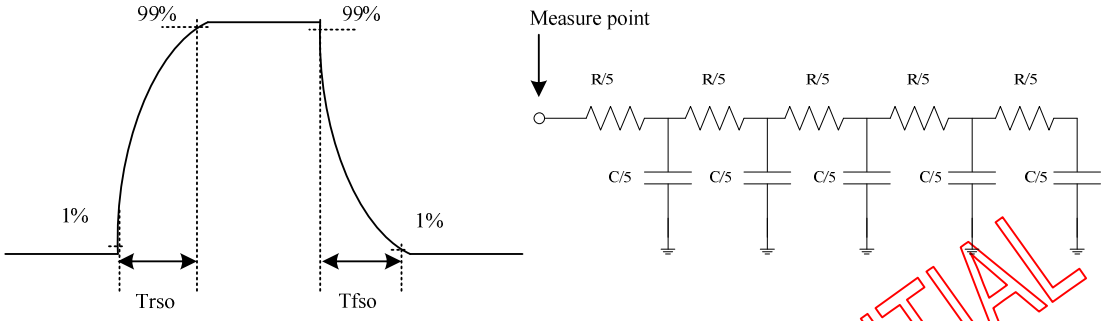


Figure 13.3: LVDS figure

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Modulation Frequency	SSC_{MF}	23	-	93	KHz	
Modulation Rate	SSC_{MR}	-	-	+3	%	

Table 12.2: SSC table

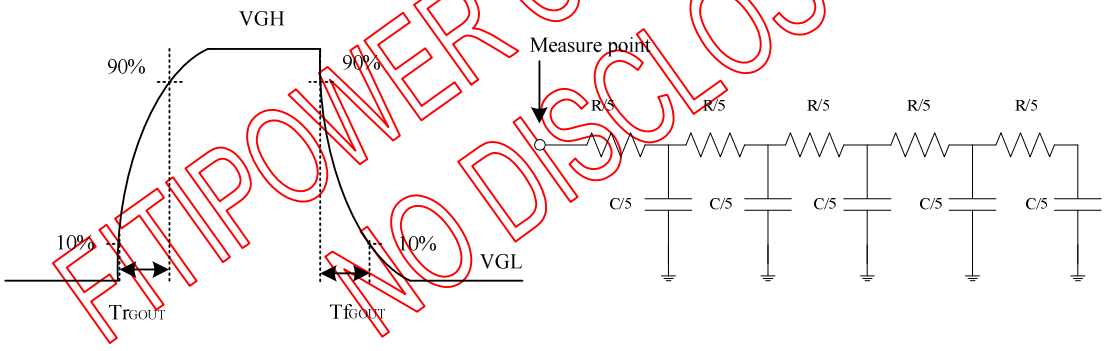
13.4 Source output timing (SOUT1 ~ SOUT1200, SDUMY)



Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Source driver rising time	Trso	TBD	-	-	TBD	µs
Source driver falling time	Tfso	TBD	-	-	TBD	µs

Table 13.3: Source output timing

Panel control signal output (GOUTL[1]~GOUTL[22] , GOUTR[1]~GOUTR[22])



Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Panel control signal rising time	T_{rGOUT}	TBD	-	-	TBD	µs
Panel control signal falling time	T_{fGOUT}	TBD	-	-	TBD	µs

Table 13.4: GOA output timing

13.5 Serial interface characteristics

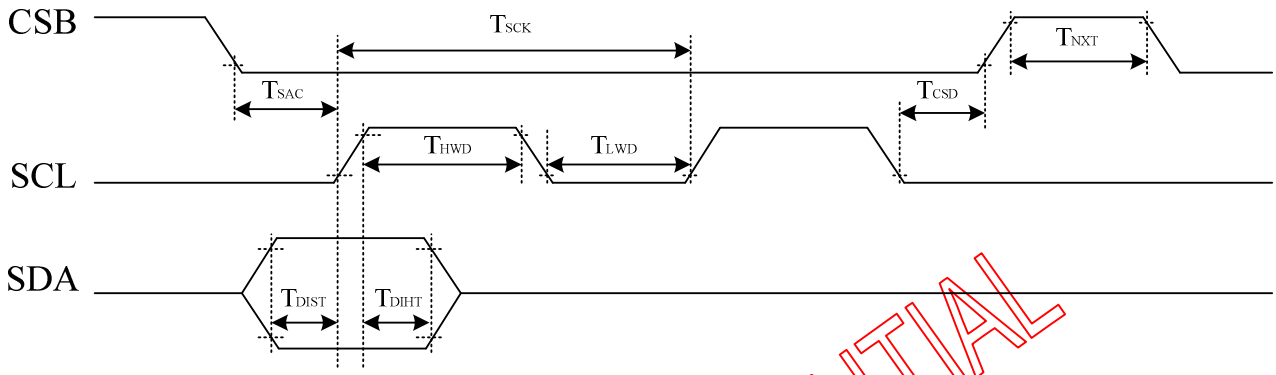


Figure 13.4: Serial interface characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
CSB assertion to first clock edge	T_{SAC}		120	-	-	ns
CSB deassertion frome last clock edge	T_{CSD}		120	-	-	ns
CSB next control enable	T_E		200	-	-	ns
SCL period time	T_{SCK}		200	-	-	ns
SCL high period time	T_{HWD}		100	-	-	ns
SCL low period time	T_{LWD}		100	-	-	ns
SDA input data setup time	T_{DIST}		50	-	-	ns
SDA input data hold time	T_{DIHT}		50	-	-	ns

13.6 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

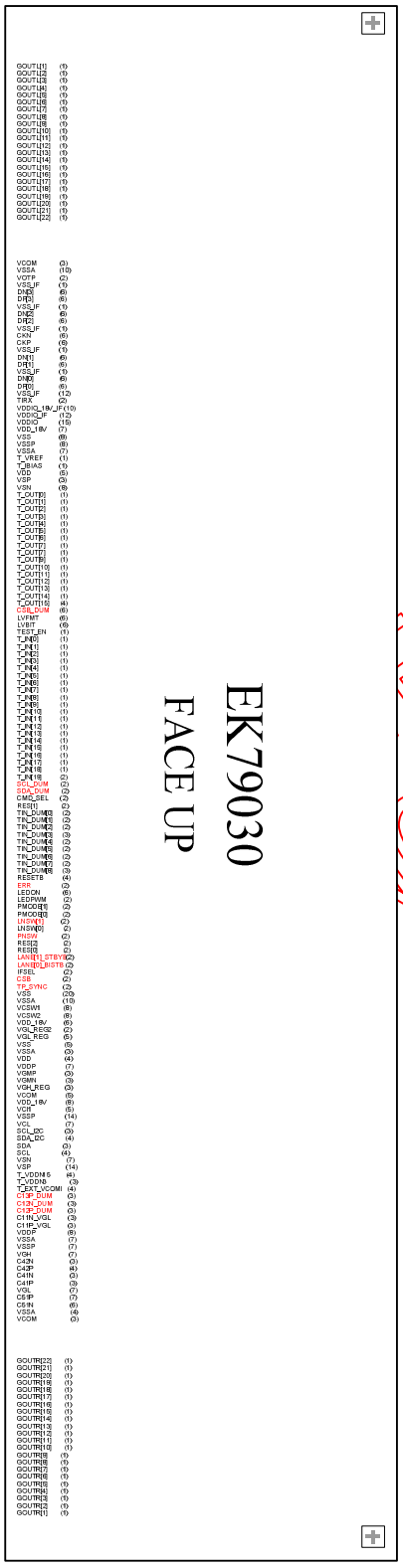
(Test condition: VDDIO=1.65V~3.6V, VSS=0V, T_A=-20 ~+85)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		20	-	-	μs

Figure 13.5: Reset timing

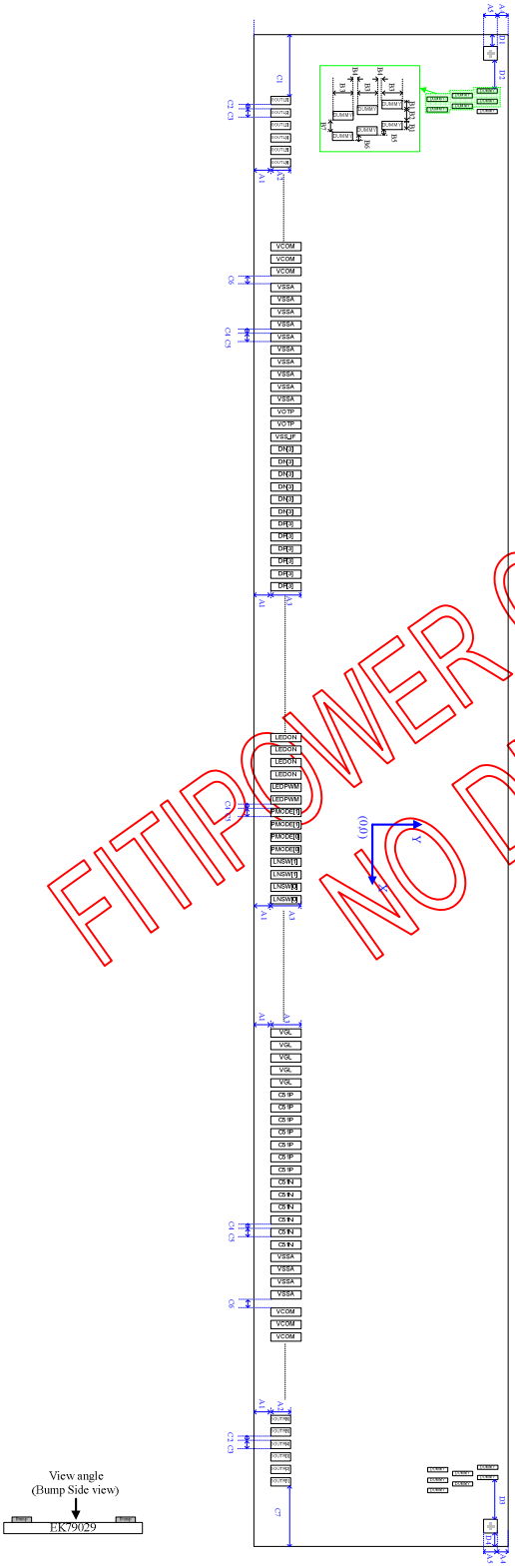
14. PIN ASSIGNMENT (IC FACE VIEW)

14.1 Pad sequence



14.2 Bump information

14.2.1 Chip outline dimension



14.2.2 Pad information

Symbol	Dimension
A1	32
A2	43
A3	93
A4	33
A5	50

Symbol	Dimension
B1	16
B2	17
B3	73
B4	17
B5	11
B6	11
B7	17
-	
-	

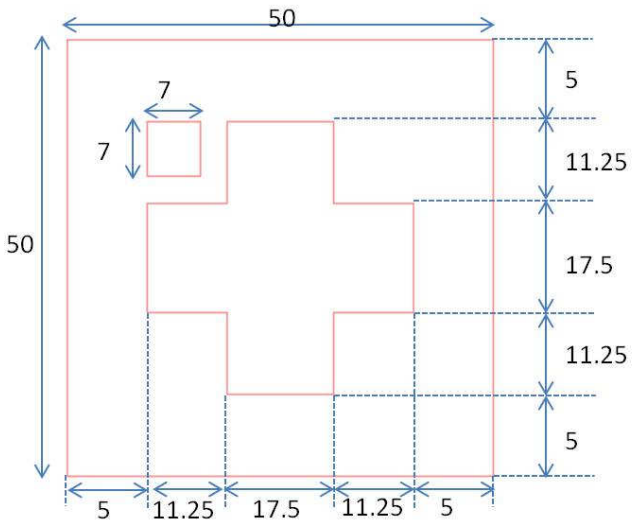
Symbol	Dimension
C1	206.5
C2	13
C3	32
C4	15
C5	30
C6	25
C7	206.5
-	
-	

Symbol	Dimension
D1	69
D2	49.5
D3	71.5
D4	69
-	
-	

14.2.3 Alignment mark

Unit : um

Left Side



Right Side