EK79652AC

Rev. 1.0

DATA SHEET

All-in-one driver with TCON for Color application

Table of Contents

All-in-one driver with TCON for Color application

1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 1-bit white/black and 1-bit red resolution output per pixel. The timing controller provides control signals for the source driver and gate drivers.

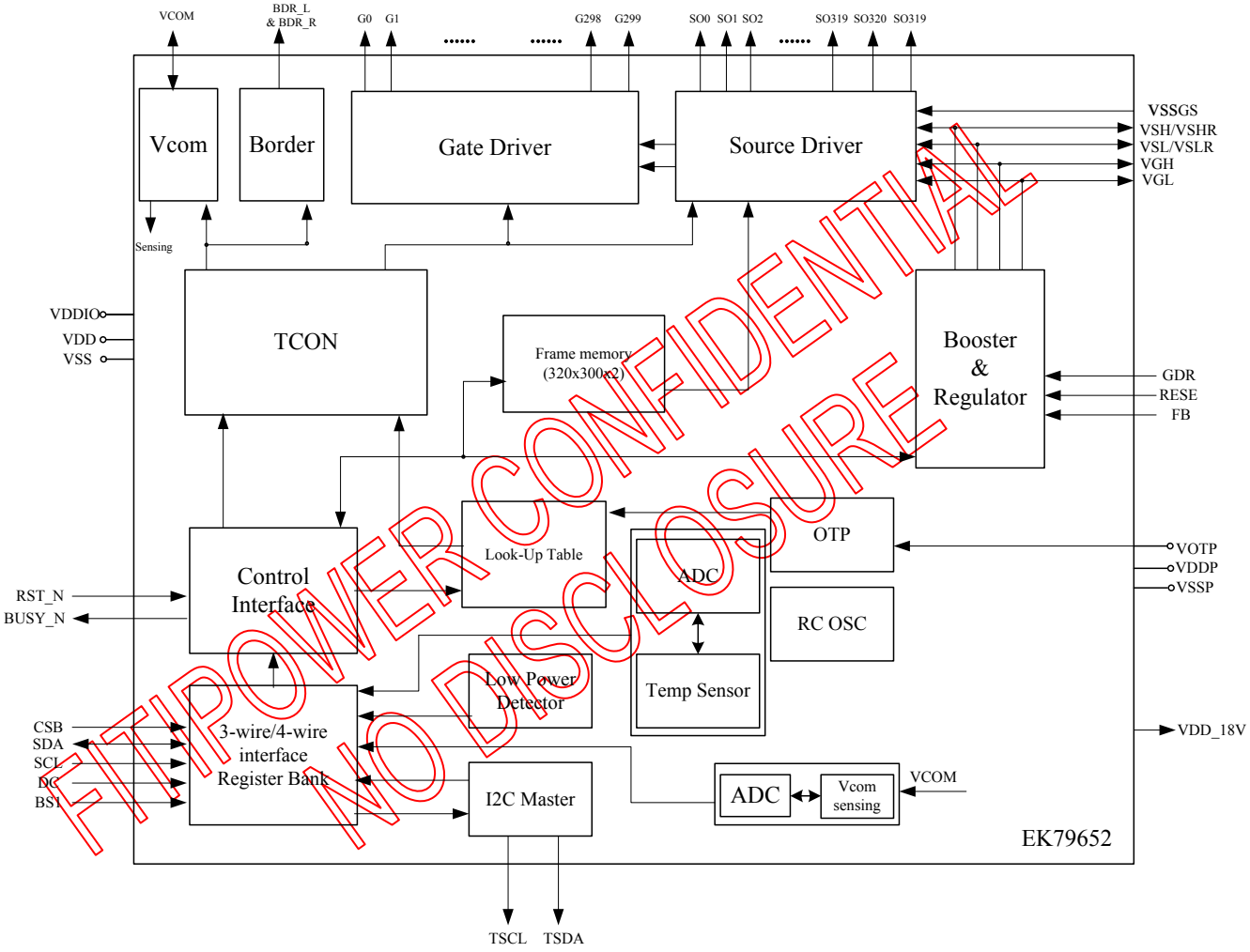
The DC-DC controller allows to generate the source output voltage VSH/VSL (+/-2.4V~+/-11V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial.

2. FEATURES

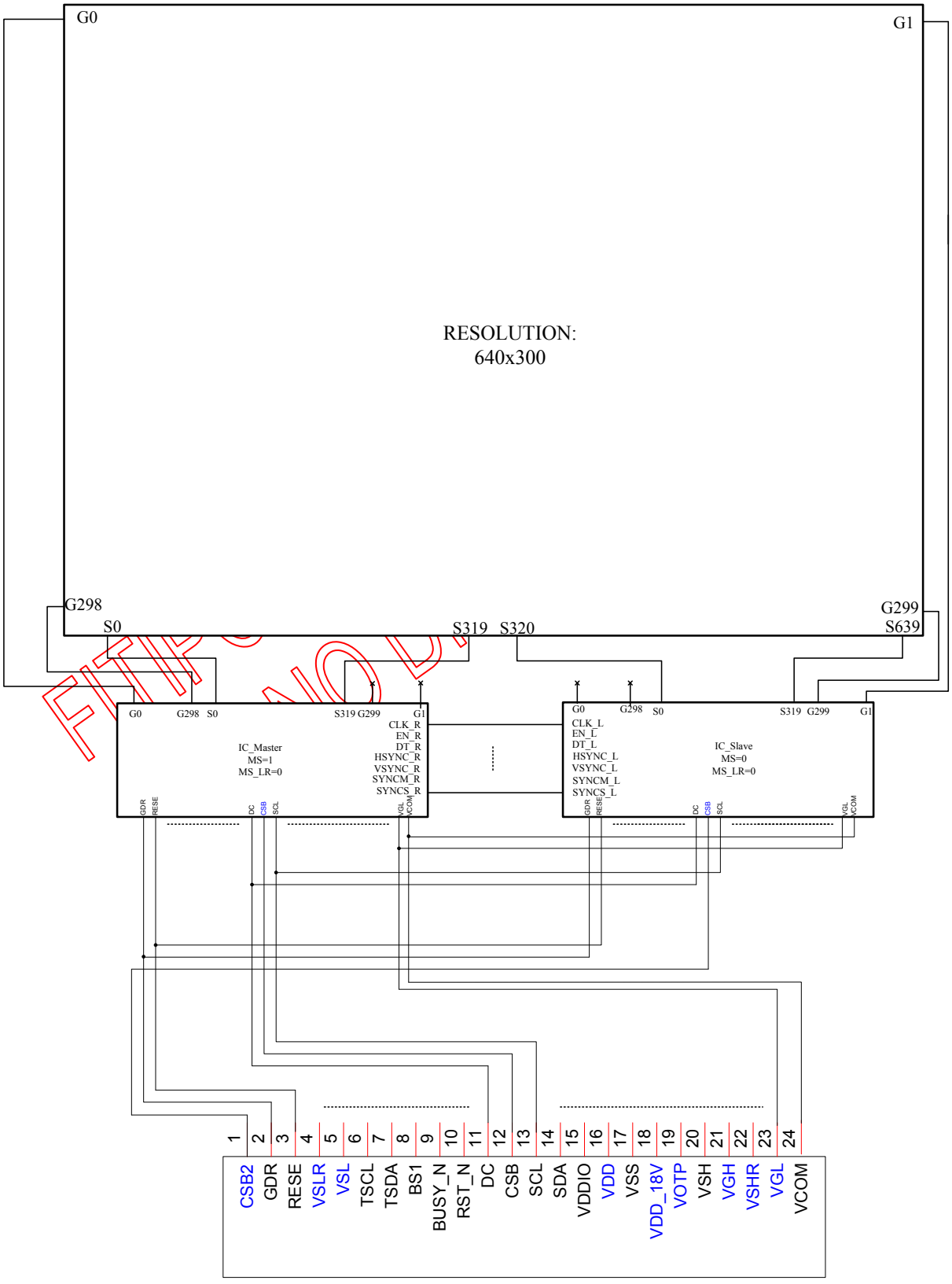
- System-on-chip (SOC) for color application
- Timing controller support several all resolution (maximum resolution 320x300)
- Support source & gate driver function:
  - 320 Outputs source driver with 1-bit white/black & 1-bit red per pixel:
    - Output dynamic range: VSH (+2.4~+11V)& VSL (-2.4~-11V) (programmable, black/white)
      VSHR: +/-2.4~+/-11V (programmable, red)
    - Output deviation: 0.1V
    - Left and Right shift capability
  - 300 Output gate driver:
    - Output dynamic range: VGH and VGL: +16V, -15V
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (6-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: (320 x 300 x 1 bit) x 2 SRAM
- Built in temperature sensor:
  - On-Chip: On-Chip: -25~50 ^{o}C ± 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}<2.5V)

- OCS : On-chip RC oscillator
- 3-wire/4-wire (SPI) serial interface for system configuration: Clock rate up to 20MHz
- Digital supply voltage: 2.3~3.6V
- OTP: 4K-byte OTP for LUT
- Partial update
- Support cascade
- Package-COG
- COM / SEG bump information
  - Bump pitch: 44 μm
  - X Bump space: 22 μm ± 3 μm, Y Bump space : 20 μm ± 3 μm,
  - Bump Area: 1210 μm^2

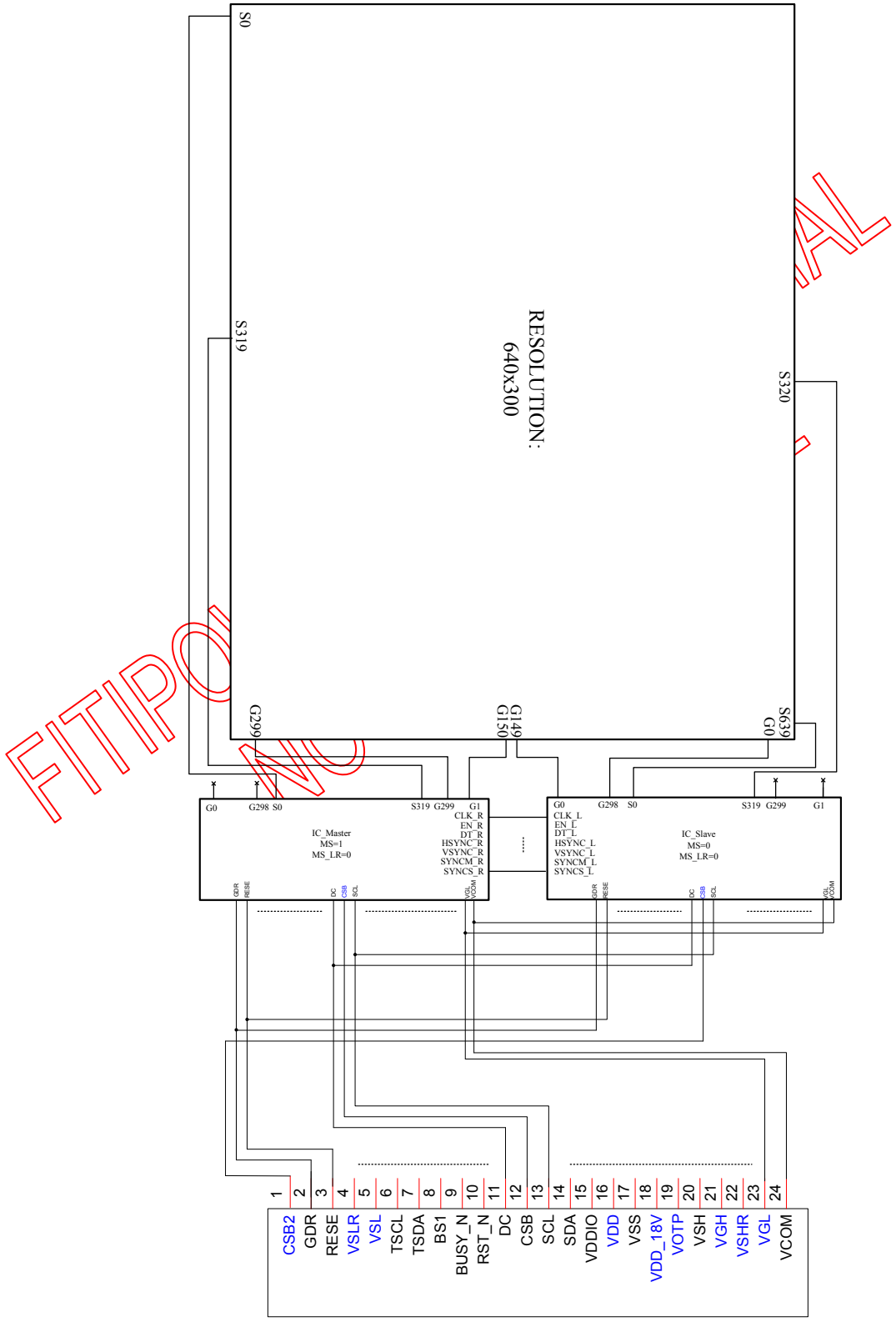
3. BLOCK DIAGRAM



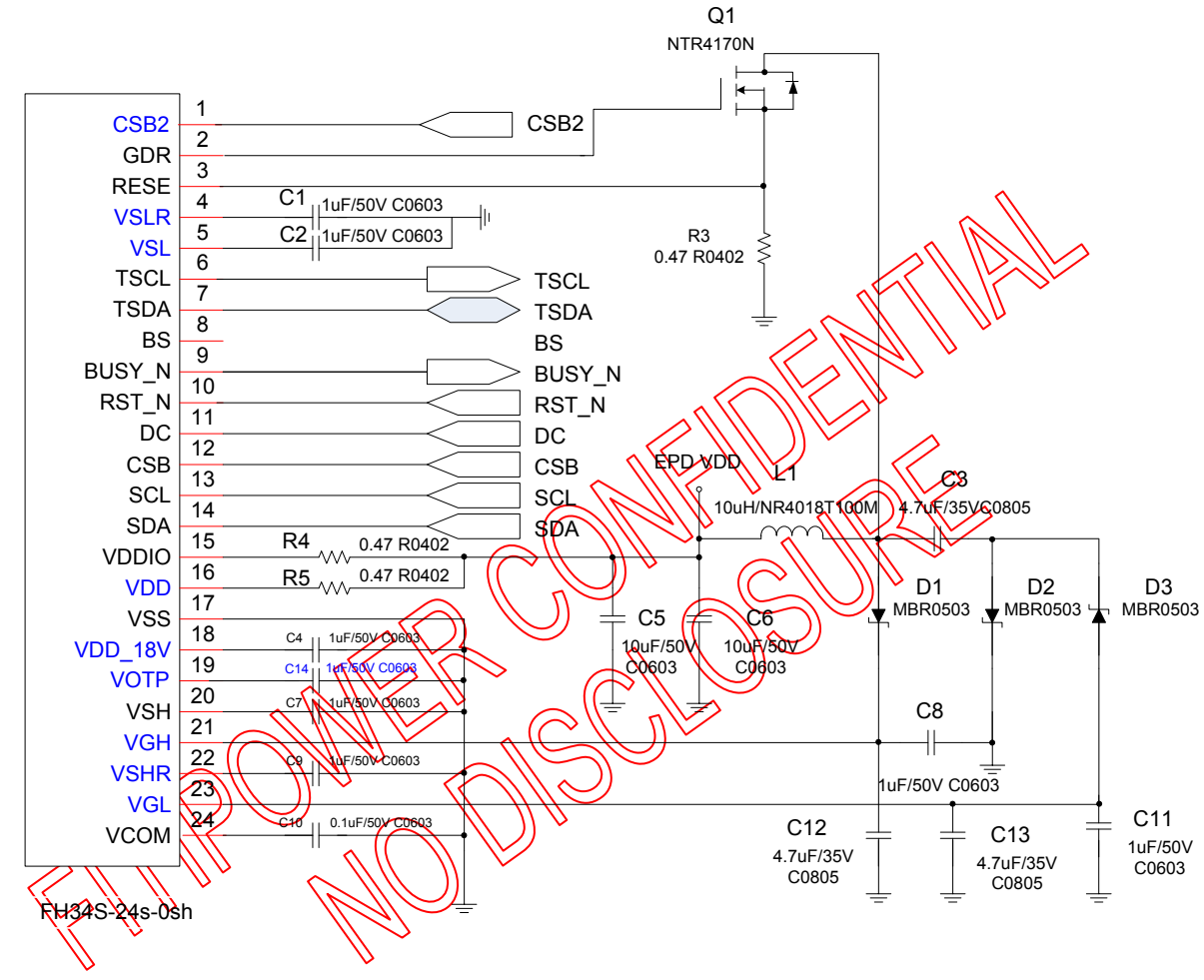
Cascade type 1

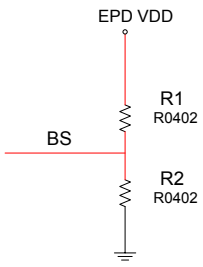


Cascade type 2



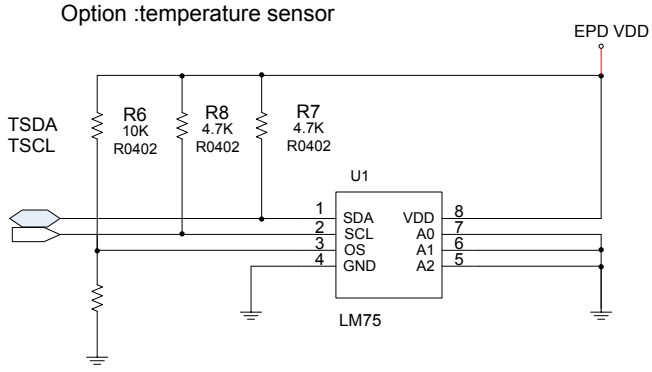
4. APPLICATION CIRCUIT





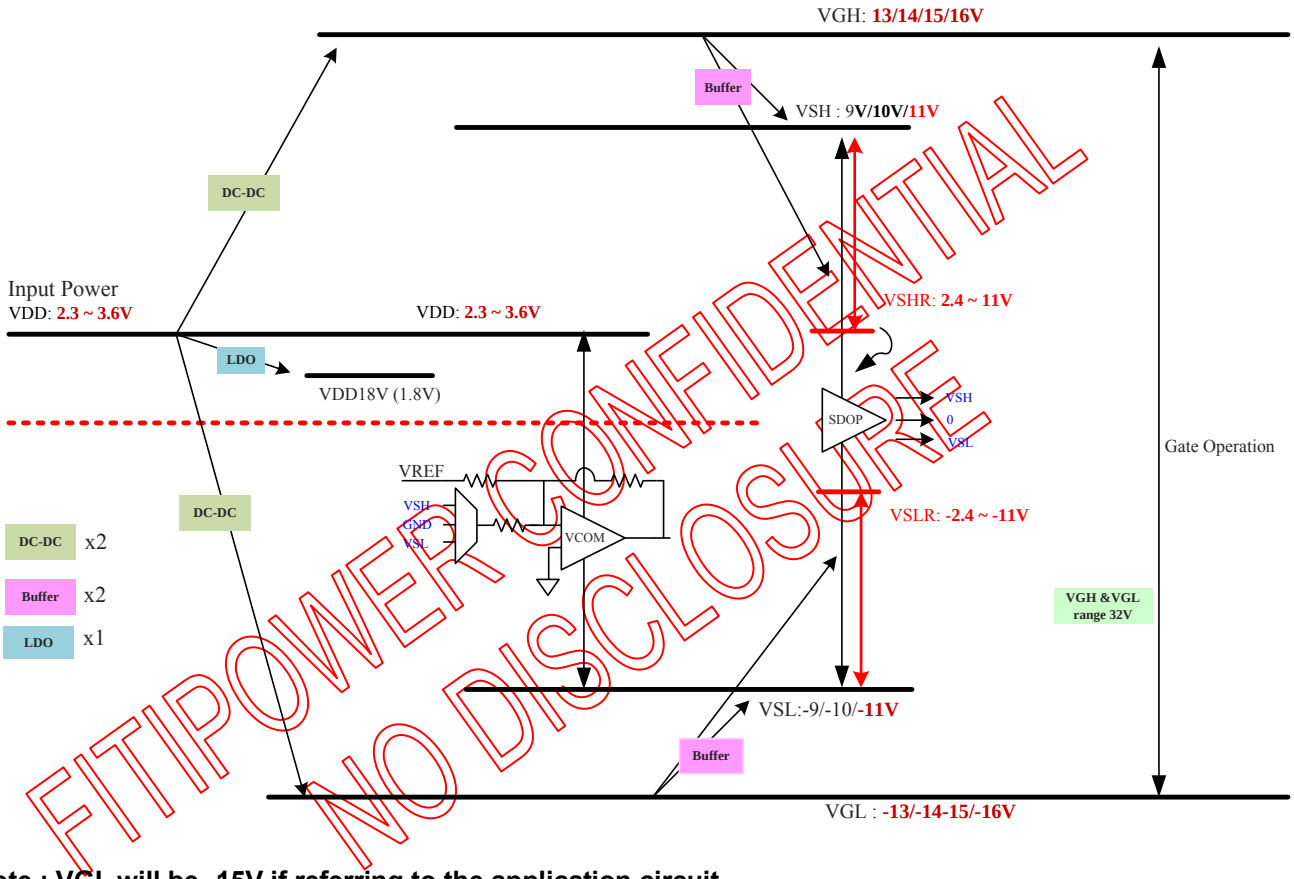
Option :temperature sensor

	R1	R2
3- wire SPI (CS#, SDA, SCL)	10K	NC
4-wire SPI (D/C#, CS#, SDA, SCL)	NC	10K



5. APPLICATION POWER CIRCUIT

5.1 Power Generation



Note : VGL will be -15V if referring to the application circuit,

6. PIN DESCRIPTION

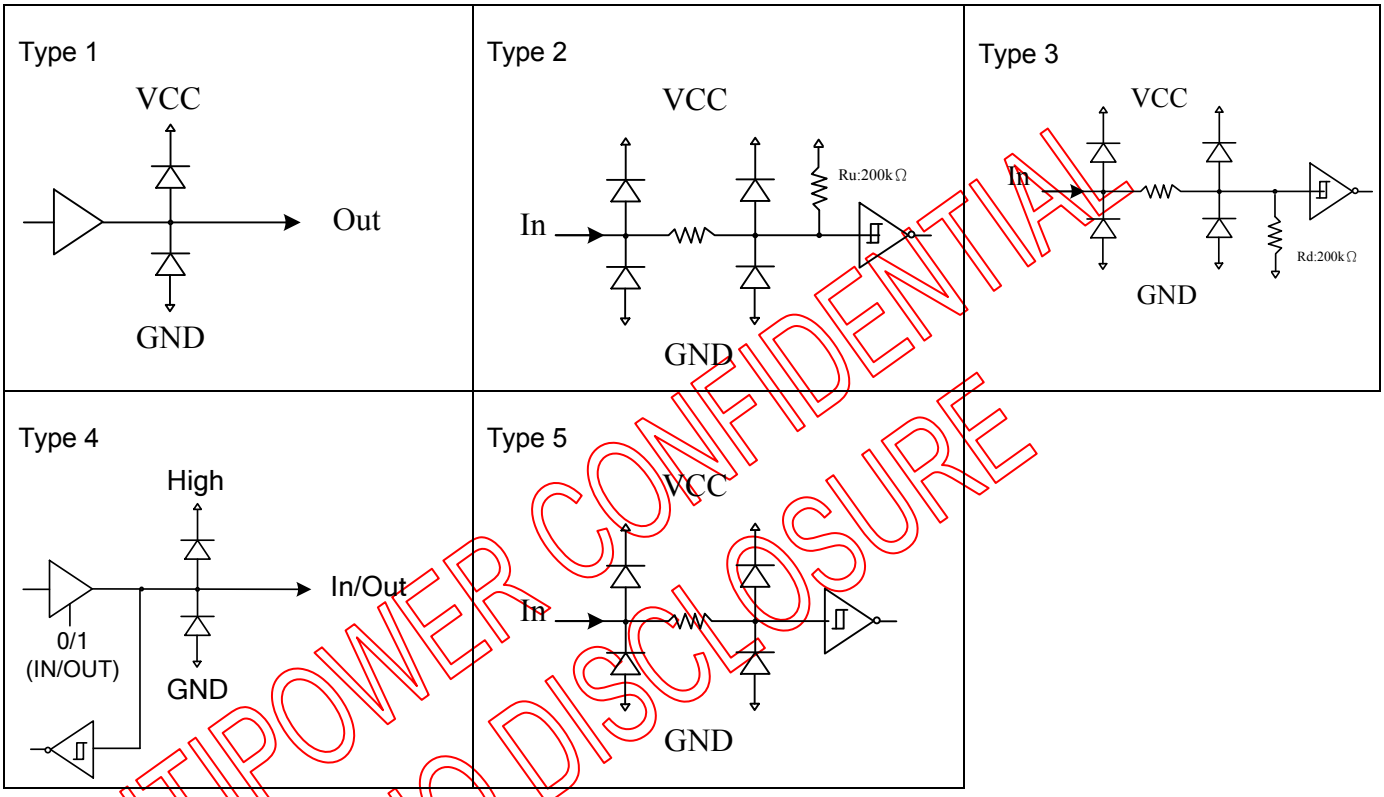
6.1 Pin define

Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 2	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 3	Serial communication clock input.
DC	I	Type 2	Serial communication Command/Data input L: Command H: data (default)
Control Interface			
RST_N	I	Type 2	Global reset pin. Low reset. **(normal pull high)** When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= "0" : Driver is busy, data/VCOM is transforming. BUSY_N= "1" : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF(Default) Note: please always keep L or H.
TSCL	O	Type1	I^2C clock for external temperature sensor
TSDA	I/O	Type 4	I^2C data for external temperature sensor
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
Output Driver			
S[0,319]	O	-	Source driver output signals.
G[0,299]	O	-	Gate driver output signals..
Border			
BDR_L, BDR_R	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM_PASSR / VCOM_PASSL	I /O		VCOM Internal Pass Line
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (VSH-VCM_DC) v 2. (-VCM_DC) v 3. (VSL-VCM_DC) v. 4. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.

Pin Name	Pin Type	I/O Structure	Description
FB	P	-	Keep open
VGH	P	Type 4	Positive gate voltage
VGL	P	Type 4	Negative gate voltage.
VSH	P	Type 4	Positive source voltage
VSL	P	Type 4	Negative source voltage.
VSHR	P	Type 4	Positive source voltage for Red
VSLR	P	Type 4	negative source voltage for Red
Power Supply			
VSSP	P	-	DCDC Ground
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_18V	P	-	1.8V voltage input &output
VOTP	P	-	OTP program power (7.5V)
VSSGS	P		Driver Ground
Reserved Pins			
TP[66:0]	I/O	-	Leave it floating
MS_LR	I	Type 5	Cascade direction 0 : Master(right side output) -> Slave(left side input) 1 : Slave(right side input) <- master(left side output)
VSYNC_R	I/O	Type 4	Cascade right side Vsync
VSYNC_L	I/O	Type 4	Cascade left side Vsync
SYNCM_R	I/O	Type 4	Cascade master right side state sync
SYNCM_L	I/O	Type 4	Cascade master left side state sync
SYNCS_R	I/O	Type 4	Cascade slave right side state sync
SYNCS_L	I/O	Type 4	Cascade slave left side state sync
CLK_L	I/O	Type 4	Cascade left side reference clock pin
CLK_R	I/O	Type 4	Cascade right side reference clock pin
HSYNC_L	I/O	Type 4	Cascade left side system clock pin
HSYNC_R	I/O	Type 4	Cascade right side system clock pin
EN_L	I/O	Type 4	Cascade left side enable pin
EN_R	I/O	Type 4	Cascade right side enable pin
DT_L	I/O	Type 4	Cascade left side data pin for temperature data
DT_R	I/O	Type 4	Cascade right side data pin for temperature data

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6.2 I/O Pin Structure



6.3 Value of wiring resistance to each pin

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VCOM_PASSR	5ohm	TSDA	100ohm
VCOM	5ohm	TSCL	100ohm
VGL	5ohm	MS	5ohm
VSHR	5ohm	MS_LR	5ohm
VGH	5ohm	VSL	5ohm
VSH	5ohm	VSLR	5ohm
VOTP	5ohm	RESE	100ohm
VDD_18V	5ohm	GDR	100ohm
VSSA	5ohm	SYNCS_L	100ohm
VSSGS	5ohm	SYNCM_L	100ohm
VSS	5ohm	VSYCM_L	100ohm
VSSP	5ohm	HSYNC_L	100ohm
VDD	5ohm	DT_L	100ohm
VDDP	5ohm	EN_L	100ohm
VDDIO	5ohm	CLK_L	100ohm
SDA	100ohm	CLK_R	100ohm
SCL	100ohm	EN_R	100ohm
CSB	100ohm	DT_R	100ohm
DC	100ohm	HSYNC_R	100ohm
RST_N	100ohm	VSYNC_R	100ohm
BUSY_N	100ohm	SYNCM_R	100ohm

BS	100ohm	SYNCS_R	100ohm

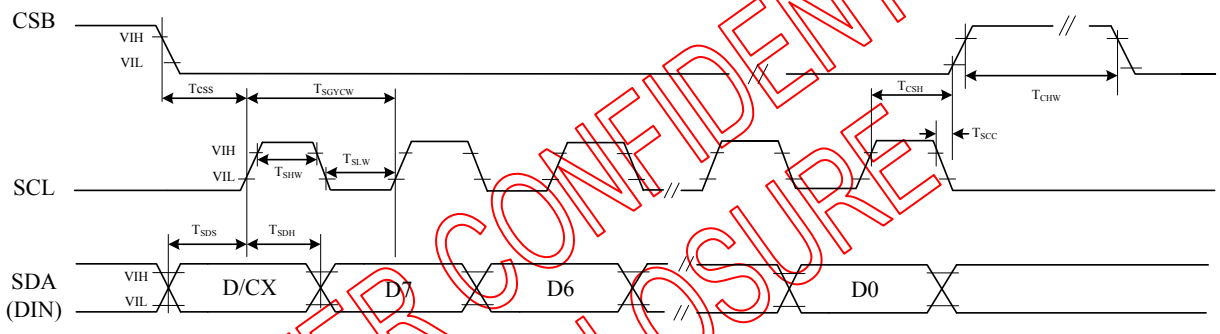
7. SPI COMMAND DESCRIPTION

7.1 "3-Wire" Serial Port Interface

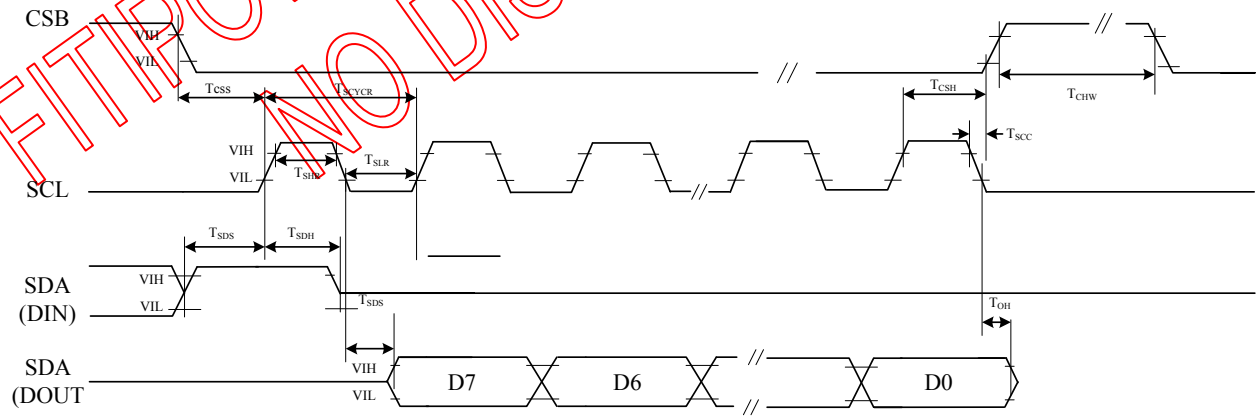
EK79652 use the 3-wire serial port as communication interface for all the function and command setting.

3-Wire communication can be bi-directional controlled by the "R/W" bit in address field. EK79652 3-Wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-Wire bus itself.

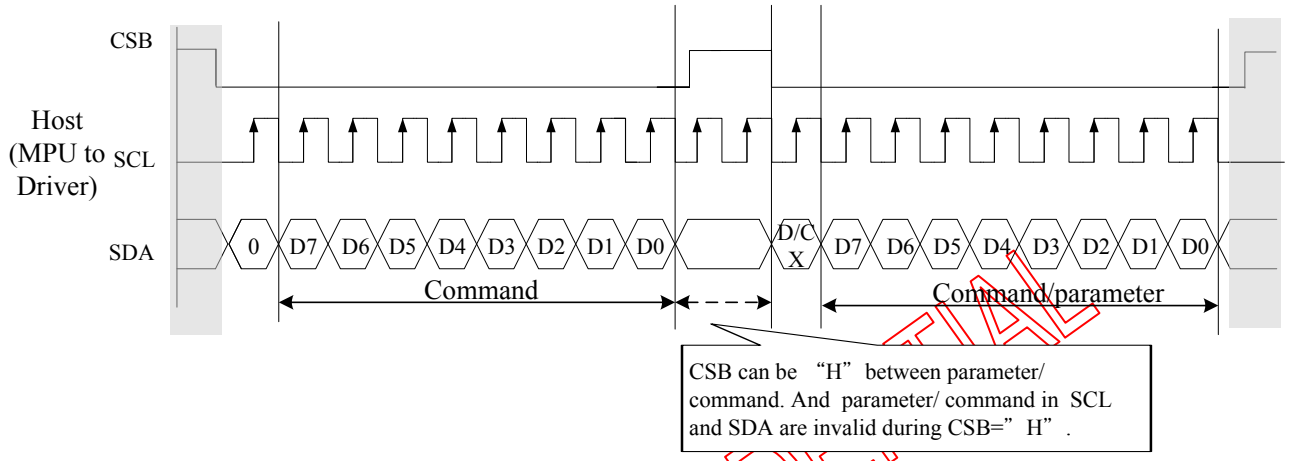
Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".



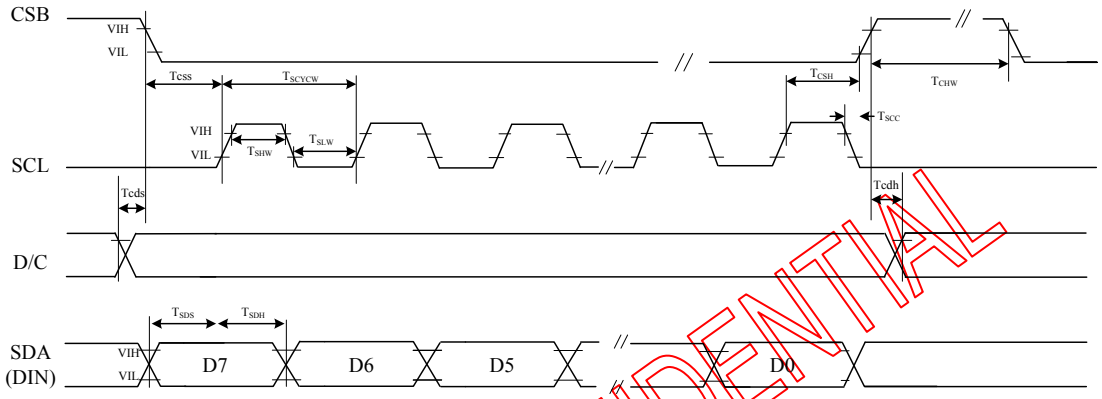
3 pin serial interface characteristics (write mode)



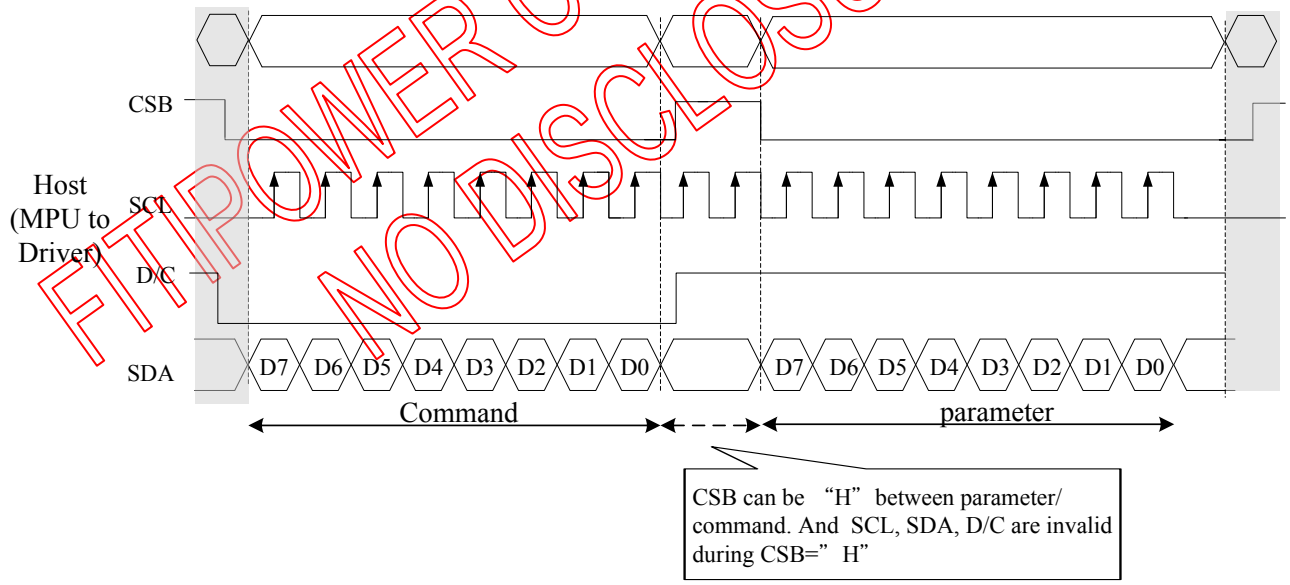
3 pin serial interface characteristics (read mode)



7.2 “4-Wire” Serial Port Interface



4 pin serial interface characteristics



8. SPI CONTROL REGISTERS:

8.1 Register Table

Following table list all the SPI control registers and bit name definition for EK79652. Refer to the next section for detail register function description.

Address	command	Bit										
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	07h
R01H	Power setting (PWR)	W	1	-	-	-	-	-		VDS_EN	VDG_EN	03h
		W	1			-	-	-	VCOM_HV	VGHL_LV [1]	VGHL_LV [0]	00h
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	26h
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
		W	1		VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	03h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-		T_VDS_OFF [1]	T_VDS_OFF [0]					00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R05H	Power ON Measure (PMES)	W	0	0	0	0	0	0	1	0	1	05H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	0	1	1	06H
		W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	03h
		W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	00h
		W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	26h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission1 (DTM1)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	00h
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	0	1	12H
R13H	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	0	0	13H
		W	1	#	#	#	#	#	#	#	#	00H
R14H	Partial Data Start transmission1 (PDTM1)	W	0	0	0	0	1	0	1	0	0	14H
		W	1	#	#	#	#	#	#	#	#	00H
R15H	Partial Data Start transmission 2 (PDTM2)	W	0	0	0	0	1	0	1	0	1	15H
		W	1	#	#	#	#	#	#	#	#	00H
R16H	Partial Display Refresh(PDRF)	W	0	0	0	0	1	0	1	1	0	16H
		W	1	#	#	#	#	#	#	#	#	00H
R20H	LUT for VCOM (LUT1)	W	0	0	0	1	0	0	0	0	0	20H
		W	1	#	#	#	#	#	#	#	#	00H
R21H	White to White LUT (LUTWW)	W	0	0	0	1	0	0	0	0	1	21H
		W	1	#	#	#	#	#	#	#	#	00H
R22H	Black to White LUT (LUTBW/LUTR)	W	0	0	0	1	0	0	0	1	0	22H
		W	1	#	#	#	#	#	#	#	#	00H
R23H	White to Black LUT (LUTWB/LUTW)	W	0	0	0	1	0	0	0	1	1	23H
		W	1	#	#	#	#	#	#	#	#	00H
R24H	Black to Black LUT (LUTBB/LUTB)	W	0	0	0	1	0	0	1	0	0	24H
		W	1	#	#	#	#	#	#	#	#	00H

R30H	OSC control (OSC)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	SEL_DIV[1:0]		SEL_F[4:0]					3Ch
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	
		R	1	D2	D1	D0	-	-	-	-	-	
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO0]	
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	0	1	43H
		W	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	
		W	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	
R60H	TCON setting (TCON)	W	0	0	1	1	0	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1								HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	HRES(1)	-	00h
		W	1								VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	
R62H	Source & gate start setting	W	0	0	1	1	0	0	0	1	0	
		W	1								S_start [8]	
		W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	S_start (2)	S_start (1)	S_start (0)	
		W	1				gscan				G_start [8]	
		W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	00h
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	-	PTL_flag	I^2C_ERR	I^2C_ BUSYN	Data_flag	PON	POF	BUSY_N	02h
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	00h
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	VCDS[6]	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	00h
RA0H	Program Mode (PGM)	W	0	1	0	1	0	0	0	0	0	A0H
		W	1	1	0	1	0	0	1	0	1	A5h
RA1H	Active program(APG)	W	0	1	0	1	0	0	0	0	1	A1H
RA2H	Read OTP Data (ROTP)	W	0	1	0	1	0	0	0	1	0	A2H
		R	1	#	#	#	#	#	#	#	#	
RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H
		W	1	-	-	-	-	cce_sel	cce_lr	TSFIX	CCEIN	00h
RE5H	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

8.2 Register Description

8.2.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	07h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

Bit	Name	Description
0	RST_N	RST_N function 1 : no effect. 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V(default)
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. **(default)**
2	SHL	SHL function 0: Shift left; First data=Sn →Sn-1 → …→S2 →Last data=S1. 1: Shift right; First data=S1→ S2 → …→Sn-1 → Last data=Sn. **(default)**
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→ G2 → Last line=G1. **(default)** 1:Scan up; First line=G1 →G2 →…→Gn-1 →Last line=Gn.
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. **(default)** 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP(default) 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 00: Display resolution is 320x300. **(default)** 01: Display resolution is 300x200 10: Display resolution is 296x160 11: Display resolution is 296x128

Notes:
1. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.

2. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.

8.2.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
2nd Parameter	W	1			-	-	-	VCOM_HV	VGHL_LV [1]	VGHL_LV [0]	00h
3rd Parameter	W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	26h
4th Parameter	W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
5th Parameter	W	1		VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	**Gate power selection.** 0 : External VDNS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL.
1	VDS_EN	**Source power selection.** 0 : External source power from VSH/VSL pins. 1 : Internal DC/DC function for generate VSH/VSL.

2nd Parameter:

Bit	Name	Description
1-0	VGHL_LV	**VGHL_LV Voltage Level.** 00: VGH=16 v, VGL=-16v (default) 01: VGH=15 v, VGL=-15v 10: VGH=14 v, VGL=-14v 11: VGH=13 v, VGL=-13v
2	VCOM_HV	**VCOM Voltage Level** 0: VCOMH=VSH+VCOMDC,VCOML=VSL+VCOMDC 1: VCOMH=VGH, VCOML=VGL

3rd Parameter: Internal VSH power selection for B/W LUT. **(Default value: 100110b)**

Bit	Name	Description
5-0	**VSH**	**Internal VSH power selection.** 000000: 2.4 v 000001: 2.6 v 000010: 2.8 v 000011: 3.0 v .... 010111: 7.0V 011000: 7.2 V 011001: 7.4 V 100110: 10.0V

		100111: 10.2 V 101000: 10.4 V 101001: 10.6V 101010: 10.8V 101011: 11.0V

4th Parameter: Internal VSL power selection for B/W LUT. **(Default value: 100110b)**

Bit	Name	Description
5-0	**VSL**	**Internal VSL power selection.** 000000: -2.4 v 000001: -2.6 v 000010: -2.8 v 000011: -3.0 v …. 010111: -7.0V 011000: -7.2 V 011001: -7.4 V …. 100110: -10.0V 100111: -10.2 V 101000: -10.4 V 101001: -10.6V 101010: -10.8V 101011: -11.0V

5th Parameter: Internal VSHR power selection for Red LUT. **(Default value: 000011b)**

Bit	Name	Description
5-0	**VSHR/VSLR**	**Internal VSL power selection.** 000000: 2.4 v 000001: 2.6 v 000010: 2.8 v 000011: 3.0 v …. 010111: 7.0V 011000: 7.2 V 011001: 7.4 V …. 100110: 10.0V 100111: 10.2 V 101000: 10.4 V 101001: 10.6V 101010: 10.8V 101011: 11.0V
6		0:"+", default 1:"-"

Note:
1.VSH>VSHR
2.VSL<VSLR

Restriction	

8.2.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	

8.2.4 R03H (PFS): Power off Sequence Setting Register

R03H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PFS	W	0	0	0	0	0	0	0	1	1	03H
1st Parameter	W	1	-	-	Vsh_off[1]	Vsh_off [0]	Vsl_off[1]	vsl_off[0]	vshr_off[1]	vshr_off[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :
1st Parameter:

Bit	Name	Description
1-0	**vshr_off**	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
3-2	**vsl_off**	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
5-4	**vsh_off**	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms

Restriction

8.2.5 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power off sequence, BUSY_N signal will rise from low to high.
Restriction	

8.2.6 R05H (PMES): Power ON Measure Command

R05H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PMES	W	0	0	0	0	0	0	1	0	1	05H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).
Restriction	

8.2.7 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	0	1	1	06H
1st Parameter	W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	03h
2nd Parameter	W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	00h
3rd Parameter	W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	26h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
2-0	**Driving strength of phase A**	000: 0.27uS 001: 0.34uS 010: 0.40uS 011: 0.54uS 100: 0.80uS 101: 1.54uS 110: 3.34uS 111: 6.58uS (default)
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase A**	00: 10mS (default) 01: 20mS 10: 30mS 11: 100mS

2nd Parameter:

Bit	Name	Description
2-0	**Driving strength of phase B**	000: 0.27uS 001: 0.34uS 010: 0.40uS 011: 0.54uS 100: 0.80uS 101: 1.54uS 110: 3.34uS 111: 6.58uS (default)
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase B**	00: 10mS (default) 01: 20mS 10: 30mS 11: 100mS

<table>
<tr><td>Description</td><td>3rd Parameter:

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>2-0</td><td>Minimum OFF time setting of GDR in phase C</td><td>000: 0.27uS
001: 0.34uS
010: 0.40uS
011: 0.54uS
100: 0.80uS
101: 1.54uS
110: 3.34uS
111: 6.58uS (default)</td></tr>
<tr><td>5-3</td><td>Driving strength of phase C</td><td>000: Strength 1
001: Strength 2
010: Strength 3 (default)
011: Strength 4
100: Strength 5
101: Strength 6
110: Strength 7
111: Strength 8</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

8.2.8 R07H (DSLP): Deep Sleep

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	

8.2.9 R10H (DTM1): Data Start transmission 1 Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
...	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM.
Restriction	

8.2.10 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter: Bit / Name / Description 7 / -- / 0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data. After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = "1".

8.2.11 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0".
Restriction	This command only actives when BUSY_N = "1".

8.2.12 R13H (DTM2): Data Start transmission 2 Register

R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
...	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

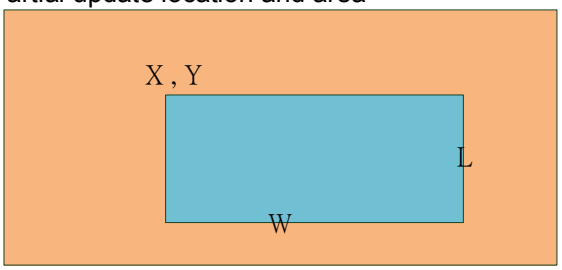
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM.
Restriction	

8.2.13 R14H (PDTM1): Partial Data Start transmission 1 Register

R14H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM1	W	0	0	0	0	1	0	1	0	0	14H
1st Parameter	W	1								X[8]	00h
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	
3rd Parameter										Y[8]	
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	
5th Parameter	W	1								W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	
7th Parameter										L[8]	
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	
	W	1									
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

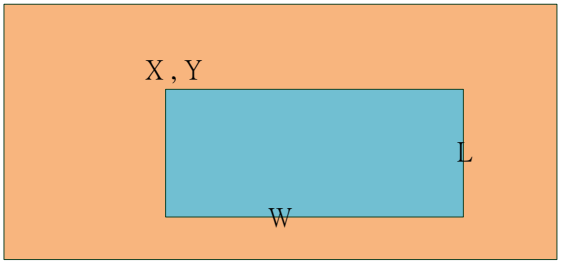
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indisates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

8.2.14 R15H (PDTM2): Partial Data Start transmission 2 Register

R15H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM2	W	0	0	0	0	1	0	1	0	1	15H
1st Parameter	W	1								X[8]	00h
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	
3rd Parameter										Y[8]	
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	
5th Parameter	W	1								W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	
7th Parameter										L[8]	
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	
	W	1									
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

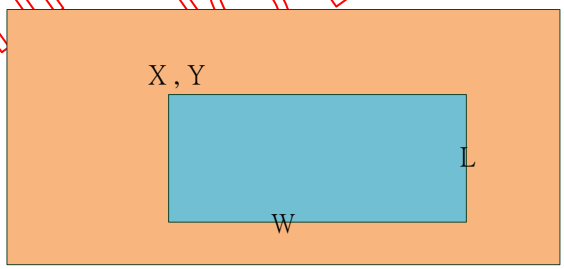
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indisates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

8.2.15 R16H (PDRF): Partial Display Refresh Command

R16H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDRF	W	0	0	0	0	1	0	1	1	0	16H
1st Parameter	W	1	DFV_EN							X[8]	00h
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	
										Y[8]	
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	
5th Parameter	W	1								W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	
										L[8]	
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: While user sent this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. Only the area (X,Y, W, L) would update, the others pixel output would follow VCOM LUT After display refresh command, BUSY_N signal will become "0".  Note: X and W should be the multiple of 8. DFV_EN: data follow VCOM function on display area. DFV_EN=1: Only effective in B/W mode, if pixel from "New data" SRAM equal to "Old data" SRAM on display area, this pixel output would follow VCOM LUT. DFV_EN=0: Data doesn't follow VCOM LUT.
Restriction	this command only active when BUSY_N = "1".

8.2.21 R30H (OSC): OSC control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
OSC	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	SEL_DIV[1:0]		SEL_F[5:0]						3Ch

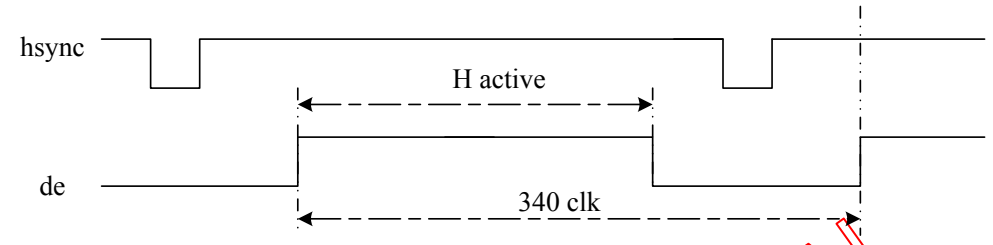
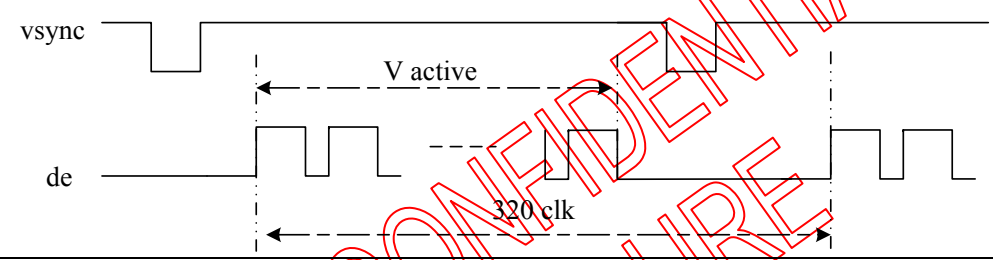
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

The command controls the OSC clock frequency. The OSC structure must support the following frame rates:

SEL_F[5:0]	SEL_DIV[1:0]				SEL_F[5:0]	SEL_DIV[1:0]			
	00	01	10	11		00	01	10	11
000000	156.25	78.13	39.06	-	100000	153.49	76.75	38.37	-
000001	159.01	79.5	39.75	-	100001	150.74	75.37	37.68	-
000010	161.76	80.88	40.44	20.22	100010	147.98	73.99	36.99	-
000011	164.52	82.26	41.13	20.57	100011	145.22	72.61	36.31	-
000100	167.28	83.64	41.82	20.91	100100	142.46	71.23	35.62	-
000101	170.04	85.02	42.51	21.25	100101	139.71	69.85	34.93	-
000110	172.79	86.4	43.2	21.6	100110	136.95	68.47	34.24	-
000111	175.55	87.78	43.89	21.94	100111	134.19	67.1	33.55	-
001000	178.31	89.15	44.58	22.29	101000	131.43	65.72	32.86	-
001001	181.07	90.53	45.27	22.63	101001	128.68	64.34	32.17	-
001010	183.82	91.91	45.96	22.98	101010	125.92	62.96	31.48	-
001011	186.58	93.29	46.65	23.32	101011	123.16	61.58	30.79	-
001100	189.34	94.67	47.33	23.67	101100	120.4	60.2	30.1	-
001101	192.1	96.05	48.02	24.01	101101	117.65	58.82	29.41	-
001110	194.85	97.43	48.71	24.36	101110	114.89	57.44	28.72	-
001111	197.61	98.81	49.4	24.7	101111	112.13	56.07	28.03	-
010000	-	100.18	50.09	25.05	110000	109.38	54.69	27.34	-
010001	-	101.56	50.78	25.39	110001	106.62	53.31	26.65	-
010010	-	102.94	51.47	25.74	110010	103.86	51.93	25.97	-
010011	-	104.32	52.16	26.08	110011	101.1	50.55	25.28	-
010100	-	105.7	52.85	26.42	110100	98.35	49.17	24.59	-
010101	-	107.08	53.54	26.77	110101	95.59	47.79	23.9	-
010110	-	108.46	54.23	27.11	110110	92.83	46.42	23.21	-
010111	-	109.83	54.92	27.46	110111	90.07	45.04	22.52	-
011000	-	111.21	55.61	27.8	111000	87.32	43.66	21.83	-
011001	-	112.59	56.3	28.15	111001	84.56	42.28	21.14	-
011010	-	113.97	56.99	28.49	111010	81.8	40.9	20.45	-
011011	-	115.35	57.67	28.84	111011	79.04	39.52	-	-
011100	-	116.73	58.36	29.18	111100	76.29	38.14	-	-
011101	-	118.11	59.05	29.53	111101	73.53	36.76	-	-
011110	-	119.49	59.74	29.87	111110	70.77	35.39	-	-
011111	-	120.86	60.43	30.22	111111	68.01	34.01	-	-

remark	-Horizental  -Vertical 
Restriction	

8.2.22 R40H (TSC): Temperature Sensor Command

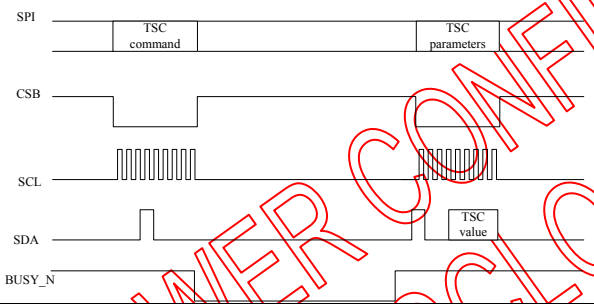
R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	
2nd Parameter	R	1	D2	D1	D0	-	-	-	-	-	

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:
This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.
If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.23 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Bit	temperature
2-0	mean temperature offset value 000:0℃ 001:1℃ 010:2℃ …. 111:7℃
3	Positive and negative value 0:"+" 1: "-"
7	**Internal temperature sensor enable** 0: Internal temperature sensor enable.(**default)** 1: Internal temperature sensor disable, using external temperature sensor.

For example:
1100: - 4 degree c
0111: + 7 degree c

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.24 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	temperature
2-0	Pointer setting
5-3	User-defined address bits (A2, A1, A0)
7-6	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	temperature
7-0	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	temperature
7-0	LSByte of write-data to external temperature sensor

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.25 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	00h
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	temperature
7-0	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	temperature
7-0	LSByte of write-data from external temperature sensor

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.26 R50H (CDI): VCOM and DATA interval setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h

NOTE: "-" Don't care, can be set to VDD or GND level

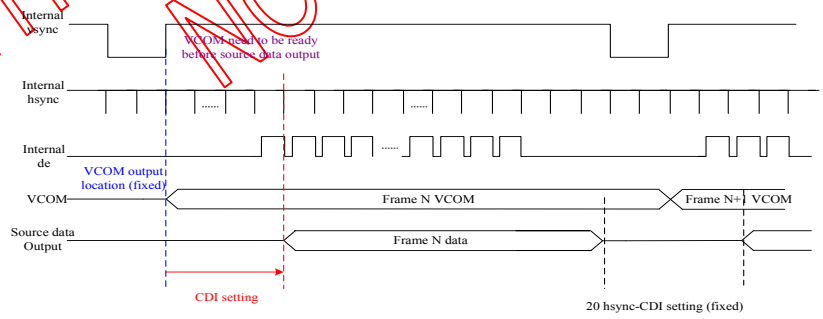
Description

-The command defines as:

1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit	
3-0	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[1:0] Border data selection.

B/W/Red mode(BWR=0)

Bit 5-4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11 (default)	Floating

B/W mode (BWR=1)

Bit 5-4	Bit7-6	description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
1 (default)	00	Floating
	01	LUTWB (1->0)
	10	LUTBW (0->1)
	11	Floating

DDX[1:0]: Data polarity
1. DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
2. DDX[0] for B/W mode

B/W/Red mode(BWR=0)

Bit 5-4	Description	
DDX[1:0]	Data (Red/B/W)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

Bit 5-4	Description	
DDX[0]	Data (B/W)	LUT
0	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
1 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

8.2.27 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD<2.5v). 1st Parameter: Bit 0 – LPD 0 – Low power input. 1 – Normal status. **(Default)**
Restriction	

8.2.28 R60H (TCON): TCON setting

R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h

NOTE: "-" Don't care, can be set to VDD or GND level

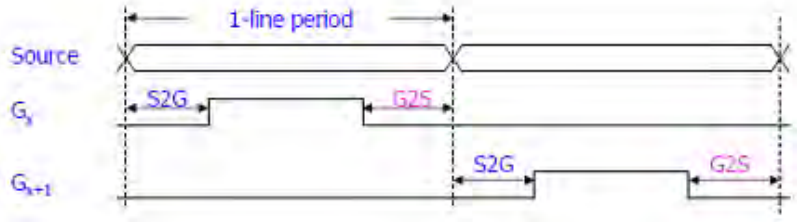
Description

- The command define Non-overlap period of gate and source as below:

1st Parameter:

Bit	Period
S2G[3:0]/G2S[3:0]	0000: 4 clock 0001: 8 clock 0010: 12 clock (default) 0011:16 clock 0100: 20 clock 0101: 24 clock 0110: 28 clock 0111: 32 clock 1000: 36 clock 1001: 40 clock 1010: 44 clock 1011: 48 clock 1100: 52 clock 1101: 56 clock 1110: 60 clock 1111: 64 clock

Period=660ns



Restriction

8.2.29 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1								HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	HRES(1)	-	00h
3rd Parameter	W	1								VRES(8)	ooh
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution = HRES Vertical display resolution = VRES Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[7:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[8:1]*2-1 EX :320X240 GD: First G active = G0 LAST active GD= 0+240-1= 239; (G239) SD : First active channel: =S0 LAST active SD=0+320-1=319; (S319)
Restriction	

8.2.30 R62H (TSGS): Source & gate start setting

R62H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSGS	W	0	0	1	1	0	0	0	1	0	62H
1st Parameter	W	1								S_start [8]	00h
2nd Parameter	W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	S_start (2)	S_start (1)	S_start (0)	00h
3rd Parameter	W	1				gscan				G_start [8]	ooh
4th Parameter	W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line 3. gscan :Gate scan select 0: Normal scan 1: Cascade type 2 scan
Restriction	

8.2.31 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: The LUT_REV is read from OTP address = 0x001.
Restriction	- This command only actives when BUSY_N = "1".

8.2.32 R71H (FLG): Status register

R71H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
FLG	W	0	0	1	1	1	0	0	0	1	71H
1st Parameter	R	1	-	-	I2C_ERR	II2C_BUSYN	Data_flag	PON	POF	BUSY_N	02h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the IC status. Host can read this data to understand the IC status. 1st Parameter:

Bit	Function
5	I2C master error status
4	I2C master busy status (low active)
3	Driver has already received one frame data
2	PON 0: Not in PON mode 1: In PON mode
1	POF 0: Not in POF mode(default) 1: In POF mode
0	Driver busy status(low active)

Restriction	User can send this command in any time. It doesn't have restriction of BUSY_N.

8.2.33 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80 H
1st Parameter	W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Function
0	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSHR during Auto Measure VCOM period.
3	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	The sensing time of VCOM detection 00: 3s 01: 5s (default) 10: 8s 11: 10s

Restriction: This command only actives when BUSY_N = "1".

8.2.34 R81H (VV): Vcom Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	(81H)
1st Parameter	R	1		VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command could get the Vcom value 1st Parameter:

Bit	Function
5-0	Vcom value 0000000: -0.1V 0000001:-0.15V 0000010:-0.2V …. 0111010:-3.0V …. 1001110:-4.0V

Restriction	This command only actives when BUSY_N = "1".

8.2.35 R82H (VDCS): Vcom_DC Setting register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	VCDS[6]	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command set the VCOM DC value. Driver will base on this value for VCM_DC. 1st Parameter:

Bit	Function
5-0	**VCOM value** 0000000:-0.1V(default) 0000001:-0.15V 0000010:-0.2V …. 0111010:-3.0V …. 1001110:-4.0V

Restriction	This command only actives when BUSY_N = "1".

8.2.36 RA0H (PGM): Program Mode

RA0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	1	0	0	0	0	0	A0H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset. The only one parameter is a check code, the command would be executed if check code = 0xA5.
Restriction	This command only actives when BUSY_N = "1".

8.2.37 RA1H (APG): Active Program

RA1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	1	0	0	0	0	1	A1H

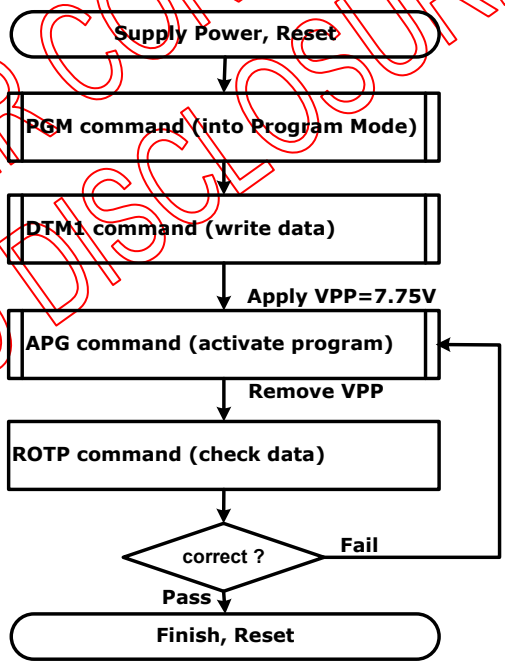
NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

8.2.38 RA2H (ROTP): Read OTP Data

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
ROTP	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	R	1	Dummy								
2nd Parameter	R	1	The data of address 0x000 in the OTP								
3rd Parameter	R	1	The data of address 0x001 in the OTP								
4th Parameter	R	1	:								
5th Parameter	R	1	The data of address (n-1) in the OTP								
6th~ (m-1)th Parameter	R	1	.....								
mth Parameter	R	1	The data of address (n) in the OTP								

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.  The sequence of programming OTP
Restriction	This command only actives when BUSY_N = "1".

8.2.39 RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	R	1	-	-	-	-	cce_sel	cce_lr	TSFIX	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is used for cascade.

1st Parameter:

Bit	
0	Output clock enable/disable. 0: Output 0V at CL pin. (default) 1: Output clock at CL pin for slave chip.
1	Let the value of slave's temperature is same as the master's. 0: Temperature value is defined by internal temperature sensor / external LM75. (default) 1: Temperature value is defined by TS_SET [7:0] registers.
2	Cascade direction 0 : Master(right side output) -> Slave(left side input) 1 : Slave(right side input) <- master(left side output)
3	Cascade LR Select 0:Pin 1:Register(cce_lr)

Restriction

This command only actives when BUSY_N = "1".

8.2.40 RE5H (TSSET): Force Temperature

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command is used to fix the temperature value of master and slave chip in cascade
Restriction	

8.3 Register Restriction

Following table will indicate the register restriction:

Register	Refresh restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R03H(PFS)	X	No action
R04H(PON)	X	Flag
R05H(PMES)	X	No action
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM1)	X	No action
R11H(DSP)	Valid (only read)	Flag
R12H(DRF)	X	Flag
R13H(DTM2)	X	No action
R14H(PDTM1)	X	No action
R15H(PDTM2)	X	No action
R16H(PDRF)	X	Flag
R20H(LUTC)	X	No action
R21H(LUTWW)	X	No action
R22H(LUTBW/LUTR)	X	No action
R23H(LUTWB/LUTW)	X	No action
R24H(LUTBB/LUTB)	X	No action
R30H(OSC)	X	No action
R40H(TSC)	Valid (only read)	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	No action
R43H(TSR)	Valid (only read)	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid (only read)	No action
R60H(TCON)	X	No action
R61H(TRES)	X	No action
R70H(REV)	Valid (only read)	No action
R71H(FLG)	Valid (only read)	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
RA0H(PGM)	X	No action
RA1H(APG)	X	Flag
RA2H(ROTP)	X	No action
RE0H(CCSET)	X	No action
RE5H(TSSET)	X	No action

9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power on Sequence

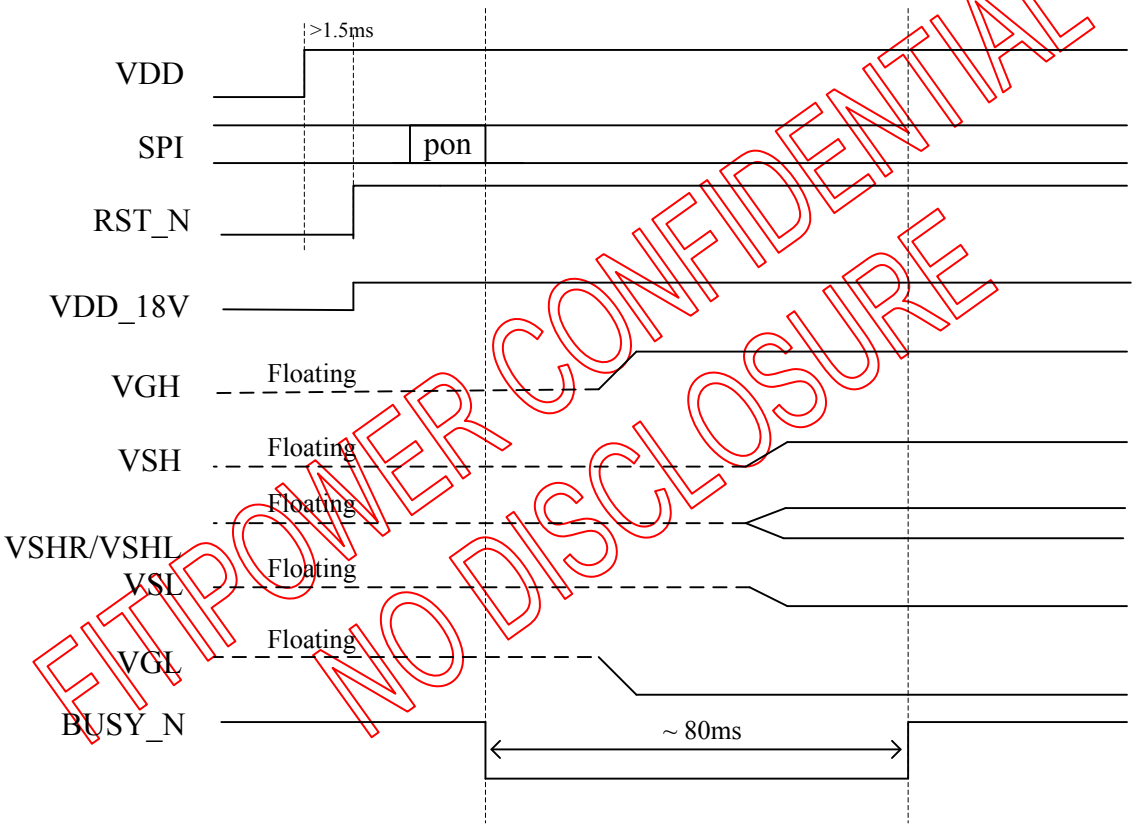


Figure 1: Power on sequence

Power off Sequence

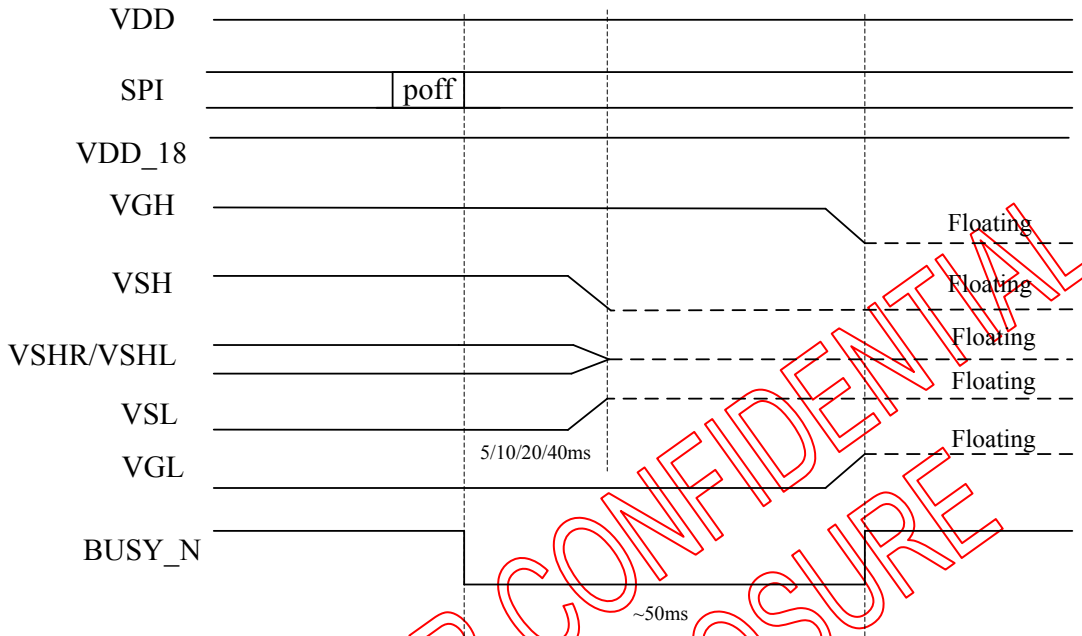


Figure 2: Power off sequence

DSLP sequence

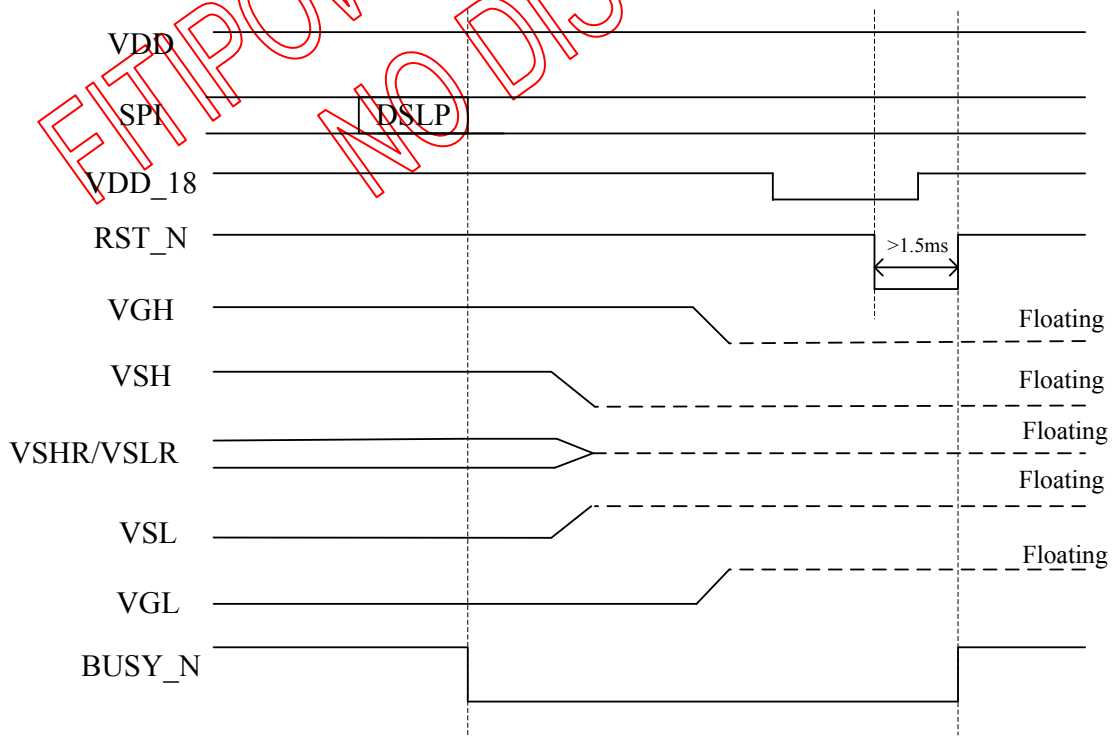


Figure 3: DSLP sequence

9.2 OTP LUT Definition

The OTP size would be 4096 Byte included temperature segment setting and 15 set waveform.

If TEMP<Boundary 0, use TR0 WF

If Boundary 0 ≦TEMP<Boundary1, use TR1

If Boundary 1 ≦TEMP<Boundary2, use TR2

.....

Addr (hex)	
00h~0Fh	Temp. segment
20h~60h	Default setting
100h	TR0 WF
200h	TR1 WF
300h	TR2 WF
400h	TR3 WF
500h	TR4 WF
600h	TR5 WF
700h	TR6 WF
800h	TR7 WF
900h	TR8 WF
A00h	TR9 WF
B00h	TR10 WF
C00h	TR11 WF
D00h	TR12 WF
E00h	TR13 WF
F00h	TR14 WF

Temperature segment:

Command	Addr (dec)	Addr(hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
--	0	000	Check Code (0xA5)							
	1	001	LUT Version							
	2	002	TEMP Boundary 0							
	3	003	TEMP Boundary 1							
	4	004	TEMP Boundary 2							
	5	005	TEMP Boundary 3							
	6	006	TEMP Boundary 4							
	7	007	TEMP Boundary 5							
	8	008	TEMP Boundary 6							
	9	009	TEMP Boundary 7							
	10	00A	TEMP Boundary 8							
	11	00B	TEMP Boundary 9							
	12	00C	TEMP Boundary 10							
	13	00D	TEMP Boundary 11							
	14	00E	TEMP Boundary 12							
	15	00F	TEMP Boundary 13							
	16~31	010~01F	Reserved							

Default setting:

	32	020	Enable OTP Setting (0xA5)						
R00H	33	021	res[1:0]		reg_en	bwr	ud	shl	shd_n	
R01H	34	022							Vds_en	Vdg_en
	35	023						Vcom_hv	Vghl_lv[1:0]	
	36	024	Vsh[5:0]							
R01H	37	025	Vsl[5:0]							
	38	026	VSHr[6:0]							
R03H	39	027			Vsh_off[1:0]		Vsl_off[1:0]		vshr_off[1:0]	
R06H	40	028	bt_pha[7:0]							
	41	029	bt_phb[7:0]							
	42	02A			bt_phc[5:0]					
R16H	43	02B	DFV_EN							
	44~50	02C~032	Reserved							
R30H	51	033	Sel_div[1:0]				Sel_f[5:0]			
R41H	52	034	tse					To[3:0]		
R42H	53	035	Wattr[7:0]							
	54	036	Wmsb[7:0]							
	55	037	Wlsb[7:0]							
R50H	56	038	vbd[1:0]		ddx[1:0]		cdi[3:0]			
R60H	57	039	s2g[3:0]				g2s[3:0]			
R61H	58	03A								hres[8]
	59	03B	hres[7:1]							
	60	03C								vres[8]
	61	03D	vres[7:0]							
R80H	62	03E			amvt[1:0]		xon	amvs	amv	amve
R82H	63	03F			vdcs[5:0]					
RE0H	64	040					cce_sel	cce_lr	tsfix	ccein
RE5H	65	041	ts_set[7:0]							
R62H	66	042								sstart[8]
	67	043	sstart[7:0]							
	68	044				gscan				gstart[8]
	69	045	gstart[7:0]							
	70~72	046~048	Reserved							
Slave setting										
	73	049	**slv_res[1:0]**		**slv_reg_en**	**slv_bwr**	**slv_ud**	**slv_shl**	**slv_shd_n**	**--**
	74	04A								**slv_sstart[8]**
	75	04B	**slv_sstart[7:0]**							
	76	04C				**slv_gscan**				**slv_gstart[8]**
	77	04D	**slv_gstart[7:0]**							

TR1~14 WF is the same as TR0 defined as below:

	Discription	Addr (dec)	Addr (hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	PS1
TR0 WF	Voltage	256	100	sel_div[1:0]		sel_f[5:0]						
		257	101	vghl_lv[1:0]		vsh[5:0]						
		258	102	-	vcom _hv	vsl[5:0]						
		259	103	-	vshr[6:0]							
		260	104	-	-	vdcs[5:0]						
	LUTC	261	106		XON							
		262	107		VCOMH							
		263	108	1th Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th Level selection [1:0]		Stage 1
		264	109	1st Frame number [7:0]								
		265	10A	2nd Frame number [7:0]								
		266	10B	3rd Frame number [7:0]								
		267	10C	4th Frame number [7:0]								
		302	12F	Repeat numbers [7:0]								
		303	130	Stage 2~ Stage 7								
		304	131									
	LUTWW	305	132	1th Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th Level selection [1:0]		Stage 1
		306	133	1st Frame number [7:0]								
		307	134	2nd Frame number [7:0]								
		308	135	3rd Frame number [7:0]								
		309	136	4th Frame number [7:0]								
		310	137	Repeat numbers [7:0]								
		311	138	Stage 2~ Stage 7								
		346	15B									
	LUTBW / LUTR	347	15C	1th Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th Level selection [1:0]		Stage 1
		348	15D	1st Frame number [7:0]								
		349	15E	2nd Frame number [7:0]								
		350	15F	3rd Frame number [7:0]								
		351	160	4th Frame number [7:0]								
		352	161	Repeat numbers [7:0]								
		353	162	Stage 2~ Stage 7								
		388	185									

	LUTWB / LUTW	389	186	1th Level selection [1:0]	2nd Level selection [1:0]	3rd Level selection [1:0]	4th Level selection [1:0]	Stage 1
		390	187	1st Frame number [7:0]				
		391	188	2nd Frame number [7:0]				
		392	189	3rd Frame number [7:0]				
		393	18A	4th Frame number [7:0]				
		394	18B	Repeat numbers [7:0]				
		395	18C	Stage 2~ Stage 7				
		430	1AF					
	LUTBB / LUTB	431	1B0	1th Level selection [1:0]	2nd Level selection [1:0]	3rd Level selection [1:0]	4th Level selection [1:0]	Stage 1
		432	1B1	1st Frame number [7:0]				
		433	1B2	2nd Frame number [7:0]				
		434	1B3	3rd Frame number [7:0]				
		435	1B4	4th Frame number [7:0]				
		436	1B5	Repeat numbers [7:0]				
		437	1B6	Stage 2~ Stage 7				
		472	1D9					

9.3 Data transmission waveform

Example1: LUT all states (7 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 v.

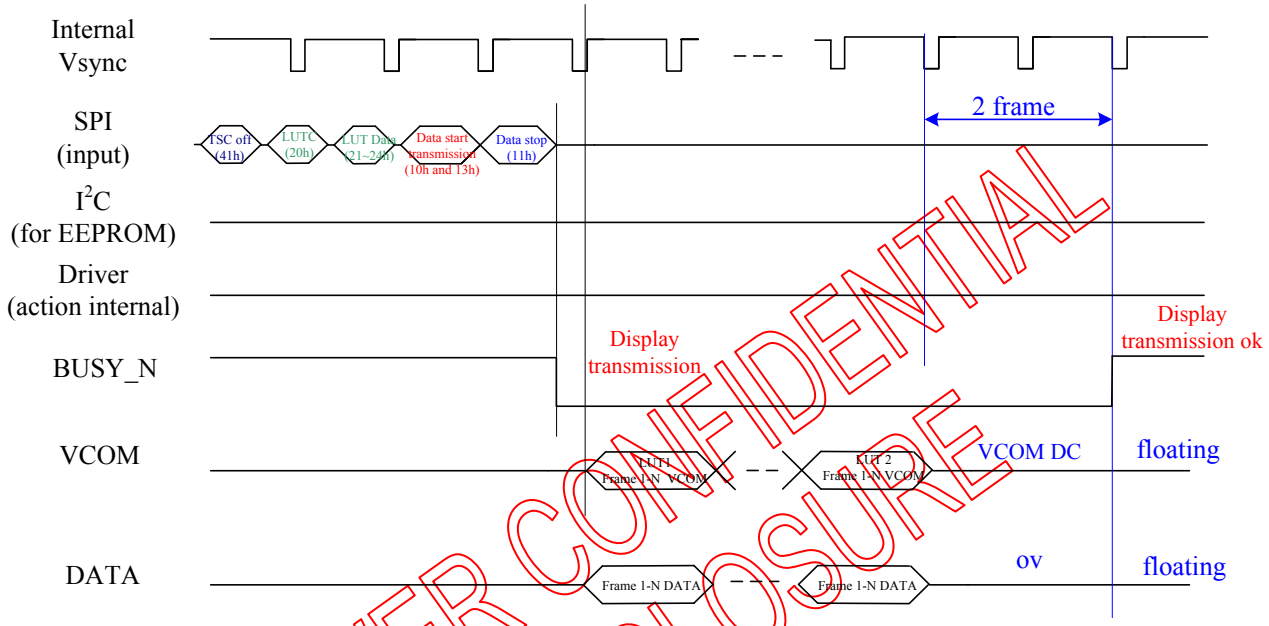


Figure 3: Data transmission example1 waveform

Example2: While level selection in LUT is "11", the driver will float VCOM and data.

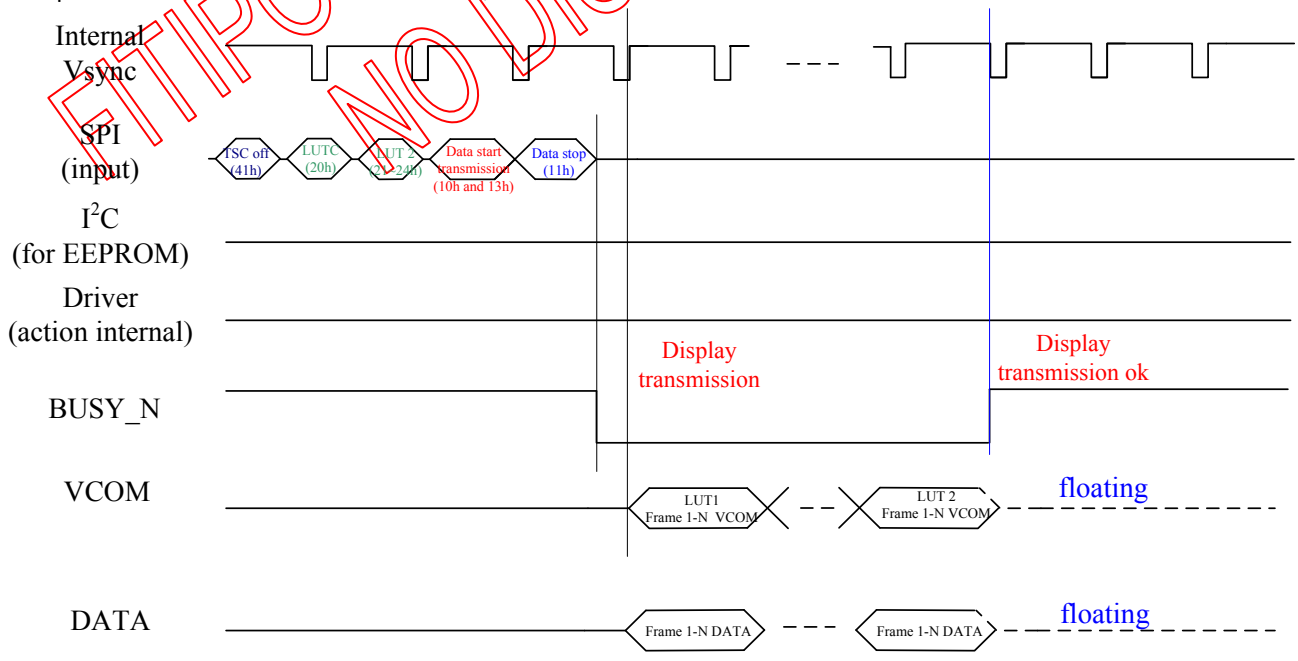


Figure 4: Data transmission example 2 waveform

9.4 Display refresh waveform

Example1: LUT all states (7 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 v.

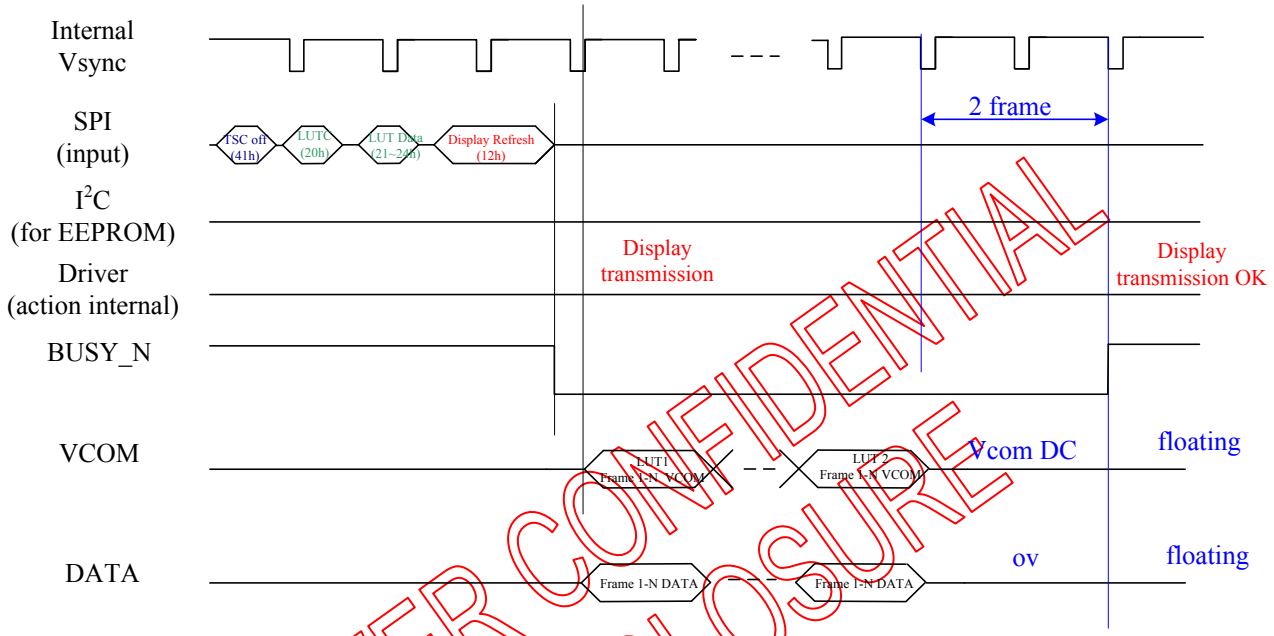


Figure 5: Display refresh example1 waveform

Example2: While level selection in LUT is "11", the driver will float VCOM and data.

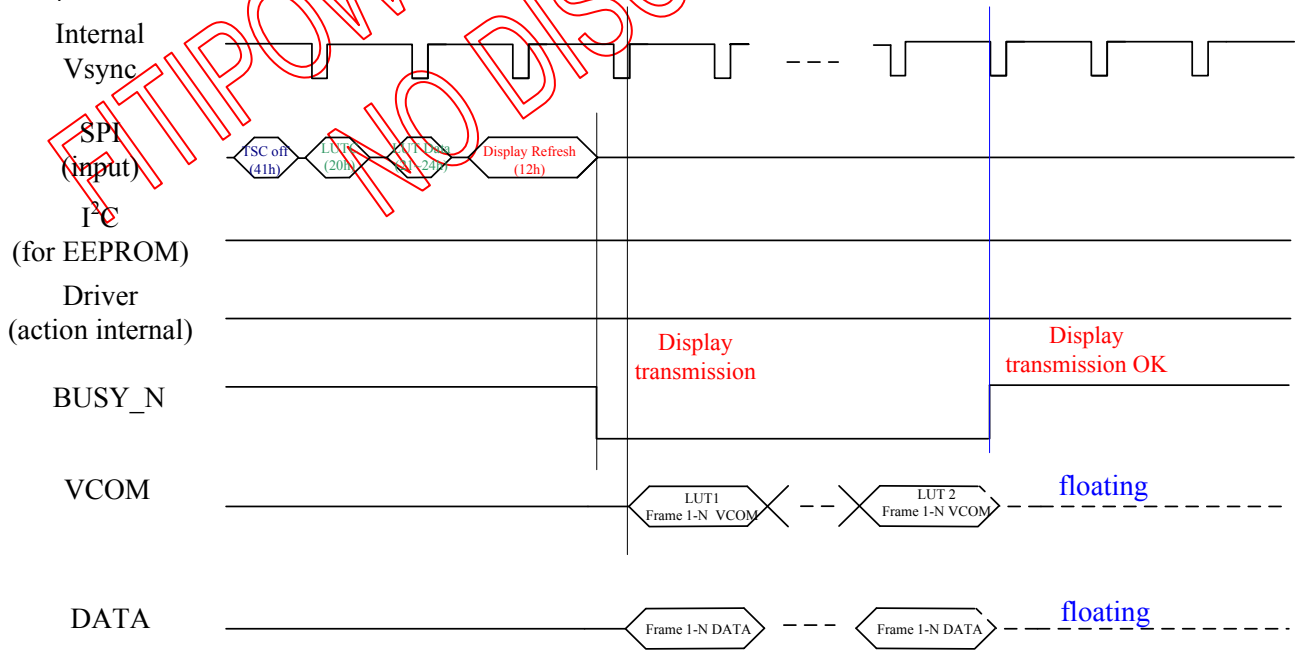


Figure 6: Display refresh example2 waveform

9.5 BUSY_N signal flow chart

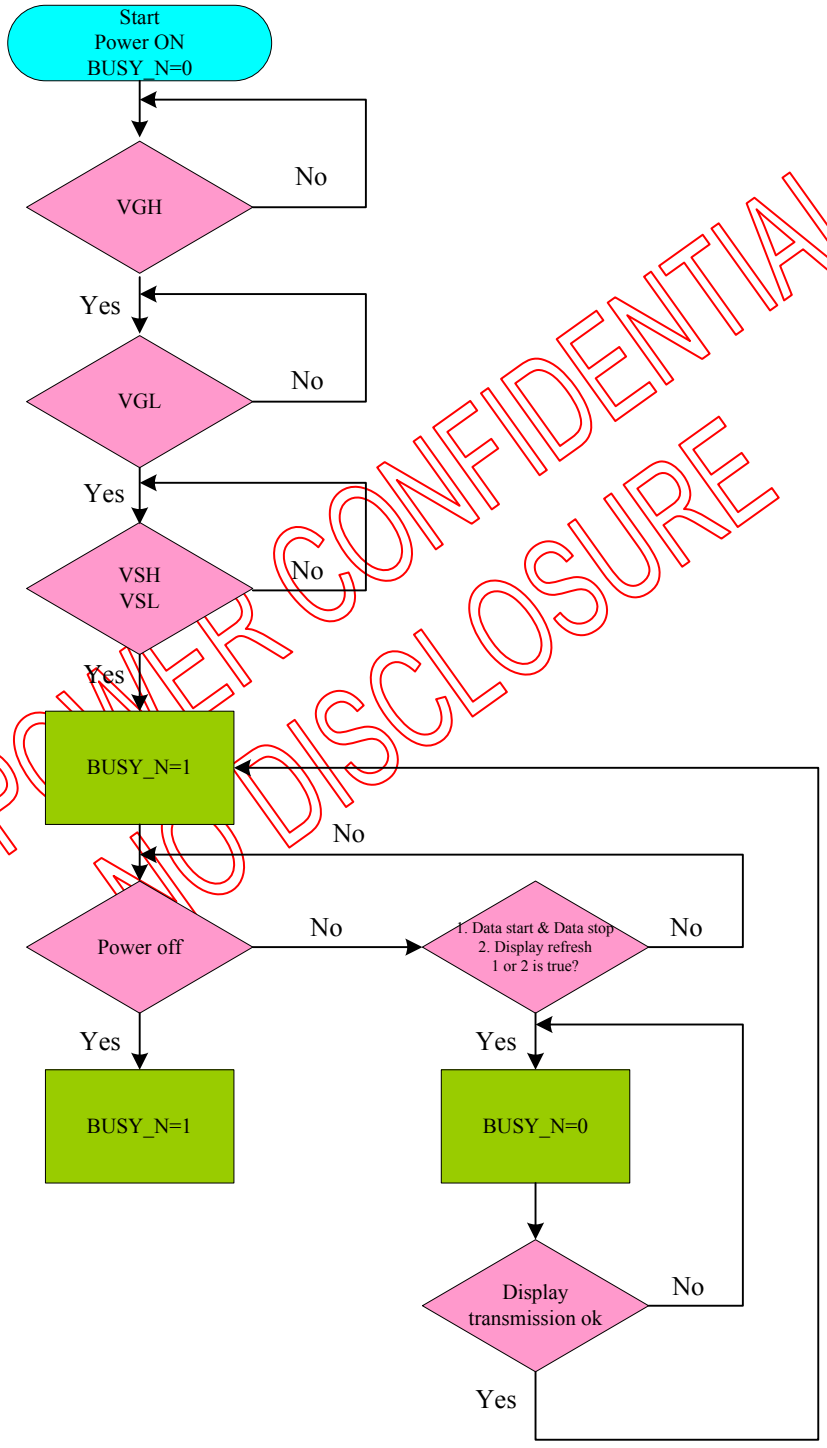


Figure 7: BUSY_N signal flow chart

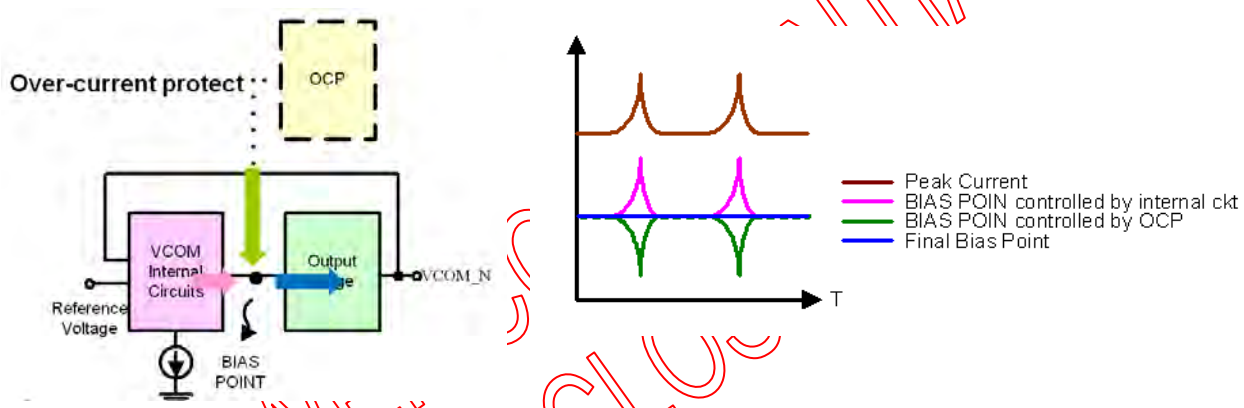
9.6 Over-Current Protect

Function:

the circuit could adjust the bias dynamically. When sensing the variation in bias point, OCP will have a reverse current.

Application:

In TFT substrate, this circuit could reduce the VCOM instant current and then decrease the VDD current. In ESL application, boost circuit take charge of the VDD instant current. Therefore, instant current still could be controlled well when turning off the OCP function.



Turn off command:

```
EPD_W21_WriteCMD(0xF8);
EPD_W21_WriteDATA (0x60);
EPD_W21_WriteDATA (0xA5);
EPD_W21_WriteCMD(0xF8);
EPD_W21_WriteDATA (0x73);
EPD_W21_WriteDATA (0x23);
EPD_W21_WriteCMD(0xF8);
EPD_W21_WriteDATA (0x7C);
EPD_W21_WriteDATA (0x00);
```

10. ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	TBD	V
Supply range	VGH-VGL	VGL-0.3	VGH+0.3	V
Analog supply	VSH	+2.4	+11	V
Analog supply	VSL	-11	-2.4	V
Analog supply	VSHR	-11	+11	
Supply voltage	VGH	-	+16	V
Supply voltage	VGL	-15	-	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

10.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.8V output voltage	VDD_18	1.62	1.8	1.98		
1.8V input voltage	VDD_18	1.62	1.8	1.98		
OTP program power	VOTP	7.25	7.5	7.75		
Digital ground	VSS		0			
DCDC ground	VSSP		0			
Low Level Input Voltage	Vil	GND	-	0.3xVDD	V	Digital input pins
High Level Input Voltage	Vih	0.7xVIO	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400μA
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400μA DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL = -400μA
Input Leakage Current	Iin	-1.0	-	+1.0	uA	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Digital Stand-by Current (power off mode)	IstVDD*	-	0	0.1	uA	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	mA	
IO Stand-by Current (power off mode)	IstVDDIO*	-	0.4	1.0	uA	All stopped
IO Operating Current	IVDDIO*	-	-	0.2	mA	No load
DCDC Stand-by Current (power off mode)	IstVDD1*	-	0	0.1	uA	All stopped
DCDC Operating Current	IVDD1*	-	-	0.5	mA	fdcdc=250kHz, No load
DCDC Operating Current	IVDD1*	-	3	5	mA	fdcdc=250kHz, External cap: PMOS=415pF, NMOS=340pF
Operating temperature	T_{op}	-30	-	85	℃	

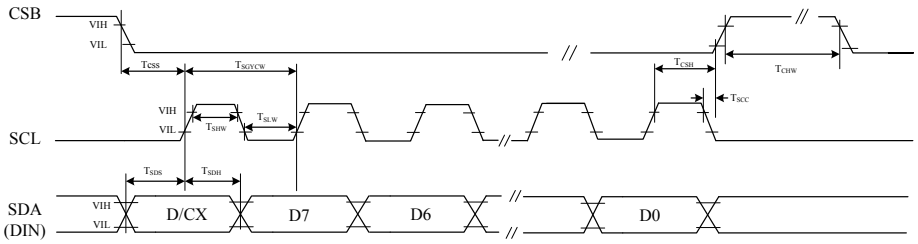
NOTE: typ. and max. values to be confirmed by design

10.3 Analog DC Characteristics

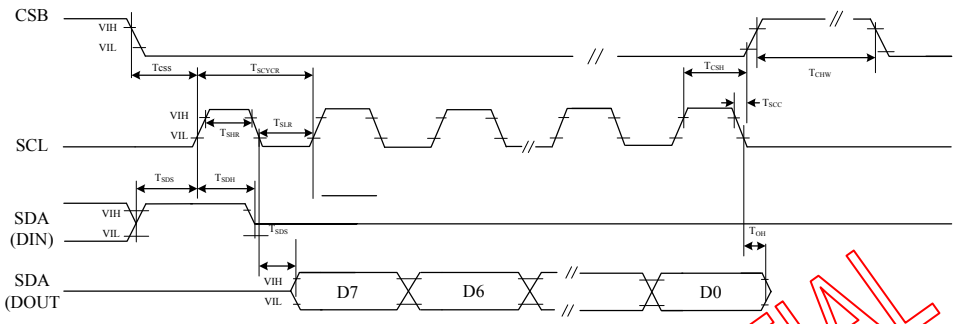
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSH		10		V	For source driver/VCOM
Positive Source voltage dev	d VSH	-300	0	+300	mV	
Negative Source voltage	VSL		-10		V	For source driver/VCOM
Negative Source voltage dev	d VSL	-300	-	+300	mV	
Positive Source voltage for Red	VSHR					
Negative Source voltage for Red	VSLR					
Analog Operating Current	Idd		TBD		mA	No load,
Dynamic Range of Output	Vdr	0.1	-	VSH-0.1	V	
Voltage Range of VGH - VGL	VGH-VGL	4.8	-	31	V	
Negative Source voltage	VGL	-15	-	-12	V	For gate driver
Negative Source voltage dev	dVGL	-400	0	+400	mV	
Positive Source voltage	VGH	13		16	V	For gate driver
Positive Source voltage dev	dVGH	-400	0	+400	mV	
Positive HV Stand-by Current (power off mode)	IstVGH*	-	0	0.2	uA	Include VSH power With load
Positive HV Operating Current	IVGH*	-	0.7	1.1	mA	Include VSH power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVGH*	-	0.8	1.2	mA	Include VSH power With load all SD=H VCOM external resistor divider not included
Negative HV Stand-by Current (power off mode)	IstVGL*	-	0	0.2	µA	Include VSH power With load
Negative HV Operating Current	IVGL*	-	0.8	1.2	mA	Include VSL power With load all SD=L
Negative HV Operating Current	IVGL*	-	0.9-	1.3	mA	Include VSL power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*		0	0.01	µA	
VINT1 Operating Current	IVINT1*			0.3	mA	

10.4 AC Characteristics

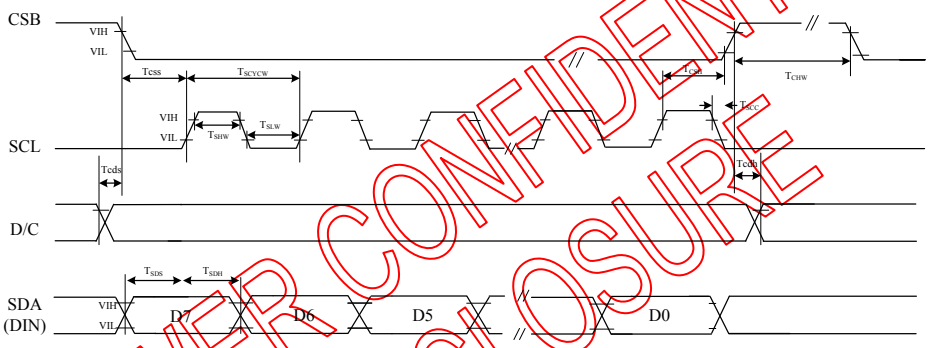
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	tCSS	60			ns	Chip select setup time
	tCSH	65			ns	Chip select hold time
	tSCC	20			ns	Chip select CSB setup time
	tCHW	150			ns	Chip select setup time
SCL	tSCYCW	100			ns	Serial clock cycle (Write)
	TSHW	35	-		ns	SCL “H” pulse width (Write)
	tSLW	35	-		ns	SCL “L” pulse width (Write)
	tSCYCR	150	-		ns	Serial clock cycle (Read)
	TSHR	60			ns	SCL “H” pulse width (Read)
	tSLR	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	tSDS	30			ns	Data setup time
	tSDH	30			ns	Data hold time
	tACC	10			ns	Access time
	tOH	15			ns	Output disable time
D/C	Tcds	20				DC setup time
	Tcdh	20				DC hold time
RC loading						
Source driver output loading	RL_S	-	13.36K		Ω	
	CL_S		39.19		pf	
Gate driver output loading	RL_S		12.32K		Ω	
	CL_S		32.09		pf	
VCOM output loading	RL_com		61.26		Ω	
	CL_com		3365.7		pf	
Driver						
Source driver rise time	trS		5		us	99% final value
Source driver fall time	tFS		5		us	
Gate driver rise time	TrG		5		us	99% final value
Gate driver fall time	tFG		5		us	
VCOM rise time	trCOM		1		ms	99% final value
VCOM fall time	tFCOM		1		ms	



3 pin serial interface characteristics (white mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics

Figure 8: SPI interface timing

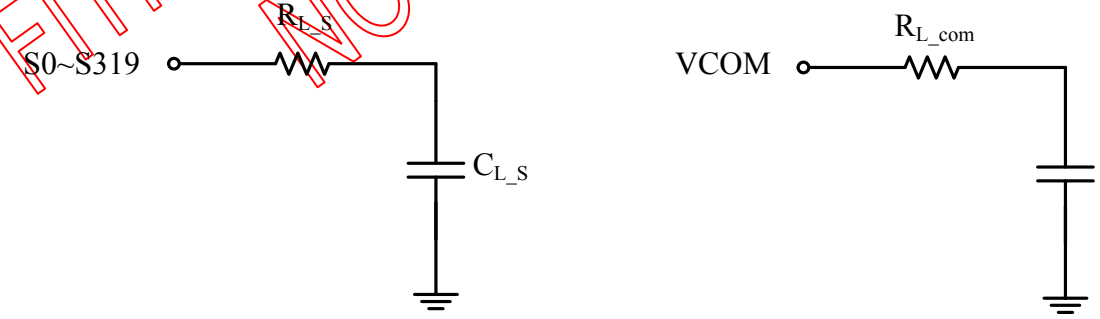
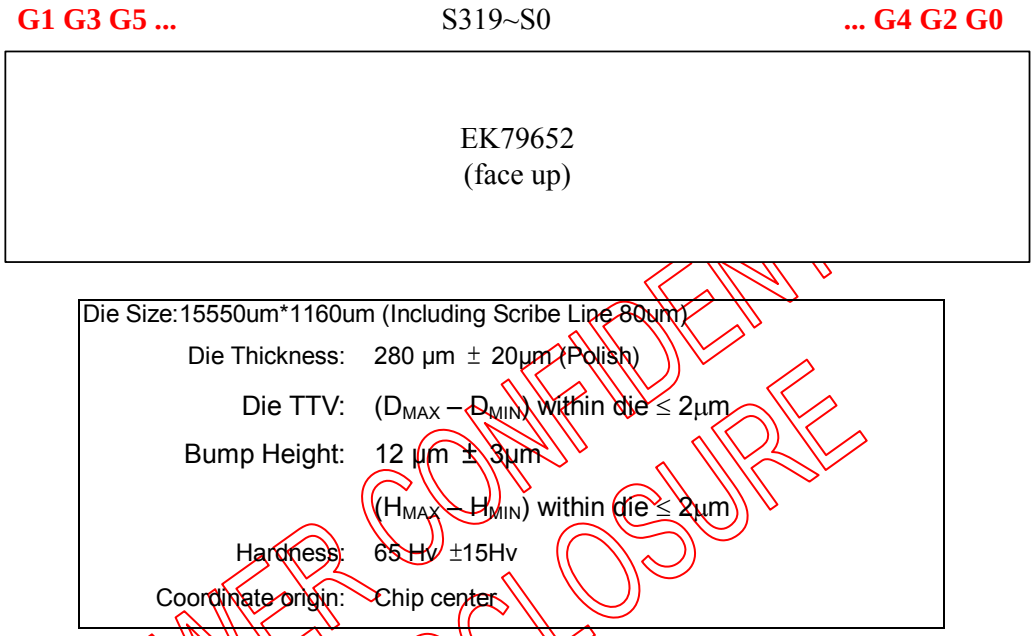


Figure 9: RC loading

11. CHIP OUTLINE DIMENSIONS

11.1 Circuit/Bump View

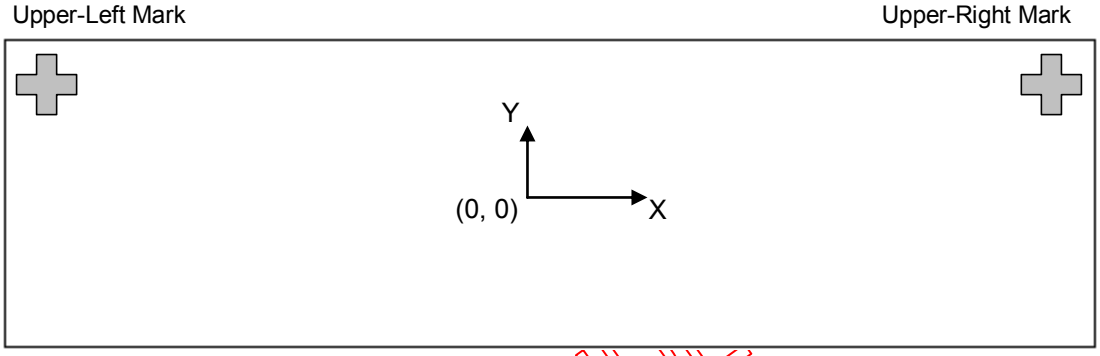


Die Size: 15550um*1160um (Including Scribe Line 80um)

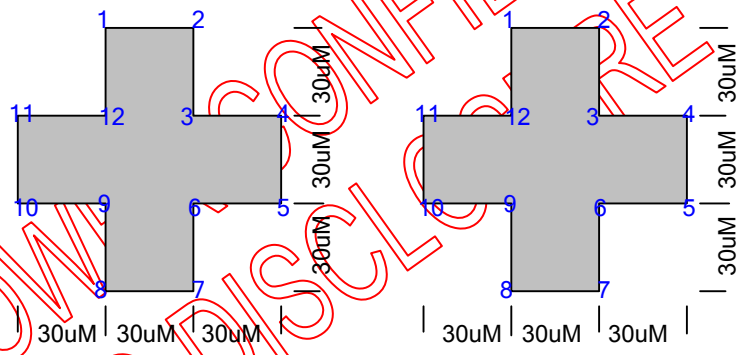
Die Thickness:	280 μm ± 20μm (Polish)
Die TTV:	$(D_{MAX} - D_{MIN})$ within die ≤ 2μm
Bump Height:	12 μm ± 3μm
	$(H_{MAX} - H_{MIN})$ within die ≤ 2μm
Hardness:	65 Hv ±15Hv
Coordinate origin:	Chip center

12. ALIGNMENT MARK INFORMATION

12.1 Location:



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-7499.5	444	7499.5	444
1	-7514.5	489	7484.5	489
2	-7484.5	489	7514.5	489
3	-7484.5	459	7514.5	459
4	-7454.5	459	7544.5	459
5	-7454.5	429	7544.5	429
6	-7484.5	429	7514.5	429
7	-7484.5	399	7514.5	399
8	-7514.5	399	7484.5	399
9	-7514.5	429	7484.5	429
10	-7544.5	429	7454.5	429
11	-7544.5	459	7454.5	459
12	-7514.5	459	7484.5	459

12.2 Pad coordinates

No.	Name	X-axis	Y-axis	W	H
1	DUMMY	-7500	-496	35	70
2	VCOM_PASSR	-7445	-496	35	70
3	VCOM_PASSR	-7390	-496	35	70
4	VCOM	-7335	-496	35	70
5	VCOM	-7280	-496	35	70
6	VCOM	-7225	-496	35	70
7	VCOM	-7170	-496	35	70
8	VCOM	-7115	-496	35	70
9	VCOM	-7060	-496	35	70
10	VCOM	-7005	-496	35	70
11	VCOM	-6950	-496	35	70
12	VCOM	-6895	-496	35	70
13	VCOM	-6840	-496	35	70
14	VCOM	-6785	-496	35	70
15	VCOM	-6730	-496	35	70
16	VCOM	-6675	-496	35	70
17	VGL	-6620	-496	35	70
18	VGL	-6565	-496	35	70
19	VGL	-6510	-496	35	70
20	VGL	-6455	-496	35	70
21	VGL	-6400	-496	35	70
22	VGL	-6345	-496	35	70
23	VGL	-6290	-496	35	70
24	VGL	-6235	-496	35	70
25	TP[0]	-6180	-496	35	70
26	TP[1]	-6125	-496	35	70
27	TP[2]	-6070	-496	35	70
28	TP[3]	-6015	-496	35	70
29	TP[4]	-5960	-496	35	70
30	TP[5]	-5905	-496	35	70
31	TP[6]	-5850	-496	35	70
32	TP[7]	-5795	-496	35	70
33	VSHR	-5740	-496	35	70
34	VSHR	-5685	-496	35	70
35	VSHR	-5630	-496	35	70
36	VSHR	-5575	-496	35	70
37	VSHR	-5520	-496	35	70
38	VSHR	-5465	-496	35	70
39	VSHR	-5410	-496	35	70
40	VSHR	-5355	-496	35	70
41	VGH	-5300	-496	35	70
42	VGH	-5245	-496	35	70
43	VGH	-5190	-496	35	70
44	VGH	-5135	-496	35	70
45	VGH	-5080	-496	35	70
46	VGH	-5025	-496	35	70
47	VGH	-4970	-496	35	70
48	VGH	-4915	-496	35	70
49	VSH	-4860	-496	35	70
50	VSH	-4805	-496	35	70
51	VSH	-4750	-496	35	70
52	VSH	-4695	-496	35	70
53	VSH	-4640	-496	35	70
54	VSH	-4585	-496	35	70
55	VSH	-4530	-496	35	70
56	VSH	-4475	-496	35	70
57	DUMMY	-4420	-496	35	70
58	DUMMY	-4365	-496	35	70

No.	Name	X-axis	Y-axis	W	H
59	VOTP	-4310	-496	35	70
60	VOTP	-4255	-496	35	70
61	VOTP	-4200	-496	35	70
62	VOTP	-4145	-496	35	70
63	DUMMY	-4090	-496	35	70
64	DUMMY	-4035	-496	35	70
65	VDD_18V	-3980	-496	35	70
66	VDD_18V	-3925	-496	35	70
67	VDD_18V	-3870	-496	35	70
68	VDD_18V	-3815	-496	35	70
69	VDD_18V	-3760	-496	35	70
70	VDD_18V	-3705	-496	35	70
71	VDD_18V	-3650	-496	35	70
72	VDD_18V	-3595	-496	35	70
73	VDD_18V	-3540	-496	35	70
74	VSSA	-3485	-496	35	70
75	VSSA	-3430	-496	35	70
76	VSSA	-3375	-496	35	70
77	VSSA	-3320	-496	35	70
78	VSSA	-3265	-496	35	70
79	VSSA	-3210	-496	35	70
80	VSSA	-3155	-496	35	70
81	VSSGS	-3100	-496	35	70
82	VSSGS	-3045	-496	35	70
83	VSSGS	-2990	-496	35	70
84	VSSGS	-2935	-496	35	70
85	VSSGS	-2880	-496	35	70
86	VSSGS	-2825	-496	35	70
87	VSSGS	-2770	-496	35	70
88	VSS	-2715	-496	35	70
89	VSS	-2660	-496	35	70
90	VSS	-2605	-496	35	70
91	VSS	-2550	-496	35	70
92	VSS	-2495	-496	35	70
93	VSS	-2440	-496	35	70
94	VSS	-2385	-496	35	70
95	VSSP	-2330	-496	35	70
96	VSSP	-2275	-496	35	70
97	VSSP	-2220	-496	35	70
98	VSSP	-2165	-496	35	70
99	VSSP	-2110	-496	35	70
100	VSSP	-2055	-496	35	70
101	VSSP	-2000	-496	35	70
102	TP[8]	-1945	-496	35	70
103	TP[9]	-1890	-496	35	70
104	TP[10]	-1835	-496	35	70
105	TP[11]	-1780	-496	35	70
106	TP[12]	-1725	-496	35	70
107	VDD	-1670	-496	35	70
108	VDD	-1615	-496	35	70
109	VDD	-1560	-496	35	70
110	VDD	-1505	-496	35	70
111	VDD	-1450	-496	35	70
112	VDD	-1395	-496	35	70
113	VDD	-1340	-496	35	70
114	VDD	-1285	-496	35	70
115	VDDP	-1230	-496	35	70
116	VDDP	-1175	-496	35	70

No.	Name	X-axis	Y-axis	W	X
117	VDDP	-1120	-496	35	70
118	VDDP	-1065	-496	35	70
119	VDDP	-1010	-496	35	70
120	VDDP	-955	-496	35	70
121	VDDP	-900	-496	35	70
122	VDDP	-845	-496	35	70
123	VDDIO	-790	-496	35	70
124	VDDIO	-735	-496	35	70
125	VDDIO	-680	-496	35	70
126	VDDIO	-625	-496	35	70
127	VDDIO	-570	-496	35	70
128	VDDIO	-515	-496	35	70
129	VDDIO	-460	-496	35	70
130	VDDIO	-405	-496	35	70
131	SDA	-350	-496	35	70
132	SDA	-295	-496	35	70
133	VSS	-240	-496	35	70
134	SCL	-185	-496	35	70
135	SCL	-130	-496	35	70
136	VDDIO	-75	-496	35	70
137	CSB	-20	-496	35	70
138	CSB	35	-496	35	70
139	VSS	90	-496	35	70
140	DC	145	-496	35	70
141	DC	200	-496	35	70
142	VDDIO	255	-496	35	70
143	RST_N	310	-496	35	70
144	RST_N	365	-496	35	70
145	VSS	420	-496	35	70
146	BUSY_N	475	-496	35	70
147	BUSY_N	530	-496	35	70
148	VDDIO	585	-496	35	70
149	BS	640	-496	35	70
150	BS	695	-496	35	70
151	VSS	750	-496	35	70
152	TSDA	805	-496	35	70
153	TSDA	860	-496	35	70
154	VDDIO	915	-496	35	70
155	TSCL	970	-496	35	70
156	TSCL	1025	-496	35	70
157	VSS	1080	-496	35	70
158	MS	1135	-496	35	70
159	MS	1190	-496	35	70
160	VDDIO	1245	-496	35	70
161	MS_LR	1300	-496	35	70
162	MS_LR	1355	-496	35	70
163	VSS	1410	-496	35	70
164	DUMMY	1465	-496	35	70
165	DUMMY	1520	-496	35	70
166	DUMMY	1575	-496	35	70
167	DUMMY	1630	-496	35	70
168	DUMMY	1685	-496	35	70
169	DUMMY	1740	-496	35	70
170	DUMMY	1795	-496	35	70
171	VSL	1850	-496	35	70
172	VSL	1905	-496	35	70
173	VSL	1960	-496	35	70
174	VSL	2015	-496	35	70
175	VSL	2070	-496	35	70
176	VSL	2125	-496	35	70

No.	Name	X-axis	Y-axis	W	X
177	VSL	2180	-496	35	70
178	VSL	2235	-496	35	70
179	VSL	2290	-496	35	70
180	VSL	2345	-496	35	70
181	VSL	2400	-496	35	70
182	DUMMY	2455	-496	35	70
183	DUMMY	2510	-496	35	70
184	DUMMY	2565	-496	35	70
185	DUMMY	2620	-496	35	70
186	VSLR	2675	-496	35	70
187	VSLR	2730	-496	35	70
188	VSLR	2785	-496	35	70
189	VSLR	2840	-496	35	70
190	VSLR	2895	-496	35	70
191	VSLR	2950	-496	35	70
192	VSLR	3005	-496	35	70
193	VSLR	3060	-496	35	70
194	VSLR	3115	-496	35	70
195	VSLR	3170	-496	35	70
196	VSLR	3225	-496	35	70
197	DUMMY	3280	-496	35	70
198	DUMMY	3335	-496	35	70
199	DUMMY	3390	-496	35	70
200	FB	3445	-496	35	70
201	FB	3500	-496	35	70
202	RESE	3555	-496	35	70
203	RESE	3610	-496	35	70
204	GDR	3665	-496	35	70
205	GDR	3720	-496	35	70
206	GDR	3775	-496	35	70
207	GDR	3830	-496	35	70
208	GDR	3885	-496	35	70
209	GDR	3940	-496	35	70
210	DUMMY	3995	-496	35	70
211	DUMMY	4050	-496	35	70
212	DUMMY	4105	-496	35	70
213	TP[13]	4160	-496	35	70
214	TP[14]	4215	-496	35	70
215	TP[15]	4270	-496	35	70
216	TP[16]	4325	-496	35	70
217	TP[17]	4380	-496	35	70
218	TP[18]	4435	-496	35	70
219	TP[19]	4490	-496	35	70
220	TP[20]	4545	-496	35	70
221	TP[21]	4600	-496	35	70
222	TP[22]	4655	-496	35	70
223	TP[23]	4710	-496	35	70
224	TP[24]	4765	-496	35	70
225	TP[25]	4820	-496	35	70
226	TP[26]	4875	-496	35	70
227	TP[27]	4930	-496	35	70
228	TP[28]	4985	-496	35	70
229	TP[29]	5040	-496	35	70
230	TP[30]	5095	-496	35	70
231	TP[31]	5150	-496	35	70
232	TP[32]	5205	-496	35	70
233	TP[33]	5260	-496	35	70
234	TP[34]	5315	-496	35	70
235	TP[35]	5370	-496	35	70
236	TP[36]	5425	-496	35	70

No.	Name	X-axis	Y-axis	W	X
237	TP[37]	5480	-496	35	70
238	TP[38]	5535	-496	35	70
239	TP[39]	5590	-496	35	70
240	TP[40]	5645	-496	35	70
241	TP[41]	5700	-496	35	70
242	TP[42]	5755	-496	35	70
243	TP[43]	5810	-496	35	70
244	TP[44]	5865	-496	35	70
245	TP[45]	5920	-496	35	70
246	TP[46]	5975	-496	35	70
247	TP[47]	6030	-496	35	70
248	TP[48]	6085	-496	35	70
249	TP[49]	6140	-496	35	70
250	TP[50]	6195	-496	35	70
251	TP[51]	6250	-496	35	70
252	TP[52]	6305	-496	35	70
253	TP[53]	6360	-496	35	70
254	TP[54]	6415	-496	35	70
255	TP[55]	6470	-496	35	70
256	TP[56]	6525	-496	35	70
257	TP[57]	6580	-496	35	70
258	TP[58]	6635	-496	35	70
259	TP[59]	6690	-496	35	70
260	TP[60]	6745	-496	35	70
261	TP[61]	6800	-496	35	70
262	TP[62]	6855	-496	35	70
263	TP[63]	6910	-496	35	70
264	TP[64]	6965	-496	35	70
265	TP[65]	7020	-496	35	70
266	TP[66]	7075	-496	35	70
267	DUMMY	7130	-496	35	70
268	DUMMY	7185	-496	35	70
269	VCOM_PASSL	7240	-496	35	70
270	VCOM_PASSL	7295	-496	35	70
271	DUMMY	7350	-496	35	70
272	DUMMY	7405	-496	35	70
273	DUMMY	7460	-496	35	70
274	DUMMY	7515	-496	35	70
275	DUMMY	7683	-407.5	70	35
276	DUMMY	7683	-327.5	70	35
277	DUMMY	7683	-247.5	70	35
278	SYNCS_L	7683	-167.5	70	35
279	SYNCM_L	7683	-87.5	70	35
280	VSYCM_L	7683	-7.5	70	35
281	HSYNC_L	7683	72.5	70	35
282	DT_L	7683	152.5	70	35
283	EN_L	7683	232.5	70	35
284	CLK_L	7683	312.5	70	35
285	DUMMY	7683	392.5	70	35
286	DUMMY	7318	428.5	22	55
287	DUMMY	7296	503.5	22	55
288	DUMMY	7274	428.5	22	55
289	DUMMY	7252	503.5	22	55
290	DUMMY	7230	428.5	22	55
291	DUMMY	7208	503.5	22	55
292	VCOM_PASSL	7186	428.5	22	55
293	VCOM_PASSL	7164	503.5	22	55
294	VCOM_PASSL	7142	428.5	22	55
295	VCOM_PASSL	7120	503.5	22	55
296	DUMMY	7098	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
297	DUMMY	7076	503.5	22	55
298	DUMMY	7054	428.5	22	55
299	DUMMY	7032	503.5	22	55
300	G[0]	7010	428.5	22	55
301	G[2]	6988	503.5	22	55
302	G[4]	6966	428.5	22	55
303	G[6]	6944	503.5	22	55
304	G[8]	6922	428.5	22	55
305	G[10]	6900	503.5	22	55
306	G[12]	6878	428.5	22	55
307	G[14]	6856	503.5	22	55
308	G[16]	6834	428.5	22	55
309	G[18]	6812	503.5	22	55
310	G[20]	6790	428.5	22	55
311	G[22]	6768	503.5	22	55
312	G[24]	6746	428.5	22	55
313	G[26]	6724	503.5	22	55
314	G[28]	6702	428.5	22	55
315	G[30]	6680	503.5	22	55
316	G[32]	6658	428.5	22	55
317	G[34]	6636	503.5	22	55
318	G[36]	6614	428.5	22	55
319	G[38]	6592	503.5	22	55
320	G[40]	6570	428.5	22	55
321	G[42]	6548	503.5	22	55
322	G[44]	6526	428.5	22	55
323	G[46]	6504	503.5	22	55
324	G[48]	6482	428.5	22	55
325	G[50]	6460	503.5	22	55
326	G[52]	6438	428.5	22	55
327	G[54]	6416	503.5	22	55
328	G[56]	6394	428.5	22	55
329	G[58]	6372	503.5	22	55
330	G[60]	6350	428.5	22	55
331	G[62]	6328	503.5	22	55
332	G[64]	6306	428.5	22	55
333	G[66]	6284	503.5	22	55
334	G[68]	6262	428.5	22	55
335	G[70]	6240	503.5	22	55
336	G[72]	6218	428.5	22	55
337	G[74]	6196	503.5	22	55
338	G[76]	6174	428.5	22	55
339	G[78]	6152	503.5	22	55
340	G[80]	6130	428.5	22	55
341	G[82]	6108	503.5	22	55
342	G[84]	6086	428.5	22	55
343	G[86]	6064	503.5	22	55
344	G[88]	6042	428.5	22	55
345	G[90]	6020	503.5	22	55
346	G[92]	5998	428.5	22	55
347	G[94]	5976	503.5	22	55
348	G[96]	5954	428.5	22	55
349	G[98]	5932	503.5	22	55
350	G[100]	5910	428.5	22	55
351	G[102]	5888	503.5	22	55
352	G[104]	5866	428.5	22	55
353	G[106]	5844	503.5	22	55
354	G[108]	5822	428.5	22	55
355	G[110]	5800	503.5	22	55
356	G[112]	5778	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
357	G[114]	5756	503.5	22	55
358	G[116]	5734	428.5	22	55
359	G[118]	5712	503.5	22	55
360	G[120]	5690	428.5	22	55
361	G[122]	5668	503.5	22	55
362	G[124]	5646	428.5	22	55
363	G[126]	5624	503.5	22	55
364	G[128]	5602	428.5	22	55
365	G[130]	5580	503.5	22	55
366	G[132]	5558	428.5	22	55
367	G[134]	5536	503.5	22	55
368	G[136]	5514	428.5	22	55
369	G[138]	5492	503.5	22	55
370	G[140]	5470	428.5	22	55
371	G[142]	5448	503.5	22	55
372	G[144]	5426	428.5	22	55
373	G[146]	5404	503.5	22	55
374	G[148]	5382	428.5	22	55
375	G[150]	5360	503.5	22	55
376	G[152]	5338	428.5	22	55
377	G[154]	5316	503.5	22	55
378	G[156]	5294	428.5	22	55
379	G[158]	5272	503.5	22	55
380	G[160]	5250	428.5	22	55
381	G[162]	5228	503.5	22	55
382	G[164]	5206	428.5	22	55
383	G[166]	5184	503.5	22	55
384	G[168]	5162	428.5	22	55
385	G[170]	5140	503.5	22	55
386	G[172]	5118	428.5	22	55
387	G[174]	5096	503.5	22	55
388	G[176]	5074	428.5	22	55
389	G[178]	5052	503.5	22	55
390	G[180]	5030	428.5	22	55
391	G[182]	5008	503.5	22	55
392	G[184]	4986	428.5	22	55
393	G[186]	4964	503.5	22	55
394	G[188]	4942	428.5	22	55
395	G[190]	4920	503.5	22	55
396	G[192]	4898	428.5	22	55
397	G[194]	4876	503.5	22	55
398	G[196]	4854	428.5	22	55
399	G[198]	4832	503.5	22	55
400	G[200]	4810	428.5	22	55
401	G[202]	4788	503.5	22	55
402	G[204]	4766	428.5	22	55
403	G[206]	4744	503.5	22	55
404	G[208]	4722	428.5	22	55
405	G[210]	4700	503.5	22	55
406	G[212]	4678	428.5	22	55
407	G[214]	4656	503.5	22	55
408	G[216]	4634	428.5	22	55
409	G[218]	4612	503.5	22	55
410	G[220]	4590	428.5	22	55
411	G[222]	4568	503.5	22	55
412	G[224]	4546	428.5	22	55
413	G[226]	4524	503.5	22	55
414	G[228]	4502	428.5	22	55
415	G[230]	4480	503.5	22	55
416	G[232]	4458	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
417	G[234]	4436	503.5	22	55
418	G[236]	4414	428.5	22	55
419	G[238]	4392	503.5	22	55
420	G[240]	4370	428.5	22	55
421	G[242]	4348	503.5	22	55
422	G[244]	4326	428.5	22	55
423	G[246]	4304	503.5	22	55
424	G[248]	4282	428.5	22	55
425	G[250]	4260	503.5	22	55
426	G[252]	4238	428.5	22	55
427	G[254]	4216	503.5	22	55
428	G[256]	4194	428.5	22	55
429	G[258]	4172	503.5	22	55
430	G[260]	4150	428.5	22	55
431	G[262]	4128	503.5	22	55
432	G[264]	4106	428.5	22	55
433	G[266]	4084	503.5	22	55
434	G[268]	4062	428.5	22	55
435	G[270]	4040	503.5	22	55
436	G[272]	4018	428.5	22	55
437	G[274]	3996	503.5	22	55
438	G[276]	3974	428.5	22	55
439	G[278]	3952	503.5	22	55
440	G[280]	3930	428.5	22	55
441	G[282]	3908	503.5	22	55
442	G[284]	3886	428.5	22	55
443	G[286]	3864	503.5	22	55
444	G[288]	3842	428.5	22	55
445	G[290]	3820	503.5	22	55
446	G[292]	3798	428.5	22	55
447	G[294]	3776	503.5	22	55
448	G[296]	3754	428.5	22	55
449	G[298]	3732	503.5	22	55
450	DUMMY	3710	428.5	22	55
451	DUMMY	3688	503.5	22	55
452	DUMMY	3665	428.5	22	55
453	DUMMY	3643	503.5	22	55
454	DUMMY	3621	428.5	22	55
455	DUMMY	3599	503.5	22	55
456	DUMMY	3577	428.5	22	55
457	DUMMY	3555	503.5	22	55
458	DUMMY	3533	428.5	22	55
459	DUMMY	3511	503.5	22	55
460	DUMMY	3488	428.5	22	55
461	DUMMY	3466	503.5	22	55
462	DUMMY	3444	428.5	22	55
463	DUMMY	3422	503.5	22	55
464	DUMMY	3400	428.5	22	55
465	DUMMY	3378	503.5	22	55
466	BDR_L	3356	428.5	22	55
467	S[0]	3334	503.5	22	55
468	S[1]	3312	428.5	22	55
469	S[2]	3290	503.5	22	55
470	S[3]	3268	428.5	22	55
471	S[4]	3246	503.5	22	55
472	S[5]	3224	428.5	22	55
473	S[6]	3202	503.5	22	55
474	S[7]	3180	428.5	22	55
475	S[8]	3158	503.5	22	55
476	S[9]	3136	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
477	S[10]	3114	503.5	22	55
478	S[11]	3092	428.5	22	55
479	S[12]	3070	503.5	22	55
480	S[13]	3048	428.5	22	55
481	S[14]	3026	503.5	22	55
482	S[15]	3004	428.5	22	55
483	S[16]	2982	503.5	22	55
484	S[17]	2960	428.5	22	55
485	S[18]	2938	503.5	22	55
486	S[19]	2916	428.5	22	55
487	S[20]	2894	503.5	22	55
488	S[21]	2872	428.5	22	55
489	S[22]	2850	503.5	22	55
490	S[23]	2828	428.5	22	55
491	S[24]	2806	503.5	22	55
492	S[25]	2784	428.5	22	55
493	S[26]	2762	503.5	22	55
494	S[27]	2740	428.5	22	55
495	S[28]	2718	503.5	22	55
496	S[29]	2696	428.5	22	55
497	S[30]	2674	503.5	22	55
498	S[31]	2652	428.5	22	55
499	S[32]	2630	503.5	22	55
500	S[33]	2608	428.5	22	55
501	S[34]	2586	503.5	22	55
502	S[35]	2564	428.5	22	55
503	S[36]	2542	503.5	22	55
504	S[37]	2520	428.5	22	55
505	S[38]	2498	503.5	22	55
506	S[39]	2476	428.5	22	55
507	S[40]	2454	503.5	22	55
508	S[41]	2432	428.5	22	55
509	S[42]	2410	503.5	22	55
510	S[43]	2388	428.5	22	55
511	S[44]	2366	503.5	22	55
512	S[45]	2344	428.5	22	55
513	S[46]	2322	503.5	22	55
514	S[47]	2300	428.5	22	55
515	S[48]	2278	503.5	22	55
516	S[49]	2256	428.5	22	55
517	S[50]	2234	503.5	22	55
518	S[51]	2212	428.5	22	55
519	S[52]	2190	503.5	22	55
520	S[53]	2168	428.5	22	55
521	S[54]	2146	503.5	22	55
522	S[55]	2124	428.5	22	55
523	S[56]	2102	503.5	22	55
524	S[57]	2080	428.5	22	55
525	S[58]	2058	503.5	22	55
526	S[59]	2036	428.5	22	55
527	S[60]	2014	503.5	22	55
528	S[61]	1992	428.5	22	55
529	S[62]	1970	503.5	22	55
530	S[63]	1948	428.5	22	55
531	S[64]	1926	503.5	22	55
532	S[65]	1904	428.5	22	55
533	S[66]	1882	503.5	22	55
534	S[67]	1860	428.5	22	55
535	S[68]	1838	503.5	22	55
536	S[69]	1816	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
537	S[70]	1794	503.5	22	55
538	S[71]	1772	428.5	22	55
539	S[72]	1750	503.5	22	55
540	S[73]	1728	428.5	22	55
541	S[74]	1706	503.5	22	55
542	S[75]	1684	428.5	22	55
543	S[76]	1662	503.5	22	55
544	S[77]	1640	428.5	22	55
545	S[78]	1618	503.5	22	55
546	S[79]	1596	428.5	22	55
547	S[80]	1574	503.5	22	55
548	S[81]	1552	428.5	22	55
549	S[82]	1530	503.5	22	55
550	S[83]	1508	428.5	22	55
551	S[84]	1486	503.5	22	55
552	S[85]	1464	428.5	22	55
553	S[86]	1442	503.5	22	55
554	S[87]	1420	428.5	22	55
555	S[88]	1398	503.5	22	55
556	S[89]	1376	428.5	22	55
557	S[90]	1354	503.5	22	55
558	S[91]	1332	428.5	22	55
559	S[92]	1310	503.5	22	55
560	S[93]	1288	428.5	22	55
561	S[94]	1266	503.5	22	55
562	S[95]	1244	428.5	22	55
563	S[96]	1222	503.5	22	55
564	S[97]	1200	428.5	22	55
565	S[98]	1178	503.5	22	55
566	S[99]	1156	428.5	22	55
567	S[100]	1134	503.5	22	55
568	S[101]	1112	428.5	22	55
569	S[102]	1090	503.5	22	55
570	S[103]	1068	428.5	22	55
571	S[104]	1046	503.5	22	55
572	S[105]	1024	428.5	22	55
573	S[106]	1002	503.5	22	55
574	S[107]	980	428.5	22	55
575	S[108]	958	503.5	22	55
576	S[109]	936	428.5	22	55
577	S[110]	914	503.5	22	55
578	S[111]	892	428.5	22	55
579	S[112]	870	503.5	22	55
580	S[113]	848	428.5	22	55
581	S[114]	826	503.5	22	55
582	S[115]	804	428.5	22	55
583	S[116]	782	503.5	22	55
584	S[117]	760	428.5	22	55
585	S[118]	738	503.5	22	55
586	S[119]	716	428.5	22	55
587	S[120]	694	503.5	22	55
588	S[121]	672	428.5	22	55
589	S[122]	650	503.5	22	55
590	S[123]	628	428.5	22	55
591	S[124]	606	503.5	22	55
592	S[125]	584	428.5	22	55
593	S[126]	562	503.5	22	55
594	S[127]	540	428.5	22	55
595	S[128]	518	503.5	22	55
596	S[129]	496	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
597	S[130]	474	503.5	22	55
598	S[131]	452	428.5	22	55
599	S[132]	430	503.5	22	55
600	S[133]	408	428.5	22	55
601	S[134]	386	503.5	22	55
602	S[135]	364	428.5	22	55
603	S[136]	342	503.5	22	55
604	S[137]	320	428.5	22	55
605	S[138]	298	503.5	22	55
606	S[139]	276	428.5	22	55
607	S[140]	254	503.5	22	55
608	S[141]	232	428.5	22	55
609	S[142]	210	503.5	22	55
610	S[143]	188	428.5	22	55
611	S[144]	166	503.5	22	55
612	S[145]	144	428.5	22	55
613	S[146]	122	503.5	22	55
614	S[147]	100	428.5	22	55
615	S[148]	78	503.5	22	55
616	S[149]	56	428.5	22	55
617	S[150]	34	503.5	22	55
618	S[151]	12	428.5	22	55
619	S[152]	-10	503.5	22	55
620	S[153]	-32	428.5	22	55
621	S[154]	-54	503.5	22	55
622	S[155]	-76	428.5	22	55
623	S[156]	-98	503.5	22	55
624	S[157]	-120	428.5	22	55
625	S[158]	-142	503.5	22	55
626	S[159]	-164	428.5	22	55
627	S[160]	-186	503.5	22	55
628	S[161]	-208	428.5	22	55
629	S[162]	-230	503.5	22	55
630	S[163]	-252	428.5	22	55
631	S[164]	-274	503.5	22	55
632	S[165]	-296	428.5	22	55
633	S[166]	-318	503.5	22	55
634	S[167]	-340	428.5	22	55
635	S[168]	-362	503.5	22	55
636	S[169]	-384	428.5	22	55
637	S[170]	-406	503.5	22	55
638	S[171]	-428	428.5	22	55
639	S[172]	-450	503.5	22	55
640	S[173]	-472	428.5	22	55
641	S[174]	-494	503.5	22	55
642	S[175]	-516	428.5	22	55
643	S[176]	-538	503.5	22	55
644	S[177]	-560	428.5	22	55
645	S[178]	-582	503.5	22	55
646	S[179]	-604	428.5	22	55
647	S[180]	-626	503.5	22	55
648	S[181]	-648	428.5	22	55
649	S[182]	-670	503.5	22	55
650	S[183]	-692	428.5	22	55
651	S[184]	-714	503.5	22	55
652	S[185]	-736	428.5	22	55
653	S[186]	-758	503.5	22	55
654	S[187]	-780	428.5	22	55
655	S[188]	-802	503.5	22	55
656	S[189]	-824	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
657	S[190]	-846	503.5	22	55
658	S[191]	-868	428.5	22	55
659	S[192]	-890	503.5	22	55
660	S[193]	-912	428.5	22	55
661	S[194]	-934	503.5	22	55
662	S[195]	-956	428.5	22	55
663	S[196]	-978	503.5	22	55
664	S[197]	-1000	428.5	22	55
665	S[198]	-1022	503.5	22	55
666	S[199]	-1044	428.5	22	55
667	S[200]	-1066	503.5	22	55
668	S[201]	-1088	428.5	22	55
669	S[202]	-1110	503.5	22	55
670	S[203]	-1132	428.5	22	55
671	S[204]	-1154	503.5	22	55
672	S[205]	-1176	428.5	22	55
673	S[206]	-1198	503.5	22	55
674	S[207]	-1220	428.5	22	55
675	S[208]	-1242	503.5	22	55
676	S[209]	-1264	428.5	22	55
677	S[210]	-1286	503.5	22	55
678	S[211]	-1308	428.5	22	55
679	S[212]	-1330	503.5	22	55
680	S[213]	-1352	428.5	22	55
681	S[214]	-1374	503.5	22	55
682	S[215]	-1396	428.5	22	55
683	S[216]	-1418	503.5	22	55
684	S[217]	-1440	428.5	22	55
685	S[218]	-1462	503.5	22	55
686	S[219]	-1484	428.5	22	55
687	S[220]	-1506	503.5	22	55
688	S[221]	-1528	428.5	22	55
689	S[222]	-1550	503.5	22	55
690	S[223]	-1572	428.5	22	55
691	S[224]	-1594	503.5	22	55
692	S[225]	-1616	428.5	22	55
693	S[226]	-1638	503.5	22	55
694	S[227]	-1660	428.5	22	55
695	S[228]	-1682	503.5	22	55
696	S[229]	-1704	428.5	22	55
697	S[230]	-1726	503.5	22	55
698	S[231]	-1748	428.5	22	55
699	S[232]	-1770	503.5	22	55
700	S[233]	-1792	428.5	22	55
701	S[234]	-1814	503.5	22	55
702	S[235]	-1836	428.5	22	55
703	S[236]	-1858	503.5	22	55
704	S[237]	-1880	428.5	22	55
705	S[238]	-1902	503.5	22	55
706	S[239]	-1924	428.5	22	55
707	S[240]	-1946	503.5	22	55
708	S[241]	-1968	428.5	22	55
709	S[242]	-1990	503.5	22	55
710	S[243]	-2012	428.5	22	55
711	S[244]	-2034	503.5	22	55
712	S[245]	-2056	428.5	22	55
713	S[246]	-2078	503.5	22	55
714	S[247]	-2100	428.5	22	55
715	S[248]	-2122	503.5	22	55
716	S[249]	-2144	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
717	S[250]	-2166	503.5	22	55
718	S[251]	-2188	428.5	22	55
719	S[252]	-2210	503.5	22	55
720	S[253]	-2232	428.5	22	55
721	S[254]	-2254	503.5	22	55
722	S[255]	-2276	428.5	22	55
723	S[256]	-2298	503.5	22	55
724	S[257]	-2320	428.5	22	55
725	S[258]	-2342	503.5	22	55
726	S[259]	-2364	428.5	22	55
727	S[260]	-2386	503.5	22	55
728	S[261]	-2408	428.5	22	55
729	S[262]	-2430	503.5	22	55
730	S[263]	-2452	428.5	22	55
731	S[264]	-2474	503.5	22	55
732	S[265]	-2496	428.5	22	55
733	S[266]	-2518	503.5	22	55
734	S[267]	-2540	428.5	22	55
735	S[268]	-2562	503.5	22	55
736	S[269]	-2584	428.5	22	55
737	S[270]	-2606	503.5	22	55
738	S[271]	-2628	428.5	22	55
739	S[272]	-2650	503.5	22	55
740	S[273]	-2672	428.5	22	55
741	S[274]	-2694	503.5	22	55
742	S[275]	-2716	428.5	22	55
743	S[276]	-2738	503.5	22	55
744	S[277]	-2760	428.5	22	55
745	S[278]	-2782	503.5	22	55
746	S[279]	-2804	428.5	22	55
747	S[280]	-2826	503.5	22	55
748	S[281]	-2848	428.5	22	55
749	S[282]	-2870	503.5	22	55
750	S[283]	-2892	428.5	22	55
751	S[284]	-2914	503.5	22	55
752	S[285]	-2936	428.5	22	55
753	S[286]	-2958	503.5	22	55
754	S[287]	-2980	428.5	22	55
755	S[288]	-3002	503.5	22	55
756	S[289]	-3024	428.5	22	55
757	S[290]	-3046	503.5	22	55
758	S[291]	-3068	428.5	22	55
759	S[292]	-3090	503.5	22	55
760	S[293]	-3112	428.5	22	55
761	S[294]	-3134	503.5	22	55
762	S[295]	-3156	428.5	22	55
763	S[296]	-3178	503.5	22	55
764	S[297]	-3200	428.5	22	55
765	S[298]	-3222	503.5	22	55
766	S[299]	-3244	428.5	22	55
767	S[300]	-3266	503.5	22	55
768	S[301]	-3288	428.5	22	55
769	S[302]	-3310	503.5	22	55
770	S[303]	-3332	428.5	22	55
771	S[304]	-3354	503.5	22	55
772	S[305]	-3376	428.5	22	55
773	S[306]	-3398	503.5	22	55
774	S[307]	-3420	428.5	22	55
775	S[308]	-3442	503.5	22	55
776	S[309]	-3464	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
777	S[310]	-3486	503.5	22	55
778	S[311]	-3508	428.5	22	55
779	S[312]	-3530	503.5	22	55
780	S[313]	-3552	428.5	22	55
781	S[314]	-3574	503.5	22	55
782	S[315]	-3596	428.5	22	55
783	S[316]	-3618	503.5	22	55
784	S[317]	-3640	428.5	22	55
785	S[318]	-3662	503.5	22	55
786	S[319]	-3684	428.5	22	55
787	BDR_R	-3706	503.5	22	55
788	DUMMY	-3728	428.5	22	55
789	DUMMY	-3750	503.5	22	55
790	DUMMY	-3772	428.5	22	55
791	DUMMY	-3794	503.5	22	55
792	DUMMY	-3816	428.5	22	55
793	DUMMY	-3838	503.5	22	55
794	DUMMY	-3860	428.5	22	55
795	DUMMY	-3882	503.5	22	55
796	DUMMY	-3904	428.5	22	55
797	G[299]	-3926	503.5	22	55
798	G[297]	-3948	428.5	22	55
799	G[295]	-3970	503.5	22	55
800	G[293]	-3992	428.5	22	55
801	G[291]	-4014	503.5	22	55
802	G[289]	-4036	428.5	22	55
803	G[287]	-4058	503.5	22	55
804	G[285]	-4080	428.5	22	55
805	G[283]	-4102	503.5	22	55
806	G[281]	-4124	428.5	22	55
807	G[279]	-4146	503.5	22	55
808	G[277]	-4168	428.5	22	55
809	G[275]	-4190	503.5	22	55
810	G[273]	-4212	428.5	22	55
811	G[271]	-4234	503.5	22	55
812	G[269]	-4256	428.5	22	55
813	G[267]	-4278	503.5	22	55
814	G[265]	-4300	428.5	22	55
815	G[263]	-4322	503.5	22	55
816	G[261]	-4344	428.5	22	55
817	G[259]	-4366	503.5	22	55
818	G[257]	-4388	428.5	22	55
819	G[255]	-4410	503.5	22	55
820	G[253]	-4432	428.5	22	55
821	G[251]	-4454	503.5	22	55
822	G[249]	-4476	428.5	22	55
823	G[247]	-4498	503.5	22	55
824	G[245]	-4520	428.5	22	55
825	G[243]	-4542	503.5	22	55
826	G[241]	-4564	428.5	22	55
827	G[239]	-4586	503.5	22	55
828	G[237]	-4608	428.5	22	55
829	G[235]	-4630	503.5	22	55
830	G[233]	-4652	428.5	22	55
831	G[231]	-4674	503.5	22	55
832	G[229]	-4696	428.5	22	55
833	G[227]	-4718	503.5	22	55
834	G[225]	-4740	428.5	22	55
835	G[223]	-4762	503.5	22	55
836	G[221]	-4784	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
837	G[219]	-4806	503.5	22	55
838	G[217]	-4828	428.5	22	55
839	G[215]	-4850	503.5	22	55
840	G[213]	-4872	428.5	22	55
841	G[211]	-4894	503.5	22	55
842	G[209]	-4916	428.5	22	55
843	G[207]	-4938	503.5	22	55
844	G[205]	-4960	428.5	22	55
845	G[203]	-4982	503.5	22	55
846	G[201]	-5004	428.5	22	55
847	G[199]	-5026	503.5	22	55
848	G[197]	-5048	428.5	22	55
849	G[195]	-5070	503.5	22	55
850	G[193]	-5092	428.5	22	55
851	G[191]	-5114	503.5	22	55
852	G[189]	-5136	428.5	22	55
853	G[187]	-5158	503.5	22	55
854	G[185]	-5180	428.5	22	55
855	G[183]	-5202	503.5	22	55
856	G[181]	-5224	428.5	22	55
857	G[179]	-5246	503.5	22	55
858	G[177]	-5268	428.5	22	55
859	G[175]	-5290	503.5	22	55
860	G[173]	-5312	428.5	22	55
861	G[171]	-5334	503.5	22	55
862	G[169]	-5356	428.5	22	55
863	G[167]	-5378	503.5	22	55
864	G[165]	-5400	428.5	22	55
865	G[163]	-5422	503.5	22	55
866	G[161]	-5444	428.5	22	55
867	G[159]	-5466	503.5	22	55
868	G[157]	-5488	428.5	22	55
869	G[155]	-5510	503.5	22	55
870	G[153]	-5532	428.5	22	55
871	G[151]	-5554	503.5	22	55
872	G[149]	-5576	428.5	22	55
873	G[147]	-5598	503.5	22	55
874	G[145]	-5620	428.5	22	55
875	G[143]	-5642	503.5	22	55
876	G[141]	-5664	428.5	22	55
877	G[139]	-5686	503.5	22	55
878	G[137]	-5708	428.5	22	55
879	G[135]	-5730	503.5	22	55
880	G[133]	-5752	428.5	22	55
881	G[131]	-5774	503.5	22	55
882	G[129]	-5796	428.5	22	55
883	G[127]	-5818	503.5	22	55
884	G[125]	-5840	428.5	22	55
885	G[123]	-5862	503.5	22	55
886	G[121]	-5884	428.5	22	55
887	G[119]	-5906	503.5	22	55
888	G[117]	-5928	428.5	22	55
889	G[115]	-5950	503.5	22	55
890	G[113]	-5972	428.5	22	55
891	G[111]	-5994	503.5	22	55
892	G[109]	-6016	428.5	22	55
893	G[107]	-6038	503.5	22	55
894	G[105]	-6060	428.5	22	55
895	G[103]	-6082	503.5	22	55
896	G[101]	-6104	428.5	22	55

No.	Name	X-axis	Y-axis	W	X
897	G[99]	-6126	503.5	22	55
898	G[97]	-6148	428.5	22	55
899	G[95]	-6170	503.5	22	55
900	G[93]	-6192	428.5	22	55
901	G[91]	-6214	503.5	22	55
902	G[89]	-6236	428.5	22	55
903	G[87]	-6258	503.5	22	55
904	G[85]	-6280	428.5	22	55
905	G[83]	-6302	503.5	22	55
906	G[81]	-6324	428.5	22	55
907	G[79]	-6346	503.5	22	55
908	G[77]	-6368	428.5	22	55
909	G[75]	-6390	503.5	22	55
910	G[73]	-6412	428.5	22	55
911	G[71]	-6434	503.5	22	55
912	G[69]	-6456	428.5	22	55
913	G[67]	-6478	503.5	22	55
914	G[65]	-6500	428.5	22	55
915	G[63]	-6522	503.5	22	55
916	G[61]	-6544	428.5	22	55
917	G[59]	-6566	503.5	22	55
918	G[57]	-6588	428.5	22	55
919	G[55]	-6610	503.5	22	55
920	G[53]	-6632	428.5	22	55
921	G[51]	-6654	503.5	22	55
922	G[49]	-6676	428.5	22	55
923	G[47]	-6698	503.5	22	55
924	G[45]	-6720	428.5	22	55
925	G[43]	-6742	503.5	22	55
926	G[41]	-6764	428.5	22	55
927	G[39]	-6786	503.5	22	55
928	G[37]	-6808	428.5	22	55
929	G[35]	-6830	503.5	22	55
930	G[33]	-6852	428.5	22	55
931	G[31]	-6874	503.5	22	55
932	G[29]	-6896	428.5	22	55
933	G[27]	-6918	503.5	22	55
934	G[25]	-6940	428.5	22	55
935	G[23]	-6962	503.5	22	55
936	G[21]	-6984	428.5	22	55
937	G[19]	-7006	503.5	22	55
938	G[17]	-7028	428.5	22	55
939	G[15]	-7050	503.5	22	55
940	G[13]	-7072	428.5	22	55
941	G[11]	-7094	503.5	22	55
942	G[9]	-7116	428.5	22	55
943	G[7]	-7138	503.5	22	55
944	G[5]	-7160	428.5	22	55
945	G[3]	-7182	503.5	22	55
946	G[1]	-7204	428.5	22	55
947	DUMMY	-7226	503.5	22	55
948	DUMMY	-7248	428.5	22	55
949	VCOM_PASSR	-7270	503.5	22	55
950	VCOM_PASSR	-7292	428.5	22	55
951	VCOM_PASSR	-7314	503.5	22	55
952	VCOM_PASSR	-7336	428.5	22	55
953	DUMMY	-7358	503.5	22	55
954	DUMMY	-7380	428.5	22	55
955	DUMMY	-7683	392.5	70	35
956	CLK_R	-7683	312.5	70	35

No.	Name	X-axis	Y-axis	W	X
957	EN_R	-7683	232.5	70	35
958	DT_R	-7683	152.5	70	35
959	HSYNC_R	-7683	72.5	70	35
960	VSYNC_R	-7683	-7.5	70	35
961	SYNCM_R	-7683	-87.5	70	35
962	SYNCS_R	-7683	-167.5	70	35
963	DUMMY	-7683	-247.5	70	35
964	DUMMY	-7683	-327.5	70	35
965	DUMMY	-7683	-407.5	70	35

13. REVISION HISTORY

Revision	Content	Page	Date
1.0	1.new issue AB to AC version update: Add OCP circuit statement	69	2017/11/23