GC9203

a-Si TFT LCD Single Chip Driver

176RGBx220 Resolution and 262K color

Specification

Preliminary Version 1.00
2016.01.21

GalaxyCore Incorporation

Table of Content

1. Introduction

The GC9203 is a 262,144-color single-chip SoC driver for a-TFT liquid crystal display with resolution of 176RGBx220 dots, comprising a 528-channel source driver, a 220-channel gate driver, 87,120 bytes GRAM for graphic data of 176RGBx220 dots, and power supply circuit.

The GC9203 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

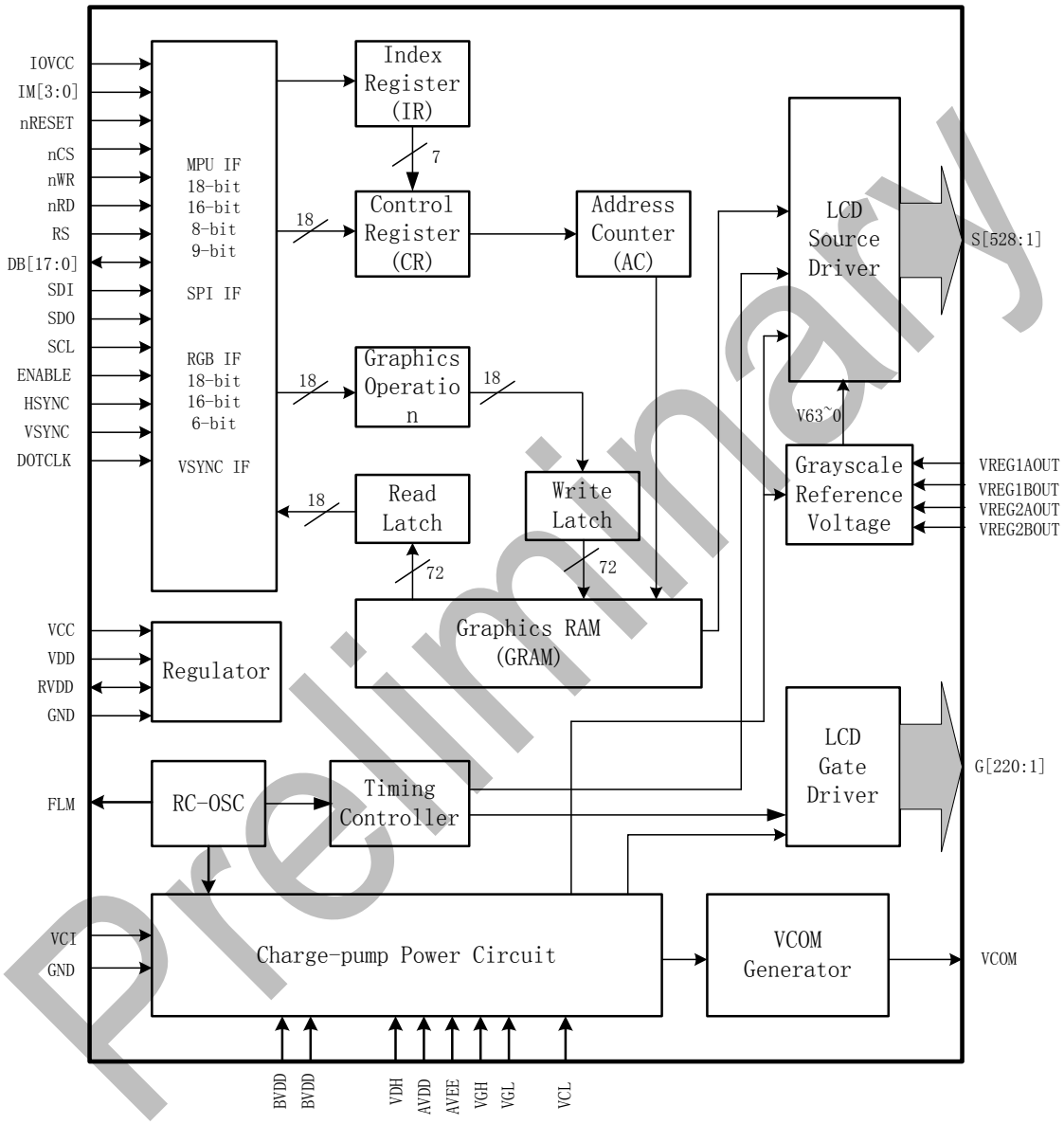
The GC9203 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. GC9203 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9203 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- a-TFT LCD driver with on-chip full display RAM: 87,120 bytes
- Display resolution: [176xRGB](H) x 220(V)
- LCD Driver Output Circuits
  - 528 source outputs
  - 220 gate outputs
  - Common electrode output (VCOM)
- Driving Algorithm Support
  - 1-dot/2-dot/4-dot/8-dot Inversion
  - Column Inversion
- Display Colors (Color Mode)
  - Full Color: 262K, RGB=(666) max., Idle Mode Off
  - Color Reduce: 8-color, RGB=(111), Idle Mode On
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits bus width with i80 system interface
  - 8-bits, 9-bits, 16-bits, 18-bits bus width with m68 system interface
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 8-bits, 9-bits, 24bits Serial Peripheral Interface (SPI)
  - 2 data lane SPI
- Abundant functions for color display control
  - γ -correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function
- Power saving function:
  - 8-color mode
  - Standby mode
- Partial drive function, enabling partially driving an LCD panel at positions specified by user
- Window address function to specify a rectangular area for internal GRAM access
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V (interface I/O)
  - Analog Voltage (VDD to AGND): 2.5V ~ 3.3V
- On-Chip Power System
  - Source Voltage (VREG1A, VREG2A,VREG1B/ VREG2B): +6.0V,-3.0V,+1.5V
  - VCOM level: GND
  - Gate driver HIGH level (VGH to AGND): +10.0V
  - Gate driver LOW level (VGL to AGND): -10.0V
- Operate temperature range: -40℃to 85℃

3. Block Diagram

3.1. Block diagram



3.2. Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Type</th><th>Con</th><th>Descriptions</th></tr>
<tr><td colspan="4">IO Interface</td></tr>
<tr><td>IM3,
IM2,
IM1,
IM0/ID</td><td>I</td><td>MCU</td><td>Select the MCU system interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MCU-Interface Mode</th><th>DB Pins in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>M68-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>M68-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>I80-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>I80-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>24-bit 3wires Serial Peripheral interface(SPI)</td><td>SDI, SDO, SCL, CSX</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9-bit 3wires Serial Peripheral interface</td><td>SDA ,SCL, CSX</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8-bit 4wires Serial Peripheral interface</td><td>SDA ,SCL, CSX, RS</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>M68-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>M68-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>I80-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>I80-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting Invalid</td><td></td></tr>
</table>
When the 24-bit 3wires serial peripheral interface is selected, IM0 pin is used for the device code ID setting</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU</td><td>A chip select signal.
Low: the GC9203 is selected and accessible
High: the GC9203 is not selected and not accessible
Fix to VDDI level when not in use.</td></tr>
<tr><td>RSX</td><td>I</td><td>MCU</td><td>A register select signal.
Low: select a register address
High: select a register data
Fix to GND level when not in use.</td></tr>
<tr><td>WRX
/SCL</td><td>I</td><td>MCU</td><td>In 80-system mode, this serves as a write strobe signal (WRX).
In SPI mode, it serves as a synchronous clock (SCL).</td></tr>
<tr><td>RDX</td><td>I</td><td>MCU</td><td>In 80-system mode, this serves as a read strobe signal. (RDX).
Must be fixed to GND level when SPI mode.</td></tr>
<tr><td>RESETB</td><td>I</td><td>MCU</td><td>A reset pin.
Initializes the GC9203 with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>MCU</td><td>18-bit parallel bi-directional data bus for system interface
Serves as an input data bus for MPU I/F.</td></tr>
</table>

			8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. **Serves as an input data bus for RGB I/F.** 6-bit interface: DB[17:12] 16-bit interface: {DB[17:13], DB[11:1]} 18-bit interface: DB[17:0] **Unused pins must be fixed GND level.**
SDA/SDI	I/O	MCU	Serial data input (SDI) pin in serial interface operation. The data is latched on the rising edge of the SCL signal. **Fix to GND level when not in use.**
SDO	O	MCU	Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. **When the SPI interface is not used, please let SDO as floating.**
DOTCLK	O	MCU	A dot clock signal. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK **Fix to GND level when not in use**
VSYNC	I	MCU	A frame synchronizing signal. VSPL = "0": Active low. VSPL = "1": Active high. **Fix to GND level when not in use.**
HSYNC	I	MCU	A line synchronizing signal. HSPL = "0": Active low. HSPL = "1": Active high. **Fix to GND level when not in use.**
ENABLE	I	MCU	A data ENEABLE signal in RGB interface mode. Low: Select (access enabled) High: Not select (access inhibited) The EPL bit inverts the polarity of the ENABLE signal. **Fix to GND level when not in use.**
FLM	O	MCU	Tearing effect output pin to synchronize MCU to frame writing, **If not used, open this pin.**
LCD Driving signals			
S528~S1	O	LCD	Source output voltage signals applied to liquid crystal. To change the shift direction of signal outputs, use the SS bit. SS = "0", the data in the RAM address "00000h" is output from S1 SS = "1", the data in the RAM address "00000h" is output from S528. S1, S4, S7, … display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ...
G220~G1	O	LCD	Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines

VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel.
Charge-pump and Regulator Circuit			
AVDD	O	OPEN	Power pad for analog circuit, A power supply pin for generating VREG1A
AVEE	O	OPEN	Power pad for analog circuit, A power supply pin for generating VREG2A
VREG1A	O	OPEN	A power output of gray scale voltage generator(positive)
VREG1B	O	OPEN	A power output of gray scale voltage generator(positive)
VREG2A	O	OPEN	A power output of gray scale voltage generator(negative)
VREG2B	O	OPEN	A power output of gray scale voltage generator(negative)
DVDD	P	OPEN	Power supply for memory and internal logic circuit.
VGH	O	OPEN	Power output pin for gate driver(positive)
VGL	O	OPEN	Power output pin for gate driver(negative)
Power Pads			
VCI	I	Power	A supply voltage to the analog circuit and charge-pump. Connect this pin to an external power supply
VDDI	I	Power	A supply voltage to the interface pins
VSSA	P	GND	GND for analog circuits/ booster circuits
VSSR	P	GND	GND for logic circuits

Liquid crystal power supply specifications Table 1

No.	Item		Description
1	TFT data lines		528 pins (176*RGB)
2	TFT gate lines		220 pins
3	TFT Display's Capacitor Structure		Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1~S528	V0~V63 gray scales
		G1~G220	VGH-VGL
		VCOM	GND
5	Input Voltage	VDDI	1.65~3.30V
		VCI	2.50~3.30V
6	Liquid Crystal Drive Voltages	VREG1A	6.0V
		VREG2A	-3.0V

		VREG1B	1.5V
		VREG2B	1.5V
		VGH	10.0V
		VGL	-10.0V

3.3. PAD coordinates

	Pad name	X	Y
1	DUMMY1	-6695	-240
2	DUMMY2	-6635	-240
3	VCOM	-6575	-240
4	VCOM	-6515	-240
5	VCOM	-6455	-240
6	VCOM	-6395	-240
7	DUMMY3	-6335	-240
8	VGH	-6275	-240
9	VGH	-6215	-240
10	VGH	-6155	-240
11	VGH	-6095	-240
12	VGH	-6035	-240
13	DUMMY4	-5975	-240
14	VGL	-5915	-240
15	VGL	-5855	-240
16	VGL	-5795	-240
17	VGL	-5735	-240
18	VGL	-5675	-240
19	DUMMY5	-5615	-240
20	VCL	-5555	-240
21	VCL	-5495	-240
22	VCL	-5435	-240
23	VDH	-5375	-240
24	VDH	-5315	-240
25	VDH	-5255	-240
26	DUMMY	-5195	-240
27	DUMMY	-5135	-240
28	DUMMY	-5075	-240
29	DUMMY	-5015	-240
30	DUMMY	-4955	-240
31	DUMMY	-4895	-240
32	DUMMY6	-4835	-240
33	DUMMY7	-4775	-240
34	VSSA	-4715	-240
35	VSSA	-4655	-240
36	VSSA	-4595	-240
37	VSSA	-4535	-240
38	VSSA	-4475	-240
39	VSSA	-4415	-240
40	VSSA	-4355	-240
41	VSSA	-4295	-240
42	VSSA	-4235	-240
43	VSSA	-4175	-240
44	DUMMY	-4115	-240
45	DUMMY	-4055	-240
46	DUMMY	-3995	-240
47	DUMMY	-3935	-240
48	DUMMY	-3875	-240
49	DUMMY	-3815	-240
50	VPP_PAD	-3755	-240

No.	Pad name	X	Y
51	VPP_PAD	-3695	-240
52	VPP_PAD	-3635	-240
53	VPP_PAD	-3575	-240
54	VPP_PAD	-3515	-240
55	VPP_PAD	-3455	-240
56	VPP_PAD	-3395	-240
57	VPP_PAD	-3335	-240
58	VDDSF	-3275	-240
59	VDDSF	-3215	-240
60	VDDSF	-3155	-240
61	VDDSF	-3095	-240
62	VDDSF	-3035	-240
63	VDDSF	-2975	-240
64	VDDSF	-2915	-240
65	VDDSF	-2855	-240
66	TEST_PAD_L	-2795	-240
67	TEST_PAD_L	-2735	-240
68	TEST_PAD_L	-2675	-240
69	TEST_PAD_L	-2615	-240
70	TEST_PAD_L	-2555	-240
71	TEST_PAD_L	-2495	-240
72	BVEE	-2435	-240
73	BVEE	-2375	-240
74	BVEE	-2315	-240
75	BVEE	-2255	-240
76	BVEE	-2195	-240
77	BVEE	-2135	-240
78	BVDD	-2075	-240
79	BVDD	-2015	-240
80	BVDD	-1955	-240
81	BVDD	-1895	-240
82	BVDD	-1835	-240
83	DUMMY	-1775	-240
84	DUMMY	-1715	-240
85	DUMMY	-1655	-240
86	DUMMY	-1595	-240
87	DUMMY	-1535	-240
88	DUMMY	-1475	-240
89	DUMMY	-1415	-240
90	DUMMY	-1355	-240
91	DUMMY	-1295	-240
92	DUMMY	-1235	-240
93	DUMMY	-1175	-240
94	DUMMY	-1115	-240
95	DUMMY	-1055	-240
96	VDDA	-995	-240
97	VDDA	-935	-240
98	VDDA	-875	-240
99	VDDA	-815	-240
100	VDDA	-755	-240

No.	Pad name	X	Y
101	VDDA	-695	-240
102	VDDA	-635	-240
103	VDDA	-575	-240
104	VDDA	-515	-240
105	VDDA	-455	-240
106	DUMMY	-395	-240
107	DUMMY	-335	-240
108	DUMMY	-275	-240
109	DUMMY	-215	-240
110	DUMMY	-155	-240
111	DUMMY8	-95	-240
112	RSX	-35	-240
113	CSX	25	-240
114	VSYNC	85	-240
115	HSYNC	145	-240
116	DOTCLK	205	-240
117	ENABLE	265	-240
118	RESETB	325	-240
119	SDA	385	-240
120	RDX	445	-240
121	WRX	505	-240
122	DB<17>	565	-240
123	DB<16>	650	-240
124	DB<15>	735	-240
125	DB<14>	820	-240
126	DB<13>	905	-240
127	DB<12>	990	-240
128	DB<11>	1075	-240
129	DB<10>	1160	-240
130	DB<9>	1245	-240
131	DB<8>	1330	-240
132	DB<7>	1415	-240
133	DB<6>	1500	-240
134	DB<5>	1585	-240
135	DB<4>	1670	-240
136	DB<3>	1755	-240
137	DB<2>	1840	-240
138	DB<1>	1925	-240
139	DB<0>	2010	-240
140	IM<3>	2095	-240
141	IM<2>	2155	-240
142	IM<1>	2215	-240
143	IM<0>	2275	-240
144	SDO	2335	-240
145	EXT_CLK	2420	-240
146	FLM	2505	-240
147	A2P_TEST_PAD_R	2590	-240
148	DUMMY	2675	-240
149	DUMMY	2735	-240
150	DUMMY	2795	-240

No.	Pad name	X	Y
151	DUMMY	2855	-240
152	DUMMY	2915	-240
153	DUMMY	2975	-240
154	DUMMY	3035	-240
155	DUMMY	3095	-240
156	DUMMY	3155	-240
157	VSSR	3215	-240
158	VSSR	3275	-240
159	VSSR	3335	-240
160	VSSR	3395	-240
161	VSSR	3455	-240
162	VSSR	3515	-240
163	VSSR	3575	-240
164	VSSR	3635	-240
165	VSSR	3695	-240
166	VSSA	3755	-240
167	VSSA	3815	-240
168	VSSA	3875	-240
169	VSSA	3935	-240
170	VSSA	3995	-240
171	VSSA	4055	-240
172	VSSA	4115	-240
173	VSSA	4175	-240
174	VSSA	4235	-240
175	VSSA	4295	-240
176	VSSA	4355	-240
177	VSSA	4415	-240
178	DVDD	4475	-240
179	DVDD	4535	-240
180	DVDD	4595	-240
181	DVDD	4655	-240
182	DVDD	4715	-240
183	DVDD	4775	-240
184	DVDD	4835	-240
185	DVDD	4895	-240
186	DVDD	4955	-240
187	DVDD	5015	-240
188	DVDD	5075	-240
189	DVDD	5135	-240
190	VDDI	5195	-240
191	VDDI	5255	-240
192	VDDI	5315	-240
193	VDDI	5375	-240
194	VDDI	5435	-240
195	VDDI	5495	-240
196	DUMMY9	5555	-240
197	VREF	5615	-240
198	VREG1A	5675	-240
199	VREG1A	5735	-240
200	VREG1A	5795	-240

No.	Pad name	X	Y
201	VREG1A	5855	-240
202	AVDD	5915	-240
203	AVDD	5975	-240
204	AVEE	6035	-240
205	AVEE	6095	-240
206	VREG2A	6155	-240
207	CONTACT	6215	-240
208	CONTACT	6275	-240
209	DUMMY10	6335	-240
210	VCOM	6395	-240
211	VCOM	6455	-240
212	VCOM	6515	-240
213	VCOM	6575	-240
214	DUMMY11	6635	-240
215	DUMMY12	6695	-240
216	DUMMY13	6772	224
217	DUMMY14	6756	110
218	DUMMY15	6740	224
219	DUMMY16	6724	110
220	G<2>	6707.196	224
221	G<4>	6691.2	110
222	G<6>	6675.2	224
223	G<8>	6659.204	110
224	G<10>	6643.204	224
225	G<12>	6627.208	110
226	G<14>	6611.208	224
227	G<16>	6595.212	110
228	G<18>	6579.212	224
229	G<20>	6563.216	110
230	G<22>	6547.216	224
231	G<24>	6531.22	110
232	G<26>	6515.22	224
233	G<28>	6499.224	110
234	G<30>	6483.224	224
235	G<32>	6467.228	110
236	G<34>	6451.228	224
237	G<36>	6435.232	110
238	G<38>	6419.232	224
239	G<40>	6403.236	110
240	G<42>	6387.236	224
241	G<44>	6371.24	110
242	G<46>	6355.24	224
243	G<48>	6339.244	110
244	G<50>	6323.244	224
245	G<52>	6307.248	110
246	G<54>	6291.248	224
247	G<56>	6275.252	110
248	G<58>	6259.252	224
249	G<60>	6243.256	110
250	G<62>	6227.256	224

No.	Pad	X	Y
251	G<64>	6211.26	110
252	G<66>	6195.26	224
253	G<68>	6179.264	110
254	G<70>	6163.264	224
255	G<72>	6147.268	110
256	G<74>	6131.268	224
257	G<76>	6115.272	110
258	G<78>	6099.272	224
259	G<80>	6083.276	110
260	G<82>	6067.276	224
261	G<84>	6051.28	110
262	G<86>	6035.28	224
263	G<88>	6019.284	110
264	G<90>	6003.284	224
265	G<92>	5987.288	110
266	G<94>	5971.288	224
267	G<96>	5955.292	110
268	G<98>	5939.292	224
269	G<100>	5923.296	110
270	G<102>	5907.296	224
271	G<104>	5891.3	110
272	G<106>	5875.3	224
273	G<108>	5859.304	110
274	G<110>	5843.304	224
275	G<112>	5827.308	110
276	G<114>	5811.308	224
277	G<116>	5795.312	110
278	G<118>	5779.312	224
279	G<120>	5763.316	110
280	G<122>	5747.316	224
281	G<124>	5731.32	110
282	G<126>	5715.32	224
283	G<128>	5699.324	110
284	G<130>	5683.324	224
285	G<132>	5667.328	110
286	G<134>	5651.328	224
287	G<136>	5635.332	110
288	G<138>	5619.332	224
289	G<140>	5603.336	110
290	G<142>	5587.336	224
291	G<144>	5571.34	110
292	G<146>	5555.34	224
293	G<148>	5539.344	110
294	G<150>	5523.344	224
295	G<152>	5507.348	110
296	G<154>	5491.348	224
297	G<156>	5475.352	110
298	G<158>	5459.352	224
299	G<160>	5443.356	110
300	G<162>	5427.356	224

No.	Pad name	X	Y
301	G<164>	5411.36	110
302	G<166>	5395.36	224
303	G<168>	5379.364	110
304	G<170>	5363.364	224
305	G<172>	5347.368	110
306	G<174>	5331.368	224
307	G<176>	5315.372	110
308	G<178>	5299.372	224
309	G<180>	5283.376	110
310	G<182>	5267.376	224
311	G<184>	5251.38	110
312	G<186>	5235.38	224
313	G<188>	5219.384	110
314	G<190>	5203.384	224
315	G<192>	5187.388	110
316	G<194>	5171.388	224
317	G<196>	5155.392	110
318	G<198>	5139.392	224
319	G<200>	5123.396	110
320	G<202>	5107.396	224
321	G<204>	5091.4	110
322	G<206>	5075.4	224
323	G<208>	5059.404	110
324	G<210>	5043.404	224
325	G<212>	5027.408	110
326	G<214>	5011.408	224
327	G<216>	4995.412	110
328	G<218>	4979.412	224
329	G<220>	4963.416	110
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334	DUMMY21	4884	224
335	DUMMY22	4868	110
336	DUMMY23	4852	224
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374	S<493>	4243.504	224
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394	S<473>	3923.544	224
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410	S<457>	3667.576	224
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416	S<451>	3571.588	224
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422	S<445>	3475.6	224
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436	S<431>	3251.628	224
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464	S<403>	2803.684	224
465	S<402>	2787.688	110
466	S<401>	2771.688	224
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468	S<399>	2739.692	224
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471	S<396>	2641.706	110
472	S<395>	2625.706	224
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474	S<393>	2593.71	224
475	S<392>	2577.714	110
476	S<391>	2561.714	224
477	S<390>	2545.718	110
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479	S<388>	2513.722	110
480	S<387>	2497.722	224
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488	S<379>	2369.738	224
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497	S<370>	2225.758	110
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506	S<361>	2081.774	224
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509	S<358>	2033.782	110
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532	S<335>	1665.826	224
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559	S<308>	1233.882	110
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563	S<304>	1169.89	110
564	S<303>	1153.89	224
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580	S<287>	897.922	224
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586	S<281>	801.934	224
587	S<280>	785.938	110
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589	S<278>	753.942	110
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612	S<255>	-697.95	224
613	S<254>	-713.946	110
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617	S<250>	-777.938	110
618	S<249>	-793.938	224
619	S<248>	-809.934	110
620	S<247>	-825.934	224
621	S<246>	-841.93	110
622	S<245>	-857.93	224
623	S<244>	-873.926	110
624	S<243>	-889.926	224
625	S<242>	-905.922	110
626	S<241>	-921.922	224
627	S<240>	-937.918	110
628	S<239>	-953.918	224
629	S<238>	-969.914	110
630	S<237>	-985.914	224
631	S<236>	-1001.91	110
632	S<235>	-1017.91	224
633	S<234>	-1033.906	110
634	S<233>	-1049.906	224
635	S<232>	-1065.902	110
636	S<231>	-1081.902	224
637	S<230>	-1097.898	110
638	S<229>	-1113.898	224
639	S<228>	-1129.894	110
640	S<227>	-1145.894	224
641	S<226>	-1161.89	110
642	S<225>	-1177.89	224
643	S<224>	-1193.886	110
644	S<223>	-1209.886	224
645	S<222>	-1225.882	110
646	S<221>	-1241.882	224
647	S<220>	-1257.878	110
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655	S<212>	-1385.862	110
656	S<211>	-1401.862	224
657	S<210>	-1417.858	110
658	S<209>	-1433.858	224
659	S<208>	-1449.854	110
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661	S<206>	-1481.85	110
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663	S<204>	-1513.846	110
664	S<203>	-1529.846	224
665	S<202>	-1545.842	110
666	S<201>	-1561.842	224
667	S<200>	-1577.838	110
668	S<199>	-1593.838	224
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670	S<197>	-1625.834	224
671	S<196>	-1641.83	110
672	S<195>	-1657.83	224
673	S<194>	-1673.826	110
674	S<193>	-1689.826	224
675	S<192>	-1705.822	110
676	S<191>	-1721.822	224
677	S<190>	-1737.818	110
678	S<189>	-1753.818	224
679	S<188>	-1769.814	110
680	S<187>	-1785.814	224
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682	S<185>	-1817.81	224
683	S<184>	-1833.806	110
684	S<183>	-1849.806	224
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687	S<180>	-1897.798	110
688	S<179>	-1913.798	224
689	S<178>	-1929.794	110
690	S<177>	-1945.794	224
691	S<176>	-1961.79	110
692	S<175>	-1977.79	224
693	S<174>	-1993.786	110
694	S<173>	-2009.786	224
695	S<172>	-2025.782	110
696	S<171>	-2041.782	224
697	S<170>	-2057.778	110
698	S<169>	-2073.778	224
699	S<168>	-2089.774	110
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No.	Pad name	X	Y
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705	S<162>	-2185.762	110
706	S<161>	-2201.762	224
707	S<160>	-2217.758	110
708	S<159>	-2233.758	224
709	S<158>	-2249.754	110
710	S<157>	-2265.754	224
711	S<156>	-2281.75	110
712	S<155>	-2297.75	224
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715	S<152>	-2345.742	110
716	S<151>	-2361.742	224
717	S<150>	-2377.738	110
718	S<149>	-2393.738	224
719	S<148>	-2409.734	110
720	S<147>	-2425.734	224
721	S<146>	-2441.73	110
722	S<145>	-2457.73	224
723	S<144>	-2473.726	110
724	S<143>	-2489.726	224
725	S<142>	-2505.722	110
726	S<141>	-2521.722	224
727	S<140>	-2537.718	110
728	S<139>	-2553.718	224
729	S<138>	-2569.714	110
730	S<137>	-2585.714	224
731	S<136>	-2601.71	110
732	S<135>	-2617.71	224
733	S<134>	-2633.706	110
734	S<133>	-2649.706	224
735	S<132>	-2715.696	110
736	S<131>	-2731.696	224
737	S<130>	-2747.692	110
738	S<129>	-2763.692	224
739	S<128>	-2779.688	110
740	S<127>	-2795.688	224
741	S<126>	-2811.684	110
742	S<125>	-2827.684	224
743	S<124>	-2843.68	110
744	S<123>	-2859.68	224
745	S<122>	-2875.676	110
746	S<121>	-2891.676	224
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No.	Pad name	X	Y
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756	S<111>	-3051.656	224
757	S<110>	-3067.652	110
758	S<109>	-3083.652	224
759	S<108>	-3099.648	110
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761	S<106>	-3131.644	110
762	S<105>	-3147.644	224
763	S<104>	-3163.64	110
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765	S<102>	-3195.636	110
766	S<101>	-3211.636	224
767	S<100>	-3227.632	110
768	S<99>	-3243.632	224
769	S<98>	-3259.628	110
770	S<97>	-3275.628	224
771	S<96>	-3291.624	110
772	S<95>	-3307.624	224
773	S<94>	-3323.62	110
774	S<93>	-3339.62	224
775	S<92>	-3355.616	110
776	S<91>	-3371.616	224
777	S<90>	-3387.612	110
778	S<89>	-3403.612	224
779	S<88>	-3419.608	110
780	S<87>	-3435.608	224
781	S<86>	-3451.604	110
782	S<85>	-3467.604	224
783	S<84>	-3483.6	110
784	S<83>	-3499.6	224
785	S<82>	-3515.596	110
786	S<81>	-3531.596	224
787	S<80>	-3547.592	110
788	S<79>	-3563.592	224
789	S<78>	-3579.588	110
790	S<77>	-3595.588	224
791	S<76>	-3611.584	110
792	S<75>	-3627.584	224
793	S<74>	-3643.58	110
794	S<73>	-3659.58	224
795	S<72>	-3675.576	110
796	S<71>	-3691.576	224
797	S<70>	-3707.572	110
798	S<69>	-3723.572	224
799	S<68>	-3739.568	110
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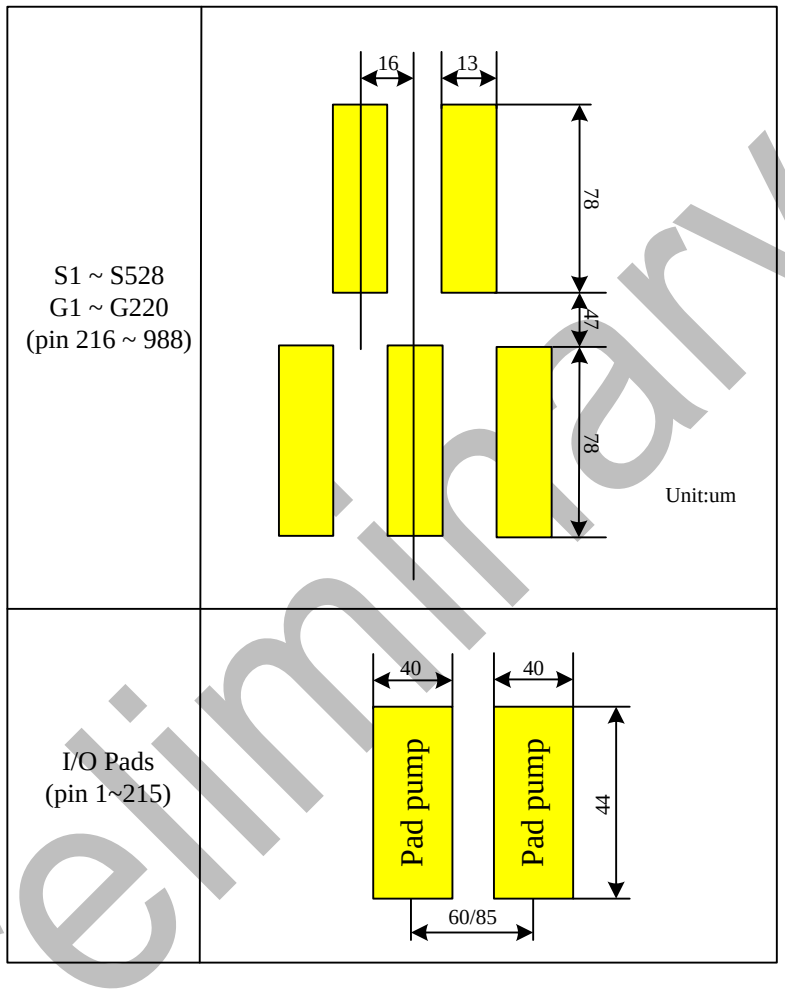
804	S<63>	-3819.	224
805	S<62>	-3835.	110
806	S<61>	-3851.	224
807	S<60>	-3867.	110
808	S<59>	-3883.	224
809	S<58>	-3899.	110
810	S<57>	-3915.	224
811	S<56>	-3931.	110
812	S<55>	-3947.	224
813	S<54>	-3963.	110
814	S<53>	-3979.	224
815	S<52>	-3995.	110
816	S<51>	-4011.	224
817	S<50>	-4027.	110
818	S<49>	-4043.	224
819	S<48>	-4059.	110
820	S<47>	-4075.	224
821	S<46>	-4091.	110
822	S<45>	-4107.	224
823	S<44>	-4123.	110
824	S<43>	-4139.	224
825	S<42>	-4155.	110
826	S<41>	-4171.	224
827	S<40>	-4187.	110
828	S<39>	-4203.	224
829	S<38>	-4219.	110
830	S<37>	-4235.	224
831	S<36>	-4251.	110
832	S<35>	-4267.	224
833	S<34>	-4283.	110
834	S<33>	-4299.	224
835	S<32>	-4315.	110
836	S<31>	-4331.	224
837	S<30>	-4347.	110
838	S<29>	-4363.	224
839	S<28>	-4379.	110
840	S<27>	-4395.	224
841	S<26>	-4411.	110
842	S<25>	-4427.	224
843	S<24>	-4443.	110
844	S<23>	-4459.	224
845	S<22>	-4475.	110
846	S<21>	-4491.	224
847	S<20>	-4507.	110
848	S<19>	-4523.	224
849	S<18>	-4539.	110
850	S<17>	-4555.	224

No.	Pad name	X	Y
851	S<16>	-4571.	110
852	S<15>	-4587.	224
853	S<14>	-4603.	110
854	S<13>	-4619.	224
855	S<12>	-4635.	110
856	S<11>	-4651.	224
857	S<10>	-4667.	110
858	S<9>	-4683.	224
859	S<8>	-4699.	110
860	S<7>	-4715.	224
861	S<6>	-4731.	110
862	S<5>	-4747.	224
863	S<4>	-4763.	110
864	S<3>	-4779.	224
865	S<2>	-4795.	110
866	S<1>	-4811.	224
867	DUMMY	-4828	110
868	DUMMY	-4844	224
869	DUMMY	-4860	110
870	DUMMY	-4876	224
871	DUMMY	-4892	110
872	DUMMY	-4908	224
873	DUMMY	-4924	110
874	DUMMY	-4940	224
875	G<219>	-4955.	110
876	G<217>	-4971.	224
877	G<215>	-4987.	110
878	G<213>	-5003.	224
879	G<211>	-5019.	110
880	G<209>	-5035.	224
881	G<207>	-5051.	110
882	G<205>	-5067.	224
883	G<203>	-5083.	110
884	G<201>	-5099.	224
885	G<199>	-5115.	110
886	G<197>	-5131.	224
887	G<195>	-5147.	110
888	G<193>	-5163.	224
889	G<191>	-5179.	110
890	G<189>	-5195.	224
891	G<187>	-5211.	110
892	G<185>	-5227.	224
893	G<183>	-5243.	110
894	G<181>	-5259.	224
895	G<179>	-5275.	110
896	G<177>	-5291.	224
897	G<175>	-5307.	110
898	G<173>	-5323.	224
899	G<171>	-5339.	110
900	G<169>	-5355.	224

No.	Pad name	X	Y
901	G<167>	-5371.364	110
902	G<165>	-5387.364	224
903	G<163>	-5403.36	110
904	G<161>	-5419.36	224
905	G<159>	-5435.356	110
906	G<157>	-5451.356	224
907	G<155>	-5467.352	110
908	G<153>	-5483.352	224
909	G<151>	-5499.348	110
910	G<149>	-5515.348	224
911	G<147>	-5531.344	110
912	G<145>	-5547.344	224
913	G<143>	-5563.34	110
914	G<141>	-5579.34	224
915	G<139>	-5595.336	110
916	G<137>	-5611.336	224
917	G<135>	-5627.332	110
918	G<133>	-5643.332	224
919	G<131>	-5659.328	110
920	G<129>	-5675.328	224
921	G<127>	-5691.324	110
922	G<125>	-5707.324	224
923	G<123>	-5723.32	110
924	G<121>	-5739.32	224
925	G<119>	-5755.316	110
926	G<117>	-5771.316	224
927	G<115>	-5787.312	110
928	G<113>	-5803.312	224
929	G<111>	-5819.308	110
930	G<109>	-5835.308	224
931	G<107>	-5851.304	110
932	G<105>	-5867.304	224
933	G<103>	-5883.3	110
934	G<101>	-5899.3	224
935	G<99>	-5915.296	110
936	G<97>	-5931.296	224
937	G<95>	-5947.292	110
938	G<93>	-5963.292	224
939	G<91>	-5979.288	110
940	G<89>	-5995.288	224
941	G<87>	-6011.284	110
942	G<85>	-6027.284	224
943	G<83>	-6043.28	110
944	G<81>	-6059.28	224
945	G<79>	-6075.276	110
946	G<77>	-6091.276	224
947	G<75>	-6107.272	110
948	G<73>	-6123.272	224
949	G<71>	-6139.268	110
950	G<69>	-6155.268	224

No.	Pad name	X	Y
951	G<67>	-6171.2	110
952	G<65>	-6187.2	224
953	G<63>	-6203.2	110
954	G<61>	-6219.2	224
955	G<59>	-6235.2	110
956	G<57>	-6251.2	224
957	G<55>	-6267.2	110
958	G<53>	-6283.2	224
959	G<51>	-6299.2	110
960	G<49>	-6315.2	224
961	G<47>	-6331.2	110
962	G<45>	-6347.2	224
963	G<43>	-6363.2	110
964	G<41>	-6379.2	224
965	G<39>	-6395.2	110
966	G<37>	-6411.2	224
967	G<35>	-6427.2	110
968	G<33>	-6443.2	224
969	G<31>	-6459.2	110
970	G<29>	-6475.2	224
971	G<27>	-6491.2	110
972	G<25>	-6507.2	224
973	G<23>	-6523.2	110
974	G<21>	-6539.2	224
975	G<19>	-6555.2	110
976	G<17>	-6571.2	224
977	G<15>	-6587.2	110
978	G<13>	-6603.2	224
979	G<11>	-6619.2	110
980	G<9>	-6635.2	224
981	G<7>	-6651.2	110
982	G<5>	-6667.2	224
983	G<3>	-6683.2	110
984	G<1>	-6699.2	224
985	DUMMY34	-6716	110
986	DUMMY35	-6732	224
987	DUMMY36	-6748	110
988	DUMMY37	-6764	224

3.4. BUMP Size



3.5. Chip Size

Chip Size: 13880um x 670um

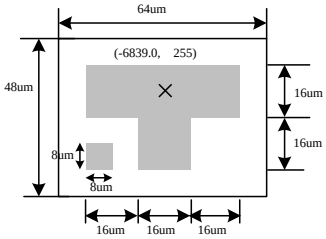
Chip thickness: 280 um / 400 um

Pad Location: Pad Center.

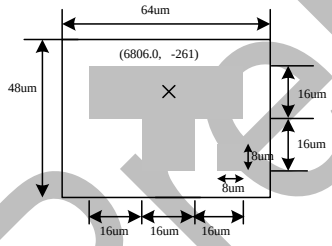
Coordinate Origin: Chip center

Au bump height: 12um

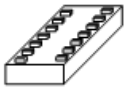
Alignment Marks-Left

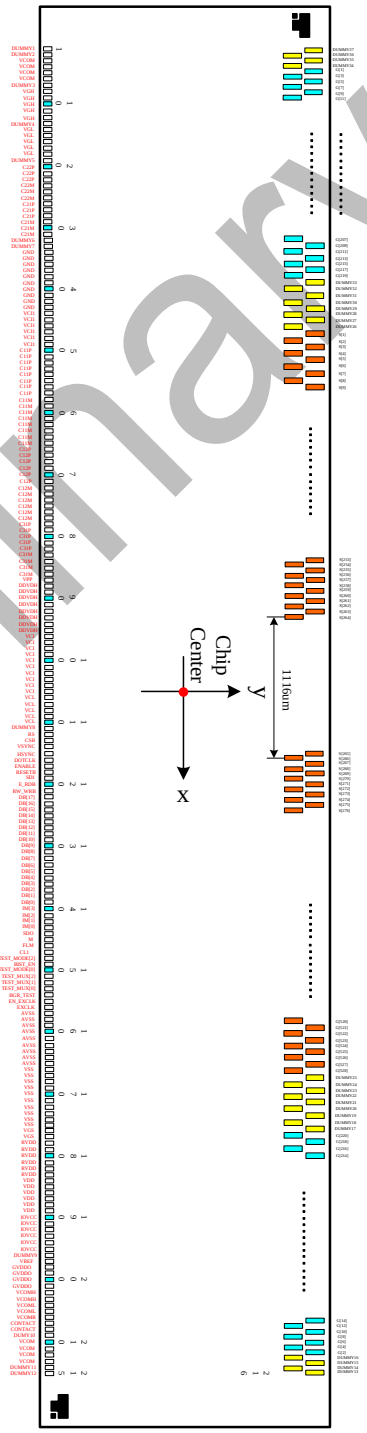


Alignment Mark-Right



Face Up
(Bimp View)





4. Block Description

MPU System Interface

GC9203 supports two system high-speed interfaces: i80/M68-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM [3:0] pins.

GC9203 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. **Therefore, invalid data are read out to the data bus when the GC9203 read the first data from the internal GRAM. Valid data are read out after the GC9203 performs the second read operation.**
Registers are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

Registers selection by system interface (8-/9-/16-/18-bit bus width)	**I80**			**M68**	
function	**RS**	E	RW	**WRX**	**RDX**
Write an index to IR register	0	1	0	0	1
Read an internal status	0	1	1	1	0
Write to control registers or the internal GRAM by WDR register.	1	1	0	0	1
Read from the internal GRAM by RDR register.	1	1	1	1	0

Registers selection by 24bit SPI system interface		
function	**R/W**	**RS**
Write an index to IR register	0	0
Read an internal status	1	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

Parallel RGB Interface

GC9203 supports the RGB interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally

supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data. In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the "External Display Interface" section. The GC9203 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data into the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 87,120 (176 x 220x 18/8) bytes, using 18 bits for each pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Register" section.

Timing Controller

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC.)

The GC9203 can provide R-C oscillation without external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be

obtained by adjusting the register setting value [R0Fh]. Since R-C oscillation stops during the standby mode, current consumption can be reduced.

LCD Driver Circuit

The LCD driver circuit of GC9203 consists of a 528-output source driver (S1 ~ S528) and a 220-output gate driver (G1~G220). Display pattern data are latched when the 528th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Driver Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1A , VREG2A , VREG1A , VREG2B , VGH , VGL and Vcom for driving an LCD.

5. System Interface

5.1. Interfaces Specifications

GC9203 has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

GC9203 also has the RGB interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB [17:0].

GC9203 operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB interfaces.

Operation Mode	**RAM Access Setting (RM)**	**Display Operation Mode (DM)**
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM =0)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM =1)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM =1)

Note 1) Registers are set only via the system interface.
Note 2) The RGB-I/F is not available simultaneously

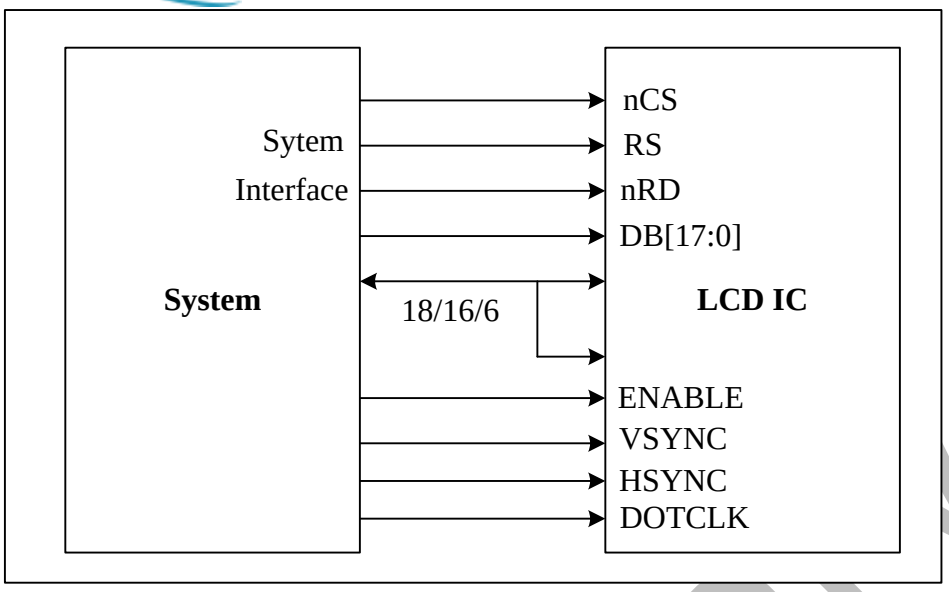


Figure1 System Interface and RGB Interface connection

5.2. MCU Interface

The following are the system interfaces available with the GC9203. The interface is selected by setting the IM [3:0] pins. The system interface is used for setting instructions and RAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	M68-system 16-bit interface	DB[17:10], DB[8:1]
0	0	0	1	M68-system 8-bit interface	DB[17:10]
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	3-wire 24-bit serial interface	SDI, SDO
0	1	1	0	3-wire 9-bit serial interface	SDA
0	1	1	1	4-wire 8-bit serial interface	SDA
1	0	0	0	M68-system18-bit interface	DB[17:0]
1	0	0	1	M68-system 9-bit interface	DB[17:9]
1	0	1	0	i80-system18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]

5.2.1. 18-bit System Interface

The data format for 18-bit data bus is as following,

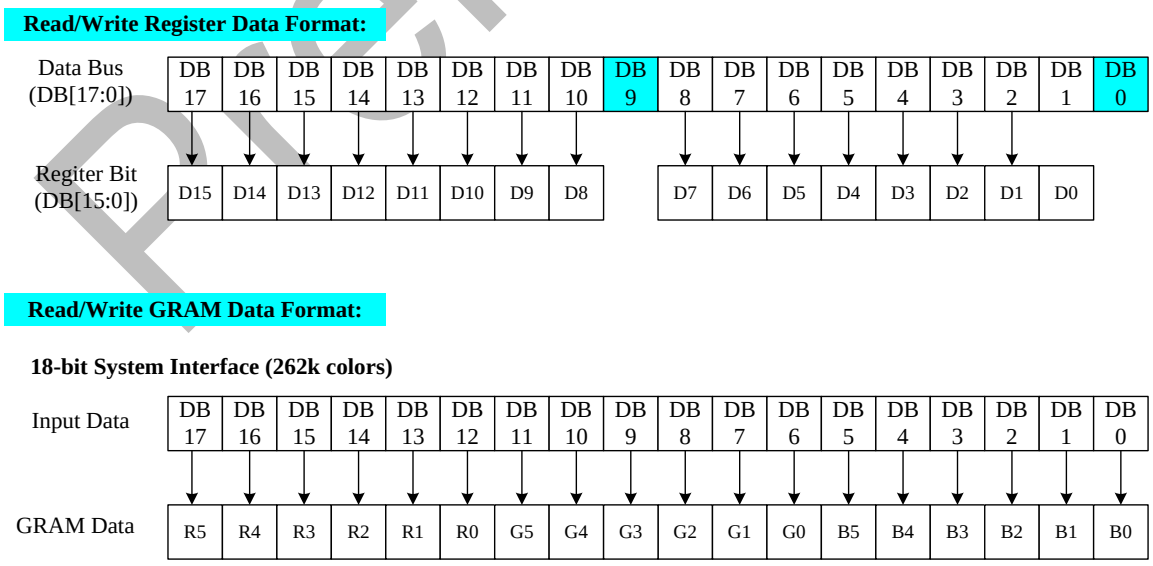


Figure2 18-bit System Interface Data Format

5.2.2. 16-bit System Interface

The data format for 16-bit data bus is as following,

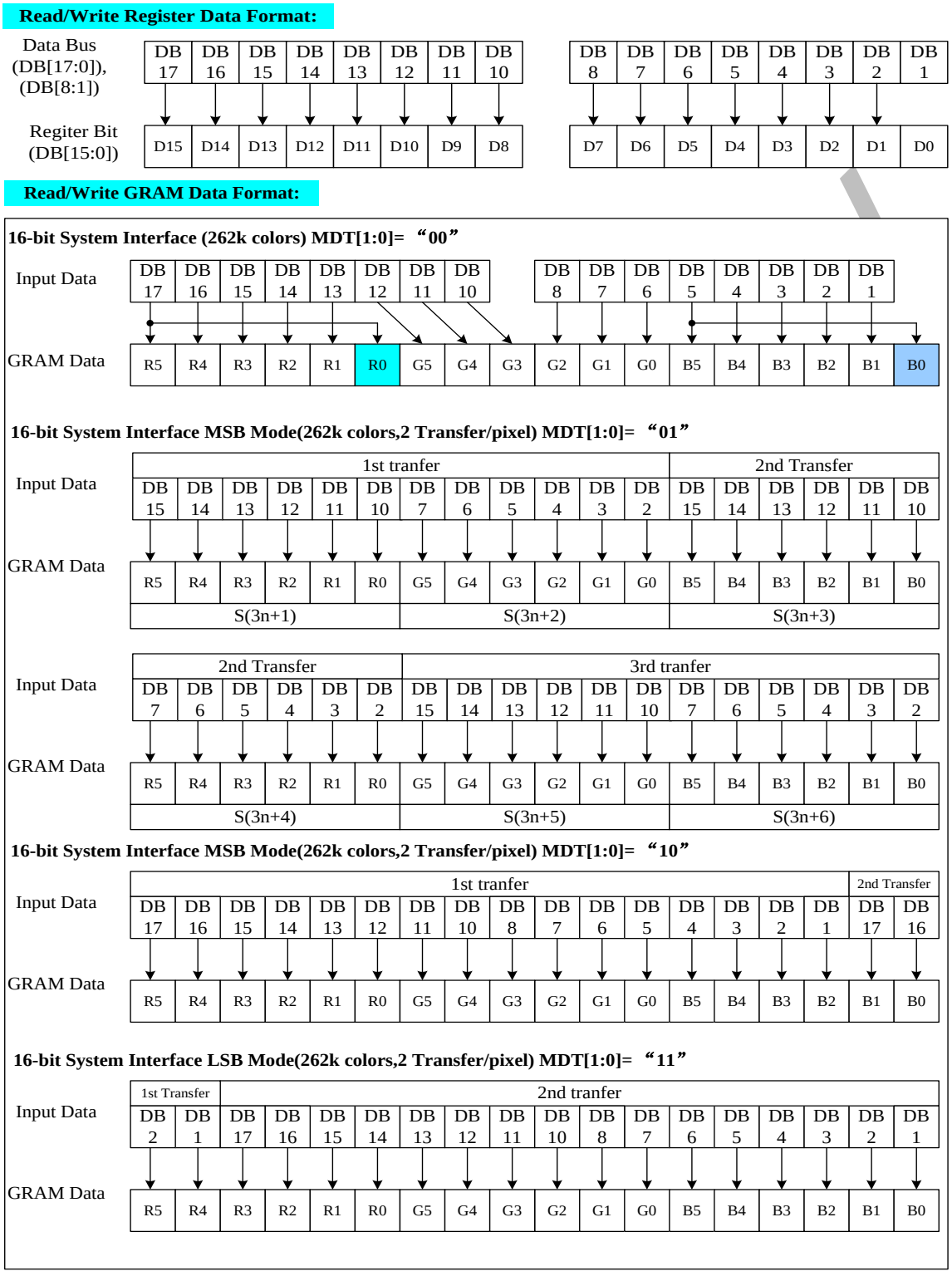
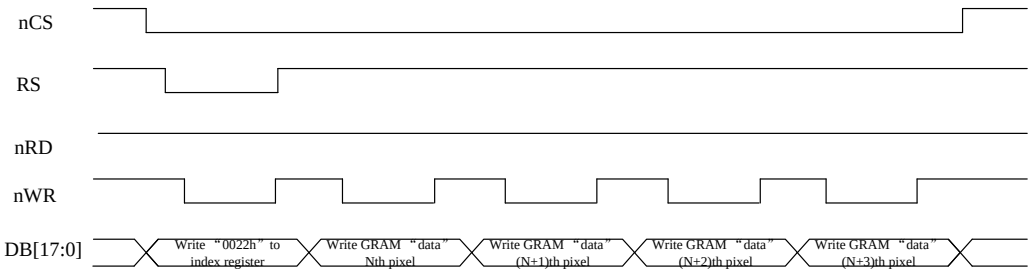


Figure3 16-bit System Interface Data Format

I80 Read/Write Timing:

(a) Write to GRAM



(b) Read from GRAM

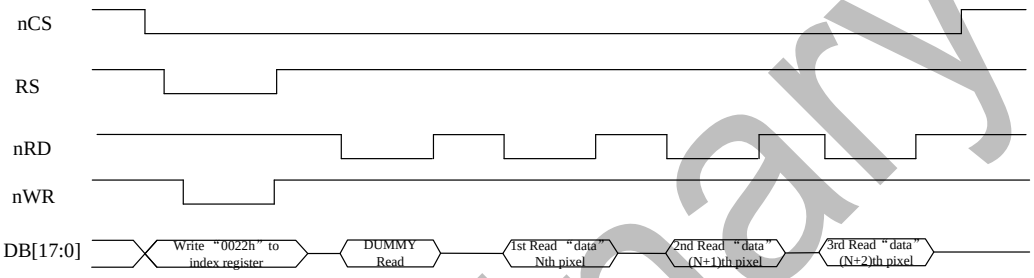
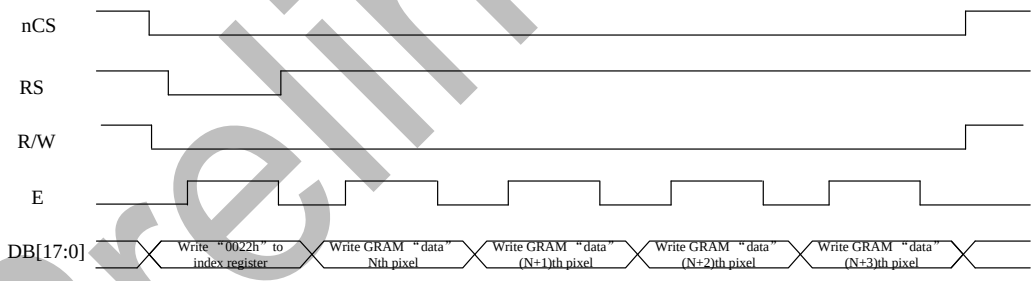


Figure4 i80 16/18-bit System Interface Timing

m68 Read/Write Timing:

(a) Write to GRAM



(b) Read from GRAM

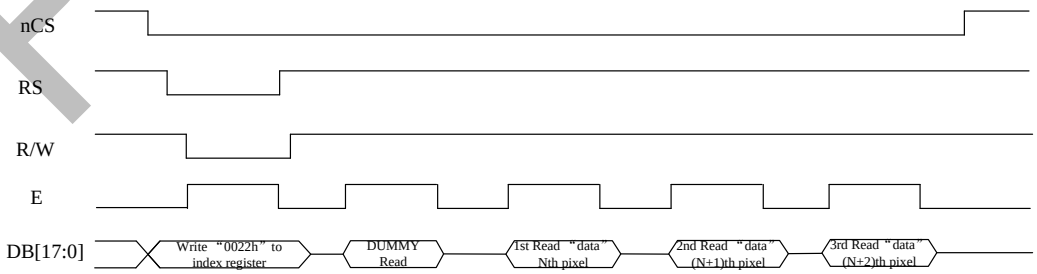
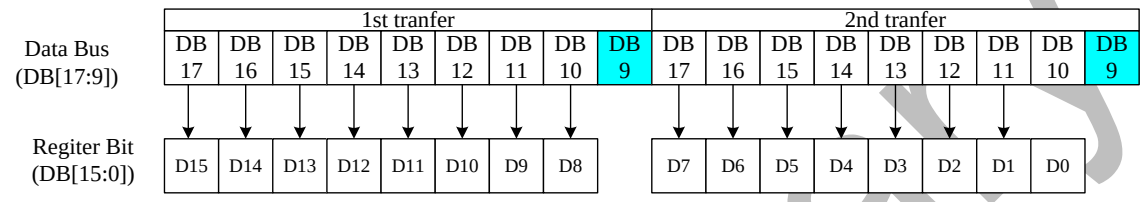


Figure5 M68 16/18-bit System Interface Timing

5.2.3. 9-bit System Interface

The DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to ground.

Read/Write Register Data Format:



Read/Write GRAM Data Format:

9-bit System Interface (262k colors)

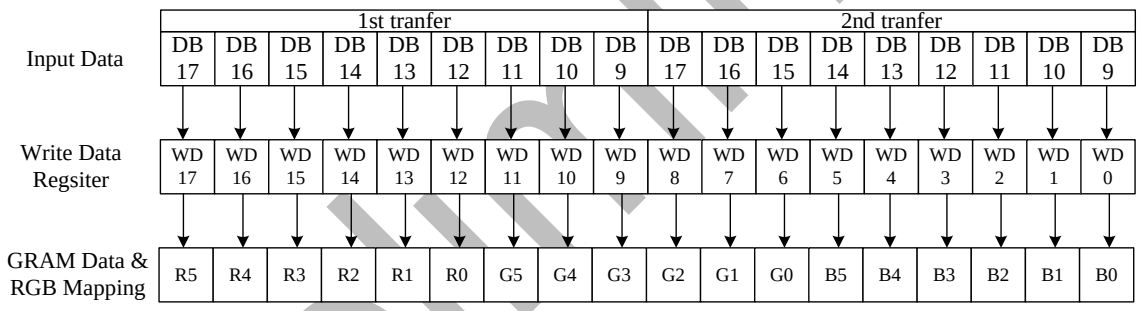


Figure6 9-bit System Interface Data Format

5.2.4. 8-bit System Interface

The DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to ground.

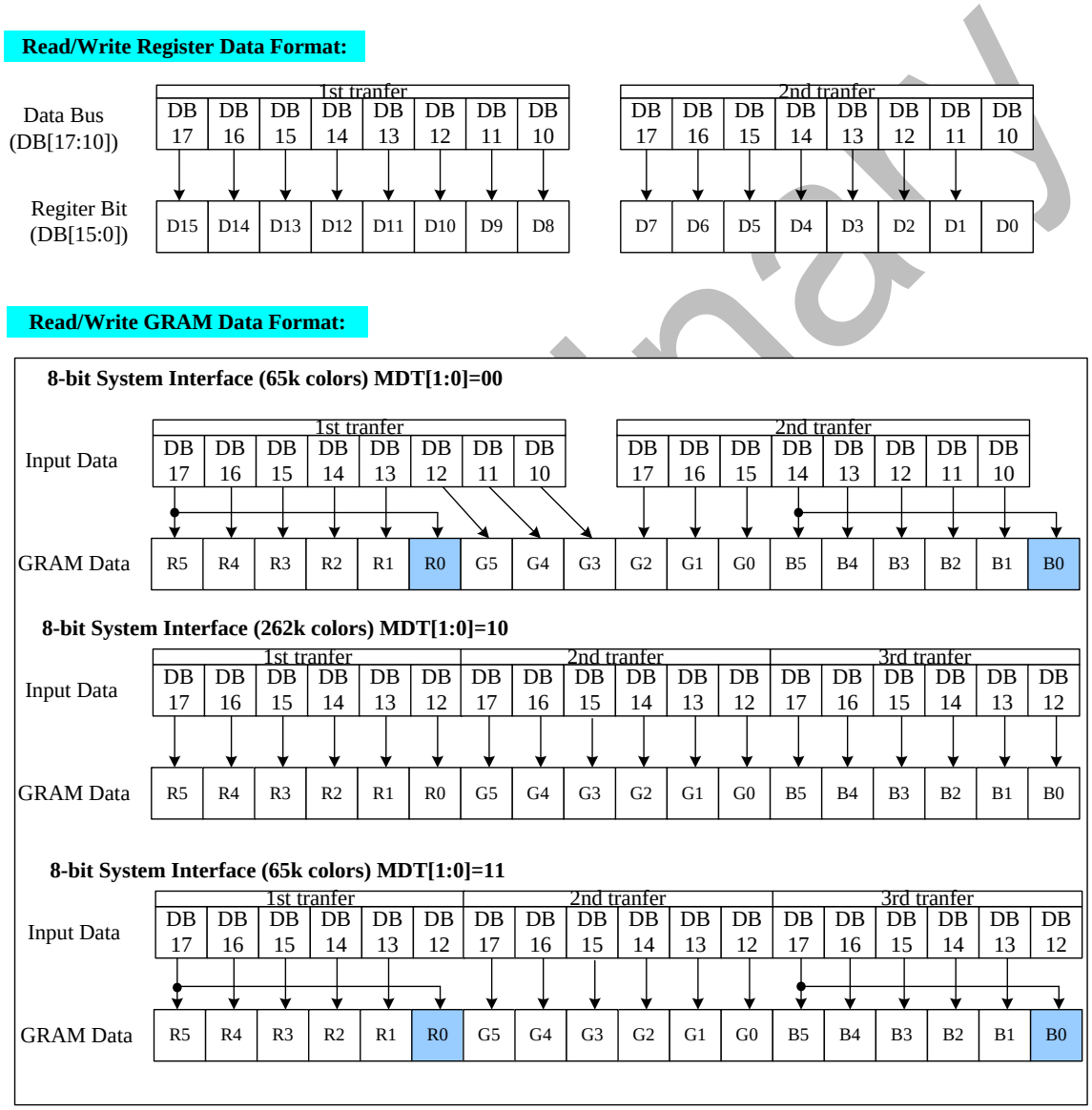


Figure7 8-bit System Interface Data Format

Data transfer synchronization in 8/9-bit bus interface mode

GC9203 supports a data transfer synchronization function to reset upper and lower counters which count the transfers number of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in then numbers of transfers between the upper and lower byte counters due to noise and so on, the “00”h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.

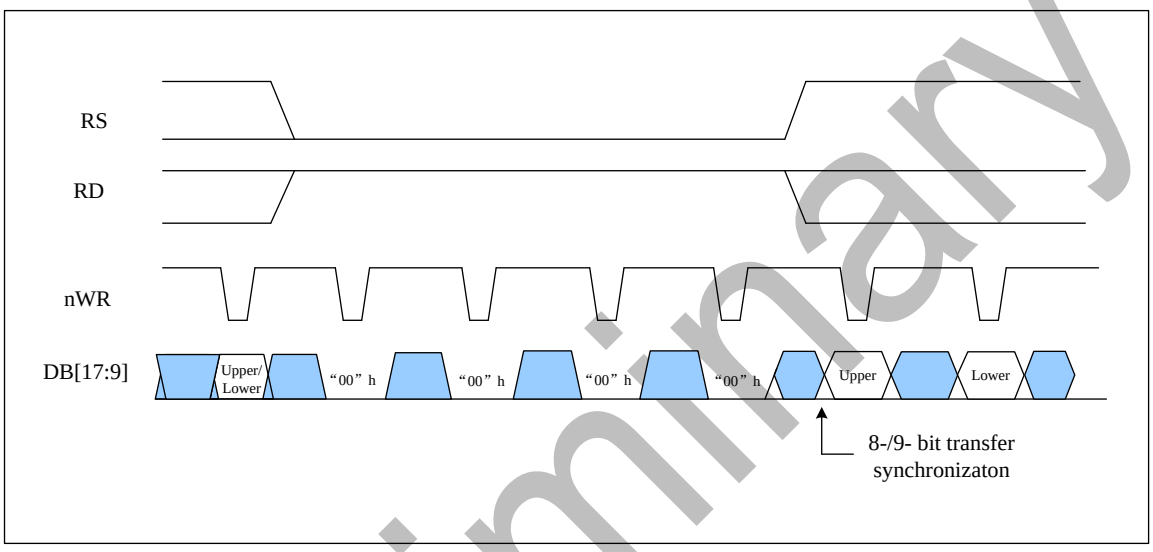


Figure8 Data Transfer Synchronization in 8/9-bit System Interface

5.3. Serial Peripheral Interface (SPI)

5.3.1. 3-wire 24-bit Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM [3:0] pins as “010x” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to ground.

The SPI interface operation enables from the falling edge of CSX and ends of data transfer on the rising edge of CSX. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by GC9203.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, GC9203 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the GC9203 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 2 bytes dummy read is necessary and the valid data starts from 3rd byte of read back data.

Start Byte Format

Transfer bits	**S**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IM0/ID pin..

RS and R/W Bit Function

RS	**R/W**	**Function**
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

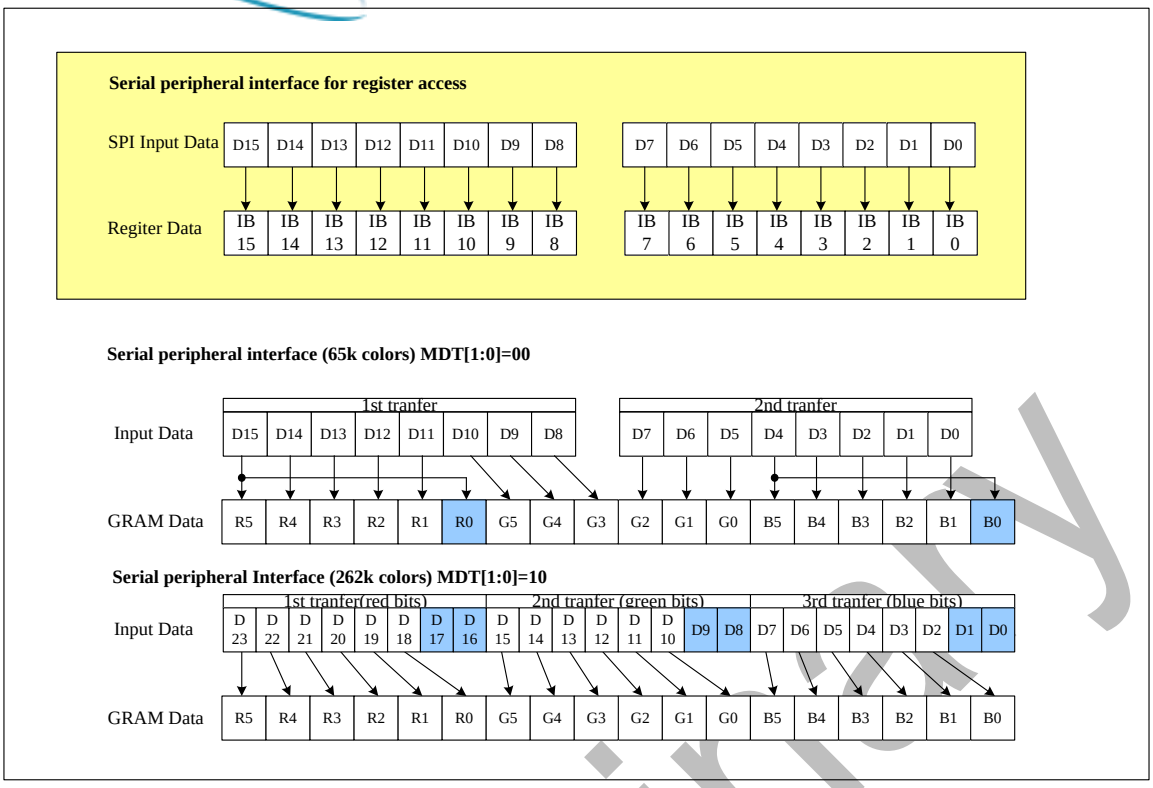


Figure9 Data Format of SPI Interface

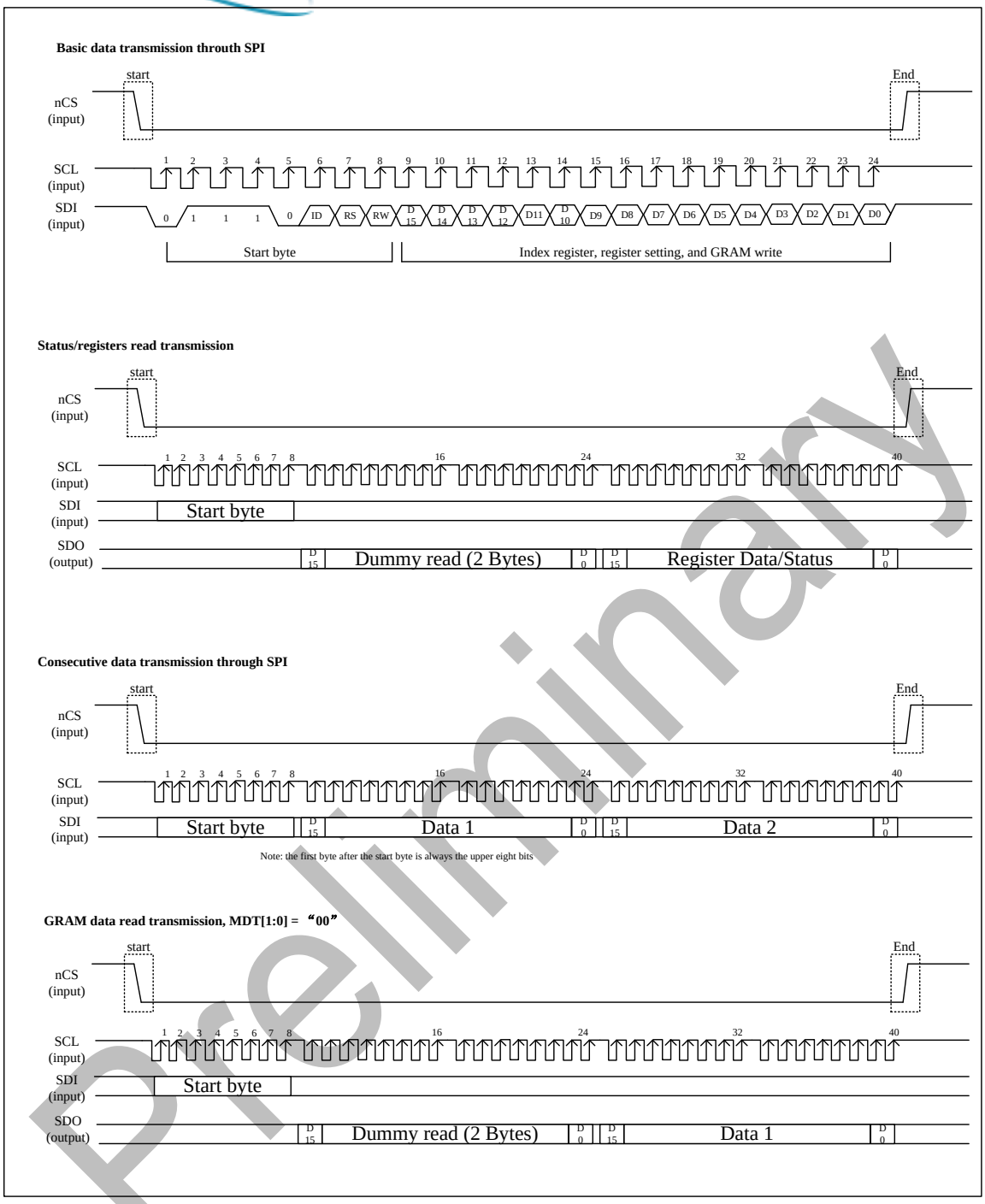


Figure10 Data transmission through SPI, 65K Color

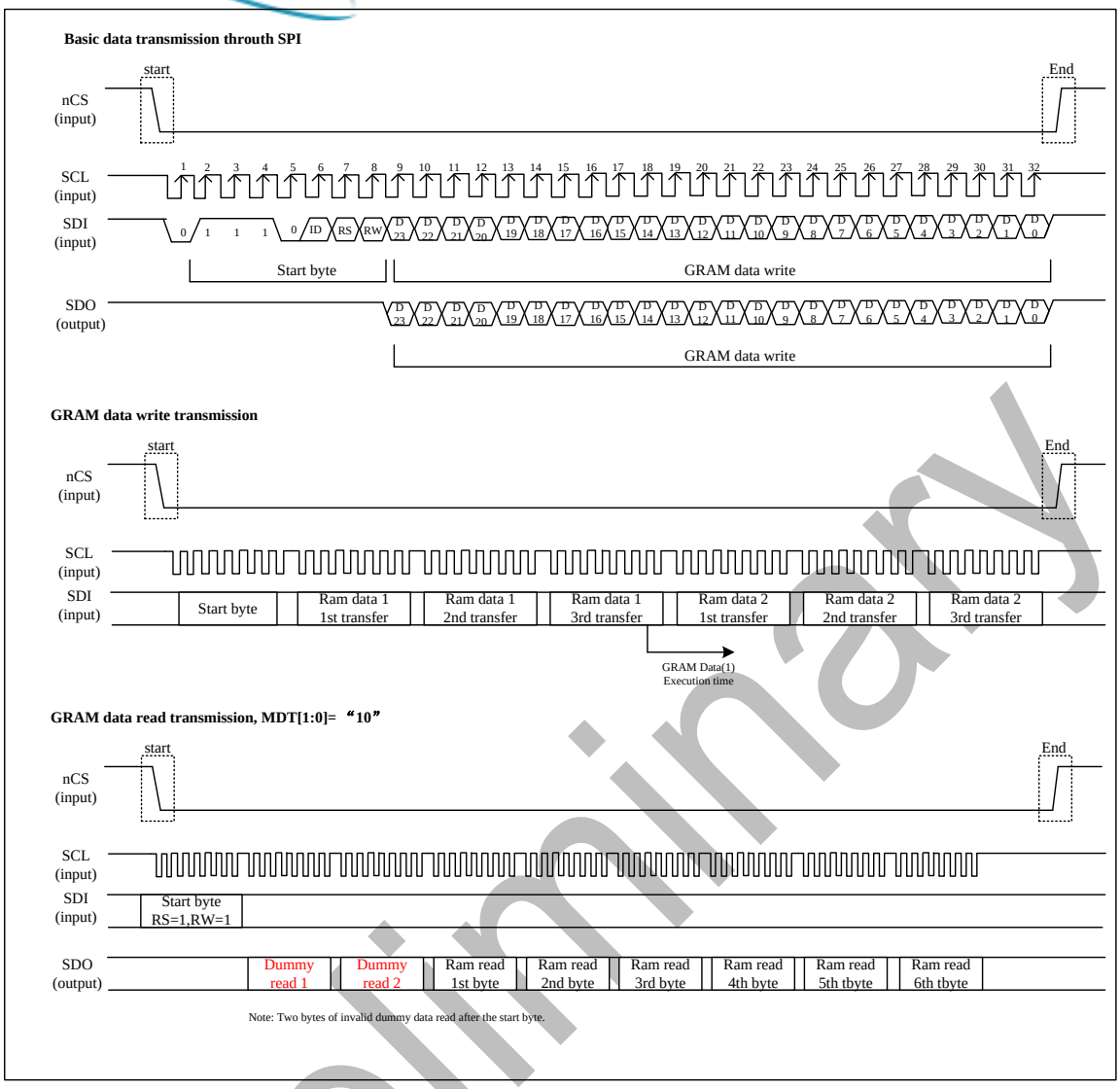


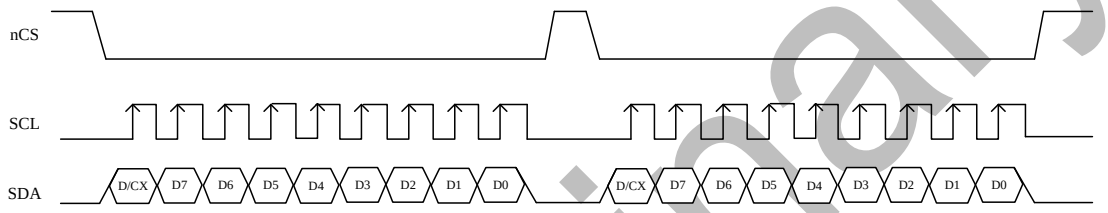
Figure11 Data transmission through SPI, 262K Color

5.3.2. 3-wire 9-bit Serial Interface

This SPI mode uses a 3-wire 9-bit serial interface. The chip-select CSX (active low) enables and disables the serial interface. SCL is the serial data clock and SDA is serial data.

Serial data must be input to SDA in the sequence D/CX, D7 to D0. The GC9203 reads the data at the rising edge of SCL signal. The first bit of serial data D/CX is data/command flag. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

Register Write Mode :

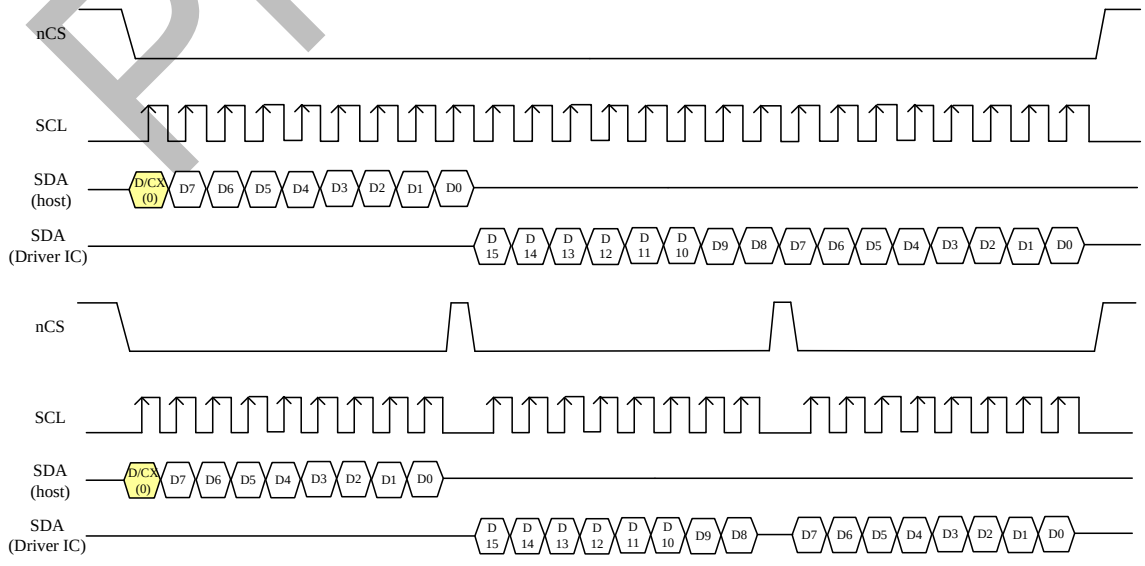


D/CX =0: register index (command)

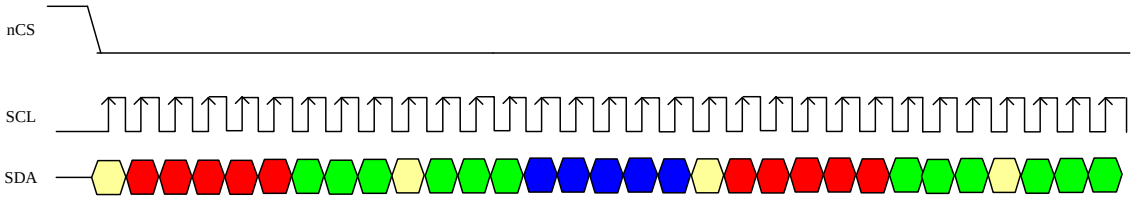
D/CX: register data or GRAMdata

Register read Mode :

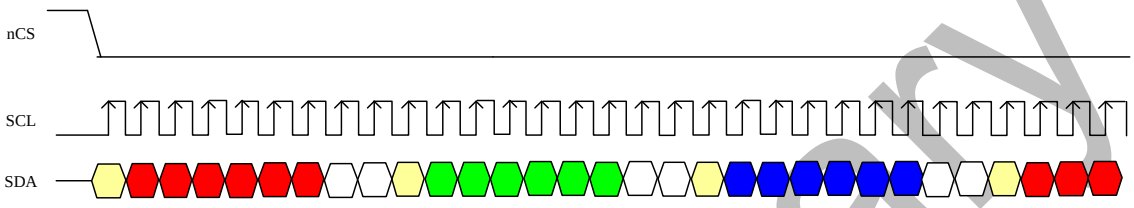
When users need to read back the register or GRAM data, the register R66h must be set as “1” first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.



Serial Data transfer interface(65K color, MDT[1:0]=“00”)



Serial Data transfer interface(262K color, MDT[1:0]=“10”)

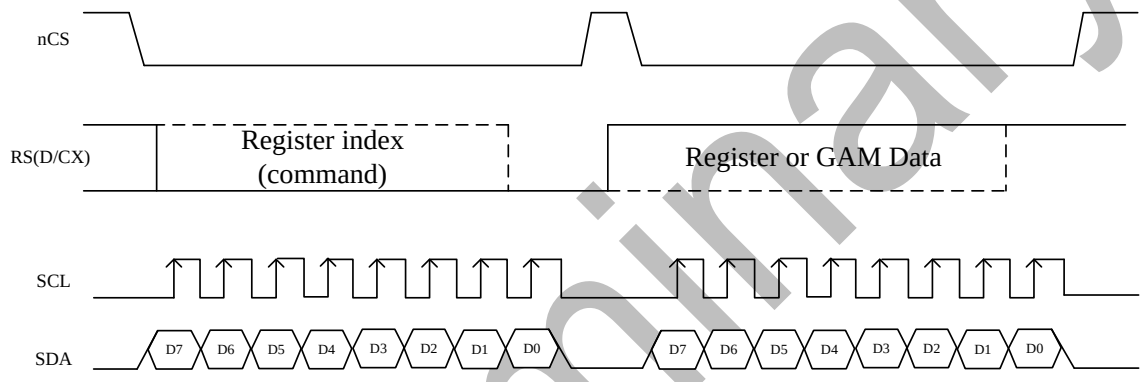


5.3.3. 4-wire 8-bit Serial Interface

This SPI mode uses a 4-wire 9-bit serial interface. The chip-select CSX (active low) enables and disables the serial interface. D/CX is the command or data select signal, SCL is the serial data clock and SDA is serial data.

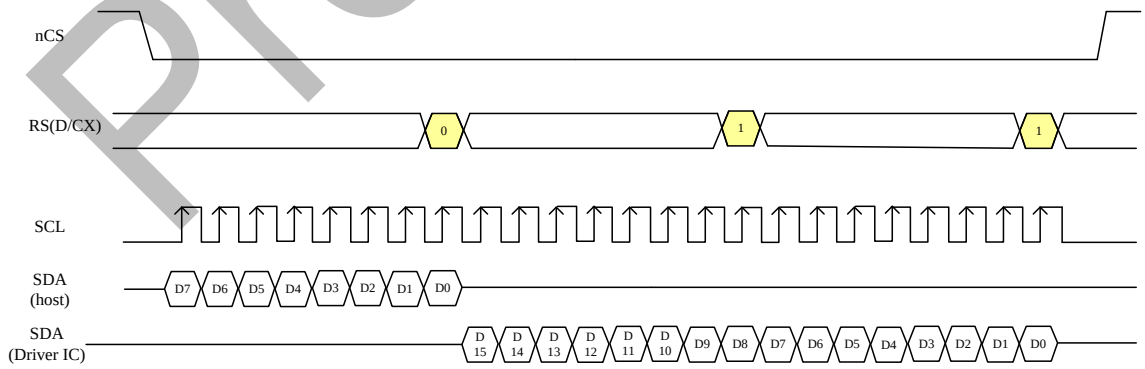
Serial data must be input to SDA in the sequence D7 to D0. The GC9203 reads the data at the rising edge of SCL signal. The D/CX signal indicates data/command. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

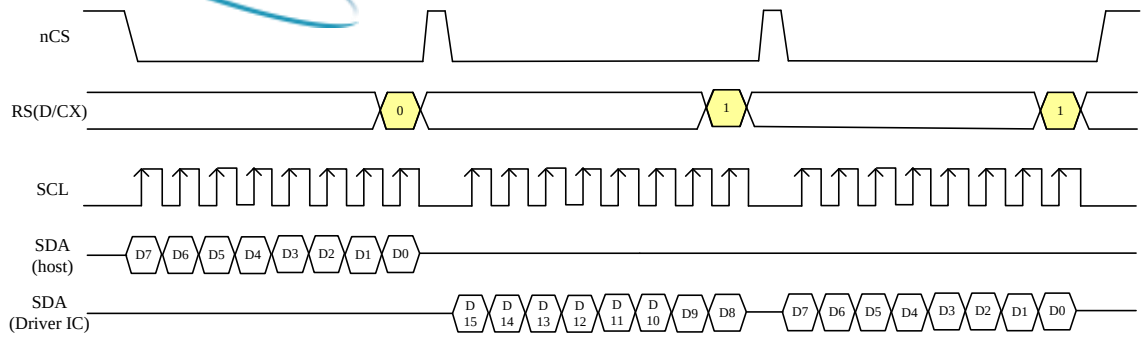
Register Write Mode :



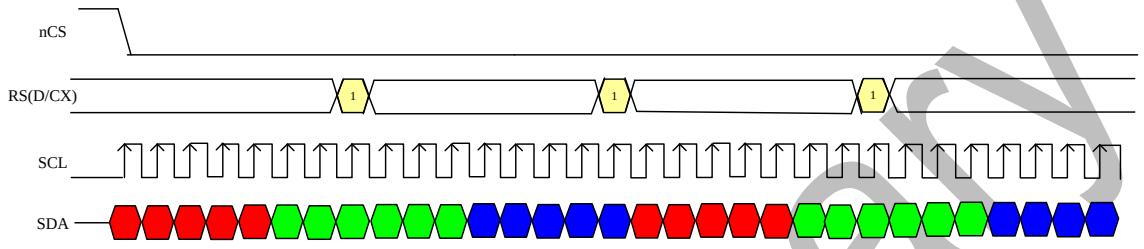
Register read Mode :

When users need to read back the register or GRAM data, the register R66h must be set as “1” first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.

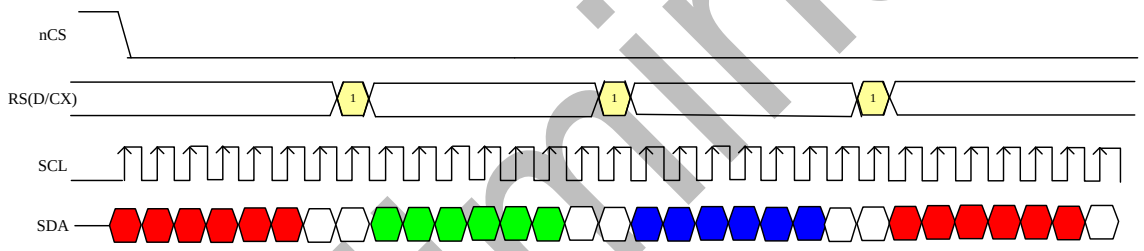




Serial Data transfer interface(65K color, MDT[1:0]=“00”)



Serial Data transfer interface(262K color, MDT[1:0]=“10”)

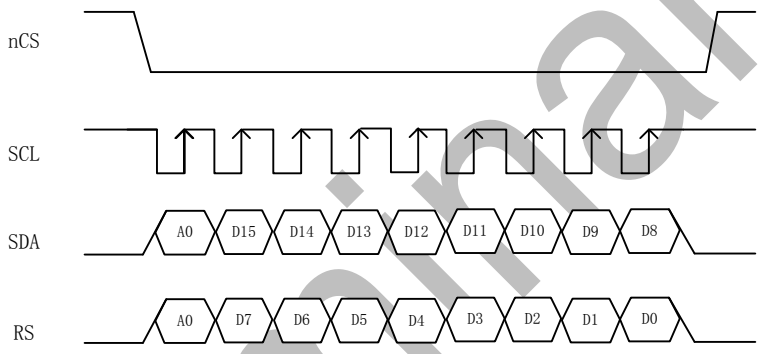


5.3.4. 2-data-line mode

This mode is active when 2data_en (R05H[3]) set to “1” in 3-wire 9bit SPI. Only frame pixel data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire 9bit SPI.

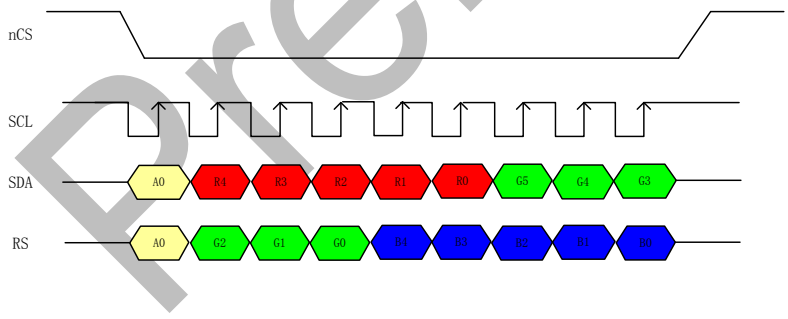
The chip-select CSX (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and RS are serial data lines.

Serial data must be input to SDA in the sequence A0, D15 to D10 and RS in the sequence A0, D7 to D0. The GC9203 reads the data at the rising edge of SCL signal. The first bit of serial data A0 is data/command flag. It must be set to "1", D15 to D0 bits are display RAM data.

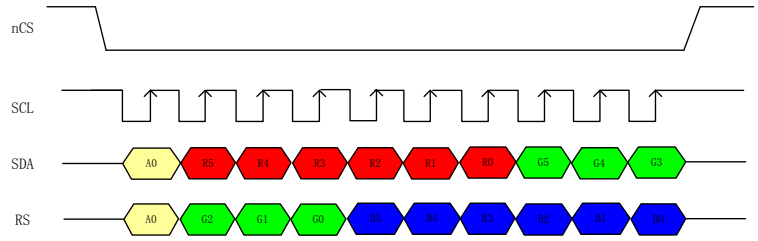


Five data formats are supported in 2-data-line mode, which is indicated by 2data_mdt (R05H[2:0]) .

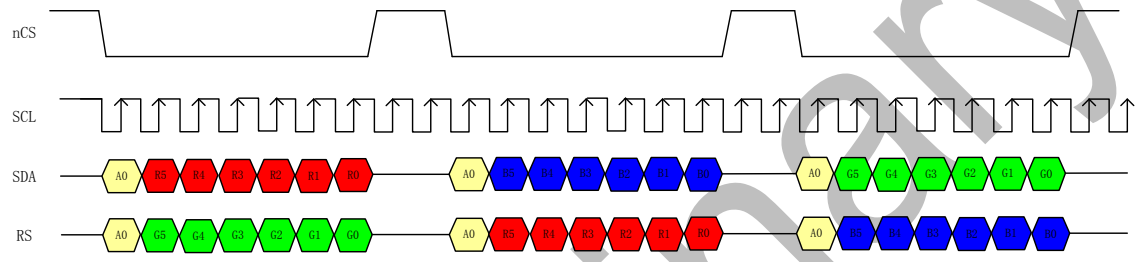
RGB565 1pixle/transition (65K color, 2data_mdt[2:0]=“000”)



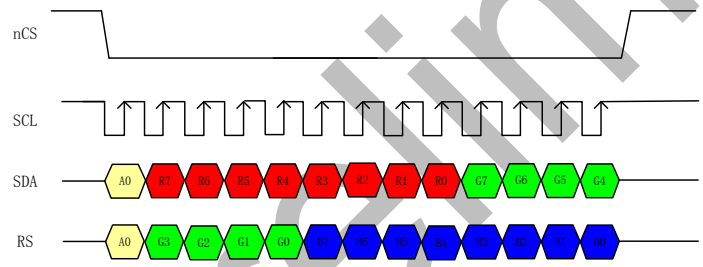
RGB666 1pixle/transition (262K color, 2data_mdt[2:0]=“001”)



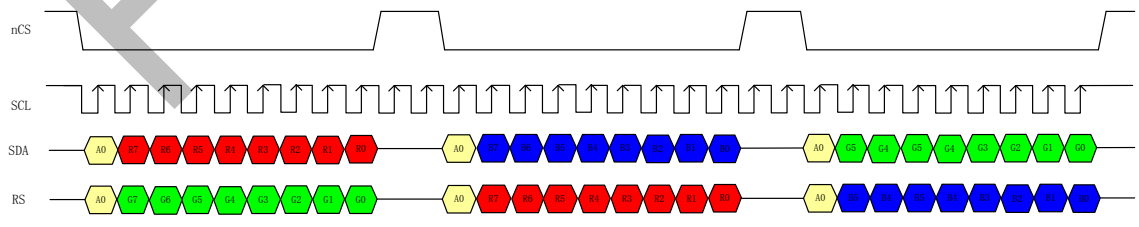
RGB666　2/3pixle/transition (262K color, 2data_mdt[2:0]=“010”)



RGB888 1pixle/transition (4M color, 2data_mdt[2:0]=“100”)

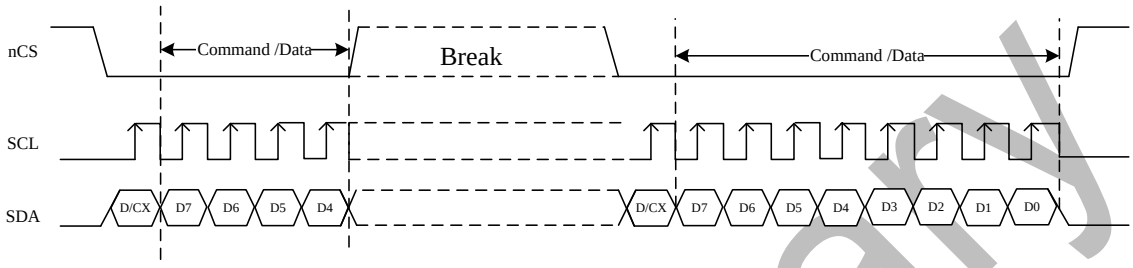


RGB888 2/3pixle/transition (4M color, 2data_mdt[2:0]=“110”)



5.3.5. Data Transfer Recovery

If there is a break in data transmission while transferring a command or GRAM data or multiple register data, before Bit D0 of the byte has been completed, then the GC9203 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte retransmitted when the chip select line (CSX) is next activated. See the following example:



If the 2 parameter of command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as show below.
Note: Break can be e.g. another command or noise pulse.

5.4. RGB Input Interface

The RGB Interface mode is available for GC9203 and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB Pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

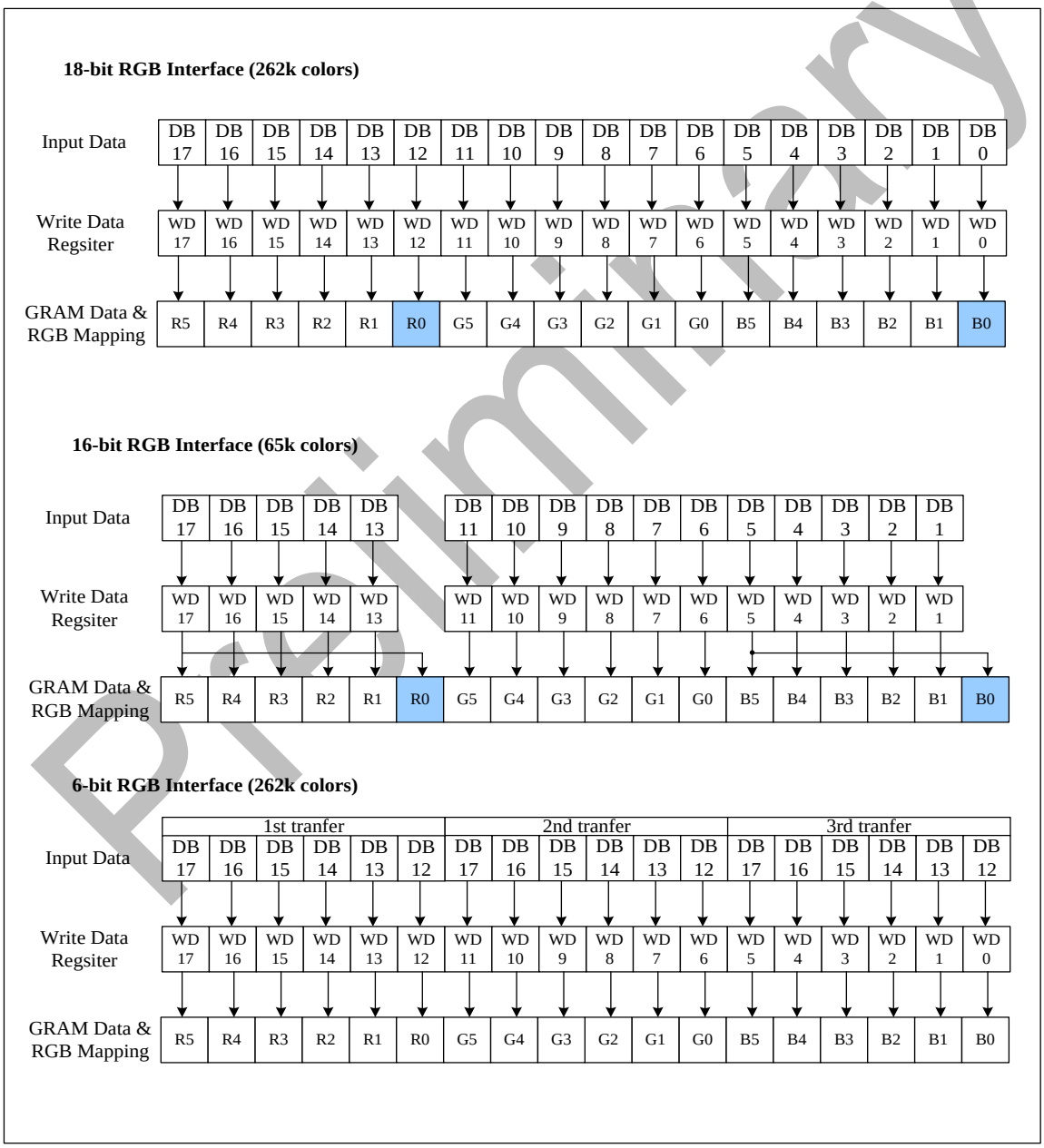


Figure12 RGB Interface Data Format

5.4.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM with the high-speed write function and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

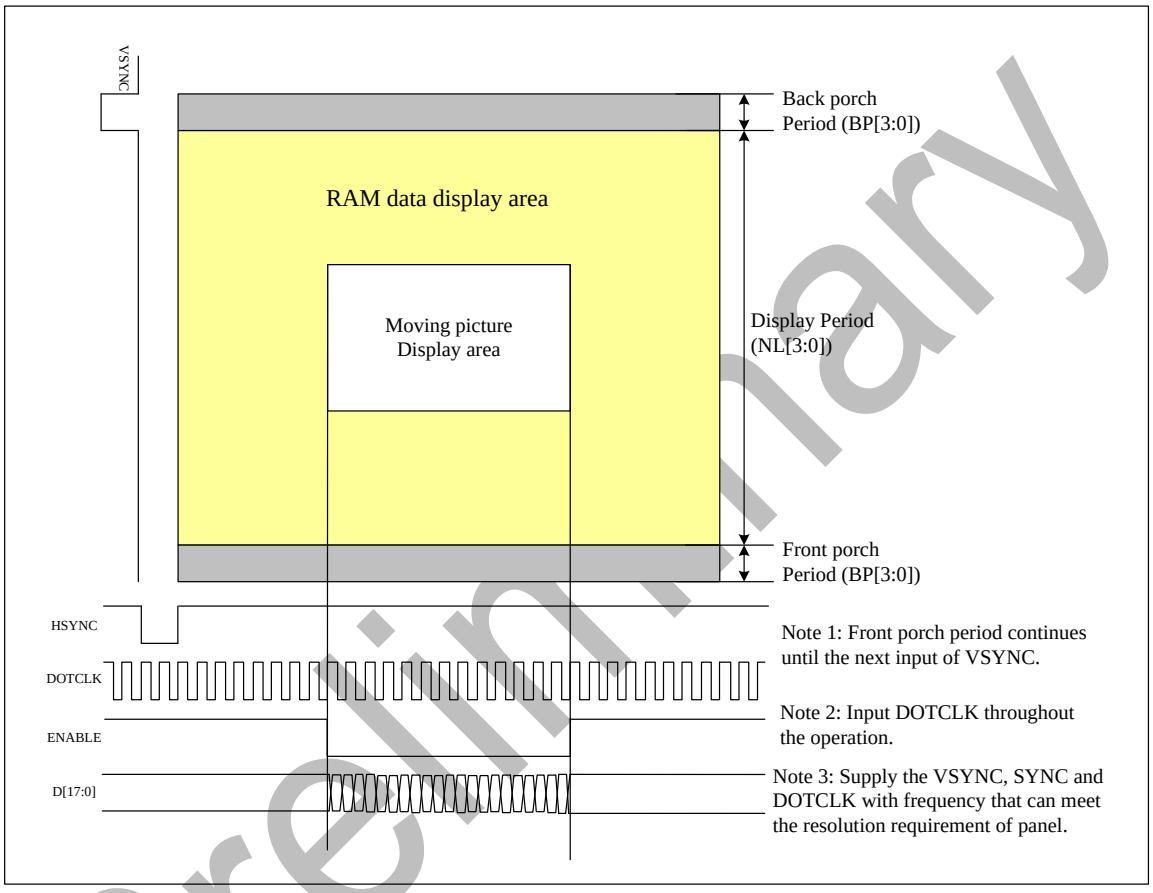


Figure13 GRAM Access Area by RGB Interface

5.4.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.

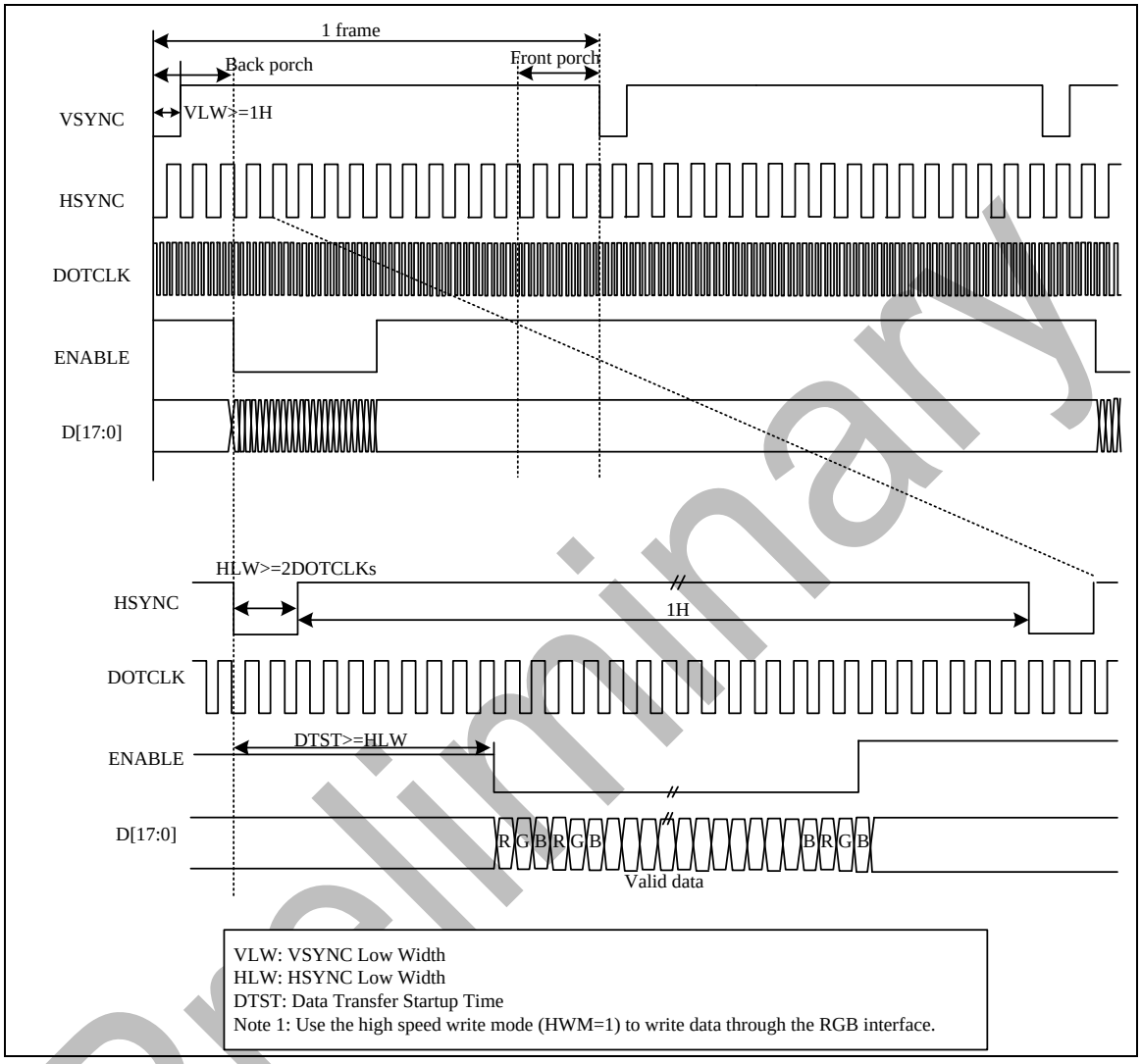
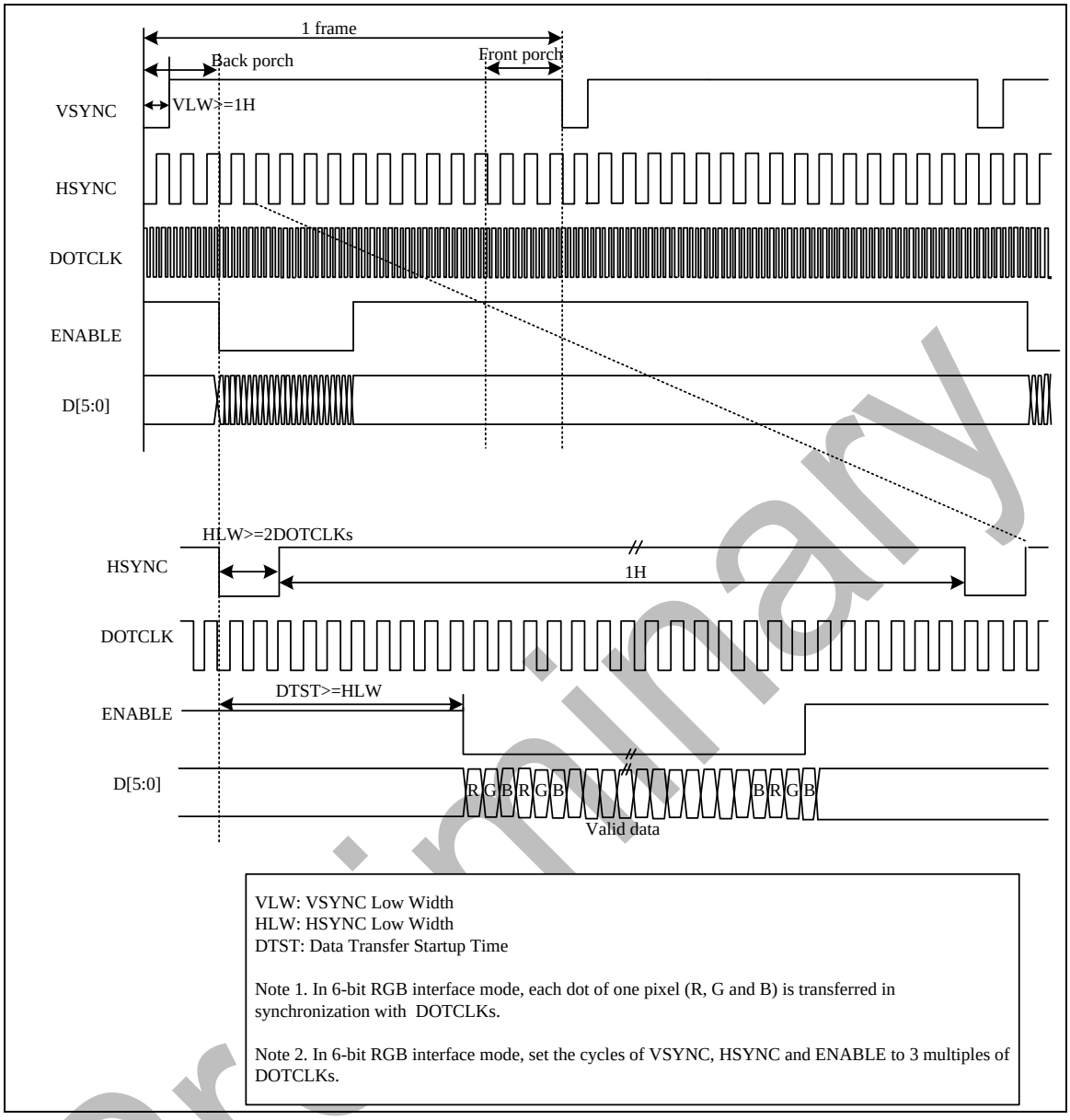


Figure14 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as below:



VLW: VSYNC Low Width
HLW: HSYNC Low Width
DTST: Data Transfer Startup Time

Note 1. In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLKs.

Note 2. In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and ENABLE to 3 multiples of DOTCLKs.

5.4.3. Moving Picture Mode

GC9203 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

GC9203 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the GC9203 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

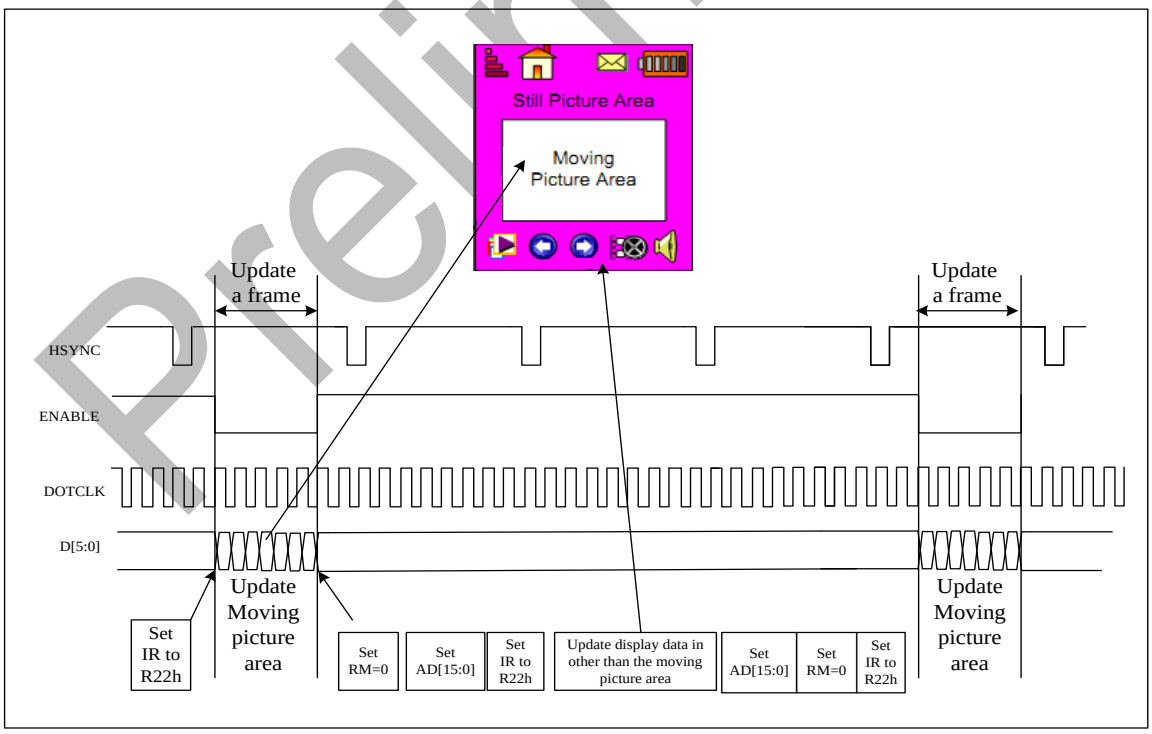
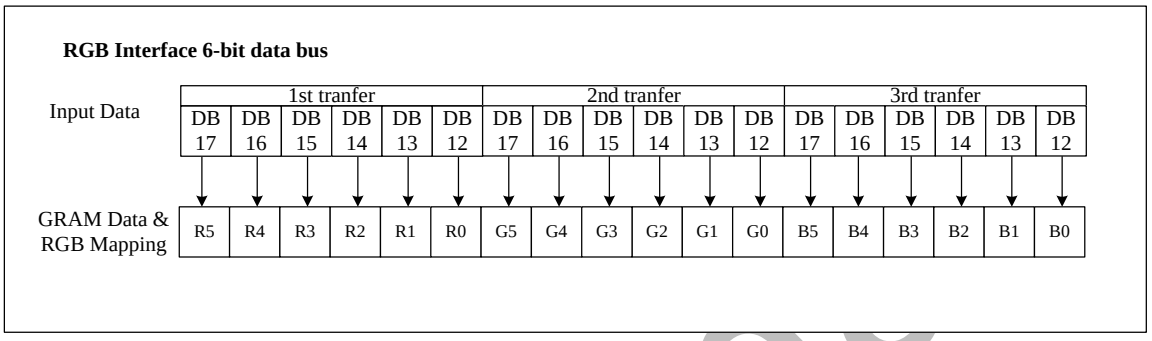


Figure14 Example of update the still and moving picture

5.4.4. 6-bit RGB Interface

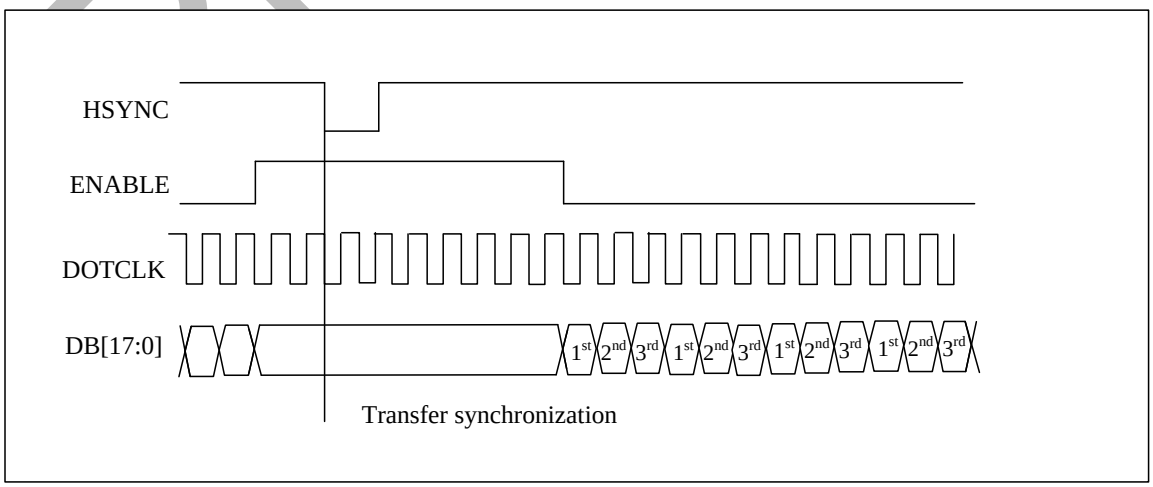
The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at ground. Registers can be set by the system interface (i80/M68/SPI).



Data transfer synchronization in 6-bit RGB interface mode

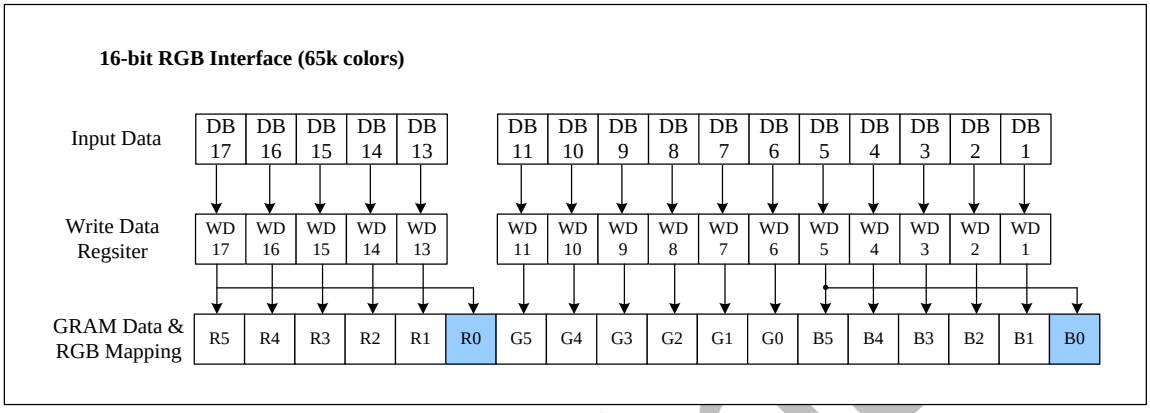
GC9203 has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



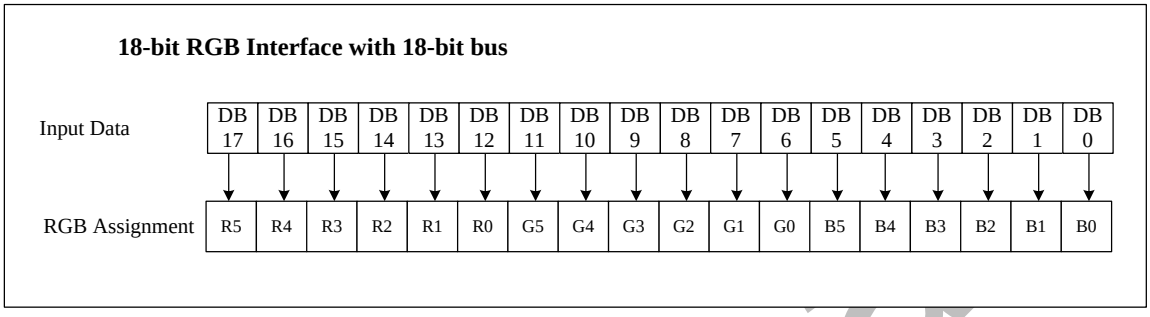
5.4.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.



5.4.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

function	RGB interface	I80/M68 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, and ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

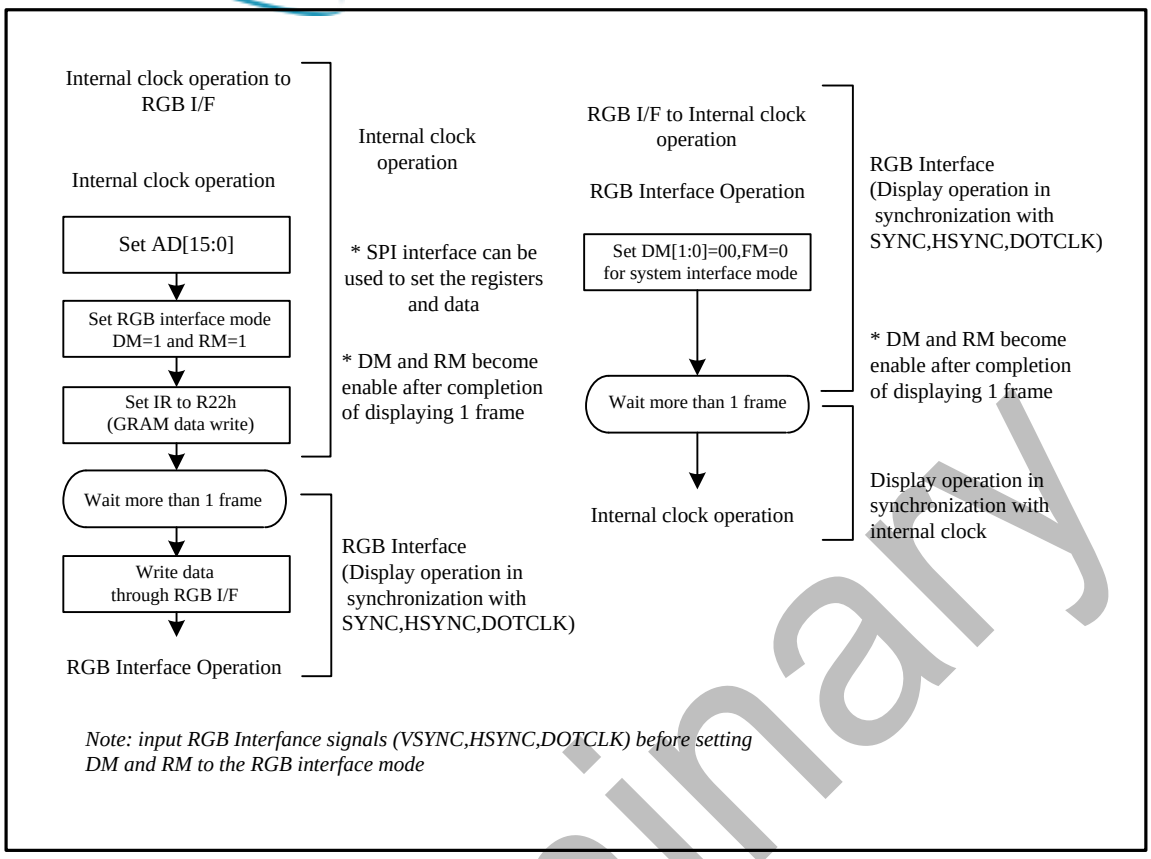


Figure15 Internal clock operation/RGB interface mode switching

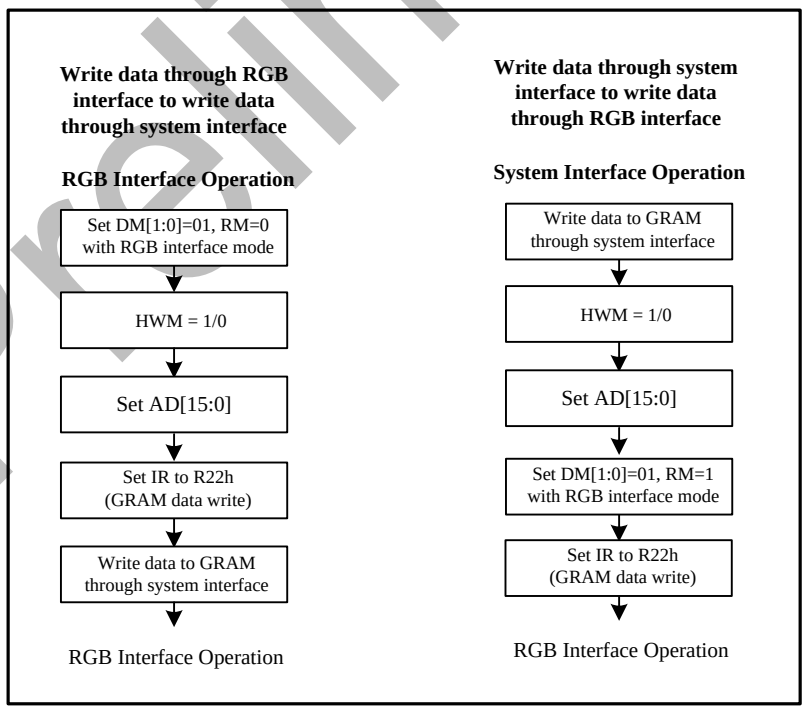


Figure16 GRAM access between system interface and RGB interface

5.4.7. RGB Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.

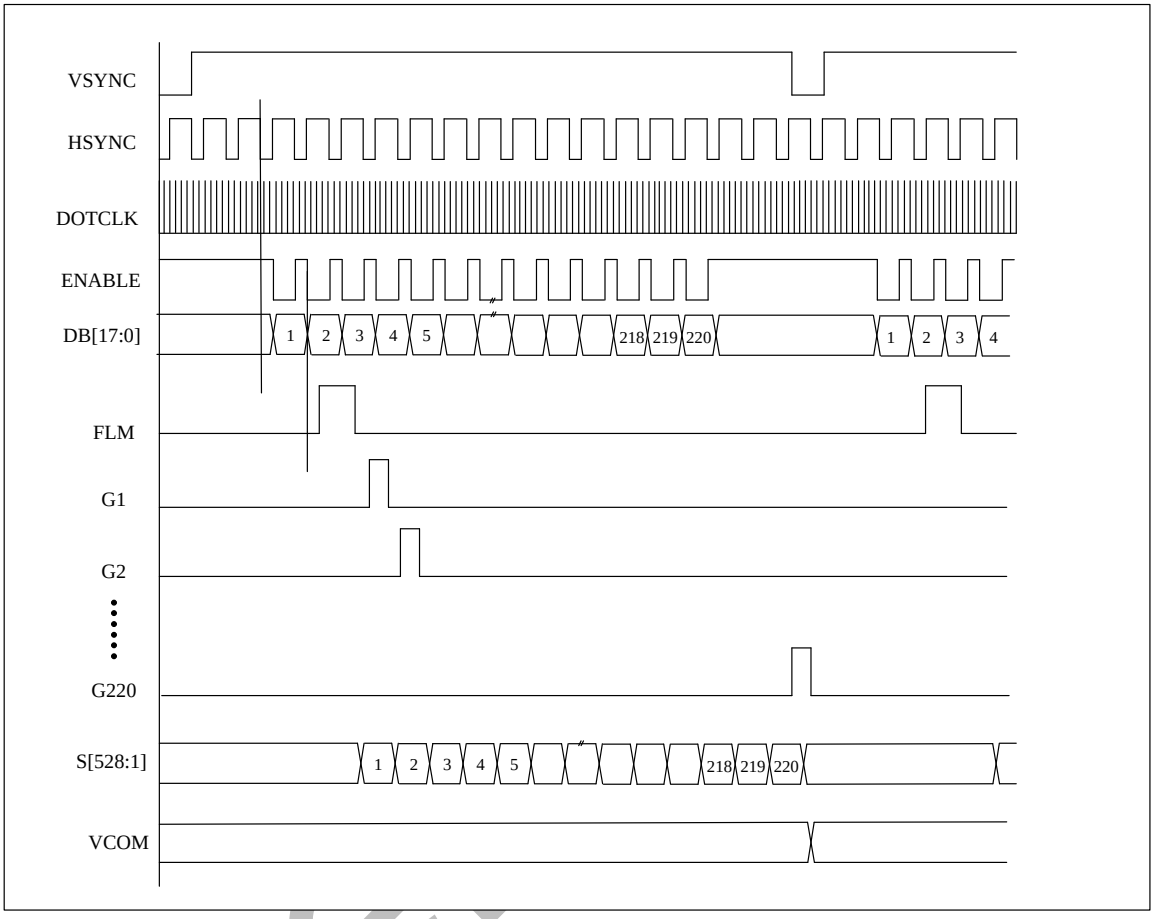


Figure17 Relationship between RGB I/F signals and LCD Driving Signals for Panel

6. Register Descriptions

6.1. Registers Access

GC9203 adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of GC9203 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (RDX/WRX) and data bus D17-0 are used to read/write the instructions and data of GC9203. The registers of the GC9203 are categorized into the following groups.

1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address (AC)
7. Transfer data to/from the internal GRAM (R22)
8. Internal grayscale γ-correction (R50 ~ R5D)

Normally, the display data (GRAM) is most often updated, and in order since the GC9203 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

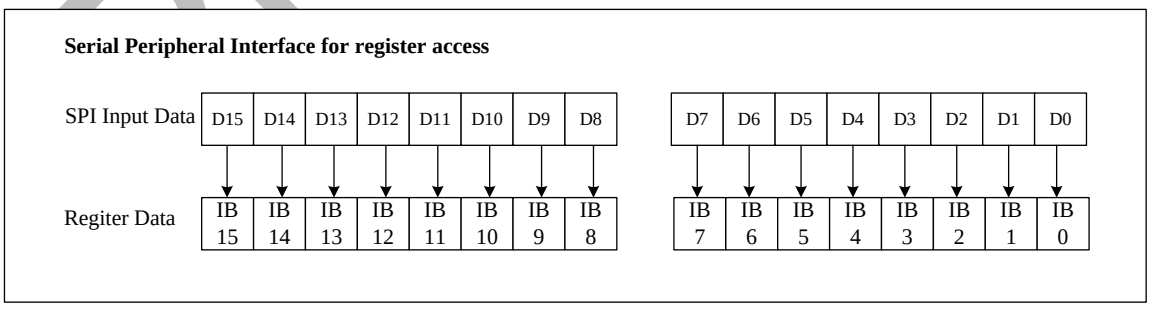
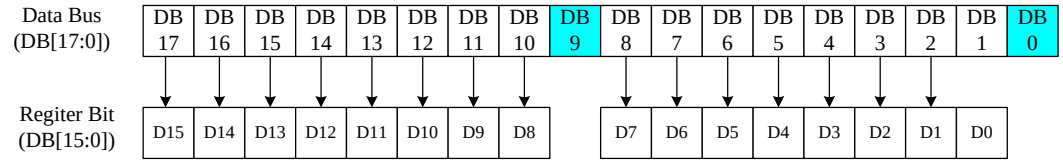
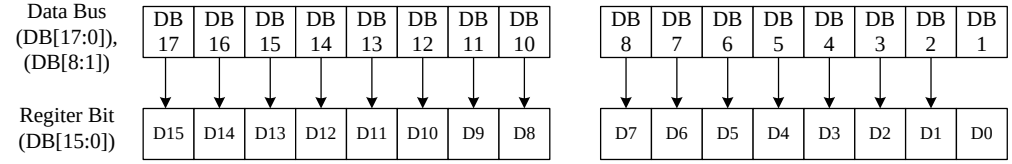


Figure18 Register Setting with Serial Peripheral Interface (SPI)

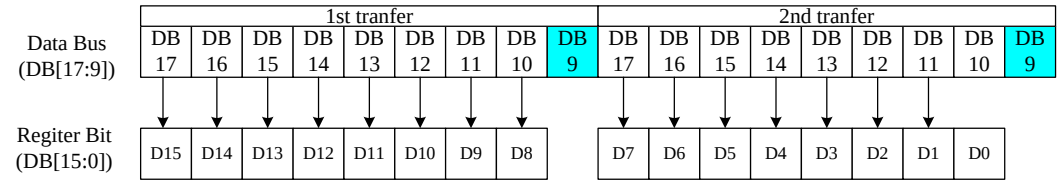
I80/M68 system 18-bit data bus interface



I80/M68 system 16-bit data bus interface



I80/M68 system 9-bit data bus interface



I80/M68 system 8-bit data bus interface/Serial peripheral interface (2/3 transmission)

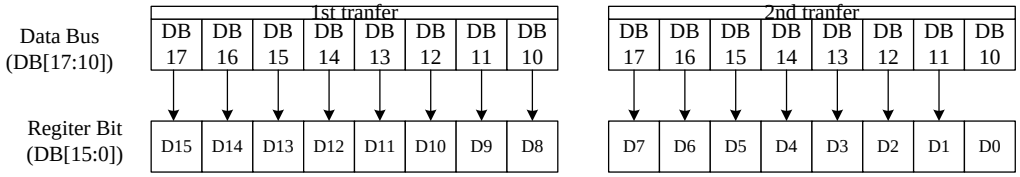
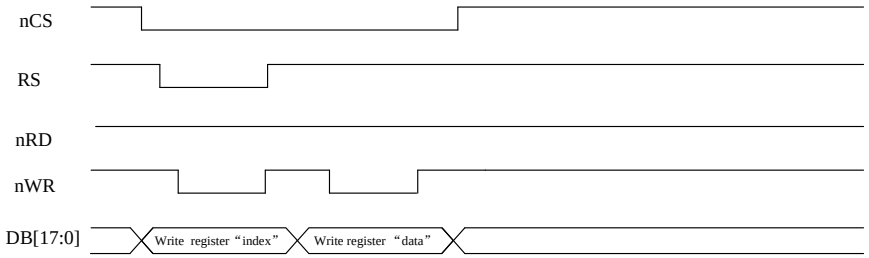


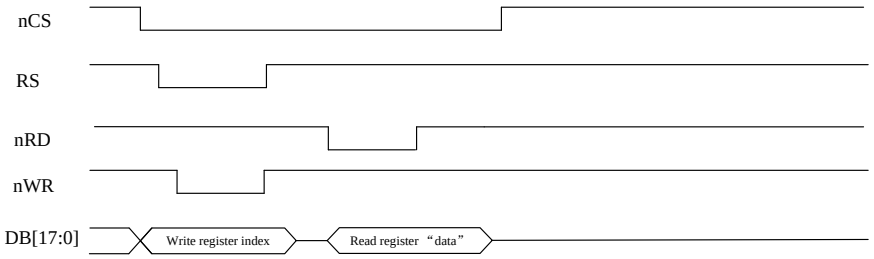
Figure19 Register setting with i80/M68 System Interface

i80 18-/16-bit System Bus Interface Timing

(a) Write to register

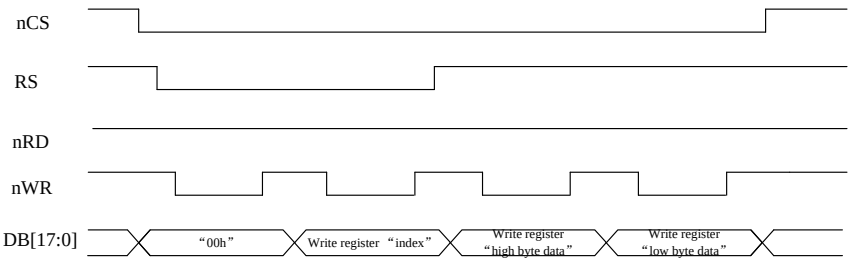


(b) Read from register



i80 9-/8-bit System Bus Interface Timing

(a) Write to register



(b) Read from regisster

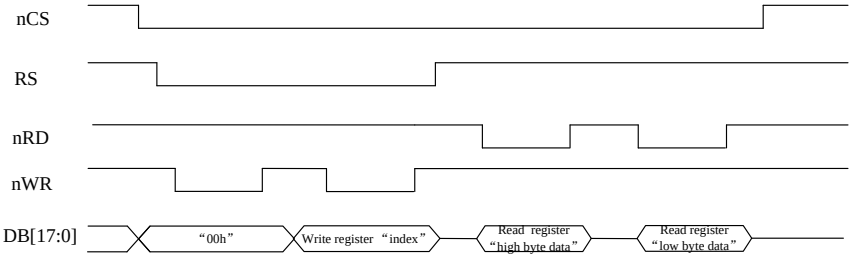
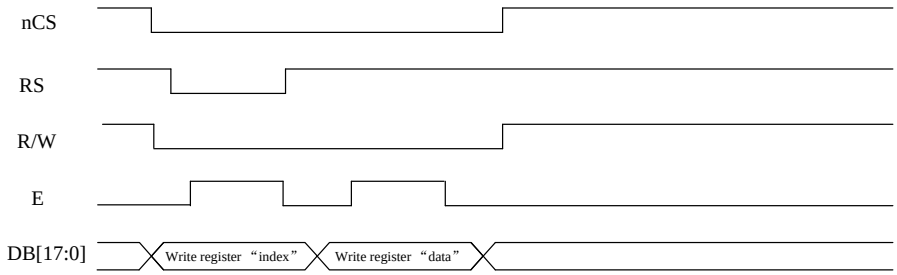


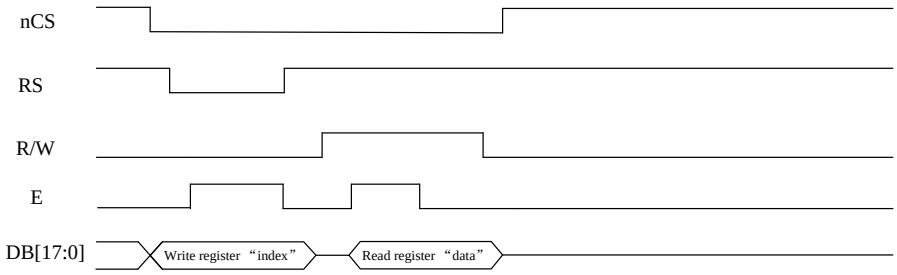
Figure20 Register Read/Write Timing of i80 System Interface

m68 18-/16-bit system Bus Interface Timing

(a) Write to register

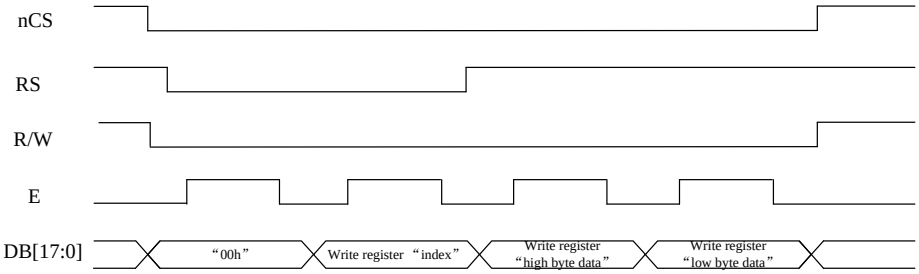


(b) Read from register



m68 9-/8-bit system Bus Interface Timing

(a) Write to register



(b) Read from register

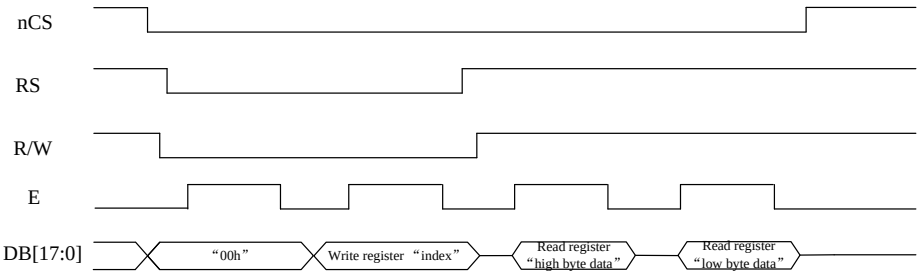


Figure21 Register Read/Write Timing of M68 System Interface

6.2. Instruction Description

ADDR	Register Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	0	0	0	0	0	0	0	0	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
00h	Driver Code Read	R	1	1	0	0	1	0	**0**	1	0	0	0	0	0	0	0	1	1
01h	Driver Output Control	W	1	VSPL 0	HSPL 0	DPL 0	EPL 0	0	SM 0	GS 0	SS 0	0	0	0	NL4 1	NL3 1	NL2 1	NL1 0	NL0 0
02h	LCD AC Driving Control	W	1	0	0	0	0	0	INV2 0	INV1 0	INV0 1	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	0	0	0	BGR 0	0	0	MDT1 0	MDT0 0	0	0	ID1 1	ID0 1	AM 0	0	0	0
05h	SPI_2DATA	W	1	0	0	0	0	0	0	0	0	0	0	0	0	2DATA_EN 0	2DATA_MDT2 0	2DATA_MDT1 0	2DATA_MDT0 0
07h	Display Control 1	W	1	0	0	0	TEMON 0	TM 0	0	0	0	0	0	0	GON 0	CL 0	REV 0	D1 0	D0 0
08h	Blank Period Control	W	1	0	0	0	0	FP3 1	FP2 0	FP1 0	FP0 0	0	0	0	0	BP3 1	BP2 0	BP1 0	BP0 0
0Ch	Interface Control	W	1	0	0	0	0	0	0	0	RM 0	0	0	0	DM 0	0	0	RIM1 0	RIM0 0
0Fh	Oscillation Control	W	1	0	0	0	0	FOSC3 0	FOSC2 1	FOSC1 1	FOSC0 1	0	0	0	0	0	0	0	OSC_ON 1
10h	Power Control 1	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB 0
11h	Power Control 2	W	1	0	0	0	APON 0	0	0	0	0	0	0	0	0	0	0	0	0
22h	Write Data to GRAM	W	1																

30h	Gate Scan Control	W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4 0	SCN3 0	SCN2 0	SCN1 0	SCN0 0
31h	Vertical Scroll Control 1	W	1	0	0	0	0	0	0	0	0	SEA7 1	SEA6 1	SEA5 0	SEA4 1	SEA3 1	SEA2 0	SEA1 1	SEA0 1
32h	Vertical Scroll Control 2	W	1	0	0	0	0	0	0	0	0	SSA7 0	SSA6 0	SSA5 0	SSA4 0	SSA3 0	SSA2 0	SSA1 0	SSA0 0
33h	Vertical Scroll Control 3	W	1	0	0	0	0	0	0	0	0	SST7 0	SST6 0	SST5 0	SST4 0	SST3 0	SST2 0	SST1 0	SST0 0
34h	Partial Driving Position -1	W	1	0	0	0	0	0	0	0	0	SE17 1	SE16 1	SE15 0	SE14 1	SE13 1	SE12 0	SE11 1	SE10 1
35h	Partial Driving Position -2	W	1	0	0	0	0	0	0	0	0	SS17 0	SS16 0	SS15 0	SS14 0	SS13 0	SS12 0	SS11 0	SS10 0
36h	WIN_HOR_ED_ADDR	W	1	0	0	0	0	0	0	0	0	HEA7 1	HEA6 0	HEA5 1	HEA4 0	HEA3 1	HEA2 1	HEA1 1	HEA0 1
37h	WIN_HOR_ST_ADDR	W	1	0	0	0	0	0	0	0	0	HSA7 0	HSA6 0	HSA5 0	HSA4 0	HSA3 0	HSA2 0	HSA1 0	HSA0 0
38h	WIN_VER_ED_ADDR	W	1	0	0	0	0	0	0	0	0	VEA7 1	VEA6 1	VEA5 0	VEA4 1	VEA3 1	VEA2 0	VEA1 1	VEA0 1
39h	WIN_VER_ST_ADDR	W	1	0	0	0	0	0	0	0	0	VSA7 0	VSA6 0	VSA5 0	VSA4 0	VSA3 0	VSA2 0	VSA1 0	VSA0 0
44h	Scan Line Set	W	1	0	0	0	0	0	0	0	0	SLS7 0	SLS6 0	SLS5 0	SLS4 0	SLS3 0	SLS2 0	SLS1 0	SLS0 0
Internal Register Below																			
50h	Gamma Control 1	W	1	VR63N3 1	VR63N2 1	VR63N1 0	VR63N0 1	VR50N3 1	VR50N2 1	VR50N1 0	VR50N0 0	J0N1 1	J0N0 0	J1N1 0	J1N0 0	VR0N3 0	VR0N2 0	VR0N1 0	VR0N0 0
51h	Gamma Control 2	W	1	0	0	VR2N5 0	VR2N4 0	VR2N3 0	VR2N2 0	VR2N1 1	VR2N0 1	0	0	VR1N5 0	VR1N4 0	VR1N3 0	VR1N2 0	VR1N1 0	VR1N0 0
52h	Gamma Control 3	W	1	0	0	0	VR6N4 0	VR6N3 0	VR6N2 1	VR6N1 1	VR6N0 0	0	0	0	VR4N3 0	VR13N3 1	VR4N2 0	VR4N1 0	VR4N0 0
53h	Gamma Control 4	W	1	0	VR20N6 0	VR20N5 1	VR20N4 0	VR20N3 1	VR20N2 0	VR20N1 1	VR20N0 1	0	0	0	0	VR13N3 0	VR13N2 1	VR13N1 0	VR13N0 1

54h	Gamma Control 5	W	1	0	VR43N6 1	VR43N5 0	VR43N4 0	VR43N3 0	VR43N2 0	VR43N1 0	VR43N0 1	0	0	VR36N2 1	VR36N1 0	VR36N0 0	VR27N2 1	VR27N1 0	VR27N0 0
55h	Gamma Control 6	W	1	0	0	0	VR59N4 1	VR59N3 1	VR59N2 0	VR59N1 0	VR59N0 0	0	0	0	VR57N4 1	VR57N3 0	VR57N2 1	VR57N1 1	VR57N0 1
56h	Gamma Control 7	W	1	0	0	VR62N5 0	VR62N4 1	VR62N3 0	VR62N2 1	VR62N1 1	VR62N0 1	0	0	VR61N5 0	VR61N4 1	VR61N3 0	VR61N2 0	VR61N1 1	VR61N0 1
57h	Gamma Control 8	W	1	VR63P3 1	VR63P2 1	VR63P1 0	VR63P0 1	VR50P3 1	VR50P2 1	VR50P1 0	VR50P0 0	J0P1 0	J0P0 1	J1P1 0	J1P0 0	VR0P3 0	VR0P2 0	VR0P1 0	VR0P0 0
58h	Gamma Control 9	W	1	0	0	VR2P5 0	VR2P4 0	VR2P3 0	VR2P2 0	VR2P1 1	VR2P0 1	0	0	VR1P5 0	VR1P4 0	VR1P3 0	VR1P2 0	VR1P1 0	VR1P0 0
59h	Gamma Control 10	W	1	0	0	0	VR6P4 0	VR6P3 1	VR6P2 1	VR6P1 0	VR6P0 1	0	0	0	VR4P3 0	VR13P3 1	VR4P2 0	VR4P1 0	VR4P0 0
5Ah	Gamma Control 11	W	1	0	VR20P6 0	VR20P5 1	VR20P4 0	VR20P3 1	VR20P2 1	VR20P1 1	VR20P0 0	0	0	0	0	VR13P3 1	VR13P2 0	VR13P1 0	VR13P0 0
5Bh	Gamma Control 12	W	1	0	VR43P6 0	VR43P5 1	VR43P4 1	VR43P3 1	VR43P2 1	VR43P1 1	VR43P0 1	0	0	VR36P2 1	VR36P1 0	VR36P0 1	VR27P2 1	VR27P1 0	VR27P0 0
5Ch	Gamma Control 13	W	1	0	0	0	VR59P4 1	VR59P3 0	VR59P2 1	VR59P1 0	VR59P0 0	0	0	0	VR57P4 1	VR57P3 1	VR57P2 0	VR57P1 0	VR57P0 0
5Dh	Gamma Control 14	W	1	0	0	VR62P5 0	VR62P4 1	VR62P3 1	VR62P2 0	VR62P1 0	VR62P0 0	0	0	VR61P5 0	VR61P4 1	VR61P3 0	VR61P2 1	VR61P1 0	VR61P0 0
E2h	CHP-CTRL1	W	1	AVEE_CLK_AD1 0	AVEE_CLK_AD0 1	0	0	1	0	1	1	AVDD_CLK_AD1 0	AVDD_CLK_AD0 1	0	0	1	0	1	1
E3h	CHP-CTRL2	W	1	1	0	0	VGL_BT 0	VGL_CLK_AD3 1	VGL_CLK_AD2 0	VGL_CLK_AD1 0	VGL_CLK_AD0 0	1	0	0	VGH_BT 0	VGH_CLK_AD3 1	VGH_CLK_AD2 0	VGH_CLK_AD1 1	VGH_CLK_AD0 0
E4h	CHP-CTRL3	W	1	0	0	0	1	VDH_CLK_AD3 1	VDH_CLK_AD2 0	VDH_CLK_AD1 0	VDH_CLK_AD0 0	0	0	0	1	VCL_CLK_AD3 0	VCL_CLK_AD2 1	VCL_CLK_AD1 0	VCL_CLK_AD0 1
E5h	CHP-CTR	W	1	0	0	0	1	0	1	0	0	1	0	0	0	0	SOU_CL	SOU_CL	SOU_CL

	L4																K_AD2 0	K_AD1 1	K_AD0 0
EBh	VREG-CTRL1	W	1	0	0	VREG1B_AD5 1	VREG1B_AD4 0	VREG1B_AD3 0	VREG1B_AD2 1	VREG1B_AD1 0	VREG1B_AD0 1	0	0	VREG1A_AD5 1	VREG1A_AD4 0	VREG1A_AD3 1	VREG1A_AD2 0	VREG1A_AD1 1	VREG1A_AD0 0
ECh	VREG-CTRL2	W	1	0	0	VREG2B_AD5 1	VREG2B_AD4 0	VREG2B_AD3 0	VREG2B_AD2 1	VREG2B_AD1 0	VREG2B_AD0 1	0	0	VREG2A_AD5 0	VREG2A_AD4 1	VREG2A_AD3 0	VREG2A_AD2 1	VREG2A_AD1 0	VREG2A_AD0 1
EEh	CHP-CTRL5	W	1	0	AVEE_AD2 0	AVEE_AD1 1	AVEE_AD0 1	0	AVDD_AD2 0	AVDD_AD1 1	AVDD_AD0 1	1	0	0	1	1	0	1	1
EFh	CHP-CTRL6	W	1	0	0	VGL_AD2 1	VGL_AD1 0	VGL_AD0 0	VGH_AD2 0	VGH_AD1 1	VGLH_AD0 0	0	BVEE_AD2 1	BVEE_AD1 0	BVEE_AD0 1	0	BVDD_AD2 0	BVDD_AD1 1	BVDD_AD0 0
FEh	INTER_REG_DIS	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FFh	INTER_REG_EN	W	1	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1

6.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	0	0	0	0	0	0	0	0	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0

The index register specifies the address of register (R00h ~ RFFh) or RAM which will be accessed.

6.2.2. Device ID Code Read (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	1	1

The device code “9203h” is read out when read this register.

6.2.3. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	VSPL	HSPL	DPL	EPL	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

VSPL: Inverts the polarity of signals from the VSYNC pin.
VSPL = ”0” : Low active.
VSPL = ”1” : High active.

HSPL: Inverts the polarity of signals from the HSYNC pin.
HSPL = ”0” : Low active.
HSPL = ”1” : High active.

DPL: Inverts the polarity of signals from the DOTCLK pin.
DPL = ”0” : Data are read on the rising edge of the DOTCLK.
DPL = ”1” : Data are read on the falling edge of the DOTCLK.

EPL: Set the polarity of the signal from the ENABLE pin in RGB interface mode.
EPL = “0”:
ENABLE = “Low” / Write data to DB[17:0]
ENABLE = “High” / Inhibit data write operation
EPL =”1”:
ENABLE = “High” / Write data to DB[17:0]
ENABLE = “Low” / Inhibit data write operation

The following table shows the relationship between the EPL, ENABLE bits, and RAM access

EPL	ENABLE	RAM write	RAM address
0	0	Enable	Updated
0	1	Inhibited	Retained
1	0	Inhibited	Retained
1	1	Enable	Updated

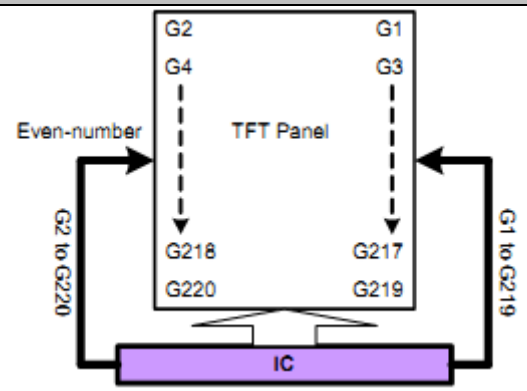
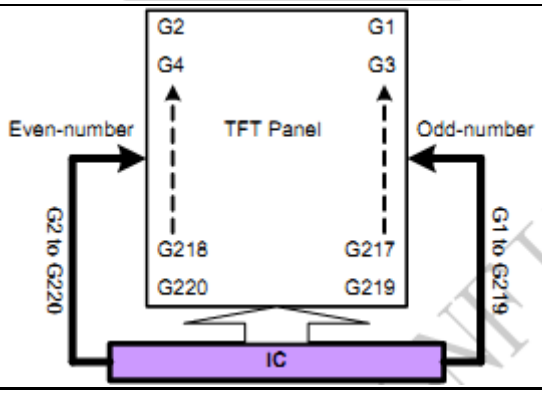
SS: Select the shift direction of outputs from the source driver.
When SS = 0, the shift direction of outputs is from S1 to S528
When SS = 1, the shift direction of outputs is from S528 to S1.

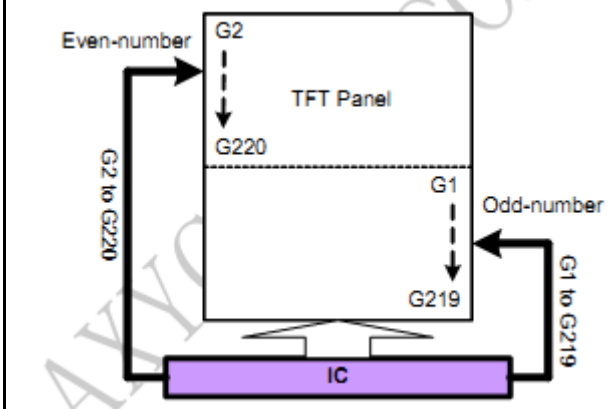
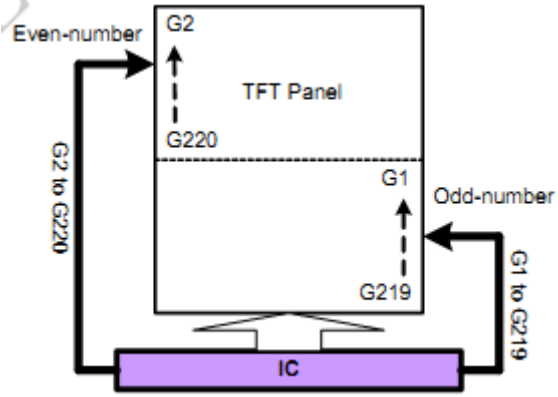
In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.
To assign R, G, B dots to the source driver pins interchangeably from S1, set SS = 0, BGR = 0.
To assign R, G, B dots to the source driver pins interchangeably from S528, set SS = 1, BGR = 1.

When changing SS or BGR bits, RAM data must be rewritten.

GS: Select the shift direction of outputs from the gate driver. The scan order is changeable in accordance to the scan mode by the gate driver. Select an optimum shift direction for the assembly.

SM: Set the scan order by the gate driver. Select an optimum scan order for the assembly

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1, G2, G3, G4 ,…,G216, G217,G218, G219, G220
0	1		G220, G219, G218, … G6, G5, G4, G3, G2, G1

1	0		G1, G3, G5, G7 , … , G211 G213, G215,G217,G219 G2, G4, G6, G8, …, G212 G214, G216, G218, G220
1	1		G220, G318, G216, …, G10, G8, G6, G4, G2 G219, G217, G215, …, G9, G7, G5, G3, G1

NL[4:0] Set the active gate driver line to drive the liquid crystal display panel with 8 multiples as the following table. The GRAM address mapping is independent from the number of gate lines set with the NL[4:0] bits.

NL4	NL3	NL2	NL1	NL0	Display Size	Number of LCD lines	Gate driver used
0	0	0	0	0	**Reserved**		
0	0	0	0	1	528*8 dots	8	G1~G8
0	0	0	1	0	528*16 dots	16	G1~G16
0	0	0	1	1	528*24 dots	24	G1~G24
0	0	1	0	0	528*32 dots	32	G1~G32
0	0	1	0	1	528*40 dots	40	G1~G40
0	0	1	1	0	528*48 dots	48	G1~G48
0	0	1	1	1	528*56 dots	56	G1~G56
0	1	0	0	0	528*64 dots	64	G1~G64
0	1	0	0	1	528*72 dots	72	G1~G72
0	1	0	1	0	528*80 dots	80	G1~G80
0	1	0	1	1	528*88 dots	88	G1~G88
0	1	1	0	0	528*96 dots	96	G1~G96
0	1	1	0	1	528*104 dots	104	G1~G104
0	1	1	1	0	528*112 dots	112	G1~G112
0	1	1	1	1	528*120 dots	120	G1~G120
1	0	0	0	0	528*128 dots	128	G1~G128
1	0	0	0	1	528*136 dots	136	G1~G136
1	0	0	1	0	528*144 dots	144	G1~G144
1	0	0	1	1	528*152 dots	152	G1~G152
1	0	1	0	0	528*160 dots	160	G1~G160
1	0	1	0	1	528*168 dots	168	G1~G168

1	1	1	1	0	528*176 dots	176	G1~G176
1	1	1	1	1	528*184 dots	184	G1~G184
1	1	0	0	0	528*192 dots	192	G1~G192
1	1	0	0	1	528*200 dots	200	G1~G200
1	1	0	1	0	528*208 dots	208	G1~G208
1	1	0	1	1	528*216 dots	216	G1~G216
1	1	1	0	0	528*220 dots	220	G1~G220

6.2.4. LCD Driving Waveform Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	0	0	INV 2	INV 1	INV 0	0	0	0	0	0	0	0	0
DEFAULT		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Set LCD inversion method as shown below.

INV[2:0]	Description
000	Column Inversion
001	1-dot Inversion
010	2-dot Inversion
011	4-dot Inversion
100	8-dot Inversion
Other	Invalid

6.2.5. Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	BGR	0	0	MDT1	MDT 0	0	0	ID1	ID0	AM	0	0	0
DEFAULT		0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0

AM Control the GRAM update direction. When AM = "0", the address is updated in horizontal writing direction. When AM = "1", the address is updated in vertical writing direction. When a window area is set by registers R44h and R45h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

I/D[1:0] Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.

	AM = 0 Horizontal	AM = 1 Vertical

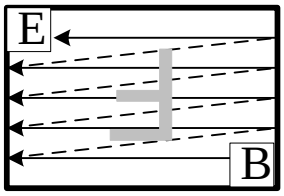
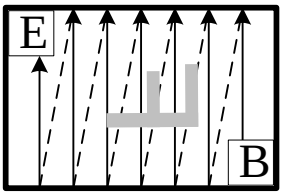
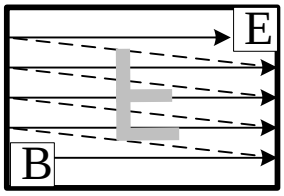
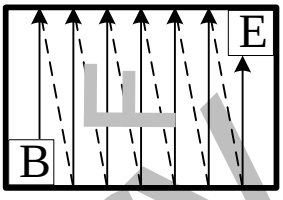
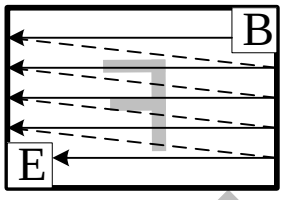
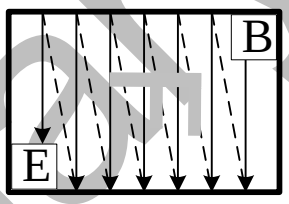
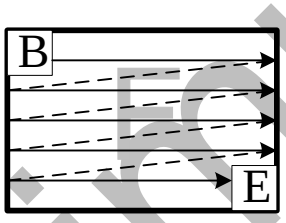
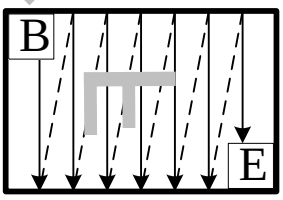
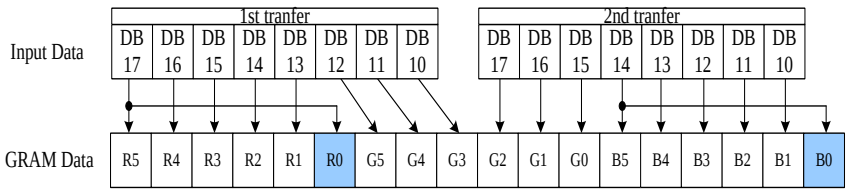
I/D[1:0] = 00 Horizontal: decrement Vertical : decrement		
I/D[1:0] = 01 Horizontal : increment Vertical : decrement		
I/D[1:0] = 10 Horizontal : decreme Vertical : increment		
I/D[1:0] = 11 Horizontal : increment Vertical : increment		

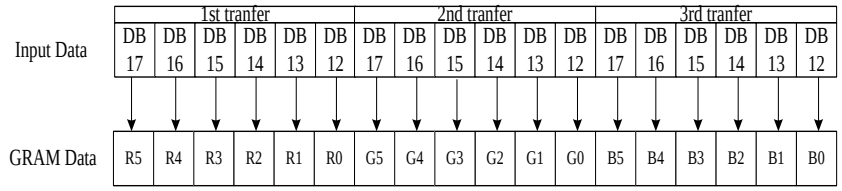
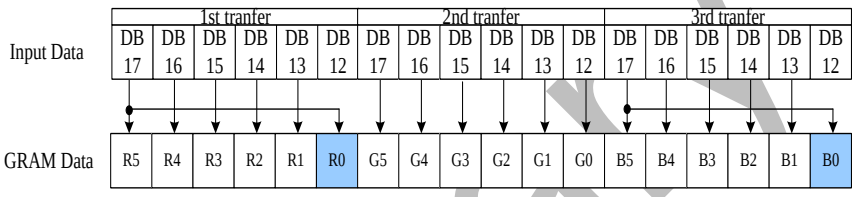
Figure25 GRAM Access Direction Setting

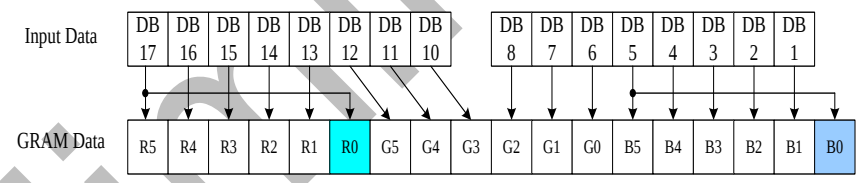
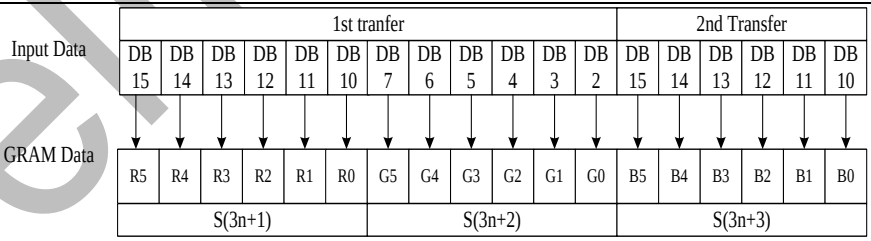
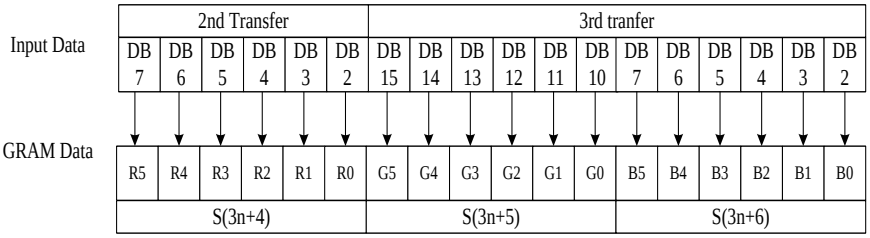
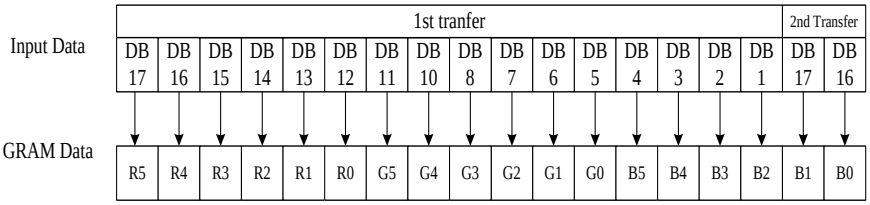
AM	I/D [1:0]	Register R20/R21 Start Address
0/1	00	DBAFh
	01	DB00h
	10	00AFh
	11	0000h

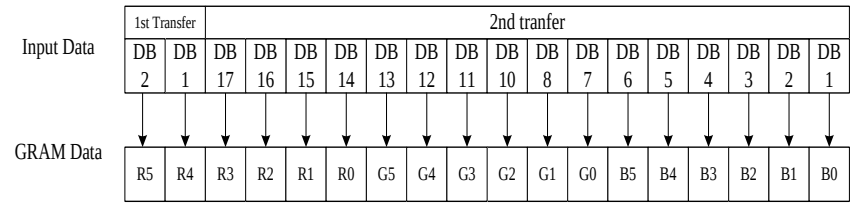
MDT[1:0]: These bits are used to set the data fromat for the 8/16-bit interface mode.

BGR Swap the R and B order of written data.

Interface	MDT[1:0]	Write Data to GRAM
8-bit Mode	00	

	01	Multiple data transfer (MDT[1:0]) function is not available.
	10	
	11	

Interface	MDT[1:0]	Write Data to GRAM
16-bit Mode	00	
	01	 
	10	

	11	

6.2.6. Spi_2data (R05h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	2DATA_EN	2DATA_MDT2	2DATA_MDT1	2DATA_MDT0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2DATA_EN Set 2_data_line mode in 3-wire SPI.

2DATA_MDT[2:0] Set pixel data format in 2_data_line mode.

2DATA_MDT[2:0]	Data Format
000	65K color 1pixle/transition
001	262K color 1pixle/transition
010	262K color 2/3pixle/transition
100	4M color 1pixle/transition
110	4M color 2/3pixle/transition

6.2.7. Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	TEMON	TM	0	0	0	0	0	0	GON	CL	REV	D1	D0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0] Set D[1:0]=”11” to turn on the display panel, and D[1:0]=”00” to turn off the display panel.

D1	D0	GON	Source Output	Gate Output	VCOM Output	Display
0	0	X	VSS	VGL	VSS	Off
0	1	0	VSS	VGL	VSS	Off
		1	VSS	Operate	VSS	Off
1	0	0	White on Normally WhitePanel Black on Normally BlackPanel	VGL	Operate	Off

		1	White on Normally WhitePanel Black on Normally BlackPanel	Operate	Operate	Off
1	1	0	Normal Display	VGL	Operate	Off
		1	Normal Display	Operate	Operate	On

Note: data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

GON Set the output level of gate driver G1 ~ G220 as follows

GON	G1~g220 Gate Output
0	VGL
1	**Normal Display**

CL When CL = "1", the 8-color display mode is selected. For details, see the "8-color Display Mode" section.

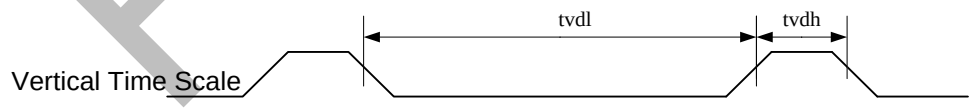
CL	Color
0	262144
1	8

REV When REV = "1", the grayscale levels can be inverted.

REV	GRAM Data	Source output in positive polarity	Display Area negative polarity
0	18'h00000	V63	V0
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V63	V0

TEMON:
TEMON = 1, Enable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.
TEMON = 0, Disable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.

When TM=0:
The Tearing Effect Output line consists of V-Blanking information only:



When TM=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

6.2.8. Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
DEFAULT		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

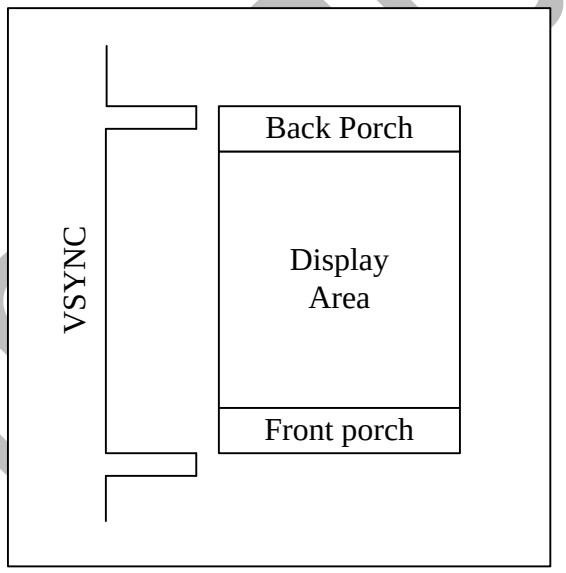
FP[3:0]/BP[3:0]

The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively When select RGB interface. When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

FP ⩾ 2 lines

BP ⩾ 2 lines

FP[3:0]	Number of lines for Front Porch
BP[3:0]	Number of lines for Back Porch
0000	Setting prohibited
0001	Setting prohibited
0010	2 lines
0011	3 lines
0100	4 lines
0101	5 lines
0110	6 lines
0111	7 lines
1000	8 lines
1001	9 lines
1010	10 lines
1011	11 lines
1100	12 lines
1101	13 lines
1110	14 lines
1111	15 lines



Note: the output timing to the LCD is delayed by 2 lines period from the input of synchronizing signal

6.2.9. RGB Input Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	RM	0	0	0	DM	0	0	RIM 1	RIM 0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0] Select the data bus width of RGB interface modes.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one transfer/pixel)
0	1	16-bit RGB interface (one transfer/pixel)
1	0	6-bit RGB interface (three transfers/pixel)
1	1	Setting disabled

DM Select the display operation mode.

DM	Display interface
0	Internal system clock
1	RGB clock

RM Select the interface to access the GRAM

RM	Interface for RAM Access
0	Internal system clock interface
1	RGB interface (when writing display data by the RGB interface.)

Display state	Operation mode	RAM Access(RM)	Display operation Mode (DM)
Still picture	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM =0)
Moving picture	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM=1)
Rewrite still picture area while RGB interface Displaying moving pictures. RGB interface (2)		System interface (RM = 0)	RGB Interface (DM=1)

Note 1) Registers are set only via the system interface or SPI interface.
Note 2) Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

6.2.10. Oscillator Control (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	FOSC3	FOSC2	FOSC1	FOSC0	0	0	0	0	0	0	0	OSC_ON
DEFAULT		0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1

FOSC[3:0]: Select the oscillation frequency of internal oscillator.

FR_SEL[3:0]	Frame Rate(HZ)	FR_SEL[3:0]	Frame Rate(HZ)
0000	32	1000	73
0001	39	1001	78
0010	44	1010	84
0011	48	1011	92
0100	54	1100	102
0101	59	1101	113
0110	63	1110	126
0111 (default)	68	1111	Setting prohibited

OSC_EN

This instruction starts the oscillator from the Halt State in the standby mode. After this instruction, Wait at least 10 ms for oscillation to stabilize before giving the next instruction.

OSC_EN	OSC Control
0	OSC. Off
1	OSC. On

6.2.11. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTB: When DSTB = 1, the GC9203 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal oscillator. Further, no external clock pulses are supplied.

Outputs	Congditions
VCOM	GND
Gate	GND
Source	GND

6.2.12. Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	APON	0	0	0	0	0	0	0	0	0	0	0	0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

APON: This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the auto booster sequence circuit is stopped. In case of APON=1, booster circuits are automatically and sequentially operated.

6.2.13. Write Data to GRAM (R22h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	GRAM DATA															

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

6.2.14. Gate Scan Control (R30h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN [4:0] The GC9203 allows specifying the gate line from which the gate driver starts scan by setting the SCN[4:0] bits.

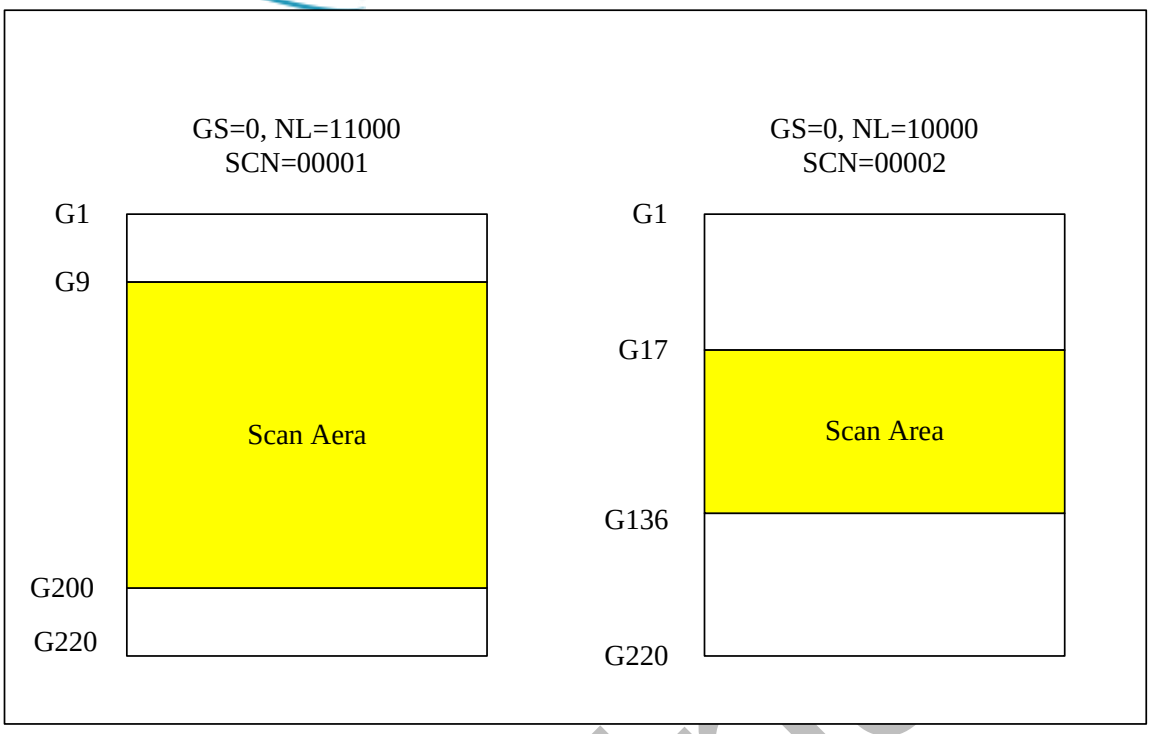


Figure28 Scanning Start Position for Gate Driver

Note: Don't set NL[4:0], SCN[4:0] over the end position of gate line (G220)

Note: Set NL[4:0] and SCN[4:0] to let the number for the end position of the gate line scans will not exceed 220.

SCN4	SCN3	SCN2	SCN1	SCN0	Scaning Start Position			
					SM=0 GS=0	SM=0 GS=1	SM=1 GS=0	SM=1 GS=1
0	0	0	0	0	G1	G220	G1	G220
0	0	0	0	1	G9	G212	G17	G204
0	0	0	1	0	G17	G204	G33	G188
0	0	0	1	1	G25	G196	G49	G172
0	0	1	0	0	G33	G188	G65	G156
0	0	1	0	1	G41	G180	G81	G140
0	0	1	1	0	G49	G172	G97	G124
0	0	1	1	1	G57	G164	G113	G108
0	1	0	0	0	G65	G156	G129	G92
0	1	0	0	1	G73	G148	G145	G76
0	1	0	1	0	G81	G140	G161	G60
0	1	0	1	1	G89	G132	G177	G44
0	1	1	0	0	G97	G124	G193	G28
0	1	1	0	1	G105	G116	G209	G12
0	1	1	1	0	G113	G108	G2	G219
0	1	1	1	1	G121	G100	G18	G203
1	0	0	0	0	G129	G92	G34	G187
1	0	0	0	1	G137	G84	G50	G171
1	0	0	1	0	G145	G76	G66	G155
1	0	0	1	1	G153	G68	G82	G139
1	0	1	0	0	G161	G60	G98	G123
1	0	1	0	1	G169	G52	G114	G107

1	0	1	1	0	G177	G44	G130	G91
1	0	1	1	1	G185	G36	G146	G75
1	1	0	0	0	G193	G28	G162	G59
1	1	0	0	1	G201	G20	G178	G43
1	1	0	1	0	G209	G12	G194	G27
1	1	0	1	1	G217	G4	G210	G11

6.2.15. Vertical Scroll Control 1 (R31h, R32h)

31h

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0
DEFAULT		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

32h

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSA[7:0]: Specify scroll start address at the scroll display for vertical smooth scrolling.

SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	Scroll Sart Line
0	0	0	0	0	0	0	0	0 lines
0	0	0	0	0	0	0	1	1 lines
0	0	0	0	0	0	1	0	2 linse
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

SEA[7:0]: Specify scroll end address at the scroll display for vertical smooth scrolling.

SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0	Scroll End Line
0	0	0	0	0	0	0	0	0 lines
0	0	0	0	0	0	0	1	1 lines
0	0	0	0	0	0	1	0	2 linse
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines

1	1	0	1	1	0	1	1	219 lines

[NOTE]
Do not set any higher raster-row than 219 (“DB”H).
Set SS17-10 ≤ SSA7-0, if set out of range, SSA7-0 = SS17-10.
Set SE17-10 ≥ SEA7-0, if set out of range, SEA7-0 = SE17-10

6.2.16. Vertical Scroll Control 1 (R33h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SST7-0: Specify scroll start and step at the scroll display for vertical smooth scrolling. Any line from the 1st to 220th can be scrolled for the number of the raster-row. After 219th line is displayed, the display restarts from the first raster-row. When SST7-0 = 00000000, Vertical Scroll Function is disabled.

SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll Lines
0	0	0	0	0	0	0	0	0 lines
0	0	0	0	0	0	0	1	1 lines
0	0	0	0	0	0	1	0	2 linse
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

[NOTE]
Do not set any higher raster-row than 219 (“DB”H)
Set SS17-10 < SSA7-0 + SST7-0 ≤ SEA7-0 ≤ SE17-10, if set out of range, Scroll function is disabled

6.2.17. Partial Screen Driving Position (R34h, R35h)

34h

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
DEFAULT		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

35h

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SE1[7:0]: Specify the driving end position for the screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For example, when SS1[7:0] = 019h and SE1[7:0] = 029h are set, the LCD driving is performed from G26 to G42, and non-display driving is performed for G1 to G25, G43, and others. Ensure that SS1[7:0] ≤ SE1[7:0] ≤ DBh.

SS1[7:0]: Specify the drive starting position for the first screen in a line unit. The LCD driving starts from the 'set value +1' gate driver.

Note: Do not set the partial setting when the operation is in the normal display condition. Set this register only when in the partial display condition.
Ex) SS1[7:0]=07h and SE1[7:0]=10h are performed from G8 to G17.

6.2.18. Horizontal and Vertical RAM Address Position (R36h/R37h, R38h/R39h)

36h

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
DEFAULT		0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1

37h

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

38h

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
DEFAULT		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

39h

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HSA[7:0]/HEA[7:0]: HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA

and HEA bits must be set before starting RAM write operation. In setting these bits, be sure “00”h ≤ HSA[7:0]< HEA[7:0] ≤ “AF”h.

VSA[7:0]/VEA[7:0] VSA[7:0] and VEA[7:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure “00”h ≤ VSA[7:0]< VEA[7:0] ≤ “DB”h.

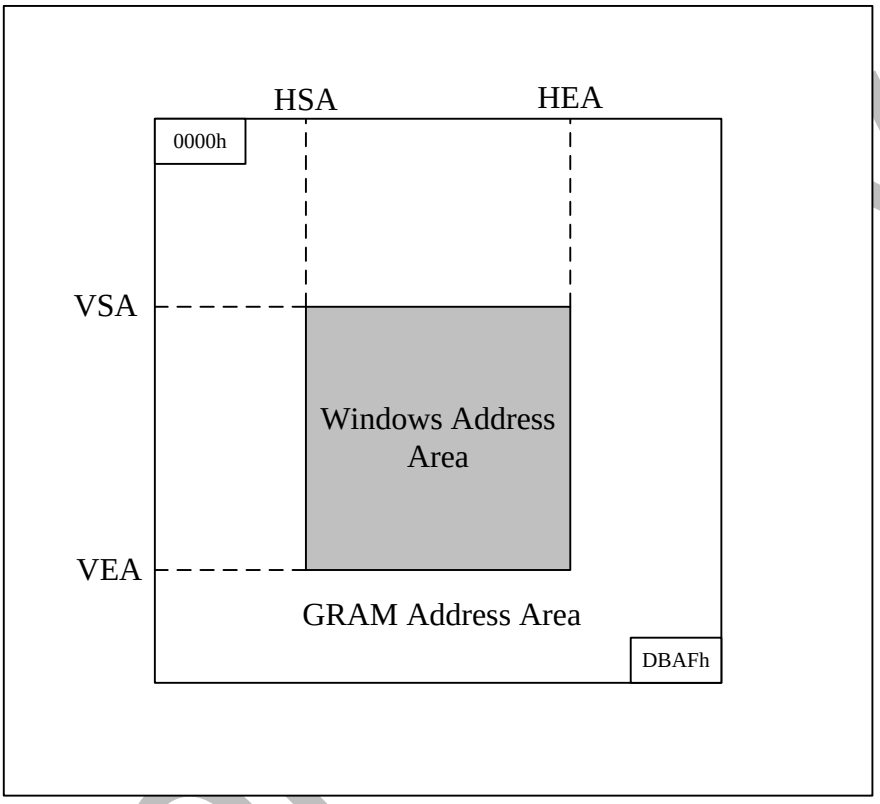


Figure29 GRAM Access Range configuration

“00”h ≤HAS[7:0] ≤HEA[7:0] ≤”AF”h
“00”h ≤VSA[7:0] ≤VEA[7:0] ≤”DB”h

Note1. The window address range must be within the GRAM address space.

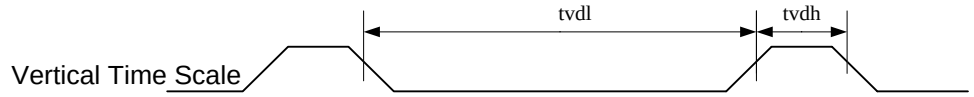
Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

6.2.19. Scan line set (R44h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	SLS 7	SLS 6	SLS 5	SLS 4	SLS 3	SLS 2	SLS 1	SLS 0
DEFAULT		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLS[7:0]: When setting the SLS[7:0] value, the following conditions shall be met: SLS[7:0]≤230

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of SLS[7:0]



Note:that set_tear_scanline with STS is equivalent to set_tear_on with 5+GateN(N=1、2、3...220)
eg:when the SLS[7:0]=6,the TE will output at the position of Gate1.
when the SLS[7:0]=7,the TE will output at the position of Gate2.
when the SLS[7:0]=8,the TE will output at the position of Gate3.
…….
The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

6.2.20. Gamma Control (R50h ~ R5Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	VR63N3	VR63N2	VR63N1	VR63N0	VR50N3	VR50N2	VR50N1	VR50N0	J0N1	J0N0	J1N1	J1N0	VR0N3	VR0N2	VR0N1	VR0N0
0	1	0	0	VR2N5	VR2N4	VR2N3	VR2N2	VR2N1	VR2N0	0	0	VR1N5	VR1N4	VR1N3	VR1N2	VR1N1	VR1N0
0	1	0	0	0	VR6N4	VR6N3	VR6N2	VR6N1	VR6N0	0	0	0	VR4N3	VR13N3	VR4N2	VR4N1	VR4N0
0	1	0	VR20N6	VR20N5	VR20N4	VR20N3	VR20N2	VR20N1	VR20N0	0	0	0	0	VR13N3	VR13N2	VR13N1	VR13N0
0	1	0	VR43N6	VR43N5	VR43N4	VR43N3	VR43N2	VR43N1	VR43N0	0	0	VR36N2	VR36N1	VR36N0	VR27N2	VR27N1	VR27N0
0	1	0	0	0	VR59N4	VR59N3	VR59N2	VR59N1	VR59N0	0	0	0	VR57N4	VR57N3	VR57N2	VR57N1	VR57N0
0	1	0	0	VR62N5	VR62N4	VR62N3	VR62N2	VR62N1	VR62N0	0	0	VR61N5	VR61N4	VR61N3	VR61N2	VR61N1	VR61N0
0	1	VR63P3	VR63P2	VR63P1	VR63P0	VR50P3	VR50P2	VR50P1	VR50P0	J0P1	J0P0	J1P1	J1P0	VR0P3	VR0P2	VR0P1	VR0P0
0	1	0	0	VR2P5	VR2P4	VR2P3	VR2P2	VR2P1	VR2P0	0	0	VR1P5	VR1P4	VR1P3	VR1P2	VR1P1	VR1P0
0	1	0	0	0	VR6P4	VR6P3	VR6P2	VR6P1	VR6P0	0	0	0	VR4P3	VR13P3	VR4P2	VR4P1	VR4P0
0	1	0	VR20P6	VR20P5	VR20P4	VR20P3	VR20P2	VR20P1	VR20P0	0	0	0	0	VR13P3	VR13P2	VR13P1	VR13P0
0	1	0	VR43P6	VR43P5	VR43P4	VR43P3	VR43P2	VR43P1	VR43P0	0	0	VR36P2	VR36P1	VR36P0	VR27P2	VR27P1	VR27P0
0	1	0	0	0	VR59P4	VR59P3	VR59P2	VR59P1	VR59P0	0	0	0	VR57P4	VR57P3	VR57P2	VR57P1	VR57P0
0	1	0	0	VR62P5	VR62P4	VR62P3	VR62P2	VR62P1	VR62P0	0	0	VR61P5	VR61P4	VR61P3	VR61P2	VR61P1	VR61P0

VR-P: The gamma fine adjustment register for the positive polarity output
VR-N: The gamma fine adjustment register for the negative polarity output.

6.2.21. CHP Control1 (RE2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	AVEE_CLK_AD1	AVEE_CLK_AD0	0	0	1	0	1	1	AVDD_CLK_AD1	AVDD_CLK_AD0	0	0	1	0	1	1
DEFAULT		0	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1

AVEE_CLK_AD: Specify operating frequency of AVEE Booster Circuit.
AVDD_CLK_AD: Specify operating frequency of AVDD Booster Circuit.

AVEE_CLK_AD	AVEE Period	AVDD_CLK_AD	AVDD Period
00	3T	00	3T
01	4T	01	4T
10	5T	10	5T
11	6T	11	6T

T: internal OSC period

6.2.22. CHP Control2 (RE3h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	VGL_BT	VGL_CLK_AD3	VGL_CLK_AD2	VGL_CLK_AD1	VGL_CLK_AD0	1	0	0	VGH_BT	VGH_CLK_AD3	VGH_CLK_AD2	VGH_CLK_AD1	VGH_CLK_AD0
DEFAULT		1	0	0	0	1	0	0	0	1	0	0	0	1	0	1	0

VGL_CLK_AD: Specify operating frequency of VGL Booster Circuit.
VGH_CLK_AD: Specify operating frequency of VGH Booster Circuit.
VGL_BT: Specify ratio of VGL to VCI
VGH_BT: Specify ratio of VGH to VCI

VGL_CLK_AD	VGL Period	VGH_CLK_AD	VGH Period
0	4T	0	4T
1	5T	1	5T
2	6T	2	6T
3	8T	3	8T
4	10T	4	10T
5	12T	5	12T
6	15T	6	15T
7	20T	7	20T
8	24T	8	24T
9	30T	9	30T
10	40T	10	40T
11	48T	11	48T
12	60T	12	60T
13	80T	13	80T
14	120T	14	120T

15	240T	15	240T

T: internal OSC period

VGL_BT	VGL ratio	VGH_BT	VGH ratio
0	-5x	0	6x
1	-4x	1	5x

6.2.23. CHP Control3 (RE4h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	VDH_CLK_AD3	VDH_CLK_AD2	VDH_CLK_AD1	VDH_CLK_AD0	0	0	0	1	VCL_CLK_AD3	VCL_CLK_AD2	VCL_CLK_AD1	VCL_CLK_AD0
DEFAULT		0	0	0	1	1	0	0	0	0	0	0	1	0	1	0	1

VDH_CLK_AD: Specify operating frequency of VDH Booster Circuit.
VCL_CLK_AD: Specify operating frequency of VCL Booster Circuit.

VDH_CLK_AD	VDH Period	VCL_CLK_AD	VCL Period
0	4T	0	4T
1	5T	1	5T
2	6T	2	6T
3	8T	3	8T
4	10T	4	10T
5	12T	5	12T
6	15T	6	15T
7	20T	7	20T
8	24T	8	24T
9	30T	9	30T
10	40T	10	40T
11	48T	11	48T
12	60T	12	60T
13	80T	13	80T
14	120T	14	120T
15	240T	15	240T

T: internal OSC period

6.2.24. CHP Control4 (RE5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	0	0	1	0	0	0	0	SOU_CLK_AD2	SOU_CLK_AD1	SOU_CLK_AD0
DEFAULT		0	0	0	1	0	1	0	0	1	0	0	0	0	0	1	0

SOU_CLK_AD: Specify operating frequency of Source Power Circuit.

SOU_CLK_AD	Source Power Period	SOU_CLK_AD	Source Power Period
000	2T	100	10T
001	4T	101	12T
010	6T	110	14T
011	8T	111	16T

T: internal OSC period

6.2.25. VERG Control1 (REBh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	VREG1B_AD5	VREG1B_AD4	VREG1B_AD3	VREG1B_AD2	VREG1B_AD1	VREG1B_AD0	0	0	VREG1A_AD5	VREG1A_AD4	VREG1A_AD3	VREG1A_AD2	VREG1A_AD1	VREG1A_AD0
DEFAULT		0	0	1	0	0	1	0	1	0	0	1	0	1	0	1	0

VREG1A_AD: Adjust the voltage amplitude of VREG1A , which is the power of positive polarity gray.
VREG1B_AD: Adjust the voltage amplitude of VREG1B , which is the power of positive polarity gray.

VREG1A_AD	VREG1A(V)	VREG1A_AD	VREG1A(V)
0	3.90	**32**	5.50
1	3.95	**33**	5.55
2	4.00	**34**	5.60
3	4.05	**35**	5.65
4	4.10	**36**	5.70
5	4.15	**37**	5.75
6	4.20	**38**	5.80
7	4.25	**39**	5.85
8	4.30	**40**	5.90
9	4.35	**41**	5.95
10	4.40	**42**	6.00
11	4.45	**43**	6.05
12	4.50	**44**	6.10
13	4.55	**45**	6.15
14	4.60	**46**	6.20
15	4.65	**47**	6.25
16	4.70	**48**	6.30
17	4.75	**49**	6.35
18	4.80	**50**	6.40
19	4.85	**51**	6.45
20	4.90	**52**	6.50
21	4.95	**53**	6.55
22	5.00	**54**	6.60
23	5.05	**55**	6.65
24	5.10	**56**	6.70
25	5.15	**57**	6.75
26	5.20	**58**	6.80
27	5.25	**59**	6.85
28	5.30	**60**	6.90
29	5.35	**61**	6.95
30	5.40	**62**	7.00
31	5.45	**63**	7.05

VREG1B_AD	VREG1B(V)	VREG1B_AD	VREG1B(V)
0	0.40	**32**	1.41
1	0.45	**33**	1.43
2	0.50	**34**	1.45
3	0.55	**35**	1.47
4	0.60	**36**	1.49
5	0.65	**37**	1.51
6	0.70	**38**	1.53
7	0.75	**39**	1.55
8	0.80	**40**	1.57
9	0.85	**41**	1.59
10	0.90	**42**	1.61
11	0.95	**43**	1.63
12	1.01	**44**	1.65
13	1.03	**45**	1.67
14	1.05	**46**	1.69
15	1.07	**47**	1.71
16	1.09	**48**	1.76
17	1.11	**49**	1.81
18	1.13	**50**	1.86
19	1.15	**51**	1.91
20	1.17	**52**	1.96
21	1.19	**53**	2.01
22	1.21	**54**	2.06
23	1.23	**55**	2.12
24	1.25	**56**	2.17
25	1.27	**57**	2.22
26	1.29	**58**	2.27
27	1.31	**59**	2.32
28	1.33	**60**	2.37
29	1.35	**61**	2.42
30	1.37	**62**	2.47
31	1.39	**63**	2.52

6.2.26. VERG Control2 (RECh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	VREG2B_AD5	VREG2B_AD4	VREG2B_AD3	VREG2B_AD2	VREG2B_AD1	VREG2B_AD0	0	0	VREG2A_AD5	VREG2A_AD4	VREG2A_AD3	VREG2A_AD2	VREG2A_AD1	VREG2A_AD0
DEFAULT		0	0	1	0	0	1	0	1	0	0	0	1	0	1	0	1

VREG2A_AD: Adjust the voltage amplitude of VREG2A , which is the power of negative polarity gray.
VREG2B_AD: Adjust the voltage amplitude of VREG2B , which is the power of negative polarity gray.

VREG2A_AD	VREG2A(V)	VREG2A_AD	VREG2A(V)
0	−1.95	**32**	−3.55
1	−2.00	**33**	−3.60
2	−2.05	**34**	−3.65

3	−2. 10	**35**	−3. 70
4	−2. 15	**36**	−3. 75
5	−2. 20	**37**	−3. 80
6	−2. 25	**38**	−3. 85
7	−2. 30	**39**	−3. 90
8	−2. 35	**40**	−3. 95
9	−2. 40	**41**	−4. 00
10	−2. 45	**42**	−4. 05
11	−2. 50	**43**	−4. 10
12	−2. 55	**44**	−4. 15
13	−2. 60	**45**	−4. 20
14	−2. 65	**46**	−4. 25
15	−2. 70	**47**	−4. 30
16	−2. 75	**48**	−4. 35
17	−2. 80	**49**	−4. 40
18	−2. 85	**50**	−4. 45
19	−2. 90	**51**	−4. 50
20	−2. 95	**52**	−4. 55
21	−3. 00	**53**	−4. 60
22	−3. 05	**54**	−4. 65
23	−3. 10	**55**	−4. 70
24	−3. 15	**56**	−4. 75
25	−3. 20	**57**	−4. 80
26	−3. 25	**58**	−4. 85
27	−3. 30	**59**	−4. 90
28	−3. 35	**60**	−4. 95
29	−3. 40	**61**	−5. 00
30	−3. 45	**62**	−5. 05
31	−3. 50	**63**	−5. 10

VREG2B_AD	VREG2B(V)	VREG2B_AD	VREG2B(V)
0	0. 40	**32**	1. 40
1	0. 45	**33**	1. 42
2	0. 50	**34**	1. 44
3	0. 55	**35**	1. 46
4	0. 60	**36**	1. 48
5	0. 65	**37**	1. 50
6	0. 70	**38**	1. 52
7	0. 75	**39**	1. 54
8	0. 80	**40**	1. 56
9	0. 85	**41**	1. 58
10	0. 90	**42**	1. 60
11	0. 95	**43**	1. 62
12	1. 00	**44**	1. 64
13	1. 02	**45**	1. 66
14	1. 04	**46**	1. 68
15	1. 06	**47**	1. 70
16	1. 08	**48**	1. 75
17	1. 10	**49**	1. 80
18	1. 12	**50**	1. 85
19	1. 14	**51**	1. 90
20	1. 16	**52**	1. 95
21	1. 18	**53**	2. 00
22	1. 20	**54**	2. 05
23	1. 22	**55**	2. 10

24	1. 24	**56**	2. 15
25	1. 26	**57**	2. 20
26	1. 28	**58**	2. 25
27	1. 30	**59**	2. 30
28	1. 32	**60**	2. 35
29	1. 34	**61**	2. 40
30	1. 36	**62**	2. 45
31	1. 38	**63**	2. 50

6.2.27. CHP Control5 (REEh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	AVEE_AD2	AVEE_AD1	AVEE_AD0	0	AVDD_AD2	AVDD_AD1	AVDD_AD0	1	0	0	1	1	0	1	1
DEFAULT		0	0	1	1	0	0	1	1	1	0	0	1	1	0	1	1

AVDD_AD: Specify voltage amplitude of AVDD
AVEE_AD: Specify voltage amplitude of AVEE

AVDD_AD	AVDD(V)	AVDD_AD	AVDD(V)
000	6.92	100	6.44
001	6.80	101	6.32
010	6.68	110	6.20
011	6.56	111	6.08

AVEE_AD	AVEE(V)	AVEE_AD	AVEE(V)
000	-4.88	100	-4.40
001	-4.76	101	-4.28
010	-4.64	110	-4.16
011	-4.52	111	-4.04

6.2.28. CHP Control6 (REFh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	VGL_AD2	VGL_AD1	VGL_AD0	VGH_AD2	VGH_AD1	VGLH_AD0	0	BVEE_AD2	BVEE_AD1	BVEE_AD0	0	BVDD_AD2	BVDD_AD1	BVDD_AD0
DEFAULT		0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0

VGL_AD: Specify voltage amplitude of VGL
VGH_AD: Specify voltage amplitude of VGH
BVDD_AD: Specify voltage amplitude of BVDD
BVDD_AD: Specify voltage amplitude of BVEE

VGL_AD	VGL(V)	VGL_AD	VGL(V)
000	-8.0	100	-10.0

001	-8.5	101	-10.5
010	-9.0	110	-11.0
011	-9.5	111	-11.5

VGH_AD	VGH(V)	VGH_AD	VGH(V)
000	9.0	100	11.0
001	9.5	101	11.5
010	10.0	110	12.0
011	10.5	111	12.5

BVDD_AD	BVDD(V)	BVDD_AD	BVDD(V)
000	7.0	100	6.5
001	6.9	101	6.4
010	6.8	110	6.3
011	6.7	111	6.2

BVEE_AD	BVEE(V)	BVEE_AD	BVEE(V)
000	-4.5	100	-4.1
001	-4.4	101	-4..0
010	-4.3	110	-3.9
011	-4.2	111	-3.8

6.2.29. INTER_REG_DIS (RFEh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

After write the IR(FEh), internal register can’t be access.

6.2.30. INTER_REG_EN (RFFh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1

After write the IR(FFh)=0x5aa5, internal register can be access.

7. GRAM Address Map & Read/Write

GC9203 has an internal graphics RAM (GRAM) of 87,120 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80/M68 system, SPI and RGB interfaces

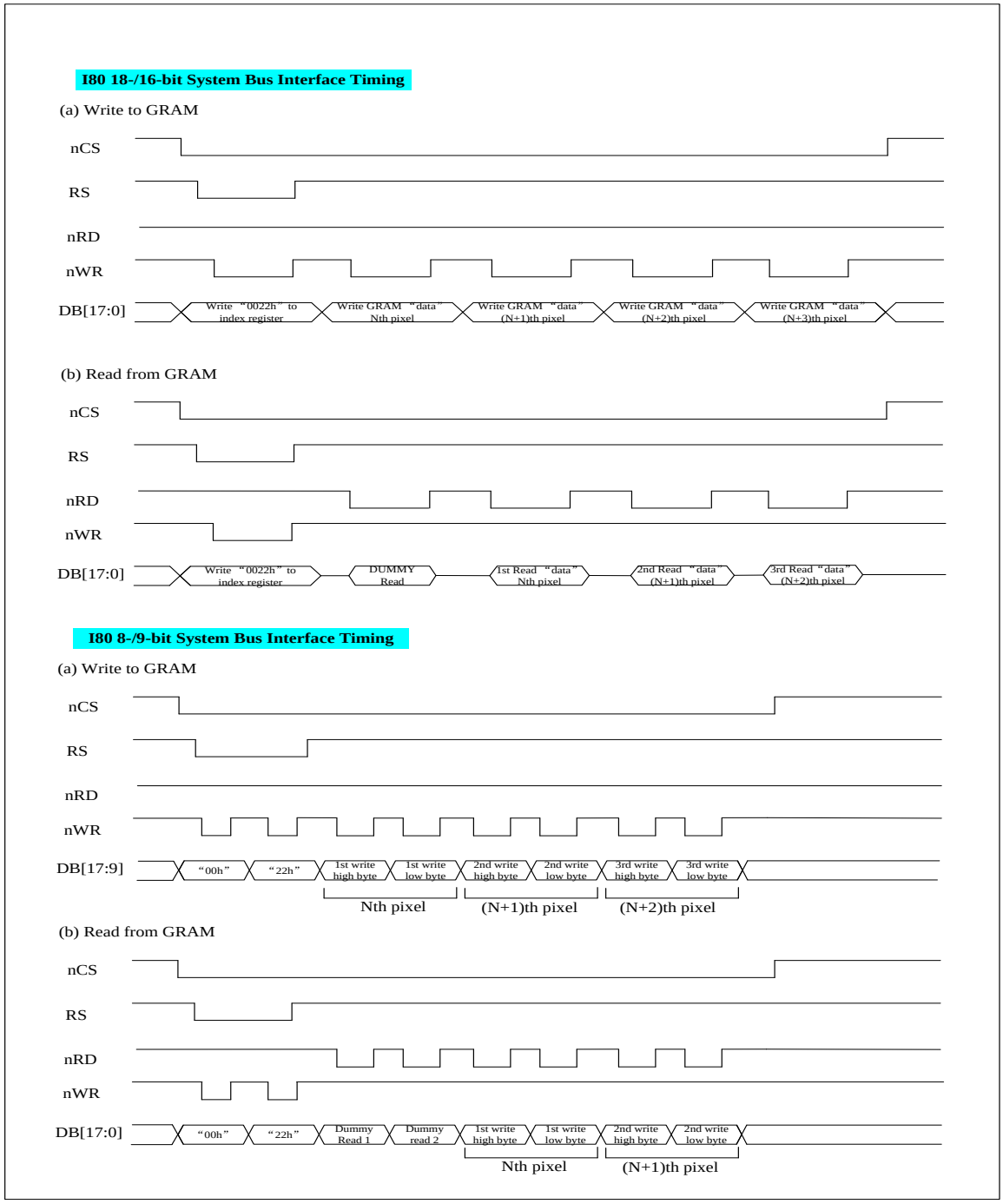
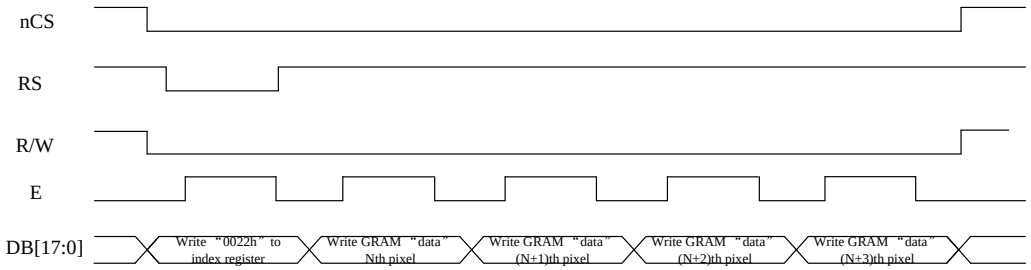


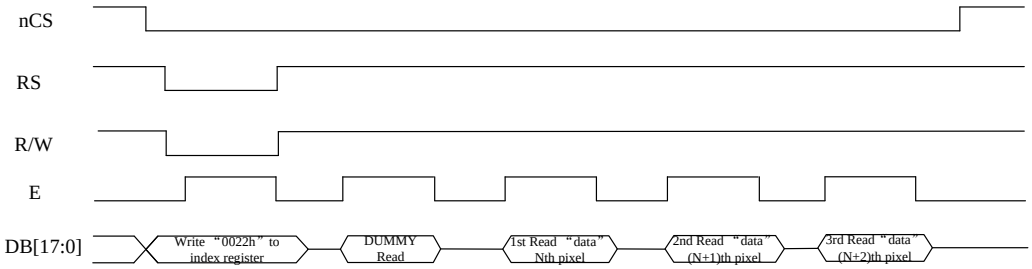
Figure30 GRAM Read/Write Timing of i80-System Interface

M68 18-/16-bit System Bus Interface Timing

(a) Write to GRAM

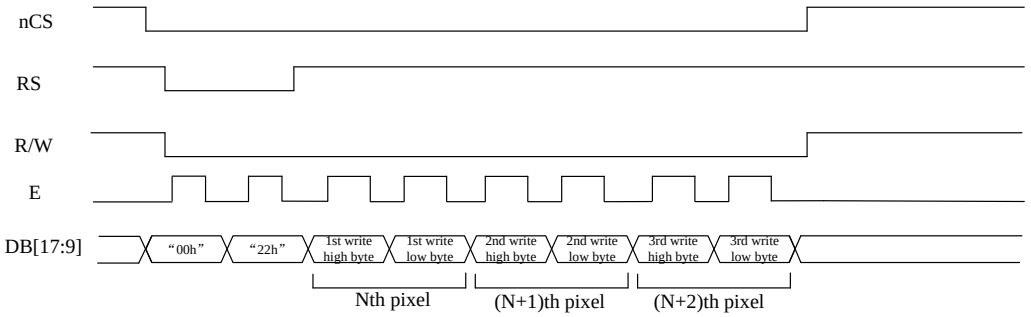


(b) Read from GRAM



M68 8-/9-bit System Bus Interface Timing

(a) Write to GRAM



(b) Read from GRAM

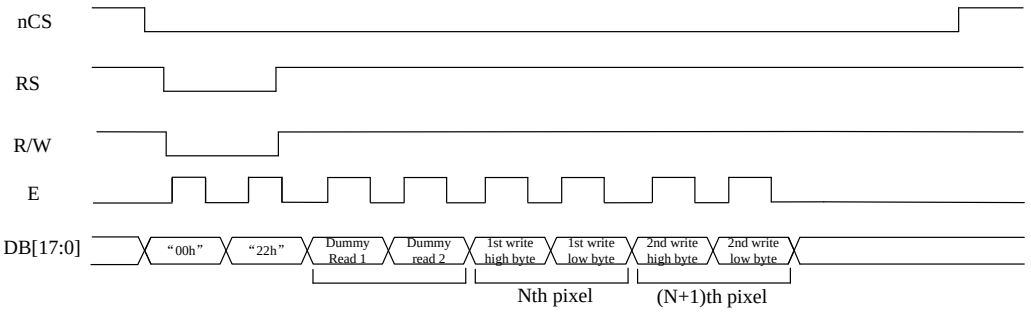


Figure31 GRAM Read/Write Timing of M68-System Interface

GRAM address map table of SS=0, BGR=0

SS=0,BGR=0		S1~S3	S4~S6	S7~S8	.	S520~S522	S523~S525	S526~S528
GS=0	GS=1	DB17~0	DB17~0	DB17~0	.	DB17~0	DB17~0	DB17~0
G1	G220	"0000h"	"0001h"	"0002h"	.	"00ADh"	"00AEh"	"00AFh"
G2	G219	"0100h"	"0101h"	"0102h"	.	"01ADh"	"01AEh"	"01AFh"
G3	G218	"0200h"	"0201h"	"0202h"	.	"02ADh"	"02AEh"	"02AFh"
G4	G217	"0300h"	"0301h"	"0302h"	.	"03ADh"	"03AEh"	"03AFh"
G5	G216	"0400h"	"0401h"	"0402h"	.	"04ADh"	"04AEh"	"04AFh"
G6	G215	"0500h"	"0501h"	"0502h"	.	"05ADh"	"05AEh"	"05AFh"
G7	G214	"0600h"	"0601h"	"0602h"	.	"06ADh"	"06AEh"	"06AFh"
G8	G213	"0700h"	"0701h"	"0702h"	.	"07ADh"	"07AEh"	"07AFh"
G9	G212	"0800h"	"0801h"	"0802h"	.	"08ADh"	"08AEh"	"08AFh"
G10	G211	"0900h"	"0901h"	"0902h"	.	"09ADh"	"09AEh"	"09AFh"
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
G211	G10	"D200h"	"D201h"	"D202h"	.	"D2ADh"	"D2AEh"	"D2AFh"
G212	G9	"D300h"	"D301h"	"D302h"	.	"D3ADh"	"D3AEh"	"D3AFh"
G213	G8	"D400h"	"D400h"	"D400h"	.	"D4ADh"	"D4AEh"	"D4AFh"
G214	G7	"D500h"	"D500h"	"D500h"	.	"D5ADh"	"D5AEh"	"D5AFh"
G215	G6	"D600h"	"D600h"	"D600h"	.	"D6ADh"	"D6AEh"	"D6AFh"
G216	G5	"D700h"	"D700h"	"D700h"	.	"D7ADh"	"D7AEh"	"D7AFh"
G217	G4	"D800h"	"D800h"	"D800h"	.	"D8ADh"	"D8AEh"	"D8AFh"
G218	G3	"D900h"	"D900h"	"D900h"	.	"D9ADh"	"D9AEh"	"D9AFh"
G219	G2	"DA00h"	"DA01h"	"DA02h"	.	"DAADh"	"DAAEh"	"DAAFh"
G220	G1	"DB00h"	"DB01h"	"DB02h"	.	"DBADh"	"DBAEh"	"DBAFh"

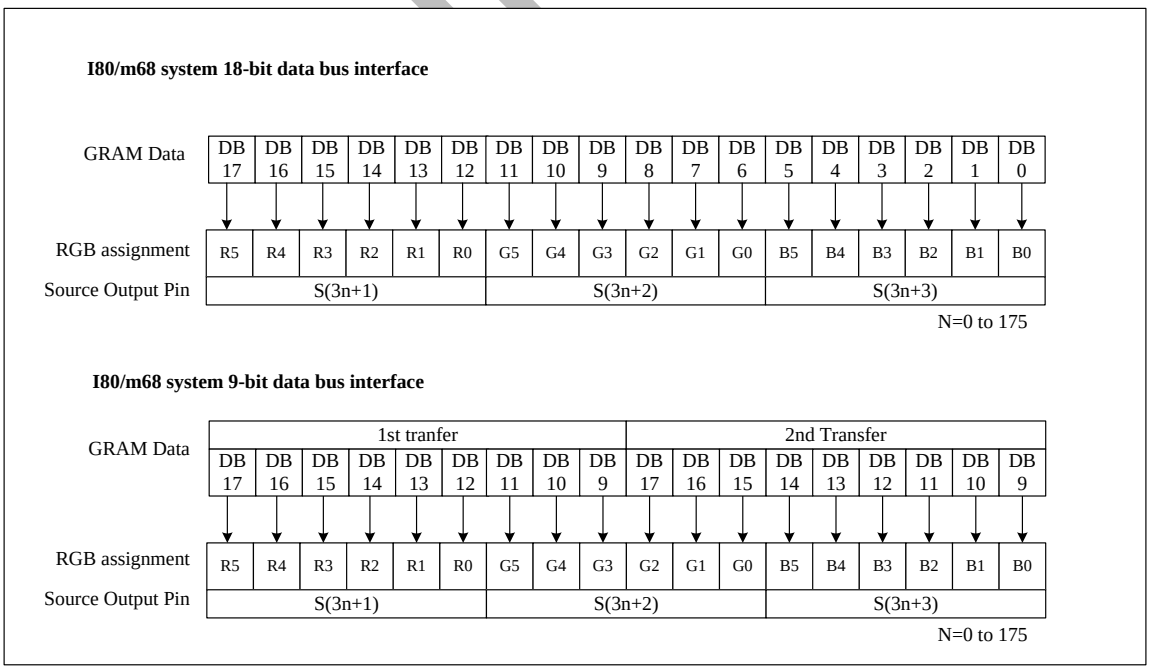


Figure32 i80-System Interface with 18-/9-bit Data Bus (SS="0", BGR="0")

GRAM address map table of SS=1, BGR=1

SS=0,BGR=0		S1~S3	S4~S6	S7~S8	.	S520~S522	S523~S525	S526~S528
GS=0	GS=1	DB17~0	DB17~0	DB17~0	.	DB17~0	DB17~0	DB17~0
G1	G220	"00AFh"	"00AEh"	"00ADh"	.	"0002h"	"0001h"	"0000h"
G2	G219	"01AFh"	"01AEh"	"01ADh"	.	"0102h"	"0101h"	"0100h"
G3	G218	"02AFh"	"02AEh"	"02ADh"	.	"0202h"	"0201h"	"0200h"
G4	G217	"03AFh"	"03AEh"	"03ADh"	.	"0302h"	"0301h"	"0300h"
G5	G216	"04AFh"	"04AEh"	"04ADh"	.	"0402h"	"0401h"	"0400h"
G6	G215	"05AFh"	"05AEh"	"05ADh"	.	"0502h"	"0501h"	"0500h"
G7	G214	"06AFh"	"06AEh"	"06ADh"	.	"0602h"	"0601h"	"0600h"
G8	G213	"07AFh"	"07AEh"	"07ADh"	.	"0702h"	"0701h"	"0700h"
G9	G212	"08AFh"	"08AEh"	"08ADh"	.	"0802h"	"0801h"	"0800h"
G10	G211	"09AFh"	"09AEh"	"09ADh"	.	"0902h"	"0901h"	"0900h"
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
G211	G10	"D2AFh"	"D2AEh"	"D2ADh"	.	"D202h"	"D201h"	"D200h"
G212	G9	"D3AFh"	"D3AEh"	"D3ADh"	.	"D302h"	"D301h"	"D300h"
G213	G8	"D4AFh"	"D4AEh"	"D4ADh"	.	"D400h"	"D400h"	"D400h"
G214	G7	"D5AFh"	"D5AEh"	"D5ADh"	.	"D500h"	"D500h"	"D500h"
G215	G6	"D6AFh"	"D6AEh"	"D6ADh"	.	"D600h"	"D600h"	"D600h"
G216	G5	"D7AFh"	"D7AEh"	"D7ADh"	.	"D700h"	"D700h"	"D700h"
G217	G4	"D8AFh"	"D8AEh"	"D8ADh"	.	"D800h"	"D800h"	"D800h"
G218	G3	"D9AFh"	"D9AEh"	"D9ADh"	.	"D900h"	"D900h"	"D900h"
G219	G2	"DAAFh"	"DAAEh"	"DAADh"	.	"DA02h"	"DA01h"	"DA00h"
G220	G1	"DBAFh"	"DBAEh"	"DBADh"	.	"DB02h"	"DB01h"	"DB00h"

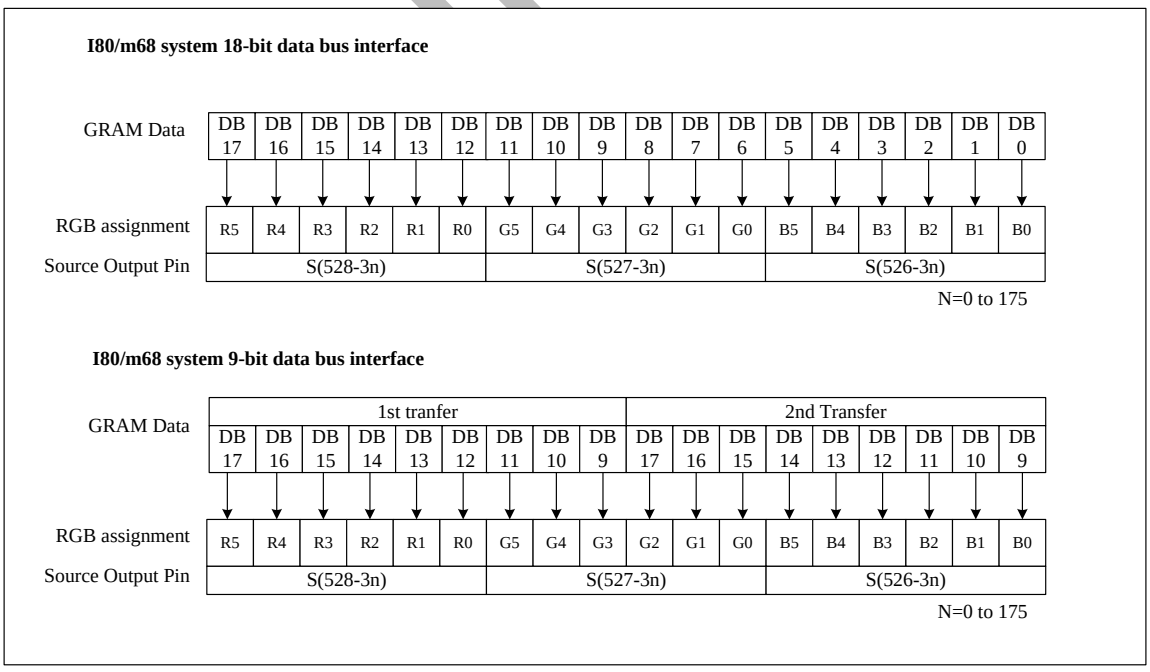


Figure33 i80-System Interface with 18-/9-bit Data Bus (SS="1", BGR="1")

8. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[7:0], end: VEA[7:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the GC9203 to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the AD[15:0] bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

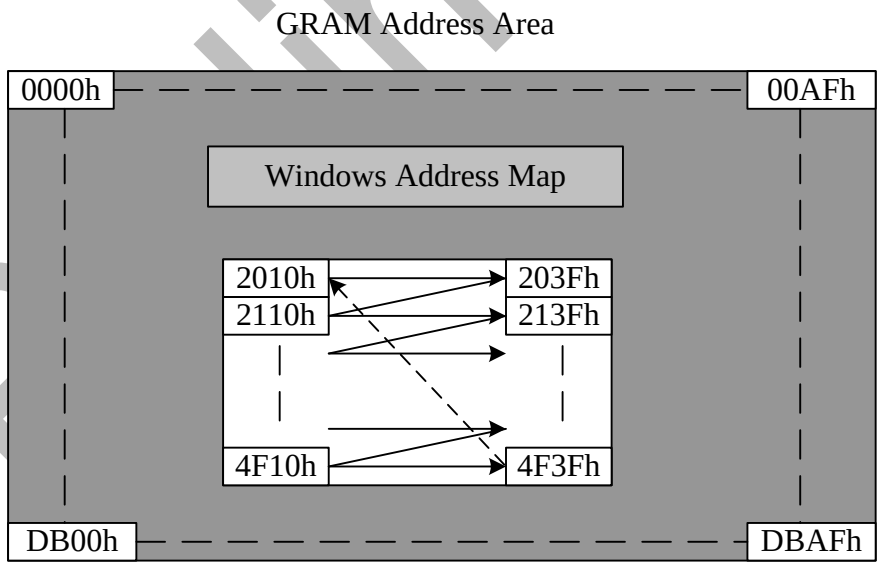
(Horizontal direction) 00H ≤ HSA[7:0] ≤ HEA[7:0] ≤ "AF" H

(Vertical direction) 00H ≤ VSA[7:0] ≤ VEA[7:0]≤ "DB" H

[RAM address, AD[15:0] (an address within a window address area)]]

RAM address) HSA[7:0] ≤ AD[7:0] ≤ HEA[7:0]

VSA[7:0] ≤ AD[15:8] ≤ VEA[7:0]



Windows address setting area

HSA[7:0] = 10h, HEA[7:0] = 3Fh, I/D = 1 (increment)

VSA[7:0] = 20h, VSA[7:0] = 4Fh, AM = 0 (horizontal writing)

Figure34 GRAM Access Window Map

9. Gamma Correction

GC9203 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9203 available with liquid crystal panels of various characteristics.

Figure85.

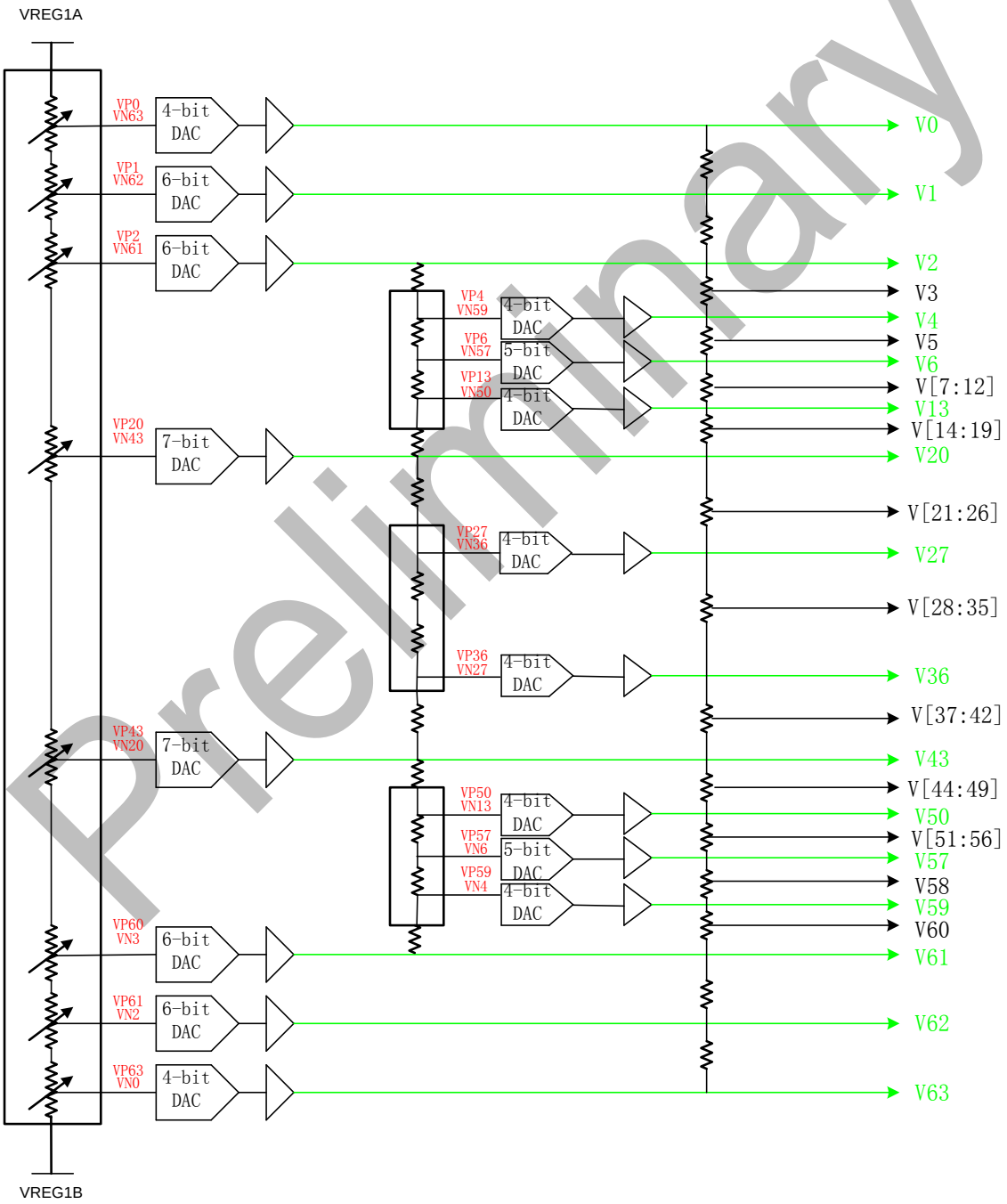
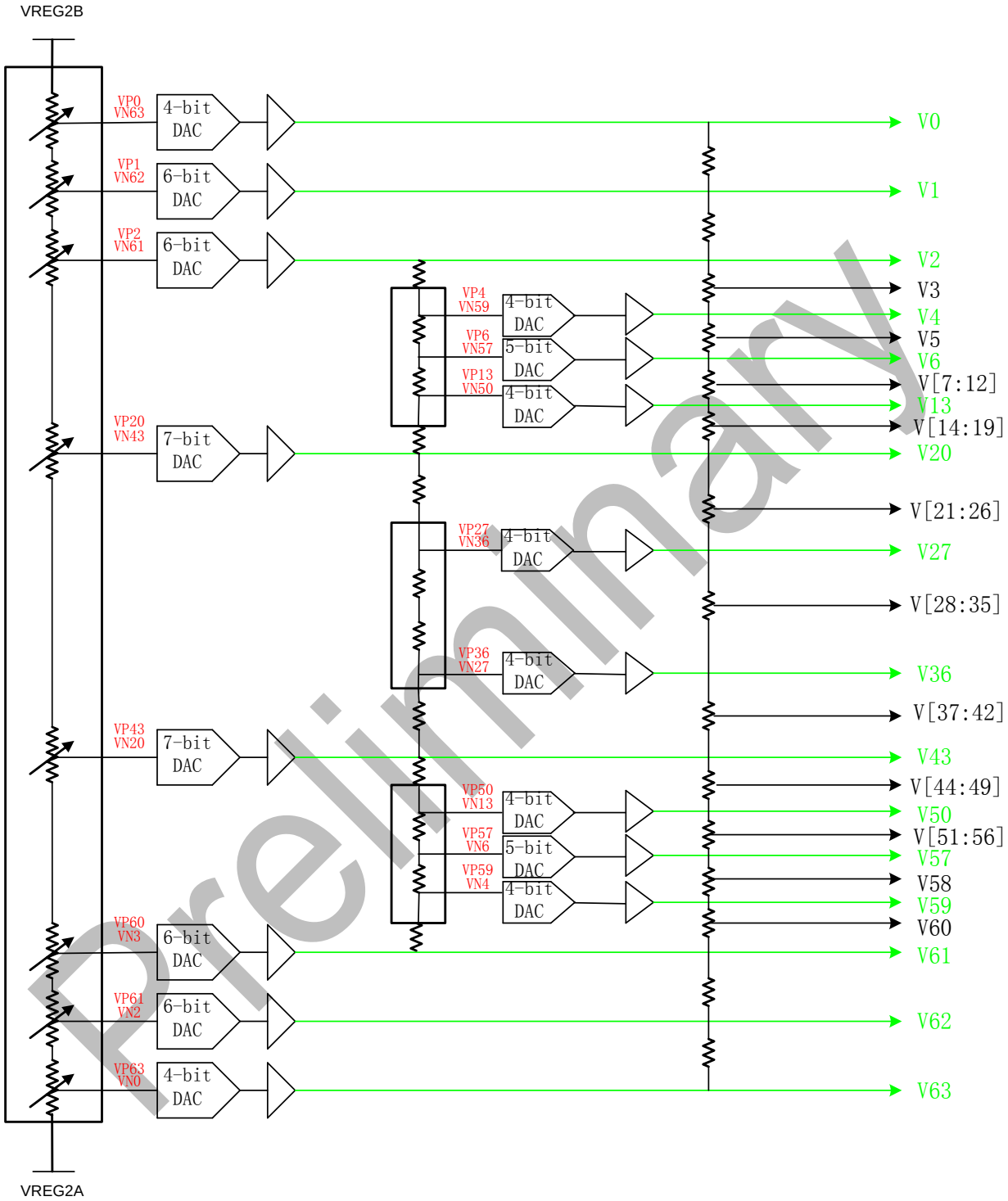
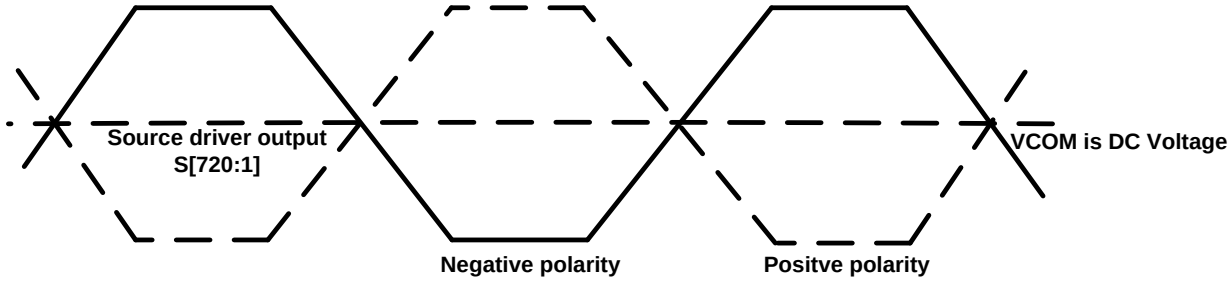


Figure86.



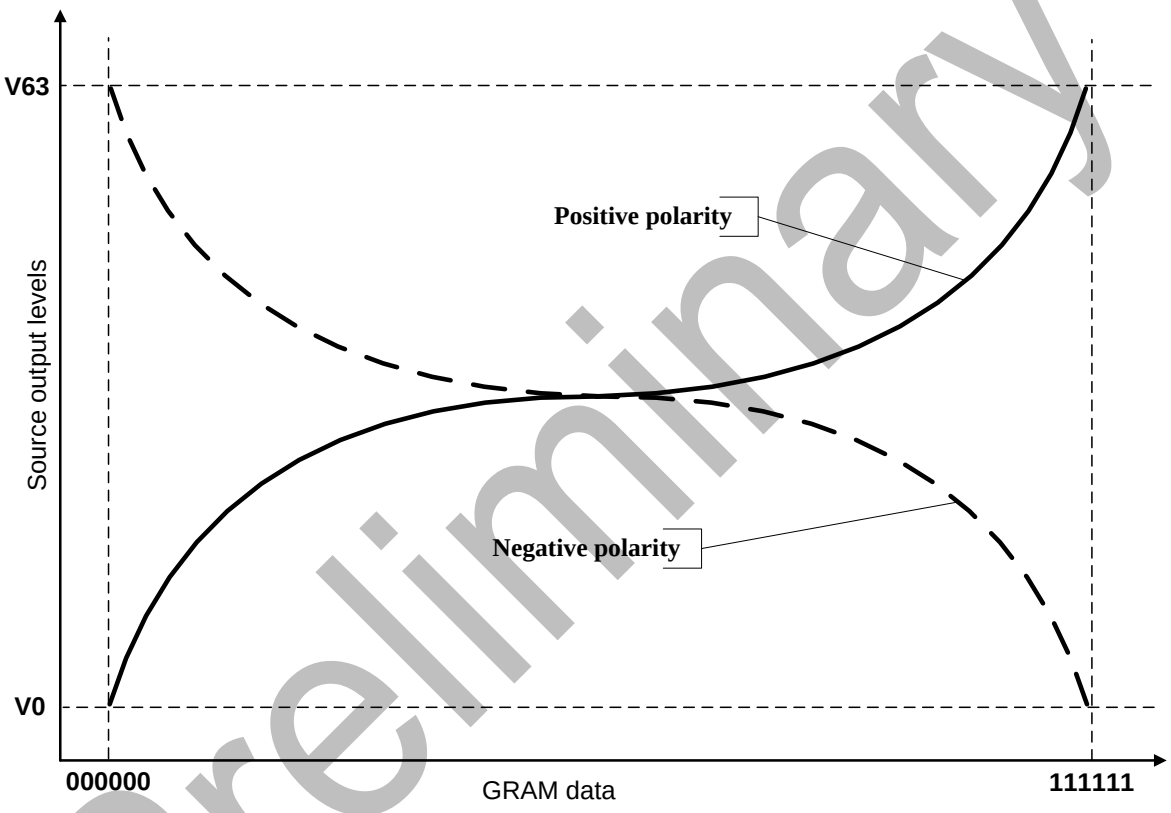
Grayscale Voltage Generation

Figure87.Dot inversion



Relationship between Source Output and VCOM

Figure88.



10. Application

10.1. Application Circuit

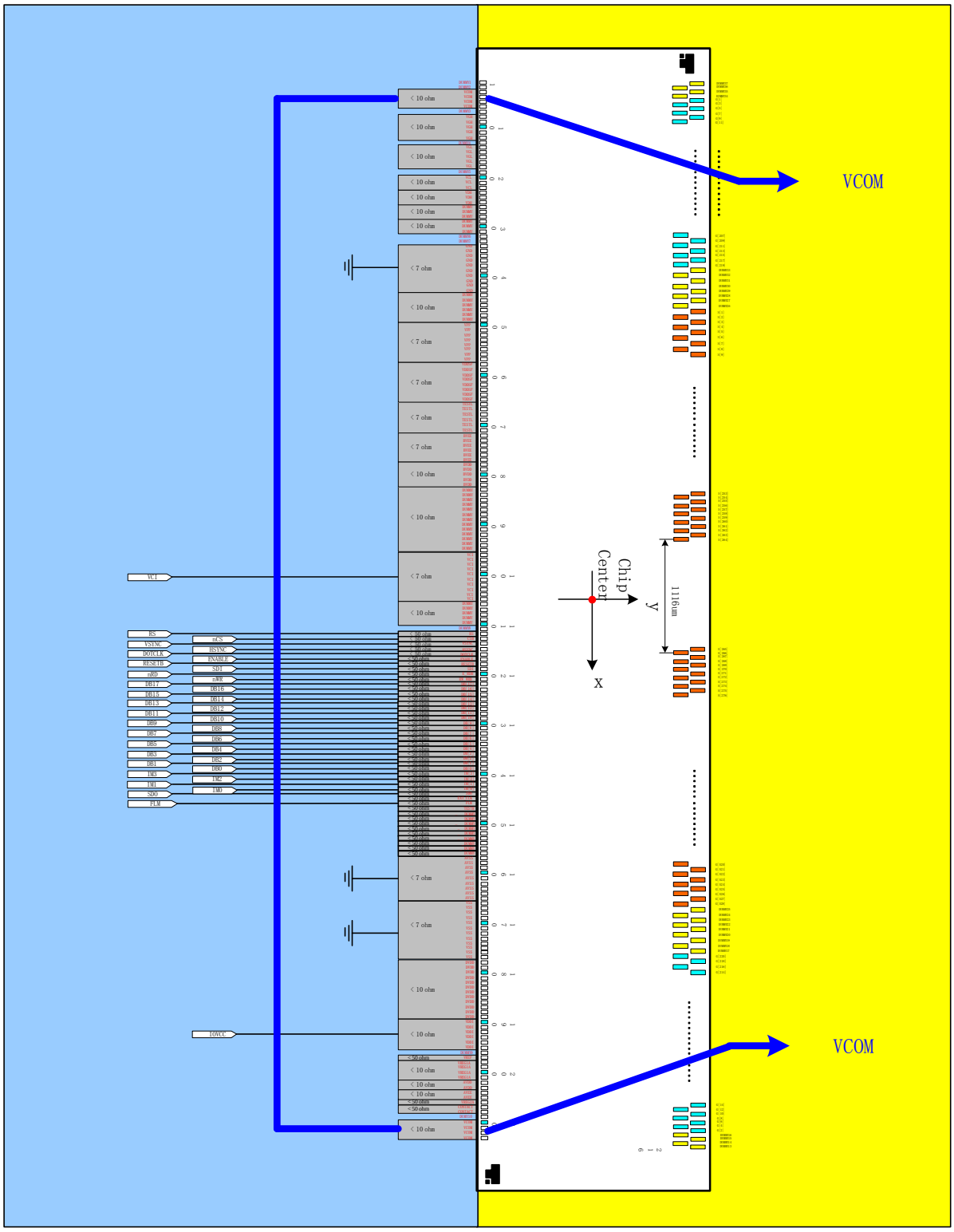


Figure41 Application Circuit Block

10.2. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the GC9203 are as follows

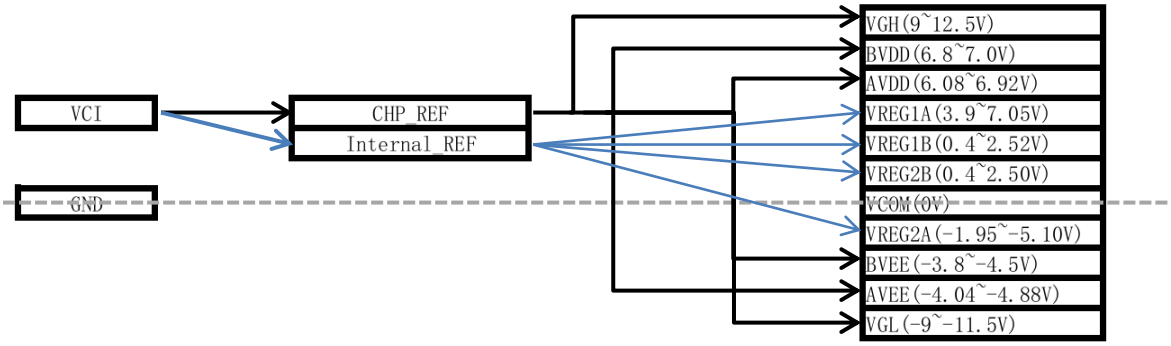


Figure42 Voltage Configuration Diagram

10.3. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for step-up circuits and operational amplifiers depends on external resistance and capacitance.

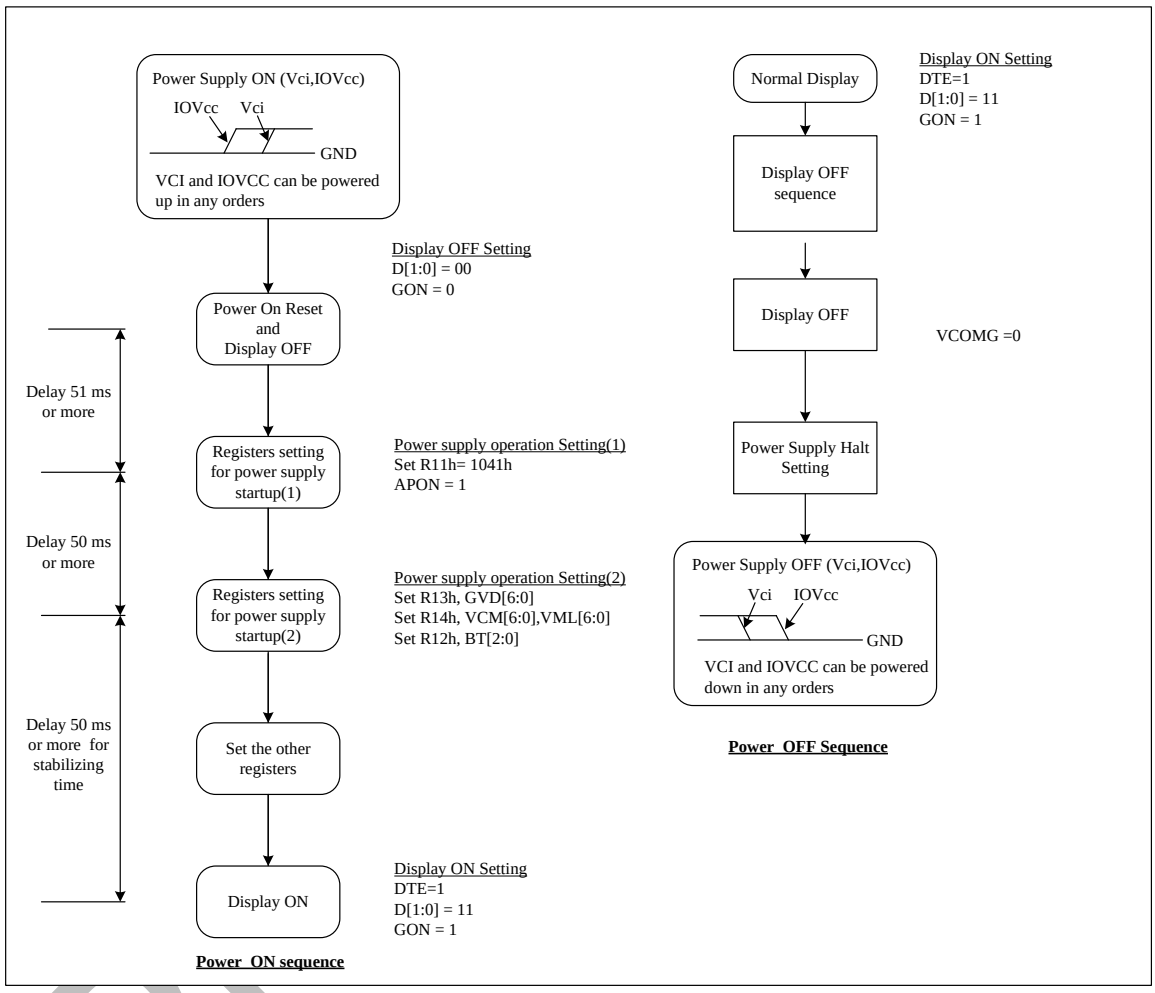


Figure43 Power On/Off Sequence

10.4. STB Mode

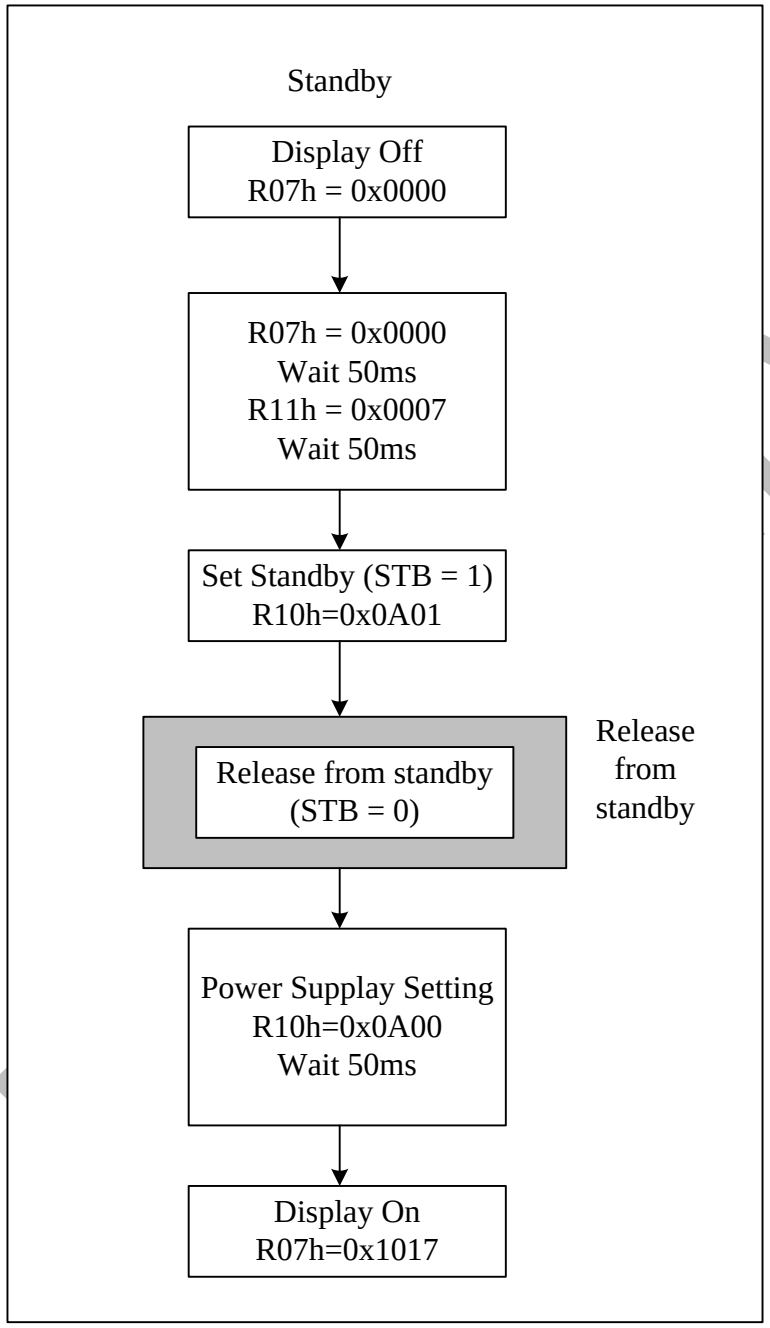


Figure44 STB Mode Register Setting Sequence

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9203 is used out of the absolute maximum ratings, the GC9203 may be permanently damaged. To use the GC9203 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the GC9203 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	VDDI	V	-0.3 ~ +4.6	1, 2
Power supply voltage (1)	VCI – GND	V	-0.3 ~ +4.6	1, 4
Power supply voltage (1)	AVDD – GND	V	-0.3 ~ +6.0	1, 4
Power supply voltage (1)	GND – VCL	V	-0.3 ~ +4.6	1
Power supply voltage (1)	AVDD – VCL	V	-0.3 ~ +9.0	1, 5
Power supply voltage (1)	VGH – GND	V	-0.3 ~ +18.5	1, 5
Power supply voltage (1)	GND – VGL	V	-0.3 ~ +18.5	1, 6
Input voltage	Vt	V	-0.3 ~ VCI + 0.3	1
Operating temperature	Topr	℃	-40 ~ +85	8, 9
Storage temperature	Tstg	℃	-55 ~ +110	8, 9

Note:
1, VCI,GND must be maintained
2. (High) VCI ≥ GND (Low), (High) VDDI ≥ GND (Low).
3. Make sure (High) VCI ≥ GND (Low).
4. Make sure (High) AVDD ≥ ASSD (Low).
5. Make sure (High) AVDD ≥ VCL (Low).
6. Make sure (High) VGH ≥ ASSD (Low).
7. Make sure (High) ASSD ≥ VGL (Low).
8. For die and wafer products, specified up to 85℃.
9. This temperature specifications apply to the TCP package

11.2. DC Characteristics

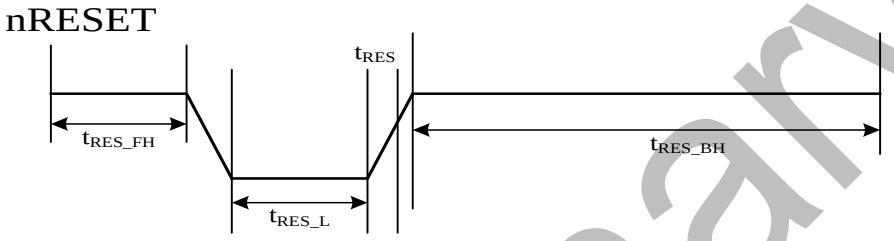
(VCI = 2.50 ~ 3.30V, VDDI = 1.65 ~ 3.30V, Ta= -40 ~ 85 ℃)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Note
Input high voltage	V_{IH}	V	VDDI= 1.65 ~ 3.3V	0.8*VDDI	-	VDDI	-
Input low voltage	V_{IL}	V	VDDI= 1.65 ~ 3.3V	0	-	0.2*VDDI	-
Output high voltage(1) (DB0-17 Pins)	V_{OH1}	V	IOH = -0.1 mA	0.8*VDDI	-	-	-
Output low voltage (DB0-17 Pins)	V_{OL1}	V	VDDI=1.65~3.3V VCI= 2.5 ~ 3.3V IOL = 0.1mA	-	-	0.2*VDDI	-
I/O leakage current	I_{LI}	μA	Vin = 0 ~ VDDI	-0.1		-0.1	-
Current consumption during standby mode (VCI – GND)	I_{ST}	μA	VCI=2.8V , Ta=25℃	-	5	30	-
LCD Driving Voltage (AVDD-GND)	AVDD	V	-	4.5	-	6	-
Output voltage deviation		mV	-		20	-	-
Dispersion of the Average Output Voltage	V	mV	-	-20	-	-20	-

11.3. Reset Timing Characteristics

Reset Timing Characteristics (VDDI = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min	Typ	Max
Reset front high-level width	t_{RES_FH}	ms	1		
Reset low-level width	t_{RES_L}	us	20		
Reset back high-level width	t_{RES_BH}	Ms	50		
Reset rise time	t_{RES}	us			10



11.4. AC Characteristics

11.4.1. i80-System Interface Timing Characteristics

Normal Write Mode (VDDI = 1.65~3.3V, VCI=2.5~3.3V)

Item		symbol	unit	min	max	Test Condition
Bus cycle time	**Write**	t_{CYCW}	ns	110	-	-
	Read	t_{CYCR}	ns	340	-	-
Write low-level pulse width		PW_{LW}	ns	55	500	-
Write high-level pulse width		PW_{HW}	ns	55	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-
Read high-level pulse width		PW_{HR}	ns	190	-	
Write/Read rise/fall time		t_{WRr}/t_{WRf}	ns	-	15	
Setup time	**Write(RS to CSX, E/WRX)**	t_{AS}	ns	10	-	
	Read(RS to CSX,RW/RDX)		ns	5	-	
Address hold time		t_{AH}	ns	5	-	
Write data set up time		t_{DSW}	ns	10	-	
Write data hold time		t_{H}	ns	15	-	
Read data delay time		t_{DDR}	ns	-	100	
Read data hold time		t_{DHR}	ns	5	-	

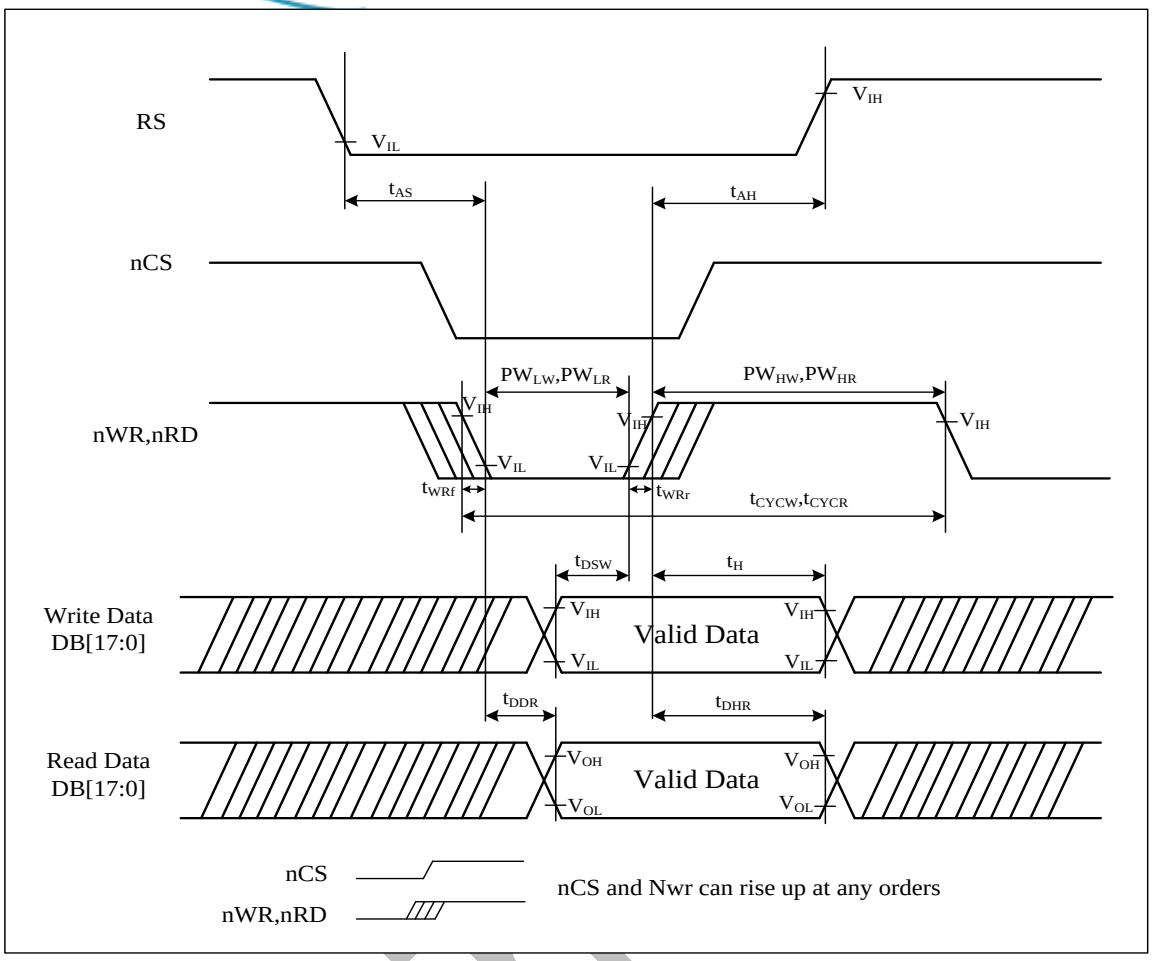


Figure45 i80-System Bus Timing

11.4.2. M68-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCI=2.5~3.3V)

Item		symbol	unit	min	max	Test Condition
Bus cycle time	**Write**	t_{CYCEW}	ns	110	-	-
	Read	t_{CYCER}	ns	340	-	-
Write low-level pulse width		PW_{ELW}	ns	55	500	-
Write high-level pulse width		PW_{EHW}	ns	55	-	-
Read low-level pulse width		PW_{ELR}	ns	150	-	-
Read high-level pulse width		PW_{EHR}	ns	190	-	
Write/Read rise/fall time		t_{WRr}/t_{WRf}	ns	-	15	
Setup time	**Write(RS to nCS, E/nWR)**	t_{ASE}	ns	10	-	
	Read(RS to nCS,RW/nRD)		ns	10	-	
Address hold time		t_{AHE}	ns	5	-	
Write data set up time		t_{DSWE}	ns	10	-	
Write data hold time		t_{HE}	ns	15	-	
Read data delay time		t_{DDRE}	ns	-	100	
Read data hold time		t_{DHRE}	ns	5	-	

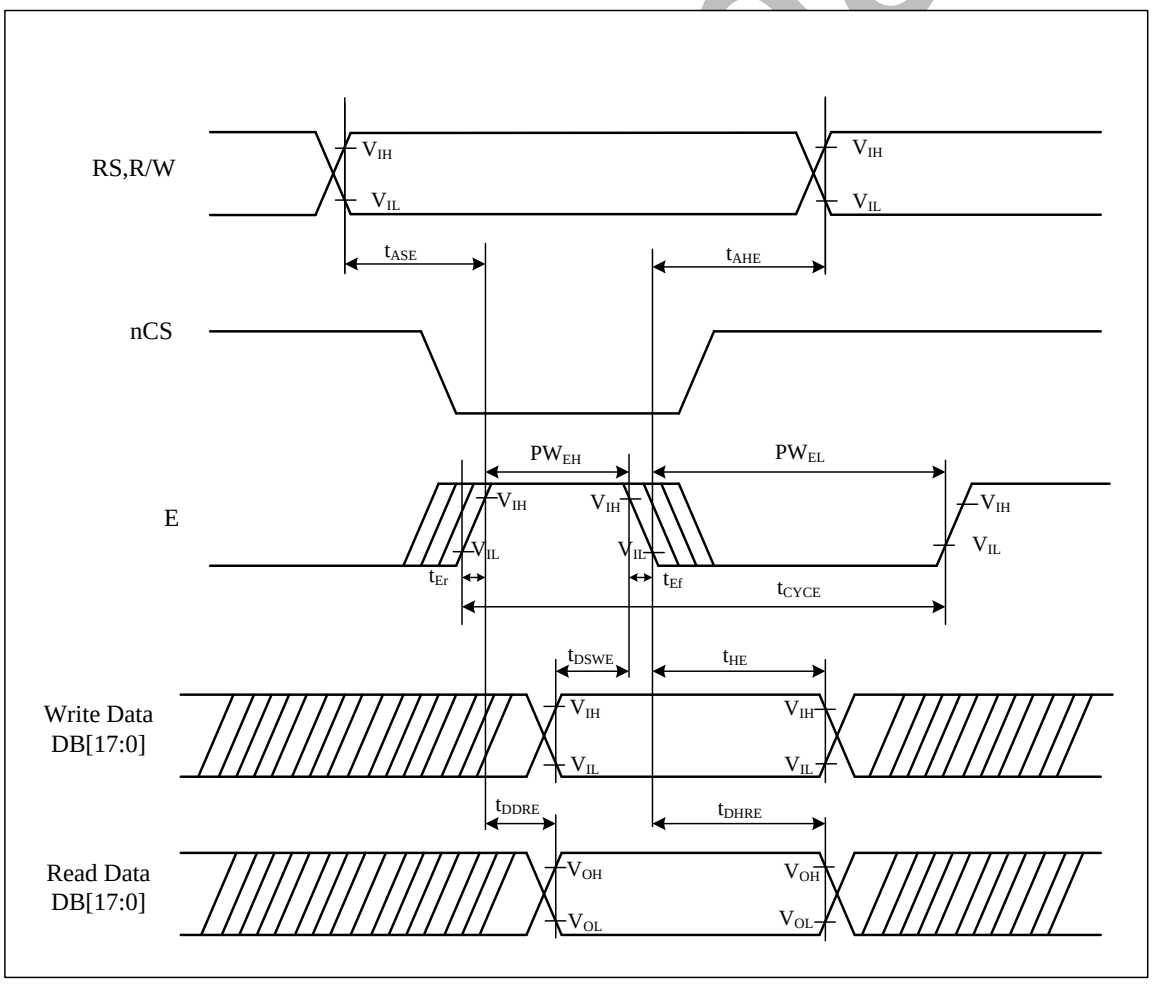


Figure47 M68-System Interface Timing

11.4.3. Serial Data Transfer Interface Timing Characteristics

(VDDI= 1.65~3.3V and VCI=2.5~3.3V)

Item		symbol	unit	min	max	Test Condition
Serial clock cycle time	**Write(received)**	t_{SCYC}	ns	80	-	VDDI=1.65~2.8V
	Write(received)	t_{SCYC}	ns	25		VDDI=2.8~3.3V
	Read(transmitted)	t_{SCYC}	ns	200	-	-
Serial clock high-level pulse width	**Write(received)**	t_{SCH}	ns	40		VDDI=1.65~3.3V
	Read(transmitted)	t_{SCH}	ns	90		
Serial clock low-level pulse width	**Write(received)**	t_{SCL}	ns	40		VDDI=1.65~3.3V
	Read(transmitted)	t_{SCL}	ns	90		
Write/Read rise/fall time		t_{SCr}, t_{SCf}	ns	-	5	
Chip select set up time		t_{CSU}	ns	10	-	
Chip select hold time		t_{CH}	ns	10	-	
Serial input data set up time		t_{SISU}	ns	5	-	
Serial input data hold time		t_{SIH}	ns	5	-	
Serial output data set up time		t_{SOD}	ns	-	200	
Serial output data hold time		t_{SOH}	ns	10	-	

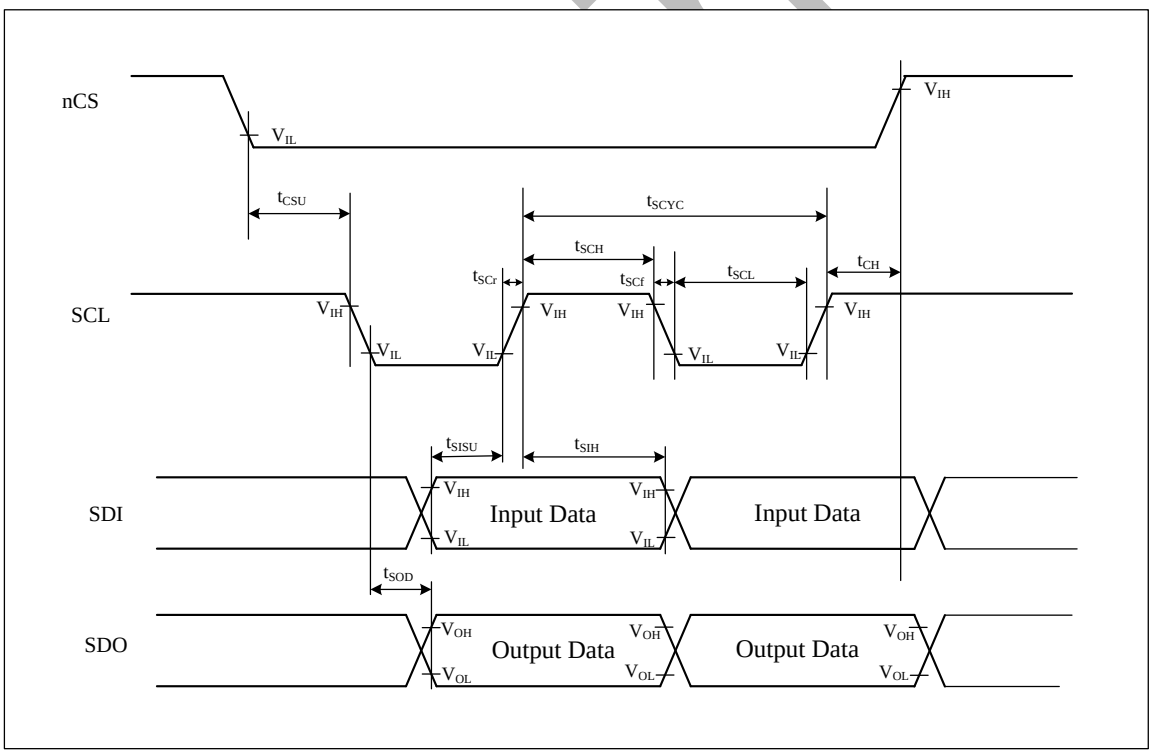


Figure48 SPI System Bus Timing

11.4.4. RGB Interface Timing Characteristics

8/16-bit Bus RGB Interface Mode (VDDI = 1.65 ~ 3.3V, VCI=2.5~3.3V)

Item	symbol	unit	min	Type	max	Test Condition
VSYNC/HSYNC setup time	t_{SYNC}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	20	-	-	-
ENABLE hold time	t_{ENH}	ns	30	-	-	-
PD Data setup time	t_{PDS}	ns	20	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	Frame rate under 100Hz
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr} , t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (VDDI = 1.65 ~ 3.3V, VCI=2.5~3.3V)

Item	symbol	unit	min	Type	max	Test Condition
VSYNC/HSYNC setup time	t_{SYNC}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	20	-	-	-
ENABLE hold time	t_{ENH}	ns	30	-	-	-
PD Data setup time	t_{PDS}	ns	20	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	Frame rate under 100Hz
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rgbr} , t_{rgbf}	ns	-	-	25	-

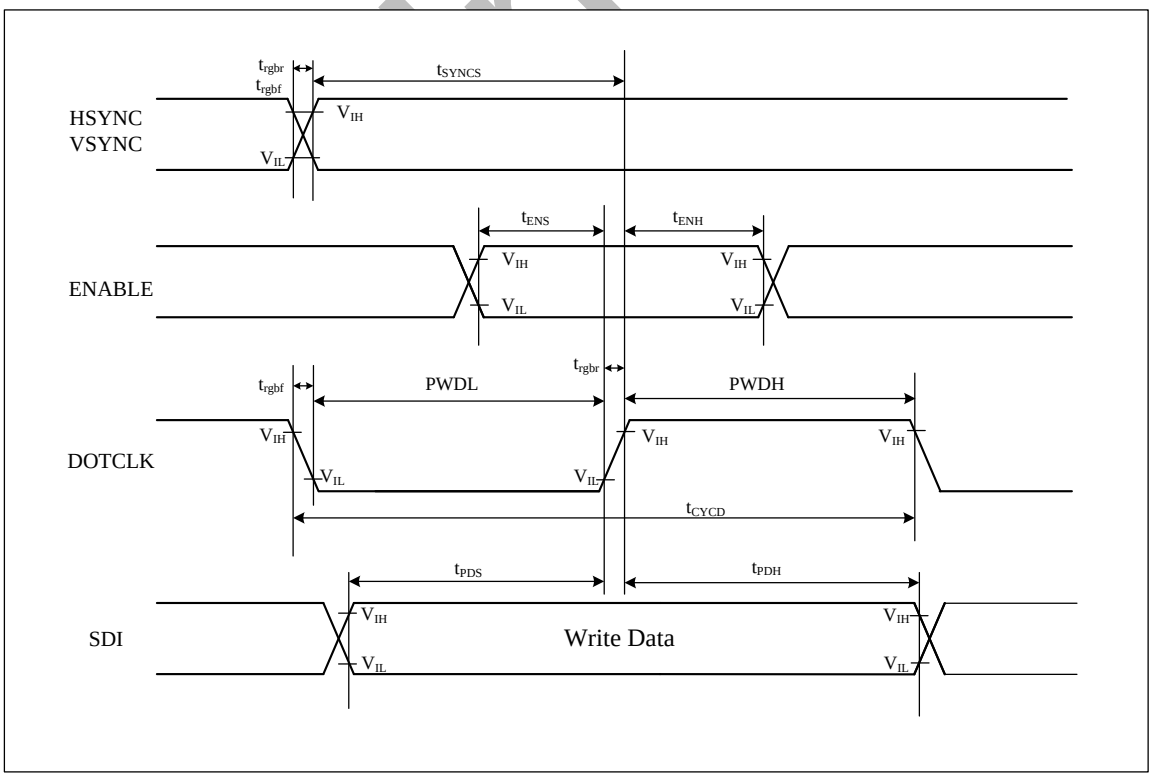


Figure49 RGB Interface Timing

12. Revision History

Version No.	Date	Page	Description
V1.00	2016-1-21	All	New Created