GC9503V

a-Si TFT LCD Single-Chip Driver 480(RGB)x864 Resolution, 16.7M-color Without internal GRAM

Specification

Version 1.00
2017.03.30

GalaxyCore Incorporation

List of Content

1 DESCRIPTION

The GC9503V device is a single-chip solution for a-Si TFT LCD that incorporates gate drivers and is capable of 480RGBx864, 480RGBx854, 480RGBx800, 480RGBx720, 480RGBx640, 480RGBx360 and 480RGBx320 without internal GRAM. It includes a timing controller with glass interface level-shifters and a glass power supply circuit.

The GC9503V supports MIPI Interface, 16/18/24 bits RGB interface, serial peripheral interfaces (SPI) interface. The GC9503V is also able to make gamma correction settings separately for RGB dots to panel characteristics, resulting in higher display qualities.

This LSI is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, including bi-directional pagers, digital audio players, cellular phones and handheld PDA.

2 FEATURES

Display resolution option
- 480RGB x 864
- 480RGB x 854
- 480RGB x 800
- 480RGB x 720
- 480RGB x 640
- 480RGB x 360
- 480RGB x 320

Display mode (Color mode)
- Full color mode: 16.7M-colors
- Reduce color mode: 262K colors
- Reduce color mode: 65K colors
- Idle mode: 8 colors

Interface
- 8-bit, 9-bit and 16-bit serial peripheral interface
- 16-/18-/24-bits RGB interface (DE mode and SYNC mode with polarity of HS/VS can be set by register)
- MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 or 2 data lane pairs)
  Supports one data lanes / maximum speed 500Mbps
  Supports two data lanes / maximum speed 500Mbps

Display features
- Individual gamma correction setting for RGB dots
- Deep standby function

On chip Build-In Circuits
- DC/DC Converter
- VGHO/VGLO voltage generator for gate control signal and panel
- Oscillator for display clock
- Supports gate control signals to gate driver in the panel

Driving Algorithm Support
- Column Inversion
- Zigzag Inversion

Supply voltage range
- I/O supply voltage range for VDDI to VSSI: 1.65V ~ 3.3V
- Analog supply voltage range for VDDB/VDDA/VDDR to VSSB/VSSA/VSSR: 2.5V ~ 3.3V
- MIPI regulator supply voltage range for VDDAM to VSSAM: 2.5V ~ 3.3V Output voltage levels

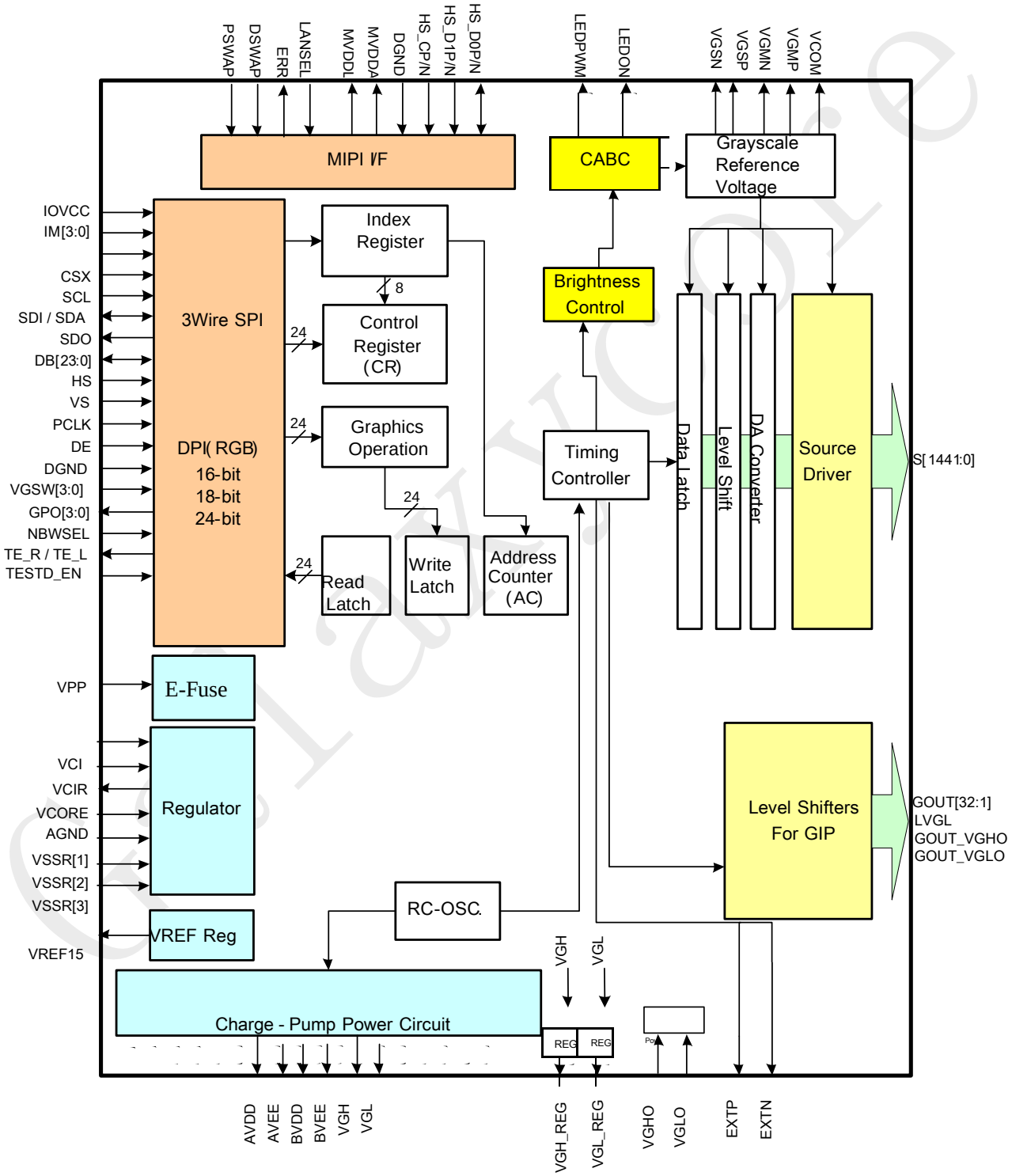
On-Chip Power System
- Positive gate driver voltage range for VGH: 9.0 ~ 12.5V
- Negative gate driver voltage range for VGLX: -8.0~ -11.5V
- Step-up 1 output voltage range for AVDD/BVDD: 6.01 ~ 7.4V

- Step-up 1 output voltage range for AVDD/BVDD: 6.01 ~ 7.4V

- Step-up 2 output voltage range for AVEE: -4.25 ~ -6.0V
- Step-up 2 output voltage range for BVEE: -4.5~ -5.2V
- Positive gamma high voltage range for VGMP: 5.7 ~ 6.3V (AVDD-0.5V)
- Positive gamma low voltage range for VGSP: 0.7 ~ 1.3V
- Negative gamma high voltage range for VGMN: -3.7 ~ -4.3V (AVEE+0.5V)
- Negative gamma low voltage range for VGSN: 0.7 ~ 1.3V
- Common electrode voltage range for VCOM: GND Level

Operate temperature range: −30℃ to +85℃

3 BLOCK DIAGRAM



4 PIN DESCRIPTION

4.1 PIN DESCRIPTION

<table>
<tr><th colspan="3">Bus Interface Pins</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>-Select the interface mode
Interface type selection. The connections of IM[3:0] which not shown in table are invalid.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8-bit spi(scl rising edge trigger),SDI/SDO</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8-bit spi(scl falling edge trigger),SDI/SDO</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>9-bit spi(scl rising edge trigger),SDI/SDO</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>9-bit spi(scl falling edge trigger),SDI/SDO</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>16-bit spi(scl rising edge trigger),SDI/SDO</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>16-bit spi(scl falling edge trigger),SDI/SDO</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="2">MIPI DSI,HSSI_D0_P/N,HSSI_D1_P/N</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>- The external reset input.
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>CSX</td><td>I</td><td>-A chip select signal.
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to DGND level when not in use.</td></tr>
<tr><td>SCL</td><td>I</td><td>- The SPI Interface (SCL): Serves as a write signal and writes data at the rising edge.
- Serial interface (SCL): Serial clock input.
Fix to DGND level when not in use.</td></tr>
<tr><td>DB[23:0]</td><td>I/O</td><td>- A 24-bit parallel bi-directional data bus for DPI (RGB) I/F
Fix to DGND level when not in use</td></tr>
<tr><td>SDI (SDA)</td><td>I/O</td><td>Serial data input pin used for the SPI Interface. SDI : Serial data input pin</td></tr>
</table>

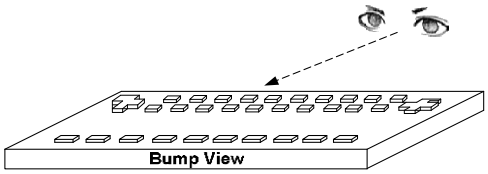
<table>
<tr><td></td><td></td><td>SDA : Serial data input/output bidirectional pin
Fix to DGND level when not in use</td></tr>
<tr><td>PCLK</td><td>I</td><td>- Dot clock signal for DPI (RGB) interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>VS</td><td>I</td><td>- Frame synchronizing signal for DPI (RGB) interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>HS</td><td>I</td><td>- Line synchronizing signal for DPI (RGB) interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>DE</td><td>I</td><td>- Data enable signal for DPI (RGB) interface operation.
Low : access enabled.
High : access inhibited.
Fix to DGND level when not in use.</td></tr>
<tr><td>HS_CP HS_CN</td><td>I</td><td>MIPI DSI differential clock pair (DSI-CLK+/-).
If MIPI are not used, they should be connected to DGND.</td></tr>
<tr><td>HS_D0P
HS_D0N
HS_D1P
HS_D1N</td><td>I/O</td><td>MIPI DSI differential data pair (DSI-Dn+/-).
If MIPI are not used, they should be connected to DGND</td></tr>
<tr><td>ERR</td><td>O</td><td>- CRC and ECC error output pin for MIPI interface, activated by S/W command. This pin is output low when it is not activated. When this pin is activated, it output high if CRC/ECC error found.
Leave the pin to open when not in use.</td></tr>
<tr><td>LANSEL</td><td>I</td><td>- Input pin to select 1 data lane or 2 data lanes in MIPI interface.
Low: 1 data lane. High: 2 data lanes.
- The pin have internal pull low resister.
Fix to DGND level when not in use.</td></tr>
<tr><td>DSWAP PSWAP</td><td>I</td><td>- Differential clock polarity swap
For MIPI DSI interface
<table>
<tr><td colspan="2">Pin Name</td><td>HS_D0P</td><td>HS_D0N</td><td>HS_CP</td><td>HS_CN</td><td>HS_D1P</td><td>HS_D1N</td></tr>
<tr><td rowspan="4">Input MIPI Signal</td><td>DSWAP=0
PSWAP=0</td><td>DSI-D0+</td><td>DSI-D0-</td><td>DSI-CLK+</td><td>DSI-CLK-</td><td>DSI-D1+</td><td>DSI-D1-</td></tr>
<tr><td>DSWAP=0
PSWAP=1</td><td>DSI-D0-</td><td>DSI-D0+</td><td>DSI-CLK-</td><td>DSI-CLK+</td><td>DSI-D1-</td><td>DSI-D1+</td></tr>
<tr><td>DSWAP=1
PSWAP=0</td><td>DSI-D1+</td><td>DSI-D1-</td><td>DSI-CLK+</td><td>DSI-CLK-</td><td>DSI-D0+</td><td>DSI-D0-</td></tr>
<tr><td>DSWAP=1
PSWAP=1</td><td>DSI-D1-</td><td>DSI-D1+</td><td>DSI-CLK-</td><td>DSI-CLK+</td><td>DSI-D0-</td><td>DSI-D0+</td></tr>
</table></td></tr>
</table>

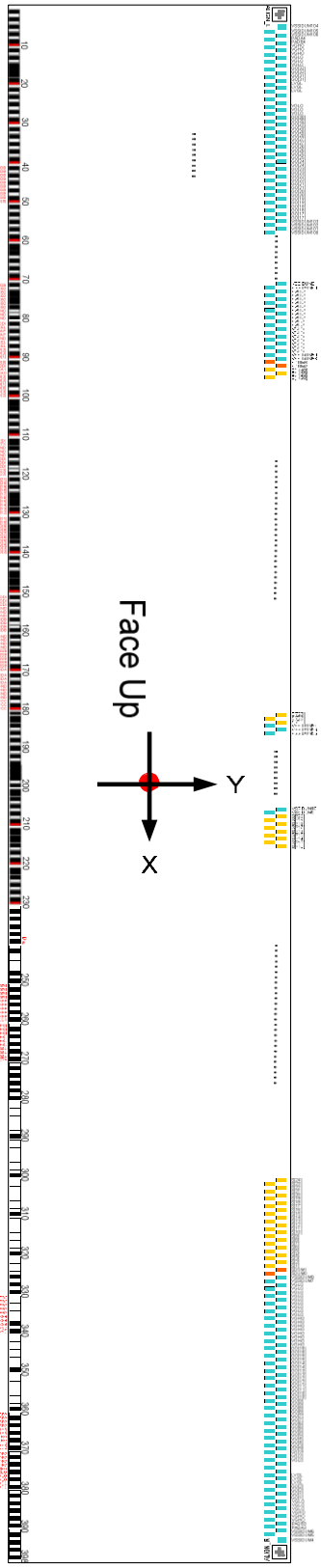
		Fix to DGND level when not in use.
NBWSEL	I	- Input pin to select the gamma voltage level sequence of V0~V255. Low: V0>V1>…>V254>V255, normally white. High: V255>V254>…>V1>V0, normally black. Fix to DGND level when not in use.
VGSW[3:0]	I	- Input pin to select the different application. - The pins have internal pull-low resister. Leave the pin to open when not in use.
GPO[3:0]	O	- General purpose output pins. Leave the pin to open when not in use.
LEDON	O	- Used for turning On/Off external LED backlight control. Leave the pin to open when not in use.
LEDPWM	O	- The PWM frequency output for LED driver control. Leave the pin to open when not in use.
Driver Output		
Pin Name	**I/O**	**Description**
S[1:1440]	O	- Source output voltage signals applied to a LCD panel.
GOUT[1:32]	O	- Gate control signals and the swing voltage level is VGHO to VGLO.
GOUT_VGHO	O	- High voltage level for GIP control signals and gate circuit of panel.
GOUT_VGLO	O	- Low voltage level for GIP control signals and gate circuit of panel.
VGHO	O	- High voltage level for GIP control signals and gate circuit of panel.
VGLO	O	- Low voltage level for GIP control signals and gate circuit of panel.
LVGL	O	- Low voltage level for gate circuit of panel.
VCOM	O	- Regulator output for common voltage of panel.
Charge Pump Pin		
Pin Name	**I/O**	**Description**
AVDD	O	OPEN
AVEE	O	OPEN
BVDD	O	OPEN
BVEE	O	OPEN
VCL	O	OPEN
VGH	O	OPEN
VGL	O	OPEN

Power Pin		
Pin Name	**I/O**	**Description**
VDDA	P	- Power supply for analog system. - VDDA,VDDB and VDDR should be the same input voltage level of 2.5 ~ 3.3V.
VDDR	P	- Power supply for regulator low voltage reference circuit. - VDDA,VDDB and VDDR should be the same input voltage level of 2.5 ~ 3.3V.
VDDB	P	- Power supply for DC/DC converter. - VDDA,VDDB and VDDR should be the same input voltage level of 2.5 ~ 3.3V.
IOVCC	P	- Power supply for I/O block. ***Excluded MIPI interface.***
VCORE	O	- internal logic voltage output
VGH_REG	O	- Output voltage generated from VGH. ***Leave the pin to open when not in use.***
VGL_REG	O	- Output voltage generated from VGL. LDO output used for panel voltage. ***Leave the pin to open when not in use.***
VGMP/VGSP	O	- Output voltage generated from DDVDH. LDO output for positive gamma voltage generator.
VGMN/VGSN	O	- Output voltage generated from DDVDL. LDO output for negative gamma voltage generator.
MVDDA	O	- Regulator output for internal MIPI DSI analog system (1.5V typical)
MVDDL	O	- Regulator output for internal MIPI DSI low power system (1.2V typical)
VSSA	P	- System ground for analog circuit.
VSSAM		- System ground for MIPI circuit.
VSSR		- System ground for internal digital system.
VSSB	P	- System ground for DC/DC convertor.
VSSI	P	- System ground for
VPP	I	- OTP programming power.

4.2 Output Bump Dimension

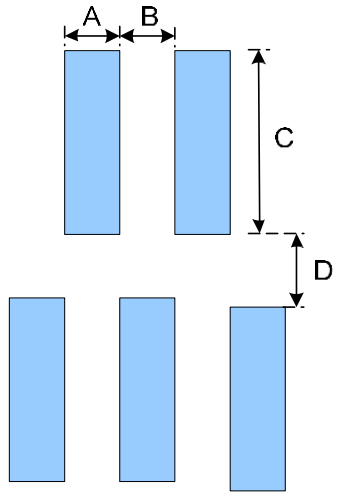
Au bump height	9 μm
Au bump size	14 μmx95 μm Gate : GO1~GO32 Source : S1~S1440
	40 μmx84 μm Input Pads : Pad 1 to Pad 398





4.3 Input Bump Dimension

- **Output Pads**



P400~P2076

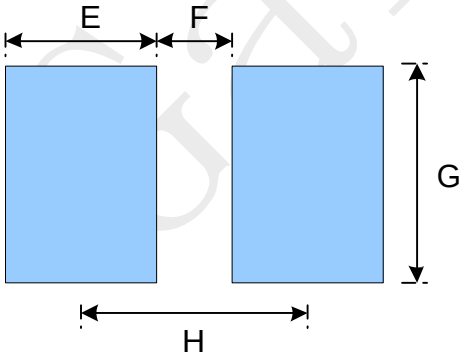
Symbol	Item	Size
A	Bump Width	14 um
B	Bump Gap 1 (Horizontal)	14 um
C	Bump Height	95 um
D	Bump Gap 2 (Vertical)	28 um

P399、P2077

Symbol	Item	Size
A	Bump Width	42 um
B	Bump Gap 1 (Horizontal)	14 um
C	Bump Height	95 um
D	Bump Gap 2 (Vertical)	28 um

- **Input Pads**

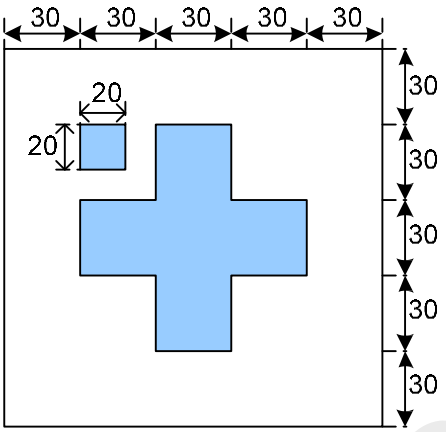
No.1~398



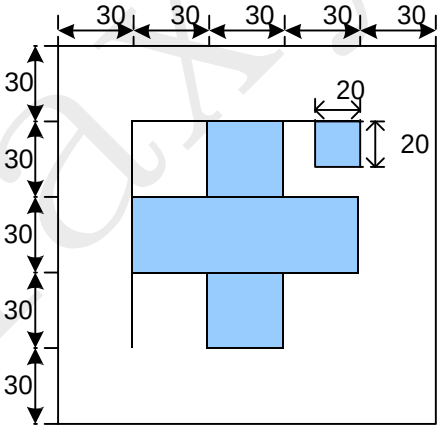
Symbol	Item	Size
E	Bump Width	40 um
F	Bump Gap	20um
G	Bump Height	84 um
H	Bump Pitch	60 um

4.4 Alignment Mark Dimension

- **Alignment Mark ALIGN_L : (X,Y)=(-11870,302)**



- **Alignment Mark ALIGN_R : (X,Y)=(+11870,302)**



4.5 Chip Information

Chip size	24000 μm x800 μm
Chip thickness	250 μm
Pad Location	Pad center
Coordinate Origin	Chip center

4.6 Pad Coordination

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1	DMY_VSS	-11910	-315	61	VREG2OUT	-8310	-315	121	DB[21]	-4710	-315	181	VCORE	-1110	-315
2	DMY_VSS	-11850	-315	62	VREG1OUT	-8250	-315	122	DB[20]	-4650	-315	182	DGND	-1050	-315
3	DMY_VSS	-11790	-315	63	DGND	-8190	-315	123	DB[19]	-4590	-315	183	DGND	-990	-315
4	PADA1	-11730	-315	64	DGND	-8130	-315	124	DB[18]	-4530	-315	184	DGND	-930	-315
5	PADB1	-11670	-315	65	DGND	-8070	-315	125	DB[17]	-4470	-315	185	DGND	-870	-315
6	VCOM	-11610	-315	66	VCORE	-8010	-315	126	DB[16]	-4410	-315	186	DGND	-810	-315
7	VCOM	-11550	-315	67	VCORE	-7950	-315	127	DB[15]	-4350	-315	187	HS_D1P	-750	-315
8	VCOM	-11490	-315	68	VCORE	-7890	-315	128	DB[14]	-4290	-315	188	HS_D1P	-690	-315
9	VCOM	-11430	-315	69	VCI	-7830	-315	129	DB[13]	-4230	-315	189	HS_D1P	-630	-315
10	VCOM	-11370	-315	70	VCI	-7770	-315	130	DB[12]	-4170	-315	190	HS_D1P	-570	-315
11	CONTACT1A	-11310	-315	71	VCI	-7710	-315	131	DB[11]	-4110	-315	191	HS_D1N	-510	-315
12	CONTACT1B	-11250	-315	72	VCL	-7650	-315	132	DB[10]	-4050	-315	192	HS_D1N	-450	-315
13	VPP	-11190	-315	73	VCL	-7590	-315	133	DB[9]	-3990	-315	193	HS_D1N	-390	-315
14	VPP	-11130	-315	74	VCL	-7530	-315	134	DB[8]	-3930	-315	194	HS_D1N	-330	-315
15	VPP	-11070	-315	75	VCL	-7470	-315	135	DB[7]	-3870	-315	195	DGND	-270	-315
16	VPP	-11010	-315	76	VCL	-7410	-315	136	DB[6]	-3810	-315	196	DGND	-210	-315
17	VPP	-10950	-315	77	VCL	-7350	-315	137	DB[5]	-3750	-315	197	HS_CP	-150	-315
18	VGL	-10890	-315	78	AGND	-7290	-315	138	DB[4]	-3690	-315	198	HS_CP	-90	-315
19	VGL	-10830	-315	79	AGND	-7230	-315	139	DB[3]	-3630	-315	199	HS_CP	-30	-315
20	VGLO	-10770	-315	80	AGND	-7170	-315	140	DB[2]	-3570	-315	200	HS_CP	30	-315
21	VGLO	-10710	-315	81	IOVCC	-7110	-315	141	DB[1]	-3510	-315	201	HS_CN	90	-315
22	VGL_REG	-10650	-315	82	LANSEL	-7050	-315	142	DB[0]	-3450	-315	202	HS_CN	150	-315
23	VGL_REG	-10590	-315	83	DSWAP	-6990	-315	143	DE	-3390	-315	203	HS_CN	210	-315
24	VGH_REG	-10530	-315	84	PSWAP	-6930	-315	144	PCLK	-3330	-315	204	HS_CN	270	-315
25	VGH_REG	-10470	-315	85	DGND	-6870	-315	145	HS	-3270	-315	205	DGND	330	-315
26	VCL	-10410	-315	86	TESTDIN[6]	-6810	-315	146	VS	-3210	-315	206	DGND	390	-315
27	VCL	-10350	-315	87	NBWSEL	-6750	-315	147	LEDPWM	-3150	-315	207	HS_D0P	450	-315
28	VCL	-10290	-315	88	VGSW[3]	-6690	-315	148	LEDON	-3090	-315	208	HS_D0P	510	-315
29	VCL	-10230	-315	89	VGSW[2]	-6630	-315	149	DMY	-3030	-315	209	HS_D0P	570	-315
30	VREF15	-10170	-315	90	VGSW[1]	-6570	-315	150	ERR	-2970	-315	210	HS_D0P	630	-315
31	VREF15	-10110	-315	91	VGSW[0]	-6510	-315	151	IOVCC	-2910	-315	211	HS_D0N	690	-315
32	VREF15	-10050	-315	92	IOVCC	-6450	-315	152	IOVCC	-2850	-315	212	HS_D0N	750	-315
33	VREF15	-9990	-315	93	TESTDIN[7]	-6390	-315	153	IOVCC	-2790	-315	213	HS_D0N	810	-315
34	AGND	-9930	-315	94	TESTDOUT[0]	-6330	-315	154	DGND	-2730	-315	214	HS_D0N	870	-315
35	AGND	-9870	-315	95	IM[3]	-6270	-315	155	DGND	-2670	-315	215	DGND	930	-315
36	AGND	-9810	-315	96	IM[2]	-6210	-315	156	DGND	-2610	-315	216	DGND	990	-315
37	AGND	-9750	-315	97	IM[1]	-6150	-315	157	DDVDH	-2550	-315	217	V12_MIPI	1050	-315
38	VCI	-9690	-315	98	IM[0]	-6090	-315	158	DDVDH	-2490	-315	218	V12_MIPI	1110	-315
39	VCI	-9630	-315	99	GPO[3]	-6030	-315	159	DDVDH	-2430	-315	219	V12_MIPI	1170	-315
40	VCI	-9570	-315	100	GPO[2]	-5970	-315	160	DDVDH	-2370	-315	220	VCORE_MIPI	1230	-315
41	VCI	-9510	-315	101	GPO[1]	-5910	-315	161	AGND	-2310	-315	221	VCORE_MIPI	1290	-315
42	VCIR	-9450	-315	102	GPO[0]	-5850	-315	162	AGND	-2250	-315	222	VCORE_MIPI	1350	-315
43	VCIR	-9390	-315	103	TESTDOUT[1]	-5790	-315	163	AGND	-2190	-315	223	VCI	1410	-315
44	VCIR	-9330	-315	104	TE_L	-5730	-315	164	AGND	-2130	-315	224	VCI	1470	-315
45	VCIR	-9270	-315	105	TESTDOUT[2]	-5670	-315	165	DDVDL	-2070	-315	225	VCI	1530	-315
46	VSSR[1]	-9210	-315	106	SDO	-5610	-315	166	DDVDL	-2010	-315	226	VCI	1590	-315
47	VSSR[1]	-9150	-315	107	SDI	-5550	-315	167	DDVDL	-1950	-315	227	VCI	1650	-315
48	VSSR[1]	-9090	-315	108	TESTDOUT[3]	-5490	-315	168	DDVDL	-1890	-315	228	VCI	1710	-315
49	VSSR[1]	-9030	-315	109	SCL	-5430	-315	169	DDVDL	-1830	-315	229	VCI	1770	-315
50	TESTDIN[0]	-8970	-315	110	TESTD_EN	-5370	-315	170	VCI	-1770	-315	230	VCI	1830	-315
51	TESTDIN[1]	-8910	-315	111	CSX	-5310	-315	171	VCI	-1710	-315	231	DMY	1890	-315
52	TESTDIN[2]	-8850	-315	112	RESX	-5250	-315	172	VCI	-1650	-315	232	TE_R	1950	-315
53	TESTDIN[3]	-8790	-315	113	DGND	-5190	-315	173	VCI	-1590	-315	233	VSSR[2]	2010	-315
54	DMY	-8730	-315	114	DGND	-5130	-315	174	DGND	-1530	-315	234	VSSR[2]	2070	-315
55	TESTDIN[4]	-8670	-315	115	DGND	-5070	-315	175	DGND	-1470	-315	235	VSSR[2]	2130	-315
56	TESTDIN[5]	-8610	-315	116	IOVCC	-5010	-315	176	DGND	-1410	-315	236	VSSR[2]	2190	-315
57	DMY	-8550	-315	117	IOVCC	-4950	-315	177	DGND	-1350	-315	237	DMY	2250	-315
58	DMY	-8490	-315	118	IOVCC	-4890	-315	178	VCORE	-1290	-315	238	DMY	2310	-315
59	DMY	-8430	-315	119	DB[23]	-4830	-315	179	VCORE	-1230	-315	239	VGH_REG	2370	-315
60	VREG2OUT	-8370	-315	120	DB[22]	-4770	-315	180	VCORE	-1170	-315	240	VGH_REG	2430	-315

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
241	EXTP	2490	-315	301	C21P	6090	-315	361	C41P	9690	-315	421	GOUT_VGLO	11438	312.5
242	EXTP	2550	-315	302	C21P	6150	-315	362	C41P	9750	-315	422	GOUT_VGLO	11424	187.5
243	DMY	2610	-315	303	C21N	6210	-315	363	C41N	9810	-315	423	GOUT[3]	11410	312.5
244	DMY	2670	-315	304	C21N	6270	-315	364	C41N	9870	-315	424	GOUT[3]	11396	187.5
245	EXTN	2730	-315	305	C21N	6330	-315	365	VGH	9930	-315	425	GOUT[4]	11382	312.5
246	EXTN	2790	-315	306	C22P	6390	-315	366	VGH	9990	-315	426	GOUT[4]	11368	187.5
247	DMY	2850	-315	307	C22P	6450	-315	367	VGHO	10050	-315	427	GOUT[5]	11354	312.5
248	DMY	2910	-315	308	C22P	6510	-315	368	VGHO	10110	-315	428	GOUT[5]	11340	187.5
249	VCIP	2970	-315	309	C22N	6570	-315	369	VGH_REG	10170	-315	429	GOUT[6]	11326	312.5
250	VCIP	3030	-315	310	C22N	6630	-315	370	VGH_REG	10230	-315	430	GOUT[6]	11312	187.5
251	VCIP	3090	-315	311	C22N	6690	-315	371	C51P	10290	-315	431	GOUT[7]	11298	312.5
252	VCIP	3150	-315	312	C23P	6750	-315	372	C51P	10350	-315	432	GOUT[7]	11284	187.5
253	VCIP	3210	-315	313	C23P	6810	-315	373	C51N	10410	-315	433	GOUT[8]	11270	312.5
254	VCIP	3270	-315	314	C23P	6870	-315	374	C51N	10470	-315	434	GOUT[8]	11256	187.5
255	CGND	3330	-315	315	C23N	6930	-315	375	VGL_REG	10530	-315	435	GOUT[9]	11242	312.5
256	CGND	3390	-315	316	C23N	6990	-315	376	VGL_REG	10590	-315	436	GOUT[9]	11228	187.5
257	CGND	3450	-315	317	C23N	7050	-315	377	VGLO	10650	-315	437	GOUT[10]	11214	312.5
258	CGND	3510	-315	318	C24P	7110	-315	378	VGLO	10710	-315	438	GOUT[10]	11200	187.5
259	CGND	3570	-315	319	C24P	7170	-315	379	VGL	10770	-315	439	GOUT[11]	11186	312.5
260	CGND	3630	-315	320	C24P	7230	-315	380	VGL	10830	-315	440	GOUT[11]	11172	187.5
261	C11P	3690	-315	321	C24N	7290	-315	381	VGL	10890	-315	441	GOUT[12]	11158	312.5
262	C11P	3750	-315	322	C24N	7350	-315	382	VGL	10950	-315	442	GOUT[12]	11144	187.5
263	C11P	3810	-315	323	C24N	7410	-315	383	DMY	11010	-315	443	GOUT[13]	11130	312.5
264	C11N	3870	-315	324	VCIP	7470	-315	384	DMY	11070	-315	444	GOUT[13]	11116	187.5
265	C11N	3930	-315	325	VCIP	7530	-315	385	DMY	11130	-315	445	GOUT[14]	11102	312.5
266	C11N	3990	-315	326	VCIP	7590	-315	386	DMY	11190	-315	446	GOUT[14]	11088	187.5
267	C12P	4050	-315	327	VCIP	7650	-315	387	CONTACT2A	11250	-315	447	GOUT[15]	11074	312.5
268	C12P	4110	-315	328	VCIP	7710	-315	388	CONTACT2B	11310	-315	448	GOUT[15]	11060	187.5
269	C12P	4170	-315	329	VCL	7770	-315	389	VCOM	11370	-315	449	GOUT[16]	11046	312.5
270	C12N	4230	-315	330	VCL	7830	-315	390	VCOM	11430	-315	450	GOUT[16]	11032	187.5
271	C12N	4290	-315	331	VCL	7890	-315	391	VCOM	11490	-315	451	GOUT_VGHO	11018	312.5
272	C12N	4350	-315	332	VCL	7950	-315	392	VCOM	11550	-315	452	GOUT_VGHO	11004	187.5
273	C13P	4410	-315	333	VCL	8010	-315	393	VCOM	11610	-315	453	GOUT_VGHO	10990	312.5
274	C13P	4470	-315	334	VCL	8070	-315	394	PADA2	11670	-315	454	GOUT_VGHO	10976	187.5
275	C13P	4530	-315	335	VCL	8130	-315	395	PADB2	11730	-315	455	GOUT_VGHO	10962	312.5
276	C13N	4590	-315	336	VSSR[3]	8190	-315	396	DMY_VSS	11790	-315	456	GOUT_VGHO	10948	187.5
277	C13N	4650	-315	337	VSSR[3]	8250	-315	397	DMY_VSS	11850	-315	457	DMY_VGH	10934	312.5
278	C13N	4710	-315	338	VSSR[3]	8310	-315	398	DMY_VSS	11910	-315	458	DMY_VGH	10920	187.5
279	C14P	4770	-315	339	CGND	8370	-315	399	DMY_VSS	11760	312.5	459	GOUT_VGLO	10906	312.5
280	C14P	4830	-315	340	CGND	8430	-315	400	DMY_VSS	11732	187.5	460	GOUT_VGLO	10892	187.5
281	C14P	4890	-315	341	CGND	8490	-315	401	DMY_VSS	11718	312.5	461	GOUT_VGLO	10878	312.5
282	C14N	4950	-315	342	CGND	8550	-315	402	PADA3	11704	187.5	462	GOUT_VGLO	10864	187.5
283	C14N	5010	-315	343	C31P	8610	-315	403	PADB3	11690	312.5	463	GOUT_VGLO	10850	312.5
284	C14N	5070	-315	344	C31P	8670	-315	404	GOUT_VGHO	11676	187.5	464	GOUT_VGLO	10836	187.5
285	DDVDH	5130	-315	345	C31P	8730	-315	405	GOUT_VGHO	11662	312.5	465	DMY_VSS	10766	312.5
286	DDVDH	5190	-315	346	C31N	8790	-315	406	GOUT_VGHO	11648	187.5	466	DMY_VSS	10752	187.5
287	DDVDH	5250	-315	347	C31N	8850	-315	407	GOUT_VGLO	11634	312.5	467	S[0]	10738	312.5
288	DDVDH	5310	-315	348	C31N	8910	-315	408	GOUT_VGLO	11620	187.5	468	S[1]	10724	187.5
289	CGND	5370	-315	349	C32P	8970	-315	409	GOUT_VGLO	11606	312.5	469	S[2]	10710	312.5
290	CGND	5430	-315	350	C32P	9030	-315	410	GOUT[1]	11592	187.5	470	S[3]	10696	187.5
291	CGND	5490	-315	351	C32P	9090	-315	411	GOUT[1]	11578	312.5	471	S[4]	10682	312.5
292	CGND	5550	-315	352	C32N	9150	-315	412	GOUT[2]	11564	187.5	472	S[5]	10668	187.5
293	CGND	5610	-315	353	C32N	9210	-315	413	GOUT[2]	11550	312.5	473	S[6]	10654	312.5
294	DDVDL	5670	-315	354	C32N	9270	-315	414	LVGL	11536	187.5	474	S[7]	10640	187.5
295	DDVDL	5730	-315	355	VCORE	9330	-315	415	LVGL	11522	312.5	475	S[8]	10626	312.5
296	DDVDL	5790	-315	356	VCORE	9390	-315	416	LVGL	11508	187.5	476	S[9]	10612	187.5
297	DDVDL	5850	-315	357	VCORE	9450	-315	417	VGH_REG	11494	312.5	477	S[10]	10598	312.5
298	DDVDL	5910	-315	358	AGND	9510	-315	418	VGH_REG	11480	187.5	478	S[11]	10584	187.5
299	DDVDL	5970	-315	359	AGND	9570	-315	419	VGH_REG	11466	312.5	479	S[12]	10570	312.5
300	C21P	6030	-315	360	AGND	9630	-315	420	GOUT_VGLO	11452	187.5	480	S[13]	10556	187.5

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
481	S[14]	10542	312.5	541	S[74]	9702	312.5	601	S[134]	8862	312.5	661	S[194]	8022	312.5
482	S[15]	10528	187.5	542	S[75]	9688	187.5	602	S[135]	8848	187.5	662	S[195]	8008	187.5
483	S[16]	10514	312.5	543	S[76]	9674	312.5	603	S[136]	8834	312.5	663	S[196]	7994	312.5
484	S[17]	10500	187.5	544	S[77]	9660	187.5	604	S[137]	8820	187.5	664	S[197]	7980	187.5
485	S[18]	10486	312.5	545	S[78]	9646	312.5	605	S[138]	8806	312.5	665	S[198]	7966	312.5
486	S[19]	10472	187.5	546	S[79]	9632	187.5	606	S[139]	8792	187.5	666	S[199]	7952	187.5
487	S[20]	10458	312.5	547	S[80]	9618	312.5	607	S[140]	8778	312.5	667	S[200]	7938	312.5
488	S[21]	10444	187.5	548	S[81]	9604	187.5	608	S[141]	8764	187.5	668	S[201]	7924	187.5
489	S[22]	10430	312.5	549	S[82]	9590	312.5	609	S[142]	8750	312.5	669	S[202]	7910	312.5
490	S[23]	10416	187.5	550	S[83]	9576	187.5	610	S[143]	8736	187.5	670	S[203]	7896	187.5
491	S[24]	10402	312.5	551	S[84]	9562	312.5	611	S[144]	8722	312.5	671	S[204]	7882	312.5
492	S[25]	10388	187.5	552	S[85]	9548	187.5	612	S[145]	8708	187.5	672	S[205]	7868	187.5
493	S[26]	10374	312.5	553	S[86]	9534	312.5	613	S[146]	8694	312.5	673	S[206]	7854	312.5
494	S[27]	10360	187.5	554	S[87]	9520	187.5	614	S[147]	8680	187.5	674	S[207]	7840	187.5
495	S[28]	10346	312.5	555	S[88]	9506	312.5	615	S[148]	8666	312.5	675	S[208]	7826	312.5
496	S[29]	10332	187.5	556	S[89]	9492	187.5	616	S[149]	8652	187.5	676	S[209]	7812	187.5
497	S[30]	10318	312.5	557	S[90]	9478	312.5	617	S[150]	8638	312.5	677	S[210]	7798	312.5
498	S[31]	10304	187.5	558	S[91]	9464	187.5	618	S[151]	8624	187.5	678	S[211]	7784	187.5
499	S[32]	10290	312.5	559	S[92]	9450	312.5	619	S[152]	8610	312.5	679	S[212]	7770	312.5
500	S[33]	10276	187.5	560	S[93]	9436	187.5	620	S[153]	8596	187.5	680	S[213]	7756	187.5
501	S[34]	10262	312.5	561	S[94]	9422	312.5	621	S[154]	8582	312.5	681	S[214]	7742	312.5
502	S[35]	10248	187.5	562	S[95]	9408	187.5	622	S[155]	8568	187.5	682	S[215]	7728	187.5
503	S[36]	10234	312.5	563	S[96]	9394	312.5	623	S[156]	8554	312.5	683	S[216]	7714	312.5
504	S[37]	10220	187.5	564	S[97]	9380	187.5	624	S[157]	8540	187.5	684	S[217]	7700	187.5
505	S[38]	10206	312.5	565	S[98]	9366	312.5	625	S[158]	8526	312.5	685	S[218]	7686	312.5
506	S[39]	10192	187.5	566	S[99]	9352	187.5	626	S[159]	8512	187.5	686	S[219]	7672	187.5
507	S[40]	10178	312.5	567	S[100]	9338	312.5	627	S[160]	8498	312.5	687	S[220]	7658	312.5
508	S[41]	10164	187.5	568	S[101]	9324	187.5	628	S[161]	8484	187.5	688	S[221]	7644	187.5
509	S[42]	10150	312.5	569	S[102]	9310	312.5	629	S[162]	8470	312.5	689	S[222]	7630	312.5
510	S[43]	10136	187.5	570	S[103]	9296	187.5	630	S[163]	8456	187.5	690	S[223]	7616	187.5
511	S[44]	10122	312.5	571	S[104]	9282	312.5	631	S[164]	8442	312.5	691	S[224]	7602	312.5
512	S[45]	10108	187.5	572	S[105]	9268	187.5	632	S[165]	8428	187.5	692	S[225]	7588	187.5
513	S[46]	10094	312.5	573	S[106]	9254	312.5	633	S[166]	8414	312.5	693	S[226]	7574	312.5
514	S[47]	10080	187.5	574	S[107]	9240	187.5	634	S[167]	8400	187.5	694	S[227]	7560	187.5
515	S[48]	10066	312.5	575	S[108]	9226	312.5	635	S[168]	8386	312.5	695	S[228]	7546	312.5
516	S[49]	10052	187.5	576	S[109]	9212	187.5	636	S[169]	8372	187.5	696	S[229]	7532	187.5
517	S[50]	10038	312.5	577	S[110]	9198	312.5	637	S[170]	8358	312.5	697	S[230]	7518	312.5
518	S[51]	10024	187.5	578	S[111]	9184	187.5	638	S[171]	8344	187.5	698	S[231]	7504	187.5
519	S[52]	10010	312.5	579	S[112]	9170	312.5	639	S[172]	8330	312.5	699	S[232]	7490	312.5
520	S[53]	9996	187.5	580	S[113]	9156	187.5	640	S[173]	8316	187.5	700	S[233]	7476	187.5
521	S[54]	9982	312.5	581	S[114]	9142	312.5	641	S[174]	8302	312.5	701	S[234]	7462	312.5
522	S[55]	9968	187.5	582	S[115]	9128	187.5	642	S[175]	8288	187.5	702	S[235]	7448	187.5
523	S[56]	9954	312.5	583	S[116]	9114	312.5	643	S[176]	8274	312.5	703	S[236]	7434	312.5
524	S[57]	9940	187.5	584	S[117]	9100	187.5	644	S[177]	8260	187.5	704	S[237]	7420	187.5
525	S[58]	9926	312.5	585	S[118]	9086	312.5	645	S[178]	8246	312.5	705	S[238]	7406	312.5
526	S[59]	9912	187.5	586	S[119]	9072	187.5	646	S[179]	8232	187.5	706	S[239]	7392	187.5
527	S[60]	9898	312.5	587	S[120]	9058	312.5	647	S[180]	8218	312.5	707	S[240]	7378	312.5
528	S[61]	9884	187.5	588	S[121]	9044	187.5	648	S[181]	8204	187.5	708	S[241]	7364	187.5
529	S[62]	9870	312.5	589	S[122]	9030	312.5	649	S[182]	8190	312.5	709	S[242]	7350	312.5
530	S[63]	9856	187.5	590	S[123]	9016	187.5	650	S[183]	8176	187.5	710	S[243]	7336	187.5
531	S[64]	9842	312.5	591	S[124]	9002	312.5	651	S[184]	8162	312.5	711	S[244]	7322	312.5
532	S[65]	9828	187.5	592	S[125]	8988	187.5	652	S[185]	8148	187.5	712	S[245]	7308	187.5
533	S[66]	9814	312.5	593	S[126]	8974	312.5	653	S[186]	8134	312.5	713	S[246]	7294	312.5
534	S[67]	9800	187.5	594	S[127]	8960	187.5	654	S[187]	8120	187.5	714	S[247]	7280	187.5
535	S[68]	9786	312.5	595	S[128]	8946	312.5	655	S[188]	8106	312.5	715	S[248]	7266	312.5
536	S[69]	9772	187.5	596	S[129]	8932	187.5	656	S[189]	8092	187.5	716	S[249]	7252	187.5
537	S[70]	9758	312.5	597	S[130]	8918	312.5	657	S[190]	8078	312.5	717	S[250]	7238	312.5
538	S[71]	9744	187.5	598	S[131]	8904	187.5	658	S[191]	8064	187.5	718	S[251]	7224	187.5
539	S[72]	9730	312.5	599	S[132]	8890	312.5	659	S[192]	8050	312.5	719	S[252]	7210	312.5
540	S[73]	9716	187.5	600	S[133]	8876	187.5	660	S[193]	8036	187.5	720	S[253]	7196	187.5

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
721	S[254]	7182	312.5	781	S[314]	6342	312.5	841	S[374]	5502	312.5	901	S[434]	4662	312.5
722	S[255]	7168	187.5	782	S[315]	6328	187.5	842	S[375]	5488	187.5	902	S[435]	4648	187.5
723	S[256]	7154	312.5	783	S[316]	6314	312.5	843	S[376]	5474	312.5	903	S[436]	4634	312.5
724	S[257]	7140	187.5	784	S[317]	6300	187.5	844	S[377]	5460	187.5	904	S[437]	4620	187.5
725	S[258]	7126	312.5	785	S[318]	6286	312.5	845	S[378]	5446	312.5	905	S[438]	4606	312.5
726	S[259]	7112	187.5	786	S[319]	6272	187.5	846	S[379]	5432	187.5	906	S[439]	4592	187.5
727	S[260]	7098	312.5	787	S[320]	6258	312.5	847	S[380]	5418	312.5	907	S[440]	4578	312.5
728	S[261]	7084	187.5	788	S[321]	6244	187.5	848	S[381]	5404	187.5	908	S[441]	4564	187.5
729	S[262]	7070	312.5	789	S[322]	6230	312.5	849	S[382]	5390	312.5	909	S[442]	4550	312.5
730	S[263]	7056	187.5	790	S[323]	6216	187.5	850	S[383]	5376	187.5	910	S[443]	4536	187.5
731	S[264]	7042	312.5	791	S[324]	6202	312.5	851	S[384]	5362	312.5	911	S[444]	4522	312.5
732	S[265]	7028	187.5	792	S[325]	6188	187.5	852	S[385]	5348	187.5	912	S[445]	4508	187.5
733	S[266]	7014	312.5	793	S[326]	6174	312.5	853	S[386]	5334	312.5	913	S[446]	4494	312.5
734	S[267]	7000	187.5	794	S[327]	6160	187.5	854	S[387]	5320	187.5	914	S[447]	4480	187.5
735	S[268]	6986	312.5	795	S[328]	6146	312.5	855	S[388]	5306	312.5	915	S[448]	4466	312.5
736	S[269]	6972	187.5	796	S[329]	6132	187.5	856	S[389]	5292	187.5	916	S[449]	4452	187.5
737	S[270]	6958	312.5	797	S[330]	6118	312.5	857	S[390]	5278	312.5	917	S[450]	4438	312.5
738	S[271]	6944	187.5	798	S[331]	6104	187.5	858	S[391]	5264	187.5	918	S[451]	4424	187.5
739	S[272]	6930	312.5	799	S[332]	6090	312.5	859	S[392]	5250	312.5	919	S[452]	4410	312.5
740	S[273]	6916	187.5	800	S[333]	6076	187.5	860	S[393]	5236	187.5	920	S[453]	4396	187.5
741	S[274]	6902	312.5	801	S[334]	6062	312.5	861	S[394]	5222	312.5	921	S[454]	4382	312.5
742	S[275]	6888	187.5	802	S[335]	6048	187.5	862	S[395]	5208	187.5	922	S[455]	4368	187.5
743	S[276]	6874	312.5	803	S[336]	6034	312.5	863	S[396]	5194	312.5	923	S[456]	4354	312.5
744	S[277]	6860	187.5	804	S[337]	6020	187.5	864	S[397]	5180	187.5	924	S[457]	4340	187.5
745	S[278]	6846	312.5	805	S[338]	6006	312.5	865	S[398]	5166	312.5	925	S[458]	4326	312.5
746	S[279]	6832	187.5	806	S[339]	5992	187.5	866	S[399]	5152	187.5	926	S[459]	4312	187.5
747	S[280]	6818	312.5	807	S[340]	5978	312.5	867	S[400]	5138	312.5	927	S[460]	4298	312.5
748	S[281]	6804	187.5	808	S[341]	5964	187.5	868	S[401]	5124	187.5	928	S[461]	4284	187.5
749	S[282]	6790	312.5	809	S[342]	5950	312.5	869	S[402]	5110	312.5	929	S[462]	4270	312.5
750	S[283]	6776	187.5	810	S[343]	5936	187.5	870	S[403]	5096	187.5	930	S[463]	4256	187.5
751	S[284]	6762	312.5	811	S[344]	5922	312.5	871	S[404]	5082	312.5	931	S[464]	4242	312.5
752	S[285]	6748	187.5	812	S[345]	5908	187.5	872	S[405]	5068	187.5	932	S[465]	4228	187.5
753	S[286]	6734	312.5	813	S[346]	5894	312.5	873	S[406]	5054	312.5	933	S[466]	4214	312.5
754	S[287]	6720	187.5	814	S[347]	5880	187.5	874	S[407]	5040	187.5	934	S[467]	4200	187.5
755	S[288]	6706	312.5	815	S[348]	5866	312.5	875	S[408]	5026	312.5	935	S[468]	4186	312.5
756	S[289]	6692	187.5	816	S[349]	5852	187.5	876	S[409]	5012	187.5	936	S[469]	4172	187.5
757	S[290]	6678	312.5	817	S[350]	5838	312.5	877	S[410]	4998	312.5	937	S[470]	4158	312.5
758	S[291]	6664	187.5	818	S[351]	5824	187.5	878	S[411]	4984	187.5	938	S[471]	4144	187.5
759	S[292]	6650	312.5	819	S[352]	5810	312.5	879	S[412]	4970	312.5	939	S[472]	4130	312.5
760	S[293]	6636	187.5	820	S[353]	5796	187.5	880	S[413]	4956	187.5	940	S[473]	4116	187.5
761	S[294]	6622	312.5	821	S[354]	5782	312.5	881	S[414]	4942	312.5	941	S[474]	4102	312.5
762	S[295]	6608	187.5	822	S[355]	5768	187.5	882	S[415]	4928	187.5	942	S[475]	4088	187.5
763	S[296]	6594	312.5	823	S[356]	5754	312.5	883	S[416]	4914	312.5	943	S[476]	4074	312.5
764	S[297]	6580	187.5	824	S[357]	5740	187.5	884	S[417]	4900	187.5	944	S[477]	4060	187.5
765	S[298]	6566	312.5	825	S[358]	5726	312.5	885	S[418]	4886	312.5	945	S[478]	4046	312.5
766	S[299]	6552	187.5	826	S[359]	5712	187.5	886	S[419]	4872	187.5	946	S[479]	4032	187.5
767	S[300]	6538	312.5	827	S[360]	5698	312.5	887	S[420]	4858	312.5	947	S[480]	4018	312.5
768	S[301]	6524	187.5	828	S[361]	5684	187.5	888	S[421]	4844	187.5	948	S[481]	4004	187.5
769	S[302]	6510	312.5	829	S[362]	5670	312.5	889	S[422]	4830	312.5	949	S[482]	3990	312.5
770	S[303]	6496	187.5	830	S[363]	5656	187.5	890	S[423]	4816	187.5	950	S[483]	3976	187.5
771	S[304]	6482	312.5	831	S[364]	5642	312.5	891	S[424]	4802	312.5	951	S[484]	3962	312.5
772	S[305]	6468	187.5	832	S[365]	5628	187.5	892	S[425]	4788	187.5	952	S[485]	3948	187.5
773	S[306]	6454	312.5	833	S[366]	5614	312.5	893	S[426]	4774	312.5	953	S[486]	3934	312.5
774	S[307]	6440	187.5	834	S[367]	5600	187.5	894	S[427]	4760	187.5	954	S[487]	3920	187.5
775	S[308]	6426	312.5	835	S[368]	5586	312.5	895	S[428]	4746	312.5	955	S[488]	3906	312.5
776	S[309]	6412	187.5	836	S[369]	5572	187.5	896	S[429]	4732	187.5	956	S[489]	3892	187.5
777	S[310]	6398	312.5	837	S[370]	5558	312.5	897	S[430]	4718	312.5	957	S[490]	3878	312.5
778	S[311]	6384	187.5	838	S[371]	5544	187.5	898	S[431]	4704	187.5	958	S[491]	3864	187.5
779	S[312]	6370	312.5	839	S[372]	5530	312.5	899	S[432]	4690	312.5	959	S[492]	3850	312.5
780	S[313]	6356	187.5	840	S[373]	5516	187.5	900	S[433]	4676	187.5	960	S[493]	3836	187.5

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
961	S[494]	3822	312.5	1021	S[554]	2982	312.5	1081	S[614]	2142	312.5	1141	S[674]	1302	312.5
962	S[495]	3808	187.5	1022	S[555]	2968	187.5	1082	S[615]	2128	187.5	1142	S[675]	1288	187.5
963	S[496]	3794	312.5	1023	S[556]	2954	312.5	1083	S[616]	2114	312.5	1143	S[676]	1274	312.5
964	S[497]	3780	187.5	1024	S[557]	2940	187.5	1084	S[617]	2100	187.5	1144	S[677]	1260	187.5
965	S[498]	3766	312.5	1025	S[558]	2926	312.5	1085	S[618]	2086	312.5	1145	S[678]	1246	312.5
966	S[499]	3752	187.5	1026	S[559]	2912	187.5	1086	S[619]	2072	187.5	1146	S[679]	1232	187.5
967	S[500]	3738	312.5	1027	S[560]	2898	312.5	1087	S[620]	2058	312.5	1147	S[680]	1218	312.5
968	S[501]	3724	187.5	1028	S[561]	2884	187.5	1088	S[621]	2044	187.5	1148	S[681]	1204	187.5
969	S[502]	3710	312.5	1029	S[562]	2870	312.5	1089	S[622]	2030	312.5	1149	S[682]	1190	312.5
970	S[503]	3696	187.5	1030	S[563]	2856	187.5	1090	S[623]	2016	187.5	1150	S[683]	1176	187.5
971	S[504]	3682	312.5	1031	S[564]	2842	312.5	1091	S[624]	2002	312.5	1151	S[684]	1162	312.5
972	S[505]	3668	187.5	1032	S[565]	2828	187.5	1092	S[625]	1988	187.5	1152	S[685]	1148	187.5
973	S[506]	3654	312.5	1033	S[566]	2814	312.5	1093	S[626]	1974	312.5	1153	S[686]	1134	312.5
974	S[507]	3640	187.5	1034	S[567]	2800	187.5	1094	S[627]	1960	187.5	1154	S[687]	1120	187.5
975	S[508]	3626	312.5	1035	S[568]	2786	312.5	1095	S[628]	1946	312.5	1155	S[688]	1106	312.5
976	S[509]	3612	187.5	1036	S[569]	2772	187.5	1096	S[629]	1932	187.5	1156	S[689]	1092	187.5
977	S[510]	3598	312.5	1037	S[570]	2758	312.5	1097	S[630]	1918	312.5	1157	S[690]	1078	312.5
978	S[511]	3584	187.5	1038	S[571]	2744	187.5	1098	S[631]	1904	187.5	1158	S[691]	1064	187.5
979	S[512]	3570	312.5	1039	S[572]	2730	312.5	1099	S[632]	1890	312.5	1159	S[692]	1050	312.5
980	S[513]	3556	187.5	1040	S[573]	2716	187.5	1100	S[633]	1876	187.5	1160	S[693]	1036	187.5
981	S[514]	3542	312.5	1041	S[574]	2702	312.5	1101	S[634]	1862	312.5	1161	S[694]	1022	312.5
982	S[515]	3528	187.5	1042	S[575]	2688	187.5	1102	S[635]	1848	187.5	1162	S[695]	1008	187.5
983	S[516]	3514	312.5	1043	S[576]	2674	312.5	1103	S[636]	1834	312.5	1163	S[696]	994	312.5
984	S[517]	3500	187.5	1044	S[577]	2660	187.5	1104	S[637]	1820	187.5	1164	S[697]	980	187.5
985	S[518]	3486	312.5	1045	S[578]	2646	312.5	1105	S[638]	1806	312.5	1165	S[698]	966	312.5
986	S[519]	3472	187.5	1046	S[579]	2632	187.5	1106	S[639]	1792	187.5	1166	S[699]	952	187.5
987	S[520]	3458	312.5	1047	S[580]	2618	312.5	1107	S[640]	1778	312.5	1167	S[700]	938	312.5
988	S[521]	3444	187.5	1048	S[581]	2604	187.5	1108	S[641]	1764	187.5	1168	S[701]	924	187.5
989	S[522]	3430	312.5	1049	S[582]	2590	312.5	1109	S[642]	1750	312.5	1169	S[702]	910	312.5
990	S[523]	3416	187.5	1050	S[583]	2576	187.5	1110	S[643]	1736	187.5	1170	S[703]	896	187.5
991	S[524]	3402	312.5	1051	S[584]	2562	312.5	1111	S[644]	1722	312.5	1171	S[704]	882	312.5
992	S[525]	3388	187.5	1052	S[585]	2548	187.5	1112	S[645]	1708	187.5	1172	S[705]	868	187.5
993	S[526]	3374	312.5	1053	S[586]	2534	312.5	1113	S[646]	1694	312.5	1173	S[706]	854	312.5
994	S[527]	3360	187.5	1054	S[587]	2520	187.5	1114	S[647]	1680	187.5	1174	S[707]	840	187.5
995	S[528]	3346	312.5	1055	S[588]	2506	312.5	1115	S[648]	1666	312.5	1175	S[708]	826	312.5
996	S[529]	3332	187.5	1056	S[589]	2492	187.5	1116	S[649]	1652	187.5	1176	S[709]	812	187.5
997	S[530]	3318	312.5	1057	S[590]	2478	312.5	1117	S[650]	1638	312.5	1177	S[710]	798	312.5
998	S[531]	3304	187.5	1058	S[591]	2464	187.5	1118	S[651]	1624	187.5	1178	S[711]	784	187.5
999	S[532]	3290	312.5	1059	S[592]	2450	312.5	1119	S[652]	1610	312.5	1179	S[712]	770	312.5
1000	S[533]	3276	187.5	1060	S[593]	2436	187.5	1120	S[653]	1596	187.5	1180	S[713]	756	187.5
1001	S[534]	3262	312.5	1061	S[594]	2422	312.5	1121	S[654]	1582	312.5	1181	S[714]	742	312.5
1002	S[535]	3248	187.5	1062	S[595]	2408	187.5	1122	S[655]	1568	187.5	1182	S[715]	728	187.5
1003	S[536]	3234	312.5	1063	S[596]	2394	312.5	1123	S[656]	1554	312.5	1183	S[716]	714	312.5
1004	S[537]	3220	187.5	1064	S[597]	2380	187.5	1124	S[657]	1540	187.5	1184	S[717]	700	187.5
1005	S[538]	3206	312.5	1065	S[598]	2366	312.5	1125	S[658]	1526	312.5	1185	S[718]	686	312.5
1006	S[539]	3192	187.5	1066	S[599]	2352	187.5	1126	S[659]	1512	187.5	1186	S[719]	672	187.5
1007	S[540]	3178	312.5	1067	S[600]	2338	312.5	1127	S[660]	1498	312.5	1187	S[720]	658	312.5
1008	S[541]	3164	187.5	1068	S[601]	2324	187.5	1128	S[661]	1484	187.5	1188	DMY_VSS	644	187.5
1009	S[542]	3150	312.5	1069	S[602]	2310	312.5	1129	S[662]	1470	312.5	1189	DMY_VSS	630	312.5
1010	S[543]	3136	187.5	1070	S[603]	2296	187.5	1130	S[663]	1456	187.5	1190	DMY	616	187.5
1011	S[544]	3122	312.5	1071	S[604]	2282	312.5	1131	S[664]	1442	312.5	1191	DMY	602	312.5
1012	S[545]	3108	187.5	1072	S[605]	2268	187.5	1132	S[665]	1428	187.5	1192	DMY	588	187.5
1013	S[546]	3094	312.5	1073	S[606]	2254	312.5	1133	S[666]	1414	312.5	1193	DMY	574	312.5
1014	S[547]	3080	187.5	1074	S[607]	2240	187.5	1134	S[667]	1400	187.5	1194	DMY	560	187.5
1015	S[548]	3066	312.5	1075	S[608]	2226	312.5	1135	S[668]	1386	312.5	1195	DMY	546	312.5
1016	S[549]	3052	187.5	1076	S[609]	2212	187.5	1136	S[669]	1372	187.5	1196	DMY	532	187.5
1017	S[550]	3038	312.5	1077	S[610]	2198	312.5	1137	S[670]	1358	312.5	1197	DMY	518	312.5
1018	S[551]	3024	187.5	1078	S[611]	2184	187.5	1138	S[671]	1344	187.5	1198	DMY	504	187.5
1019	S[552]	3010	312.5	1079	S[612]	2170	312.5	1139	S[672]	1330	312.5	1199	DMY	490	312.5
1020	S[553]	2996	187.5	1080	S[613]	2156	187.5	1140	S[673]	1316	187.5	1200	DMY	476	187.5

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1201	DMY	462	312.5	1261	S[745]	-378	312.5	1321	S[805]	-1218	312.5	1381	S[865]	-2058	312.5
1202	DMY	448	187.5	1262	S[746]	-392	187.5	1322	S[806]	-1232	187.5	1382	S[866]	-2072	187.5
1203	DMY	434	312.5	1263	S[747]	-406	312.5	1323	S[807]	-1246	312.5	1383	S[867]	-2086	312.5
1204	DMY	420	187.5	1264	S[748]	-420	187.5	1324	S[808]	-1260	187.5	1384	S[868]	-2100	187.5
1205	DMY	406	312.5	1265	S[749]	-434	312.5	1325	S[809]	-1274	312.5	1385	S[869]	-2114	312.5
1206	DMY	392	187.5	1266	S[750]	-448	187.5	1326	S[810]	-1288	187.5	1386	S[870]	-2128	187.5
1207	DMY	378	312.5	1267	S[751]	-462	312.5	1327	S[811]	-1302	312.5	1387	S[871]	-2142	312.5
1208	DMY	364	187.5	1268	S[752]	-476	187.5	1328	S[812]	-1316	187.5	1388	S[872]	-2156	187.5
1209	DMY	350	312.5	1269	S[753]	-490	312.5	1329	S[813]	-1330	312.5	1389	S[873]	-2170	312.5
1210	DMY	336	187.5	1270	S[754]	-504	187.5	1330	S[814]	-1344	187.5	1390	S[874]	-2184	187.5
1211	DMY	322	312.5	1271	S[755]	-518	312.5	1331	S[815]	-1358	312.5	1391	S[875]	-2198	312.5
1212	DMY	308	187.5	1272	S[756]	-532	187.5	1332	S[816]	-1372	187.5	1392	S[876]	-2212	187.5
1213	DMY	294	312.5	1273	S[757]	-546	312.5	1333	S[817]	-1386	312.5	1393	S[877]	-2226	312.5
1214	DMY	280	187.5	1274	S[758]	-560	187.5	1334	S[818]	-1400	187.5	1394	S[878]	-2240	187.5
1215	DMY	266	312.5	1275	S[759]	-574	312.5	1335	S[819]	-1414	312.5	1395	S[879]	-2254	312.5
1216	DMY	252	187.5	1276	S[760]	-588	187.5	1336	S[820]	-1428	187.5	1396	S[880]	-2268	187.5
1217	DMY	238	312.5	1277	S[761]	-602	312.5	1337	S[821]	-1442	312.5	1397	S[881]	-2282	312.5
1218	DMY	224	187.5	1278	S[762]	-616	187.5	1338	S[822]	-1456	187.5	1398	S[882]	-2296	187.5
1219	DMY	210	312.5	1279	S[763]	-630	312.5	1339	S[823]	-1470	312.5	1399	S[883]	-2310	312.5
1220	DMY	196	187.5	1280	S[764]	-644	187.5	1340	S[824]	-1484	187.5	1400	S[884]	-2324	187.5
1221	DMY	182	312.5	1281	S[765]	-658	312.5	1341	S[825]	-1498	312.5	1401	S[885]	-2338	312.5
1222	DMY	168	187.5	1282	S[766]	-672	187.5	1342	S[826]	-1512	187.5	1402	S[886]	-2352	187.5
1223	DMY	154	312.5	1283	S[767]	-686	312.5	1343	S[827]	-1526	312.5	1403	S[887]	-2366	312.5
1224	DMY	140	187.5	1284	S[768]	-700	187.5	1344	S[828]	-1540	187.5	1404	S[888]	-2380	187.5
1225	DMY	126	312.5	1285	S[769]	-714	312.5	1345	S[829]	-1554	312.5	1405	S[889]	-2394	312.5
1226	DMY	112	187.5	1286	S[770]	-728	187.5	1346	S[830]	-1568	187.5	1406	S[890]	-2408	187.5
1227	DMY	98	312.5	1287	S[771]	-742	312.5	1347	S[831]	-1582	312.5	1407	S[891]	-2422	312.5
1228	DMY	84	187.5	1288	S[772]	-756	187.5	1348	S[832]	-1596	187.5	1408	S[892]	-2436	187.5
1229	DMY	70	312.5	1289	S[773]	-770	312.5	1349	S[833]	-1610	312.5	1409	S[893]	-2450	312.5
1230	DMY	56	187.5	1290	S[774]	-784	187.5	1350	S[834]	-1624	187.5	1410	S[894]	-2464	187.5
1231	DMY	42	312.5	1291	S[775]	-798	312.5	1351	S[835]	-1638	312.5	1411	S[895]	-2478	312.5
1232	DMY	28	187.5	1292	S[776]	-812	187.5	1352	S[836]	-1652	187.5	1412	S[896]	-2492	187.5
1233	DMY	14	312.5	1293	S[777]	-826	312.5	1353	S[837]	-1666	312.5	1413	S[897]	-2506	312.5
1234	DMY	0	187.5	1294	S[778]	-840	187.5	1354	S[838]	-1680	187.5	1414	S[898]	-2520	187.5
1235	DMY_VSS	-14	312.5	1295	S[779]	-854	312.5	1355	S[839]	-1694	312.5	1415	S[899]	-2534	312.5
1236	DMY_VSS	-28	187.5	1296	S[780]	-868	187.5	1356	S[840]	-1708	187.5	1416	S[900]	-2548	187.5
1237	S[721]	-42	312.5	1297	S[781]	-882	312.5	1357	S[841]	-1722	312.5	1417	S[901]	-2562	312.5
1238	S[722]	-56	187.5	1298	S[782]	-896	187.5	1358	S[842]	-1736	187.5	1418	S[902]	-2576	187.5
1239	S[723]	-70	312.5	1299	S[783]	-910	312.5	1359	S[843]	-1750	312.5	1419	S[903]	-2590	312.5
1240	S[724]	-84	187.5	1300	S[784]	-924	187.5	1360	S[844]	-1764	187.5	1420	S[904]	-2604	187.5
1241	S[725]	-98	312.5	1301	S[785]	-938	312.5	1361	S[845]	-1778	312.5	1421	S[905]	-2618	312.5
1242	S[726]	-112	187.5	1302	S[786]	-952	187.5	1362	S[846]	-1792	187.5	1422	S[906]	-2632	187.5
1243	S[727]	-126	312.5	1303	S[787]	-966	312.5	1363	S[847]	-1806	312.5	1423	S[907]	-2646	312.5
1244	S[728]	-140	187.5	1304	S[788]	-980	187.5	1364	S[848]	-1820	187.5	1424	S[908]	-2660	187.5
1245	S[729]	-154	312.5	1305	S[789]	-994	312.5	1365	S[849]	-1834	312.5	1425	S[909]	-2674	312.5
1246	S[730]	-168	187.5	1306	S[790]	-1008	187.5	1366	S[850]	-1848	187.5	1426	S[910]	-2688	187.5
1247	S[731]	-182	312.5	1307	S[791]	-1022	312.5	1367	S[851]	-1862	312.5	1427	S[911]	-2702	312.5
1248	S[732]	-196	187.5	1308	S[792]	-1036	187.5	1368	S[852]	-1876	187.5	1428	S[912]	-2716	187.5
1249	S[733]	-210	312.5	1309	S[793]	-1050	312.5	1369	S[853]	-1890	312.5	1429	S[913]	-2730	312.5
1250	S[734]	-224	187.5	1310	S[794]	-1064	187.5	1370	S[854]	-1904	187.5	1430	S[914]	-2744	187.5
1251	S[735]	-238	312.5	1311	S[795]	-1078	312.5	1371	S[855]	-1918	312.5	1431	S[915]	-2758	312.5
1252	S[736]	-252	187.5	1312	S[796]	-1092	187.5	1372	S[856]	-1932	187.5	1432	S[916]	-2772	187.5
1253	S[737]	-266	312.5	1313	S[797]	-1106	312.5	1373	S[857]	-1946	312.5	1433	S[917]	-2786	312.5
1254	S[738]	-280	187.5	1314	S[798]	-1120	187.5	1374	S[858]	-1960	187.5	1434	S[918]	-2800	187.5
1255	S[739]	-294	312.5	1315	S[799]	-1134	312.5	1375	S[859]	-1974	312.5	1435	S[919]	-2814	312.5
1256	S[740]	-308	187.5	1316	S[800]	-1148	187.5	1376	S[860]	-1988	187.5	1436	S[920]	-2828	187.5
1257	S[741]	-322	312.5	1317	S[801]	-1162	312.5	1377	S[861]	-2002	312.5	1437	S[921]	-2842	312.5
1258	S[742]	-336	187.5	1318	S[802]	-1176	187.5	1378	S[862]	-2016	187.5	1438	S[922]	-2856	187.5
1259	S[743]	-350	312.5	1319	S[803]	-1190	312.5	1379	S[863]	-2030	312.5	1439	S[923]	-2870	312.5
1260	S[744]	-364	187.5	1320	S[804]	-1204	187.5	1380	S[864]	-2044	187.5	1440	S[924]	-2884	187.5

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1441	S[925]	-2898	312.5	1501	S[985]	-3738	312.5	1561	S[1045]	-4578	312.5	1621	S[1105]	-5418	312.5
1442	S[926]	-2912	187.5	1502	S[986]	-3752	187.5	1562	S[1046]	-4592	187.5	1622	S[1106]	-5432	187.5
1443	S[927]	-2926	312.5	1503	S[987]	-3766	312.5	1563	S[1047]	-4606	312.5	1623	S[1107]	-5446	312.5
1444	S[928]	-2940	187.5	1504	S[988]	-3780	187.5	1564	S[1048]	-4620	187.5	1624	S[1108]	-5460	187.5
1445	S[929]	-2954	312.5	1505	S[989]	-3794	312.5	1565	S[1049]	-4634	312.5	1625	S[1109]	-5474	312.5
1446	S[930]	-2968	187.5	1506	S[990]	-3808	187.5	1566	S[1050]	-4648	187.5	1626	S[1110]	-5488	187.5
1447	S[931]	-2982	312.5	1507	S[991]	-3822	312.5	1567	S[1051]	-4662	312.5	1627	S[1111]	-5502	312.5
1448	S[932]	-2996	187.5	1508	S[992]	-3836	187.5	1568	S[1052]	-4676	187.5	1628	S[1112]	-5516	187.5
1449	S[933]	-3010	312.5	1509	S[993]	-3850	312.5	1569	S[1053]	-4690	312.5	1629	S[1113]	-5530	312.5
1450	S[934]	-3024	187.5	1510	S[994]	-3864	187.5	1570	S[1054]	-4704	187.5	1630	S[1114]	-5544	187.5
1451	S[935]	-3038	312.5	1511	S[995]	-3878	312.5	1571	S[1055]	-4718	312.5	1631	S[1115]	-5558	312.5
1452	S[936]	-3052	187.5	1512	S[996]	-3892	187.5	1572	S[1056]	-4732	187.5	1632	S[1116]	-5572	187.5
1453	S[937]	-3066	312.5	1513	S[997]	-3906	312.5	1573	S[1057]	-4746	312.5	1633	S[1117]	-5586	312.5
1454	S[938]	-3080	187.5	1514	S[998]	-3920	187.5	1574	S[1058]	-4760	187.5	1634	S[1118]	-5600	187.5
1455	S[939]	-3094	312.5	1515	S[999]	-3934	312.5	1575	S[1059]	-4774	312.5	1635	S[1119]	-5614	312.5
1456	S[940]	-3108	187.5	1516	S[1000]	-3948	187.5	1576	S[1060]	-4788	187.5	1636	S[1120]	-5628	187.5
1457	S[941]	-3122	312.5	1517	S[1001]	-3962	312.5	1577	S[1061]	-4802	312.5	1637	S[1121]	-5642	312.5
1458	S[942]	-3136	187.5	1518	S[1002]	-3976	187.5	1578	S[1062]	-4816	187.5	1638	S[1122]	-5656	187.5
1459	S[943]	-3150	312.5	1519	S[1003]	-3990	312.5	1579	S[1063]	-4830	312.5	1639	S[1123]	-5670	312.5
1460	S[944]	-3164	187.5	1520	S[1004]	-4004	187.5	1580	S[1064]	-4844	187.5	1640	S[1124]	-5684	187.5
1461	S[945]	-3178	312.5	1521	S[1005]	-4018	312.5	1581	S[1065]	-4858	312.5	1641	S[1125]	-5698	312.5
1462	S[946]	-3192	187.5	1522	S[1006]	-4032	187.5	1582	S[1066]	-4872	187.5	1642	S[1126]	-5712	187.5
1463	S[947]	-3206	312.5	1523	S[1007]	-4046	312.5	1583	S[1067]	-4886	312.5	1643	S[1127]	-5726	312.5
1464	S[948]	-3220	187.5	1524	S[1008]	-4060	187.5	1584	S[1068]	-4900	187.5	1644	S[1128]	-5740	187.5
1465	S[949]	-3234	312.5	1525	S[1009]	-4074	312.5	1585	S[1069]	-4914	312.5	1645	S[1129]	-5754	312.5
1466	S[950]	-3248	187.5	1526	S[1010]	-4088	187.5	1586	S[1070]	-4928	187.5	1646	S[1130]	-5768	187.5
1467	S[951]	-3262	312.5	1527	S[1011]	-4102	312.5	1587	S[1071]	-4942	312.5	1647	S[1131]	-5782	312.5
1468	S[952]	-3276	187.5	1528	S[1012]	-4116	187.5	1588	S[1072]	-4956	187.5	1648	S[1132]	-5796	187.5
1469	S[953]	-3290	312.5	1529	S[1013]	-4130	312.5	1589	S[1073]	-4970	312.5	1649	S[1133]	-5810	312.5
1470	S[954]	-3304	187.5	1530	S[1014]	-4144	187.5	1590	S[1074]	-4984	187.5	1650	S[1134]	-5824	187.5
1471	S[955]	-3318	312.5	1531	S[1015]	-4158	312.5	1591	S[1075]	-4998	312.5	1651	S[1135]	-5838	312.5
1472	S[956]	-3332	187.5	1532	S[1016]	-4172	187.5	1592	S[1076]	-5012	187.5	1652	S[1136]	-5852	187.5
1473	S[957]	-3346	312.5	1533	S[1017]	-4186	312.5	1593	S[1077]	-5026	312.5	1653	S[1137]	-5866	312.5
1474	S[958]	-3360	187.5	1534	S[1018]	-4200	187.5	1594	S[1078]	-5040	187.5	1654	S[1138]	-5880	187.5
1475	S[959]	-3374	312.5	1535	S[1019]	-4214	312.5	1595	S[1079]	-5054	312.5	1655	S[1139]	-5894	312.5
1476	S[960]	-3388	187.5	1536	S[1020]	-4228	187.5	1596	S[1080]	-5068	187.5	1656	S[1140]	-5908	187.5
1477	S[961]	-3402	312.5	1537	S[1021]	-4242	312.5	1597	S[1081]	-5082	312.5	1657	S[1141]	-5922	312.5
1478	S[962]	-3416	187.5	1538	S[1022]	-4256	187.5	1598	S[1082]	-5096	187.5	1658	S[1142]	-5936	187.5
1479	S[963]	-3430	312.5	1539	S[1023]	-4270	312.5	1599	S[1083]	-5110	312.5	1659	S[1143]	-5950	312.5
1480	S[964]	-3444	187.5	1540	S[1024]	-4284	187.5	1600	S[1084]	-5124	187.5	1660	S[1144]	-5964	187.5
1481	S[965]	-3458	312.5	1541	S[1025]	-4298	312.5	1601	S[1085]	-5138	312.5	1661	S[1145]	-5978	312.5
1482	S[966]	-3472	187.5	1542	S[1026]	-4312	187.5	1602	S[1086]	-5152	187.5	1662	S[1146]	-5992	187.5
1483	S[967]	-3486	312.5	1543	S[1027]	-4326	312.5	1603	S[1087]	-5166	312.5	1663	S[1147]	-6006	312.5
1484	S[968]	-3500	187.5	1544	S[1028]	-4340	187.5	1604	S[1088]	-5180	187.5	1664	S[1148]	-6020	187.5
1485	S[969]	-3514	312.5	1545	S[1029]	-4354	312.5	1605	S[1089]	-5194	312.5	1665	S[1149]	-6034	312.5
1486	S[970]	-3528	187.5	1546	S[1030]	-4368	187.5	1606	S[1090]	-5208	187.5	1666	S[1150]	-6048	187.5
1487	S[971]	-3542	312.5	1547	S[1031]	-4382	312.5	1607	S[1091]	-5222	312.5	1667	S[1151]	-6062	312.5
1488	S[972]	-3556	187.5	1548	S[1032]	-4396	187.5	1608	S[1092]	-5236	187.5	1668	S[1152]	-6076	187.5
1489	S[973]	-3570	312.5	1549	S[1033]	-4410	312.5	1609	S[1093]	-5250	312.5	1669	S[1153]	-6090	312.5
1490	S[974]	-3584	187.5	1550	S[1034]	-4424	187.5	1610	S[1094]	-5264	187.5	1670	S[1154]	-6104	187.5
1491	S[975]	-3598	312.5	1551	S[1035]	-4438	312.5	1611	S[1095]	-5278	312.5	1671	S[1155]	-6118	312.5
1492	S[976]	-3612	187.5	1552	S[1036]	-4452	187.5	1612	S[1096]	-5292	187.5	1672	S[1156]	-6132	187.5
1493	S[977]	-3626	312.5	1553	S[1037]	-4466	312.5	1613	S[1097]	-5306	312.5	1673	S[1157]	-6146	312.5
1494	S[978]	-3640	187.5	1554	S[1038]	-4480	187.5	1614	S[1098]	-5320	187.5	1674	S[1158]	-6160	187.5
1495	S[979]	-3654	312.5	1555	S[1039]	-4494	312.5	1615	S[1099]	-5334	312.5	1675	S[1159]	-6174	312.5
1496	S[980]	-3668	187.5	1556	S[1040]	-4508	187.5	1616	S[1100]	-5348	187.5	1676	S[1160]	-6188	187.5
1497	S[981]	-3682	312.5	1557	S[1041]	-4522	312.5	1617	S[1101]	-5362	312.5	1677	S[1161]	-6202	312.5
1498	S[982]	-3696	187.5	1558	S[1042]	-4536	187.5	1618	S[1102]	-5376	187.5	1678	S[1162]	-6216	187.5
1499	S[983]	-3710	312.5	1559	S[1043]	-4550	312.5	1619	S[1103]	-5390	312.5	1679	S[1163]	-6230	312.5
1500	S[984]	-3724	187.5	1560	S[1044]	-4564	187.5	1620	S[1104]	-5404	187.5	1680	S[1164]	-6244	187.5

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1681	S[1165]	-6258	312.5	1741	S[1225]	-7098	312.5	1801	S[1285]	-7938	312.5	1861	S[1345]	-8778	312.5
1682	S[1166]	-6272	187.5	1742	S[1226]	-7112	187.5	1802	S[1286]	-7952	187.5	1862	S[1346]	-8792	187.5
1683	S[1167]	-6286	312.5	1743	S[1227]	-7126	312.5	1803	S[1287]	-7966	312.5	1863	S[1347]	-8806	312.5
1684	S[1168]	-6300	187.5	1744	S[1228]	-7140	187.5	1804	S[1288]	-7980	187.5	1864	S[1348]	-8820	187.5
1685	S[1169]	-6314	312.5	1745	S[1229]	-7154	312.5	1805	S[1289]	-7994	312.5	1865	S[1349]	-8834	312.5
1686	S[1170]	-6328	187.5	1746	S[1230]	-7168	187.5	1806	S[1290]	-8008	187.5	1866	S[1350]	-8848	187.5
1687	S[1171]	-6342	312.5	1747	S[1231]	-7182	312.5	1807	S[1291]	-8022	312.5	1867	S[1351]	-8862	312.5
1688	S[1172]	-6356	187.5	1748	S[1232]	-7196	187.5	1808	S[1292]	-8036	187.5	1868	S[1352]	-8876	187.5
1689	S[1173]	-6370	312.5	1749	S[1233]	-7210	312.5	1809	S[1293]	-8050	312.5	1869	S[1353]	-8890	312.5
1690	S[1174]	-6384	187.5	1750	S[1234]	-7224	187.5	1810	S[1294]	-8064	187.5	1870	S[1354]	-8904	187.5
1691	S[1175]	-6398	312.5	1751	S[1235]	-7238	312.5	1811	S[1295]	-8078	312.5	1871	S[1355]	-8918	312.5
1692	S[1176]	-6412	187.5	1752	S[1236]	-7252	187.5	1812	S[1296]	-8092	187.5	1872	S[1356]	-8932	187.5
1693	S[1177]	-6426	312.5	1753	S[1237]	-7266	312.5	1813	S[1297]	-8106	312.5	1873	S[1357]	-8946	312.5
1694	S[1178]	-6440	187.5	1754	S[1238]	-7280	187.5	1814	S[1298]	-8120	187.5	1874	S[1358]	-8960	187.5
1695	S[1179]	-6454	312.5	1755	S[1239]	-7294	312.5	1815	S[1299]	-8134	312.5	1875	S[1359]	-8974	312.5
1696	S[1180]	-6468	187.5	1756	S[1240]	-7308	187.5	1816	S[1300]	-8148	187.5	1876	S[1360]	-8988	187.5
1697	S[1181]	-6482	312.5	1757	S[1241]	-7322	312.5	1817	S[1301]	-8162	312.5	1877	S[1361]	-9002	312.5
1698	S[1182]	-6496	187.5	1758	S[1242]	-7336	187.5	1818	S[1302]	-8176	187.5	1878	S[1362]	-9016	187.5
1699	S[1183]	-6510	312.5	1759	S[1243]	-7350	312.5	1819	S[1303]	-8190	312.5	1879	S[1363]	-9030	312.5
1700	S[1184]	-6524	187.5	1760	S[1244]	-7364	187.5	1820	S[1304]	-8204	187.5	1880	S[1364]	-9044	187.5
1701	S[1185]	-6538	312.5	1761	S[1245]	-7378	312.5	1821	S[1305]	-8218	312.5	1881	S[1365]	-9058	312.5
1702	S[1186]	-6552	187.5	1762	S[1246]	-7392	187.5	1822	S[1306]	-8232	187.5	1882	S[1366]	-9072	187.5
1703	S[1187]	-6566	312.5	1763	S[1247]	-7406	312.5	1823	S[1307]	-8246	312.5	1883	S[1367]	-9086	312.5
1704	S[1188]	-6580	187.5	1764	S[1248]	-7420	187.5	1824	S[1308]	-8260	187.5	1884	S[1368]	-9100	187.5
1705	S[1189]	-6594	312.5	1765	S[1249]	-7434	312.5	1825	S[1309]	-8274	312.5	1885	S[1369]	-9114	312.5
1706	S[1190]	-6608	187.5	1766	S[1250]	-7448	187.5	1826	S[1310]	-8288	187.5	1886	S[1370]	-9128	187.5
1707	S[1191]	-6622	312.5	1767	S[1251]	-7462	312.5	1827	S[1311]	-8302	312.5	1887	S[1371]	-9142	312.5
1708	S[1192]	-6636	187.5	1768	S[1252]	-7476	187.5	1828	S[1312]	-8316	187.5	1888	S[1372]	-9156	187.5
1709	S[1193]	-6650	312.5	1769	S[1253]	-7490	312.5	1829	S[1313]	-8330	312.5	1889	S[1373]	-9170	312.5
1710	S[1194]	-6664	187.5	1770	S[1254]	-7504	187.5	1830	S[1314]	-8344	187.5	1890	S[1374]	-9184	187.5
1711	S[1195]	-6678	312.5	1771	S[1255]	-7518	312.5	1831	S[1315]	-8358	312.5	1891	S[1375]	-9198	312.5
1712	S[1196]	-6692	187.5	1772	S[1256]	-7532	187.5	1832	S[1316]	-8372	187.5	1892	S[1376]	-9212	187.5
1713	S[1197]	-6706	312.5	1773	S[1257]	-7546	312.5	1833	S[1317]	-8386	312.5	1893	S[1377]	-9226	312.5
1714	S[1198]	-6720	187.5	1774	S[1258]	-7560	187.5	1834	S[1318]	-8400	187.5	1894	S[1378]	-9240	187.5
1715	S[1199]	-6734	312.5	1775	S[1259]	-7574	312.5	1835	S[1319]	-8414	312.5	1895	S[1379]	-9254	312.5
1716	S[1200]	-6748	187.5	1776	S[1260]	-7588	187.5	1836	S[1320]	-8428	187.5	1896	S[1380]	-9268	187.5
1717	S[1201]	-6762	312.5	1777	S[1261]	-7602	312.5	1837	S[1321]	-8442	312.5	1897	S[1381]	-9282	312.5
1718	S[1202]	-6776	187.5	1778	S[1262]	-7616	187.5	1838	S[1322]	-8456	187.5	1898	S[1382]	-9296	187.5
1719	S[1203]	-6790	312.5	1779	S[1263]	-7630	312.5	1839	S[1323]	-8470	312.5	1899	S[1383]	-9310	312.5
1720	S[1204]	-6804	187.5	1780	S[1264]	-7644	187.5	1840	S[1324]	-8484	187.5	1900	S[1384]	-9324	187.5
1721	S[1205]	-6818	312.5	1781	S[1265]	-7658	312.5	1841	S[1325]	-8498	312.5	1901	S[1385]	-9338	312.5
1722	S[1206]	-6832	187.5	1782	S[1266]	-7672	187.5	1842	S[1326]	-8512	187.5	1902	S[1386]	-9352	187.5
1723	S[1207]	-6846	312.5	1783	S[1267]	-7686	312.5	1843	S[1327]	-8526	312.5	1903	S[1387]	-9366	312.5
1724	S[1208]	-6860	187.5	1784	S[1268]	-7700	187.5	1844	S[1328]	-8540	187.5	1904	S[1388]	-9380	187.5
1725	S[1209]	-6874	312.5	1785	S[1269]	-7714	312.5	1845	S[1329]	-8554	312.5	1905	S[1389]	-9394	312.5
1726	S[1210]	-6888	187.5	1786	S[1270]	-7728	187.5	1846	S[1330]	-8568	187.5	1906	S[1390]	-9408	187.5
1727	S[1211]	-6902	312.5	1787	S[1271]	-7742	312.5	1847	S[1331]	-8582	312.5	1907	S[1391]	-9422	312.5
1728	S[1212]	-6916	187.5	1788	S[1272]	-7756	187.5	1848	S[1332]	-8596	187.5	1908	S[1392]	-9436	187.5
1729	S[1213]	-6930	312.5	1789	S[1273]	-7770	312.5	1849	S[1333]	-8610	312.5	1909	S[1393]	-9450	312.5
1730	S[1214]	-6944	187.5	1790	S[1274]	-7784	187.5	1850	S[1334]	-8624	187.5	1910	S[1394]	-9464	187.5
1731	S[1215]	-6958	312.5	1791	S[1275]	-7798	312.5	1851	S[1335]	-8638	312.5	1911	S[1395]	-9478	312.5
1732	S[1216]	-6972	187.5	1792	S[1276]	-7812	187.5	1852	S[1336]	-8652	187.5	1912	S[1396]	-9492	187.5
1733	S[1217]	-6986	312.5	1793	S[1277]	-7826	312.5	1853	S[1337]	-8666	312.5	1913	S[1397]	-9506	312.5
1734	S[1218]	-7000	187.5	1794	S[1278]	-7840	187.5	1854	S[1338]	-8680	187.5	1914	S[1398]	-9520	187.5
1735	S[1219]	-7014	312.5	1795	S[1279]	-7854	312.5	1855	S[1339]	-8694	312.5	1915	S[1399]	-9534	312.5
1736	S[1220]	-7028	187.5	1796	S[1280]	-7868	187.5	1856	S[1340]	-8708	187.5	1916	S[1400]	-9548	187.5
1737	S[1221]	-7042	312.5	1797	S[1281]	-7882	312.5	1857	S[1341]	-8722	312.5	1917	S[1401]	-9562	312.5
1738	S[1222]	-7056	187.5	1798	S[1282]	-7896	187.5	1858	S[1342]	-8736	187.5	1918	S[1402]	-9576	187.5
1739	S[1223]	-7070	312.5	1799	S[1283]	-7910	312.5	1859	S[1343]	-8750	312.5	1919	S[1403]	-9590	312.5
1740	S[1224]	-7084	187.5	1800	S[1284]	-7924	187.5	1860	S[1344]	-8764	187.5	1920	S[1404]	-9604	187.5

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	Pad Name	X	Y
1921	S[1405]	-9618	312.5	1981	DMY	-10514	312.5	2041	GOUT[28]	-11354	312.5	ALMARK_R_T	11870	305
1922	S[1406]	-9632	187.5	1982	DMY	-10528	187.5	2042	GOUT[29]	-11368	187.5	ALMARK_L_T	-11870	305
1923	S[1407]	-9646	312.5	1983	DMY	-10542	312.5	2043	GOUT[29]	-11382	312.5			
1924	S[1408]	-9660	187.5	1984	DMY	-10556	187.5	2044	GOUT[30]	-11396	187.5			
1925	S[1409]	-9674	312.5	1985	DMY	-10570	312.5	2045	GOUT[30]	-11410	312.5			
1926	S[1410]	-9688	187.5	1986	DMY	-10584	187.5	2046	GOUT_VGLO	-11424	187.5			
1927	S[1411]	-9702	312.5	1987	DMY	-10598	312.5	2047	GOUT_VGLO	-11438	312.5			
1928	S[1412]	-9716	187.5	1988	DMY	-10612	187.5	2048	GOUT_VGLO	-11452	187.5			
1929	S[1413]	-9730	312.5	1989	DMY	-10626	312.5	2049	VGH_REG	-11466	312.5			
1930	S[1414]	-9744	187.5	1990	DMY	-10640	187.5	2050	VGH_REG	-11480	187.5			
1931	S[1415]	-9758	312.5	1991	DMY	-10654	312.5	2051	VGH_REG	-11494	312.5			
1932	S[1416]	-9772	187.5	1992	DMY	-10668	187.5	2052	LVGL	-11508	187.5			
1933	S[1417]	-9786	312.5	1993	DMY	-10682	312.5	2053	LVGL	-11522	312.5			
1934	S[1418]	-9800	187.5	1994	DMY	-10696	187.5	2054	LVGL	-11536	187.5			
1935	S[1419]	-9814	312.5	1995	DMY	-10710	312.5	2055	GOUT[31]	-11550	312.5			
1936	S[1420]	-9828	187.5	1996	DMY	-10724	187.5	2056	GOUT[31]	-11564	187.5			
1937	S[1421]	-9842	312.5	1997	DMY	-10738	312.5	2057	GOUT[32]	-11578	312.5			
1938	S[1422]	-9856	187.5	1998	DMY	-10752	187.5	2058	GOUT[32]	-11592	187.5			
1939	S[1423]	-9870	312.5	1999	DMY	-10766	312.5	2059	GOUT_VGLO	-11606	312.5			
1940	S[1424]	-9884	187.5	2000	DMY	-10780	187.5	2060	GOUT_VGLO	-11620	187.5			
1941	S[1425]	-9898	312.5	2001	DMY	-10794	312.5	2061	GOUT_VGLO	-11634	312.5			
1942	S[1426]	-9912	187.5	2002	DMY	-10808	187.5	2062	GOUT_VGHO	-11648	187.5			
1943	S[1427]	-9926	312.5	2003	DMY	-10822	312.5	2063	GOUT_VGHO	-11662	312.5			
1944	S[1428]	-9940	187.5	2004	DMY	-10836	187.5	2064	GOUT_VGHO	-11676	187.5			
1945	S[1429]	-9954	312.5	2005	DMY	-10850	312.5	2065	PADA4	-11690	312.5			
1946	S[1430]	-9968	187.5	2006	DMY	-10864	187.5	2066	PADB4	-11704	187.5			
1947	S[1431]	-9982	312.5	2007	DMY	-10878	312.5	2067	DMY_VSS	-11718	312.5			
1948	S[1432]	-9996	187.5	2008	DMY	-10892	187.5	2068	DMY_VSS	-11732	187.5			
1949	S[1433]	-10010	312.5	2009	DMY	-10906	312.5	2069	DMY_VSS	-11760	312.5			
1950	S[1434]	-10024	187.5	2010	DMY	-10920	187.5							
1951	S[1435]	-10038	312.5	2011	DMY	-10934	312.5							
1952	S[1436]	-10052	187.5	2012	DMY	-10948	187.5							
1953	S[1437]	-10066	312.5	2013	DMY	-10962	312.5							
1954	S[1438]	-10080	187.5	2014	DMY	-10976	187.5							
1955	S[1439]	-10094	312.5	2015	DMY	-10990	312.5							
1956	S[1440]	-10108	187.5	2016	DMY_VSS	-11004	187.5							
1957	S[1441]	-10122	312.5	2017	DMY_VSS	-11018	312.5							
1958	DMY_VSS	-10136	187.5	2018	GOUT[17]	-11032	187.5							
1959	DMY_VSS	-10150	312.5	2019	GOUT[17]	-11046	312.5							
1960	GOUT_VGLO	-10220	187.5	2020	GOUT[18]	-11060	187.5							
1961	GOUT_VGLO	-10234	312.5	2021	GOUT[18]	-11074	312.5							
1962	GOUT_VGLO	-10248	187.5	2022	GOUT[19]	-11088	187.5							
1963	GOUT_VGLO	-10262	312.5	2023	GOUT[19]	-11102	312.5							
1964	GOUT_VGLO	-10276	187.5	2024	GOUT[20]	-11116	187.5							
1965	GOUT_VGLO	-10290	312.5	2025	GOUT[20]	-11130	312.5							
1966	DMY_VGH	-10304	187.5	2026	GOUT[21]	-11144	187.5							
1967	DMY_VGH	-10318	312.5	2027	GOUT[21]	-11158	312.5							
1968	GOUT_VGHO	-10332	187.5	2028	GOUT[22]	-11172	187.5							
1969	GOUT_VGHO	-10346	312.5	2029	GOUT[22]	-11186	312.5							
1970	GOUT_VGHO	-10360	187.5	2030	GOUT[23]	-11200	187.5							
1971	GOUT_VGHO	-10374	312.5	2031	GOUT[23]	-11214	312.5							
1972	GOUT_VGHO	-10388	187.5	2032	GOUT[24]	-11228	187.5							
1973	GOUT_VGHO	-10402	312.5	2033	GOUT[24]	-11242	312.5							
1974	DMY_VSS	-10416	187.5	2034	GOUT[25]	-11256	187.5							
1975	DMY_VSS	-10430	312.5	2035	GOUT[25]	-11270	312.5							
1976	DMY	-10444	187.5	2036	GOUT[26]	-11284	187.5							
1977	DMY	-10458	312.5	2037	GOUT[26]	-11298	312.5							
1978	DMY	-10472	187.5	2038	GOUT[27]	-11312	187.5							
1979	DMY	-10486	312.5	2039	GOUT[27]	-11326	312.5							

5 System Interface

5.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in **Table 5.1.1**

Table 5.1.1 Interface Type Selection

IM3	IM2	IM1	IM0	Display Data	Register
1	0	0	1	RGB interface, D[23:0]	8-bit SPI, SDI/SDO serial data, SCL rising trigger
0	0	0	1	RGB interface, D[23:0]	8-bit SPI, SDI/SDO serial data, SCL falling trigger
1	0	1	0	RGB interface, D[23:0]	9-bit SPI, SDI/SDO serial data, SCL rising trigger
0	0	1	0	RGB interface, D[23:0]	9-bit SPI, SDI/SDO serial data, SCL falling trigger
0	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL rising trigger
1	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL falling trigger
x	1	0	1	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N

5.2 SPI Interface

The following is selection of interface decided by the IM [3:0] pins.

The GC9503V uses a 3-line 9-bit serial interface for communication between the host and the GC9503V. The 3-line serial interface consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). If the data bus (DB [23:0]) is not used for the data transfer of DPI interface, the unused pins are unaffected. The Serial clock (SCL) is used only for the interface with the MPU, so it can be stopped when no communication is necessary.

5.2.1 SPI-8BIT/9BIT Write Cycle Sequence

In write mode of the interface, the host writes commands and data to the GC9503V. The 3-line serial data packet contains a D/C (data/command) select bit and a transmission byte. If the D/C bit is “low”, the transmission byte is interpreted as a command byte. If the D/C bit is “high”, the transmission byte is stored in the command register as a parameter data.

Any instruction can be sent in any order to the GC9503V and the MSB is transmitted first. The serial interface is initialized when the CSX status is high. In this state, SCL clock pulse and SDI data are ineffective. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detail of data format for 3-line serial interface.

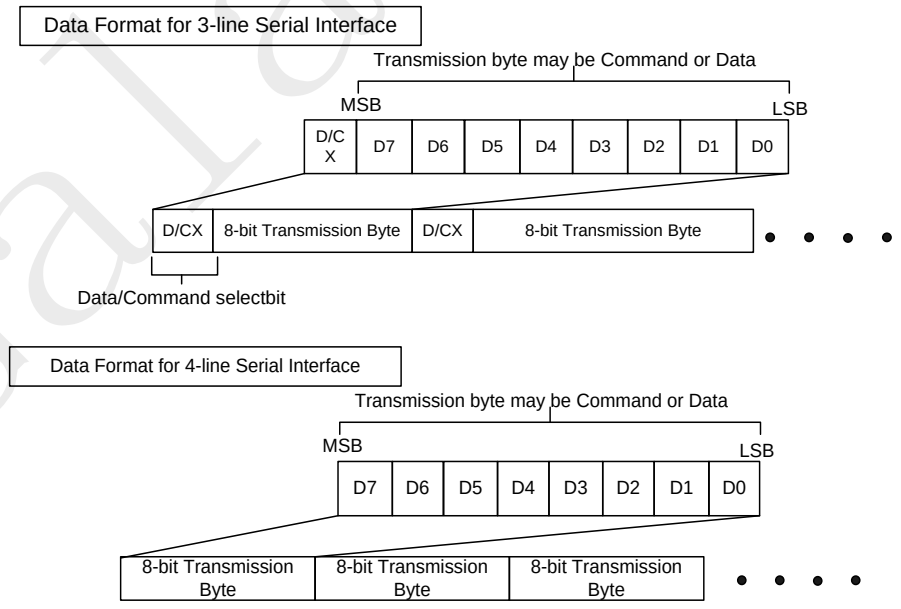


Figure 2 DBI data format

The host drives the CSX pin to low and setting the D/C bit on the SDI pin. The bit is read by the GC9503V on the first rising edge of the SCL signal. On the next falling edge of the SCL,

the MSB data bit (D7) is set on the SDI pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDI pin. If the optional D/C signal is used, a byte is eight read cycles long. The 3-line serial interface writes sequences described in the Figure 3 below

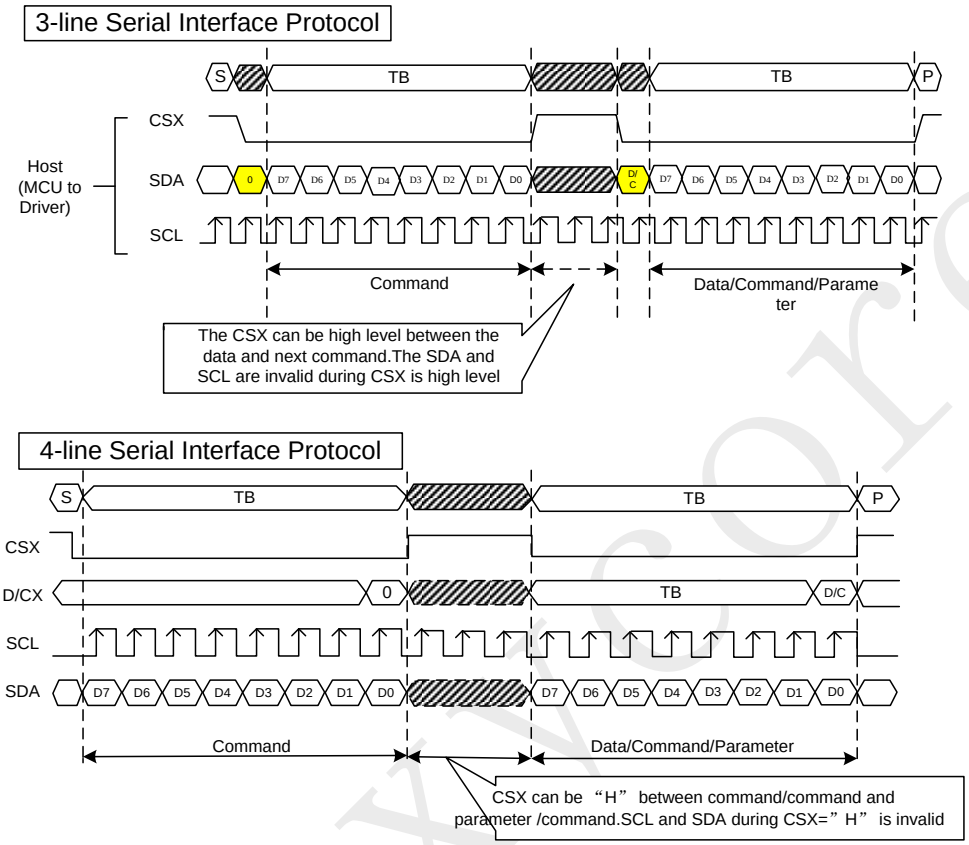


Figure 3 SPI protocol (SCL rising edge example)

5.2.2 SPI-8BIT/9BIT Read Cycle Sequence

In read mode of the interface, the host reads the register value from the GC9503V. The host sends a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The GC9503V samples the SDI (input data) at the rising edges of the SCL (serial clock), and shifts SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

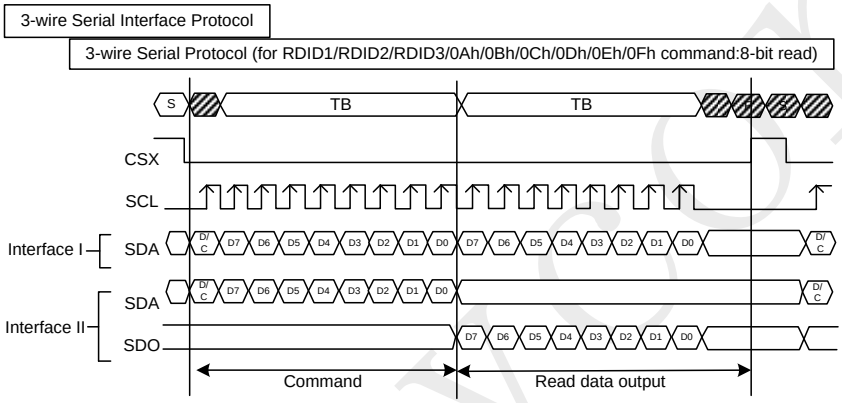


Figure 4 SPI read cycle sequence (SCL rising edge example)

5.2.3 Data Transfer Break and Recovery

If there data transmission is broken by CSX pulse while transferring a Command, Multiple parameter command, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and reset the interface so it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

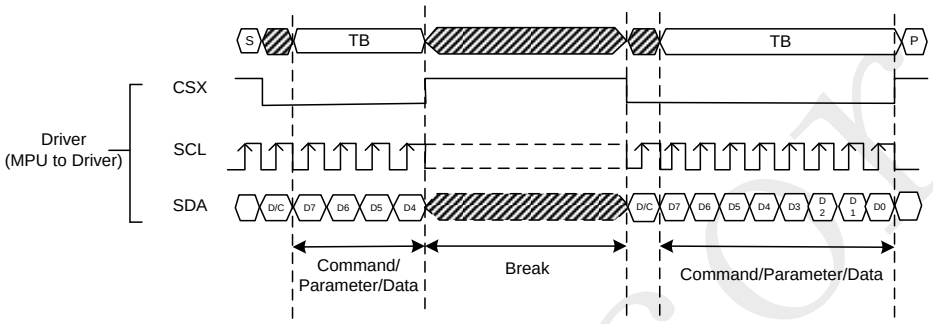


Figure 5 Data Transfer Break and Recovery (SCL rising edge example)

If there is a break in data transmission of a multiple parameter command, and the host initiates transfer of a new command, the parameters that were successfully transferred are stored and the incomplete parameter data where the break occurred is dropped. The interface is ready to receive the next byte as shown in the figure below. See diagram

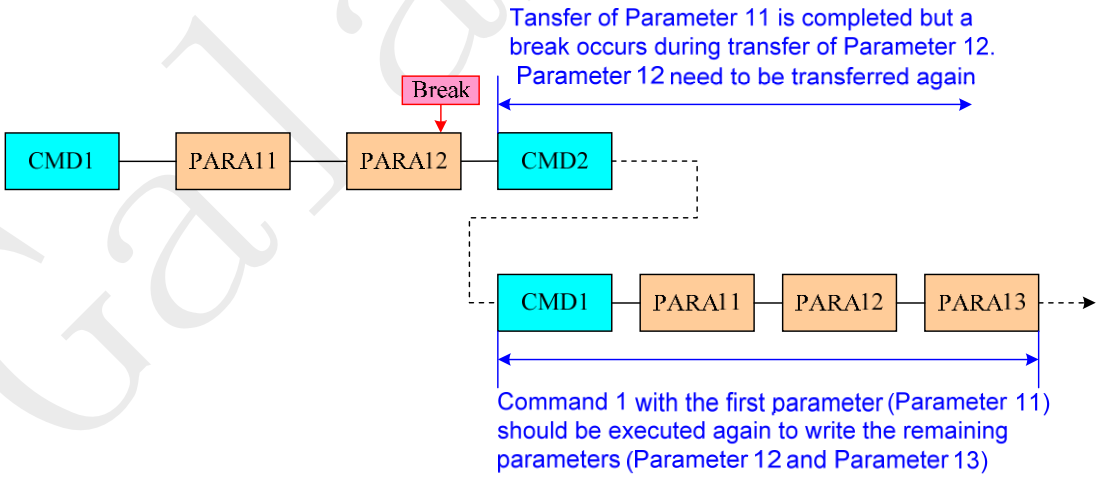


Figure 6 Data Transfer Break -Case 1

If a multiple parameter command is sent and a break occurs when a new command is sent before all the parameters are transferred, then the parameters that were successfully sent are stored and the remaining parameters of that command remain at the previous value.

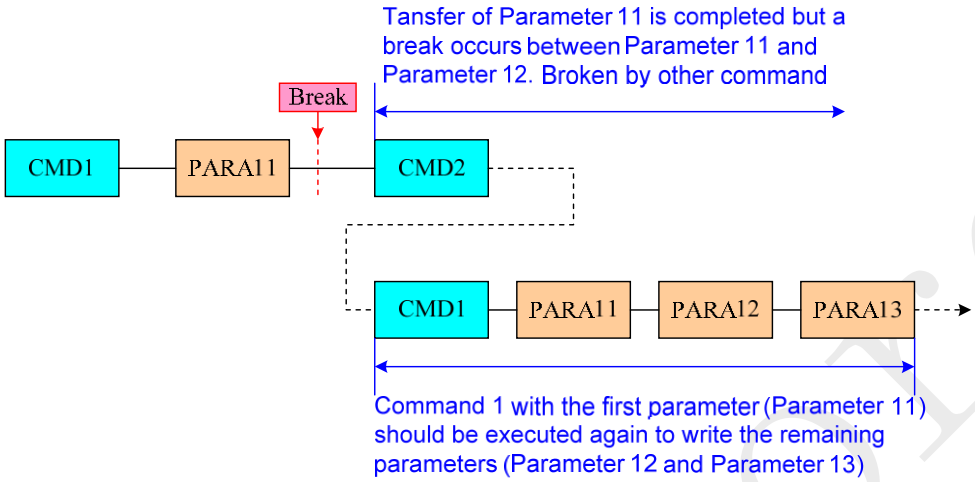


Figure 7 Data Transfer Break -Case 2

5.3 DPI (RGB) Interface

The DPI interface displaying moving pictures is selected by the GC9503V.

5.3.1DPI Interface Selection

The DPI interface is operated with VS, HS, DE PCLK, DB [23:0] lines. It supports several pixel formats that can be selected by DPI [2:0] bits in “Pixel Format Set (R3Ah)” of Page 0 command. The selection of a given interface is defined by DPI [2:0] as show in the Table 9 and Figure 10 below.

Table 9 DPI (RGB) Interface Selection

DPI [2:0]			DPI (RGB) Interface Mode	Used Pins
1	0	1	16-bit RGB interface	VS, HS, DE, PCLK,DB [20:16] , DB [13:8], DB [4:0]
1	1	0	18-bit RGB interface	VS, HS, DE, PCLK, DB [21:16] , DB [13:8], DB [5:0]
1	1	1	24-bit RGB interface	VS, HS, DE, PCLK, DB [23:0]
Others			Setting prohibited	

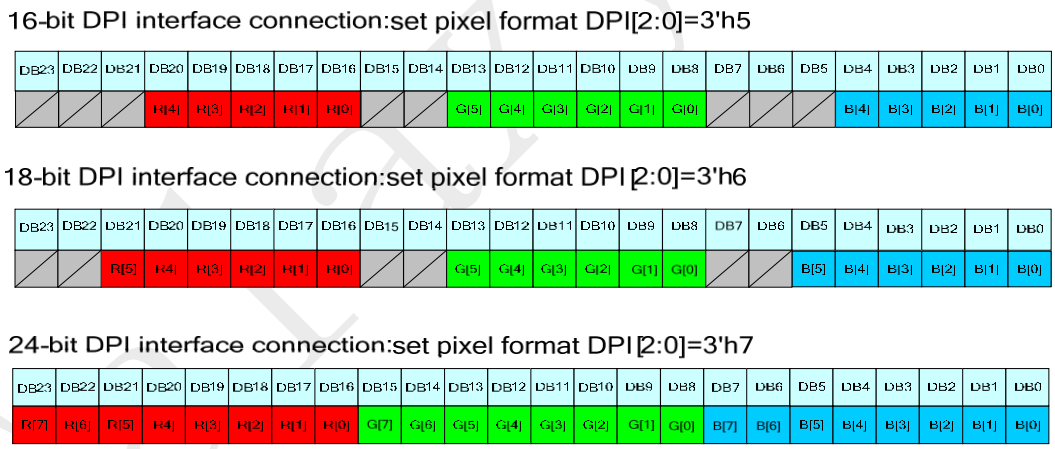


Figure 10 DPI (RGB) Interface 16/18/24-bit pixel format selection

The Pixel clock (PCLK) is running all the time without stopping, it is used for entering VS, HS, DE and DB [23:0] states when there is a rising edge of the PCLK. The PCLK can not be used as the internal clock for other functions of the display module.

Vertical synchronization (Vsync) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (Hsync) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

DE (Data Enable) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal. DB [23:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of PCLK). DB [23:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the PCLK signal.

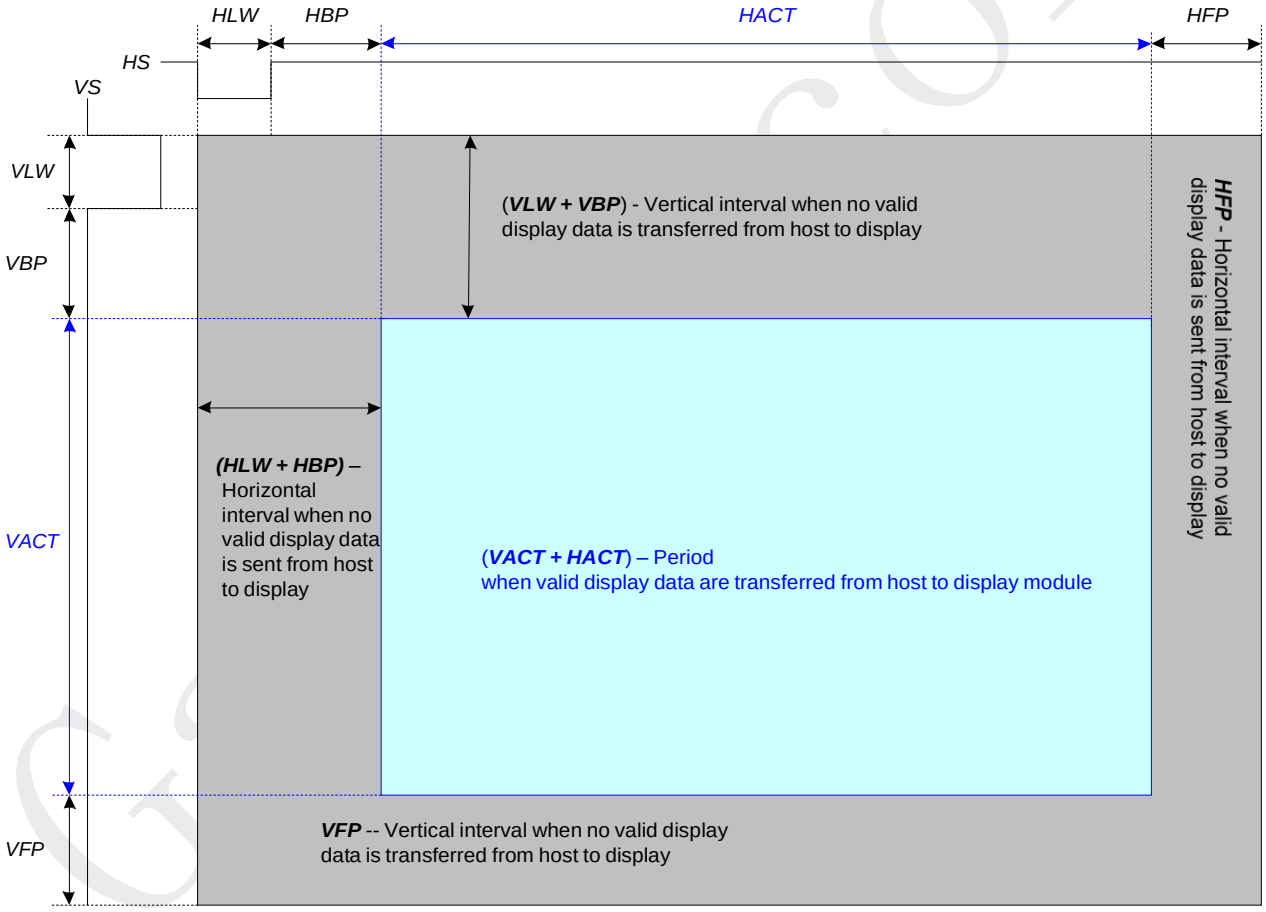
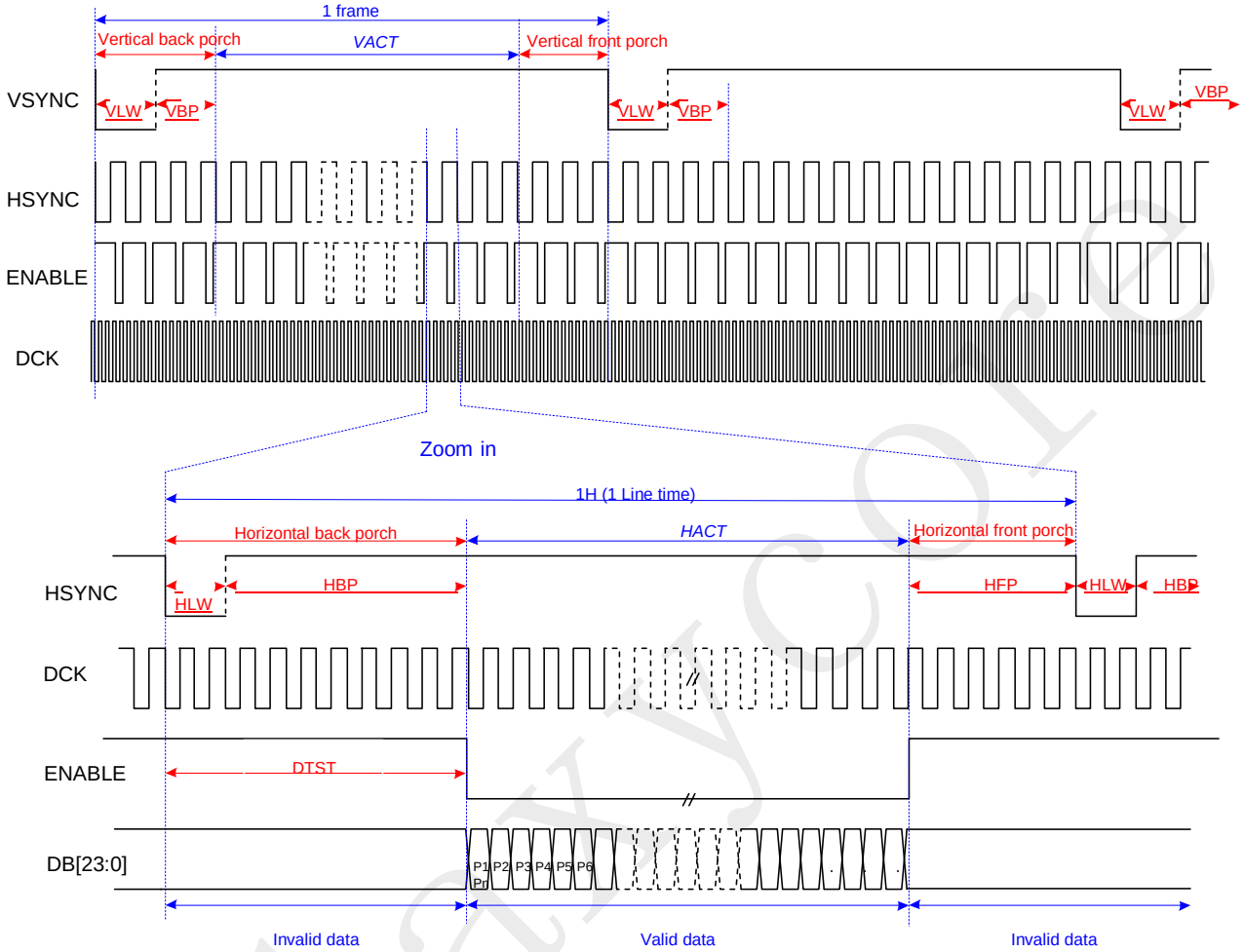


Figure 11 General DPI timing diagram

5.3.2 DPI Interface Timing

The timing chart of 24-/18-/16-bit DPI (RGB) interface mode is illustrated in Figure 12.



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2…, pixel n.

Parameter	Symbol	Conditio	Min	Typ	Max	Units
Frame Rate	FR		54		6	fps
Horizontal Low Pulse width	HLW		1		-	DOTCL
Horizontal Back Porch	HBP		2		126	DOTCL
Horizontal Address	HACT			48		DOTCL
Horizontal Front Porch	HFP		2		-	DOTCL
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.		35.	MHz

Figure 12 DPI Interface Timing diagram[Note1,Note2]

Note1. HLW+HBP+HFP >= 4.5us.
Note2. VSPL='0', HSPL='0', DPL='0' and EPL='0' of "(Interface Mode Control 21h of the Page 1)" command.

5.4 DSI system interface

5.4.1 General Description

The MIPI DSI is enabled or disabled by external IM[3:0] pin.

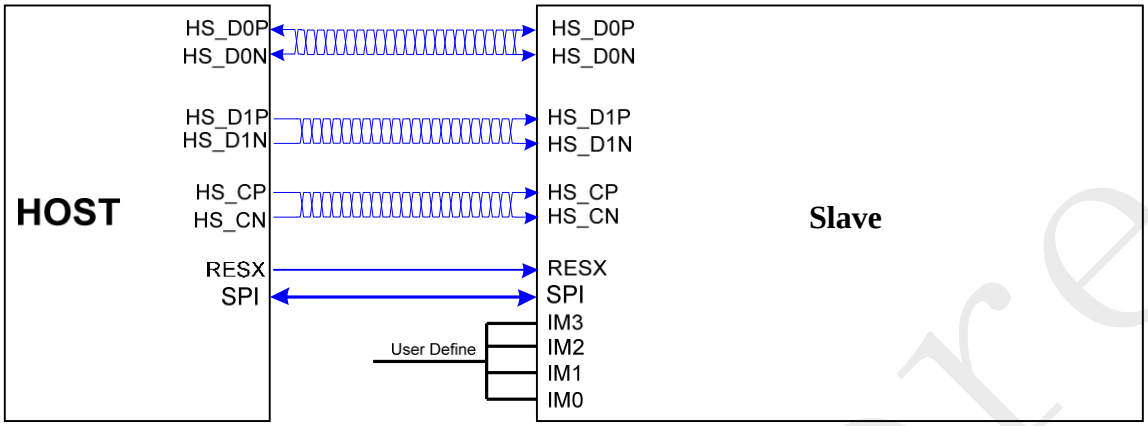


Figure 13 DSI system interface diagram

IM3	IM2	IM1	IM0	MPU Interface	Data Pin in Use
0	1	0	1	DSI interface	HS_CP, HS_CN, HS_D0P,HS_D0N, HS_D1P,HS_D1N,

The communication is separated into two different levels between the MPU and the display module:

Low level communication is done on the interface level.

High level communication is done on the packet level.

5.4.2 Interface Level Communication

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MPU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 10 High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage		High Speed	Low Power	
	DATA_P	DATA_N	Burst Mode	Control	Escape
HS-0	Low	High	Differential – 0	Note 1	Note 1
HS-1	High	Low	Differential – 1	Note 1	Note 1
LP-00	Low	Low	Not Defined	Bridge	Space
LP-01	Low	High	Not Defined	HS – Request	Mark - 0
LP-10	High	Low	Not Defined	LP - Request	Mark - 1
LP-11	High	High	Not Defined	Stop	Note 2

Note 1 *Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.*

Note 2 *If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.*

Note 3 *n = 0 and 1 (D1+/- lanes only for HS-0 and HS-1)*

5.4.3 DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

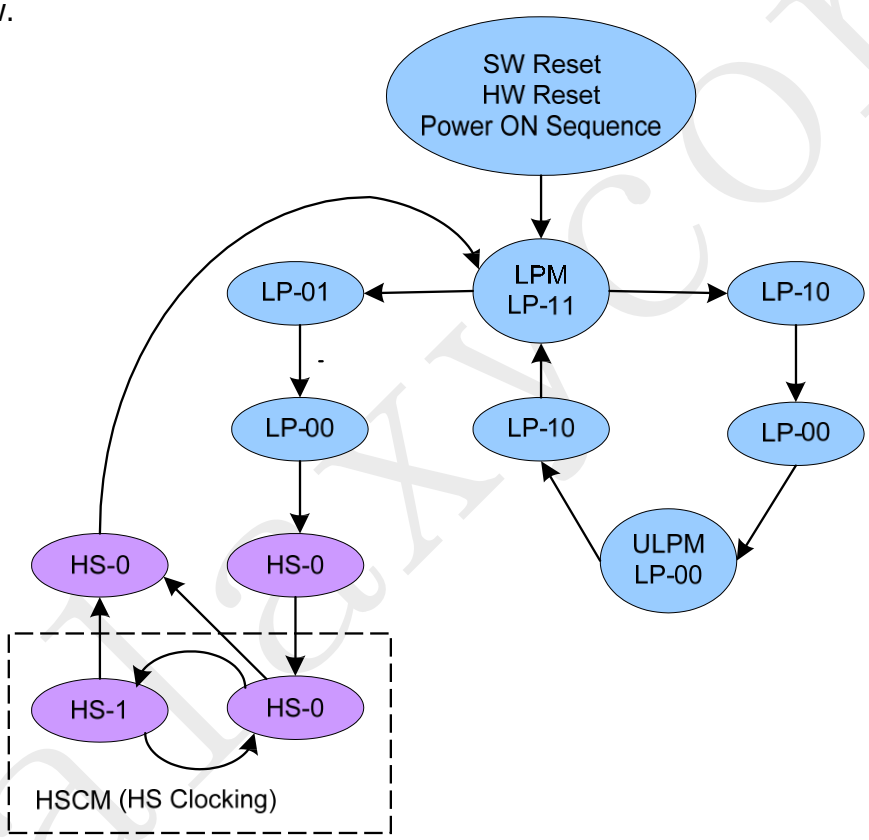


Figure 14 Clock Lanes Power Modes

5.4.4 Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

After SW Reset, HW Reset or Power On Sequence =>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM).

This sequence is illustrated below.

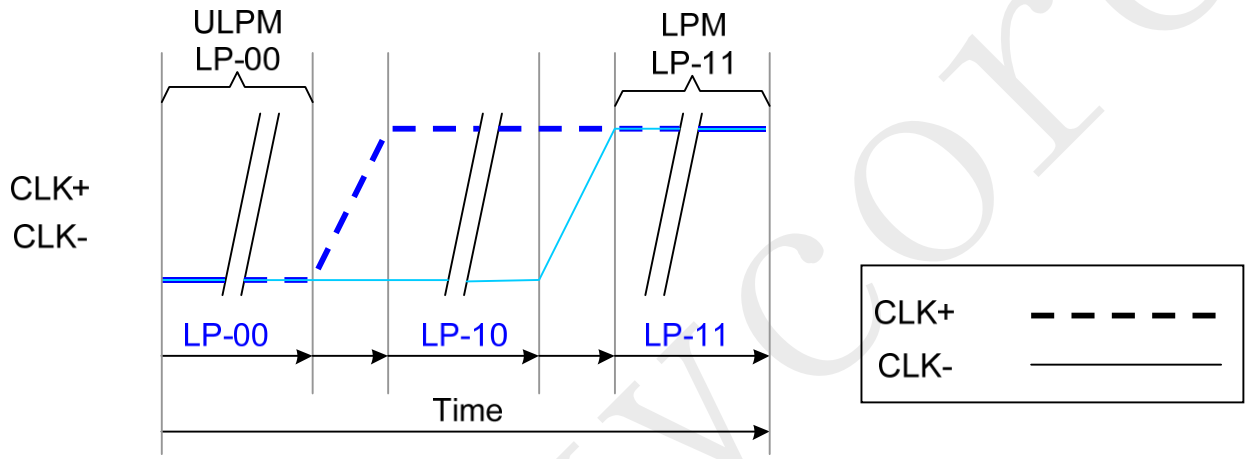


Figure 15 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.

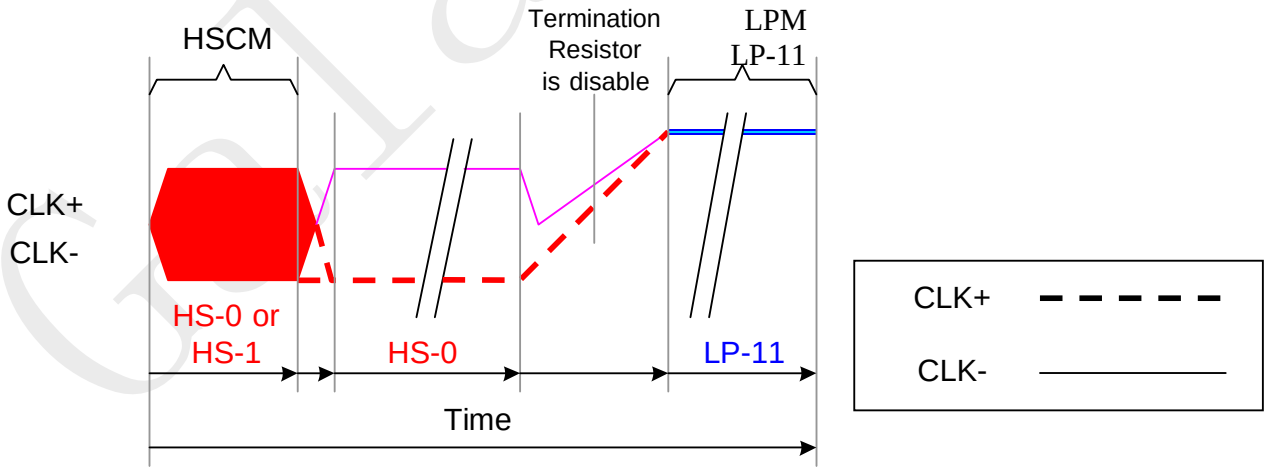


Figure 16 From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below.

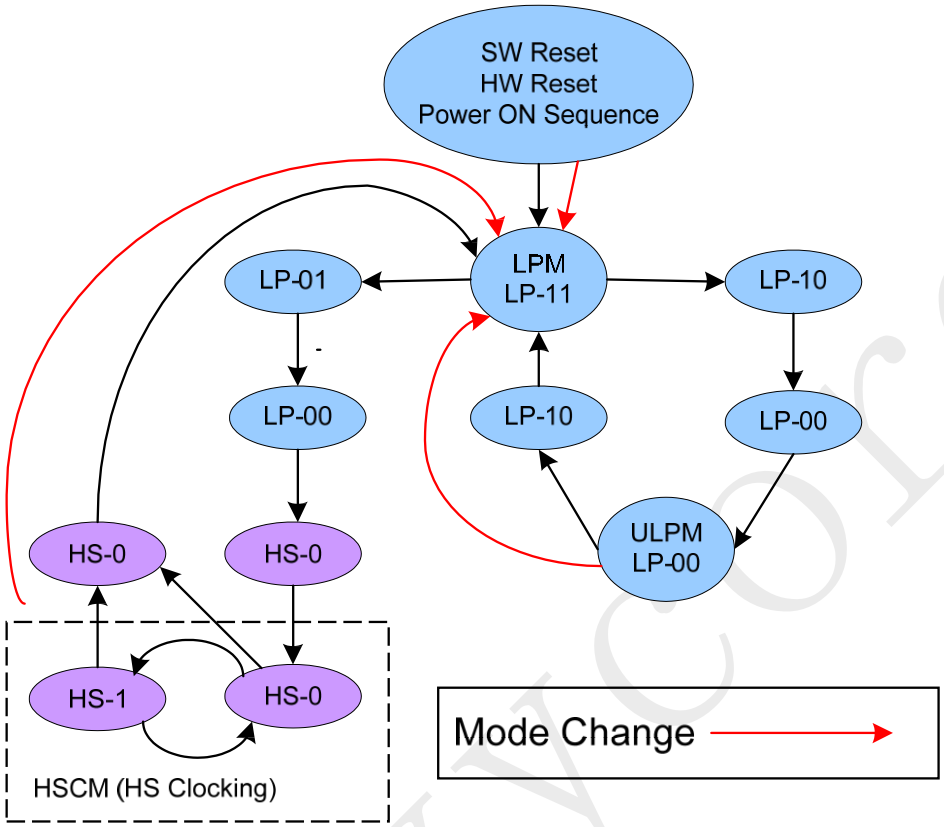


Figure 17 All Three Mode Changes to LPM on the Flow Chart

5.4.5 Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10

=>LP-00 (ULPM).

This sequence is illustrated below.

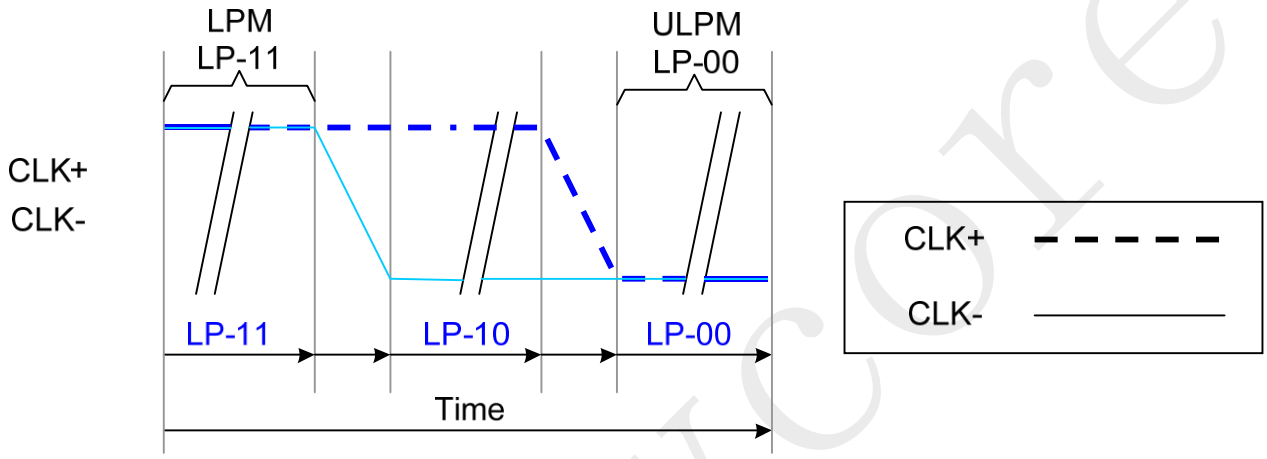


Figure 18 From LPM to ULPM

The mode change is also illustrated below.

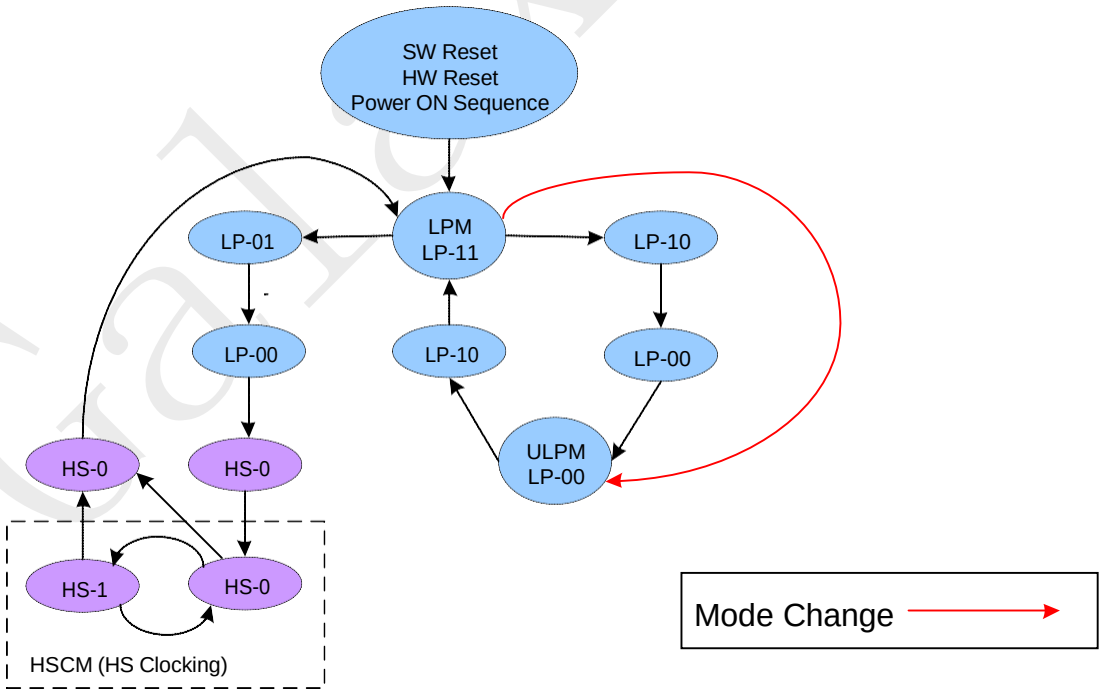


Figure 19 Mode Change from LPM to ULPM on the Flow Chart

5.4.5 High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00

=>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

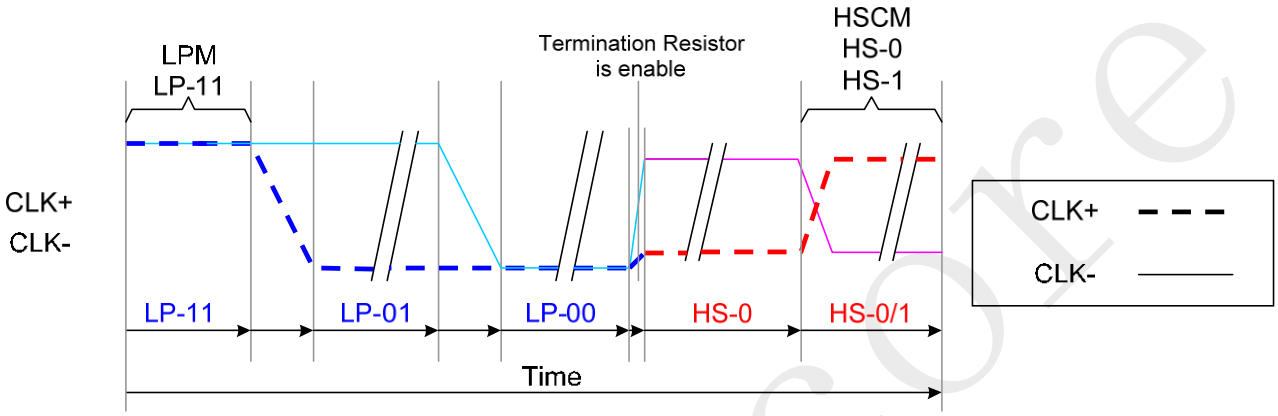


Figure 20 From LPM to HSCM

The mode change is also illustrated below.

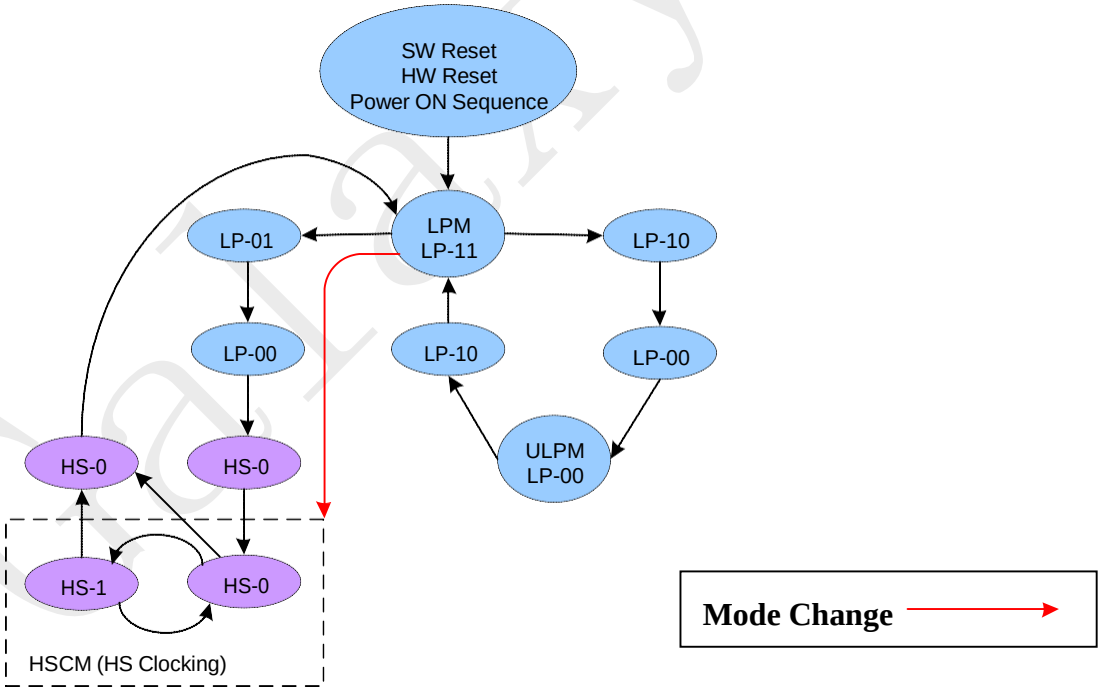


Figure 21 Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-D1+/- or DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

Even number of transitions

Start state is HS-0

End state is HS-0

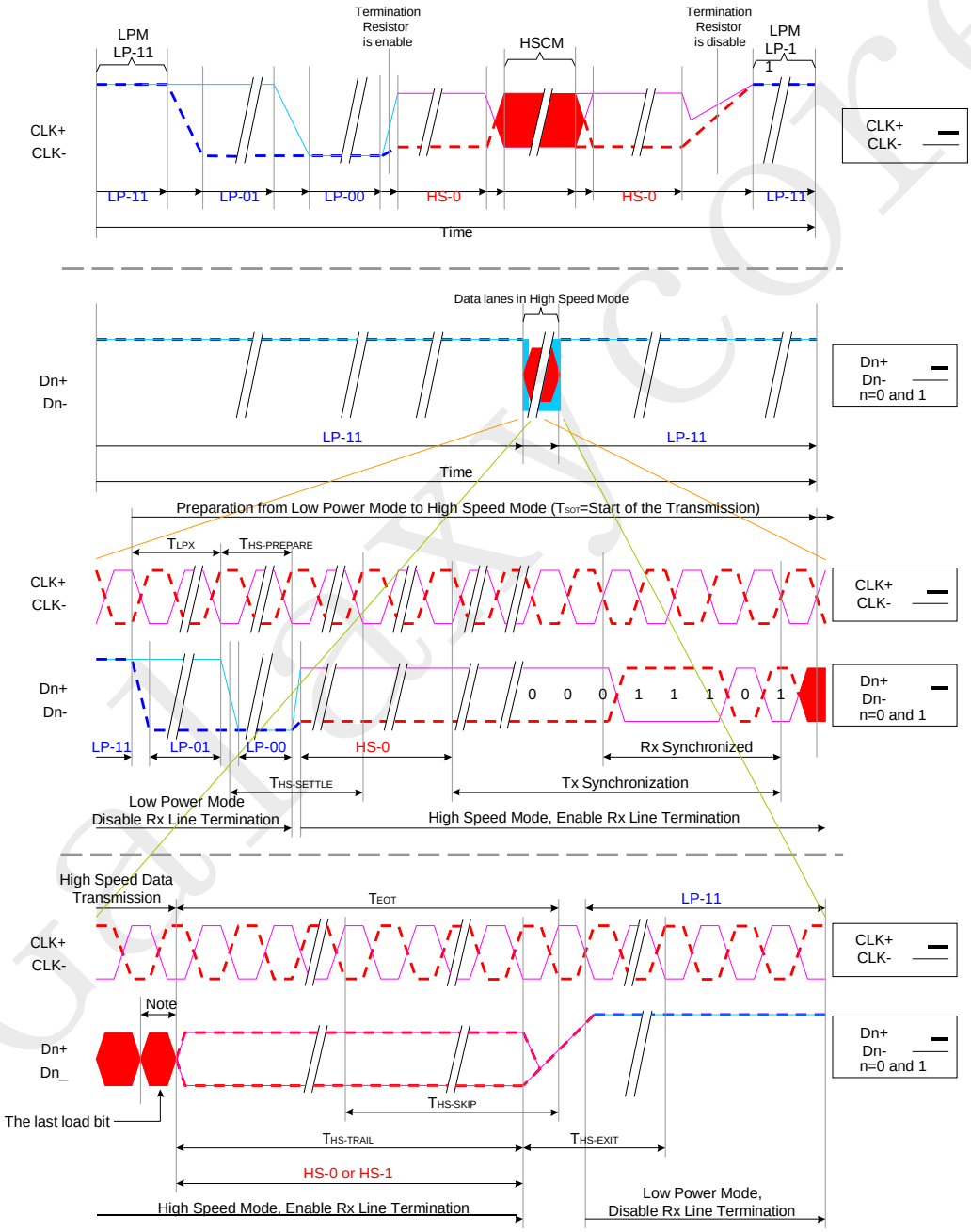


Figure 22 High Speed Clock Burst[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

5.4.6 DSI-D1 and DSI-D0 Data Lanes

DSI-D1+/- and DSI-D0+/- Data Lanes can be driven in different modes which are:

Escape Mode (Only DSI-D0+/- data lanes are used)

High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)

Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Table 11 Entering and Leaving Sequences[Note]

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 −+ LP-10 −+ LP-00 −+ LP-01 −+	LP-00 −+ LP-10 −+ LP-11
High-Speed Data	LP-11 −+ LP-01 −+ LP-00 −+ HS-0	(HS-0 or HS-1) −+ LP-11
Bus Turnaround Request	LP-11 −+ LP-10 −+ LP-00 −+ LP-10 −+	Hi-Z

Note 1. DSI-D1+/- and DSI-D0+/- data lanes are used.
2. More information on chapter “Bus Turnaround ”.

5.4.7 Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

Send “Low-Power Data Transmission” (LPDT) e.g. from the MPU to the display module,

Drive data lanes to “Ultra-Low Power State” (ULPS),

Indicate “Remote Application Reset” (RAR), which is resetting the display module,

Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MPU.

The basic sequence of the Escape Mode is as follow

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0-= 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

A load if it is needed

Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

End: LP-11

This basic construction is illustrated below:

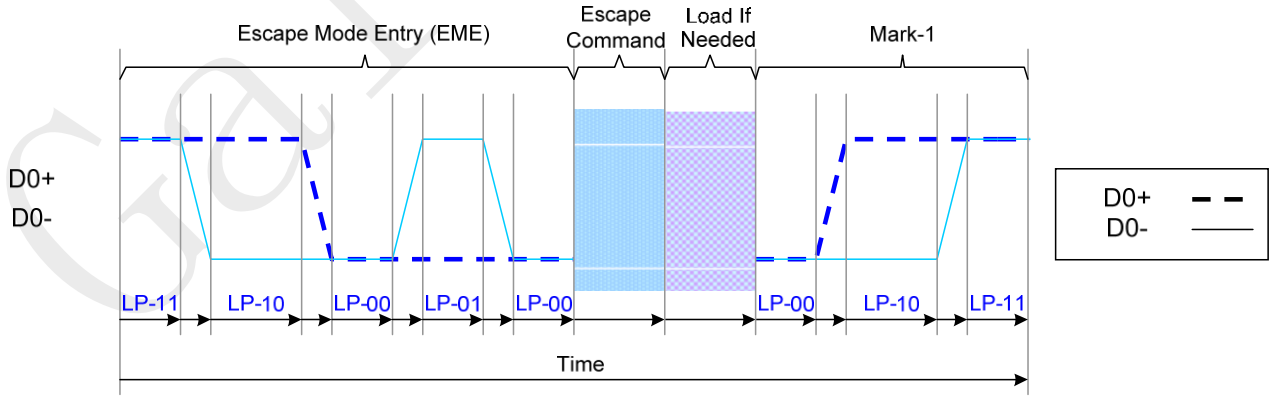


Figure 23 General Escape Mode Sequence

There are a total of eight Escape Commands (EC) divided into two types, Modes and Triggers, see Table 12: Escape Commands.

An example of a Mode type Escape Command is ‘Ultra-Low Power Mode’ where the MPU instructs the display module to enter it’s Ultra-Low Power Mode.

Escape commands are defined on the next table.

Table 12 Escape Commands[Note]

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Bit → Last Bit Transmitted)	Dn	D0
Low-Power Data	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, [Note 1]	Mo	1001 1111 b	-	-
Undefined-2, [Note 1]	Mo	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Uknown-5, [Note 1]	Trigger	1010 0000 b	-	-

Note 1. This Escape command support has not been implemented on the display module.
n = 1
x = Supported
- = Not Supported

5.4.8 Low-Power Data Transmission (LPDT)

The MPU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MPU.

The Low Power Data Transmission (LPDT) is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

Load (Data):

One or more bytes (8 bit)

Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

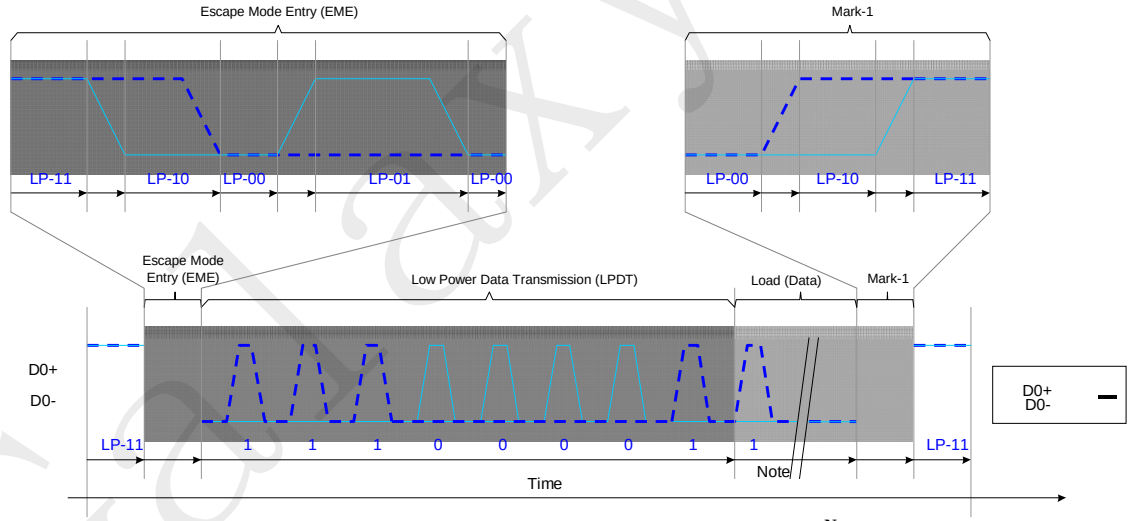


Figure 24 Low-Power Data Transmission (LPDT)[Note]

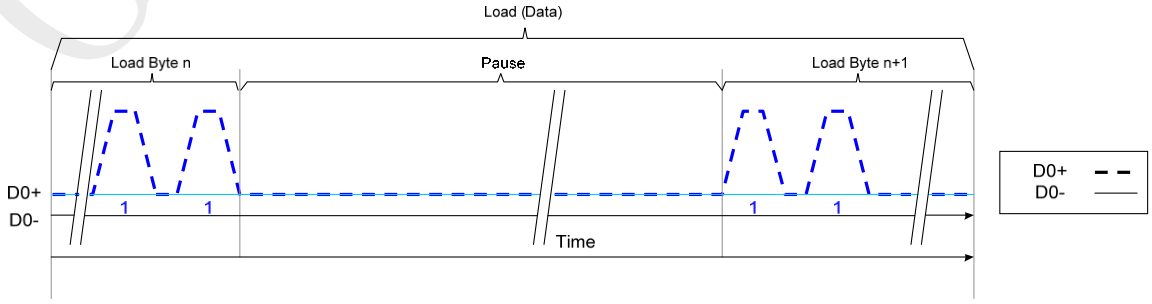


Figure 25 Pause (Example)

Note Load (Data) is presenting that the first bit is logical '1' in this example.

5.4.9 Ultra-Low Power State (ULPS)

The MPU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

Ultra-Low Power State (ULPS) when the MPU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

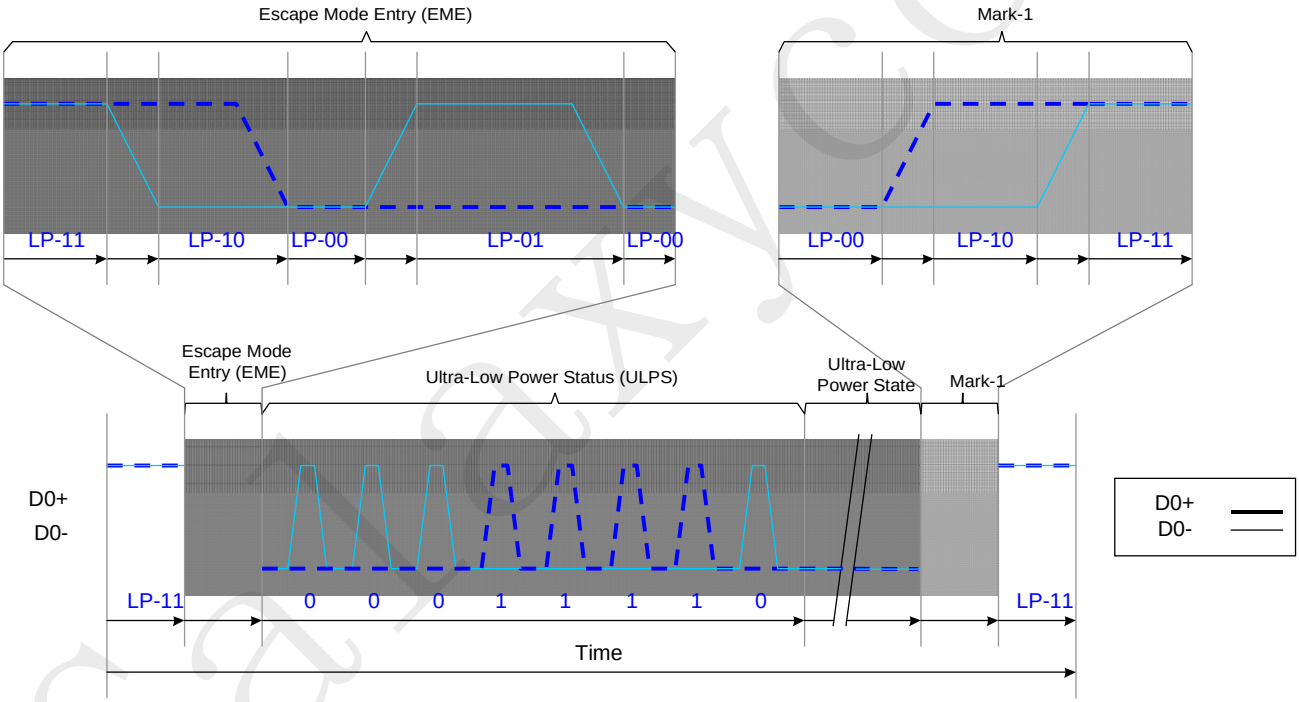


Figure 26 Ultra-Low Power State (ULPS)

5.4.10 Remote Application Reset (RAR)

The MPU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

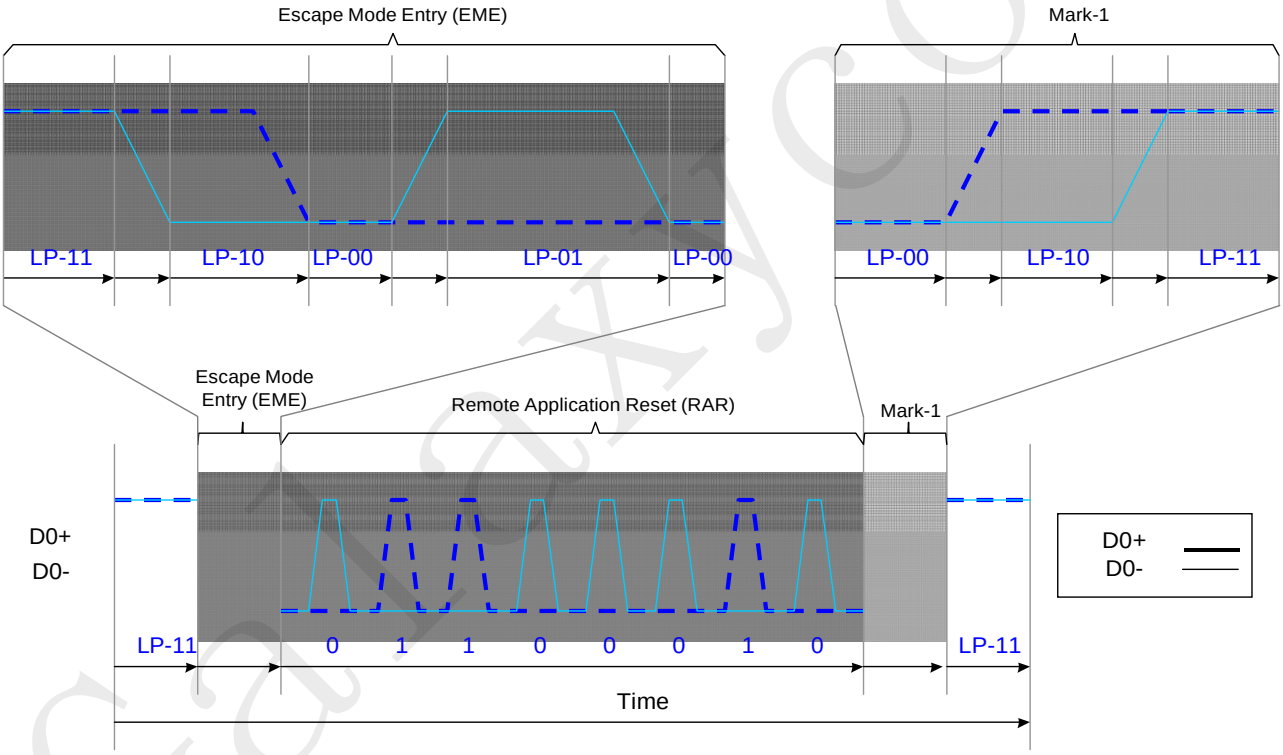


Figure 27 Remote Application Reset (RAR)

5.4.11 Acknowledge (ACK)

The display module can inform to the MPU when an error has not recognized on it by Acknowledge (ACK). The display module is sending the Acknowledge (ACK) what is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

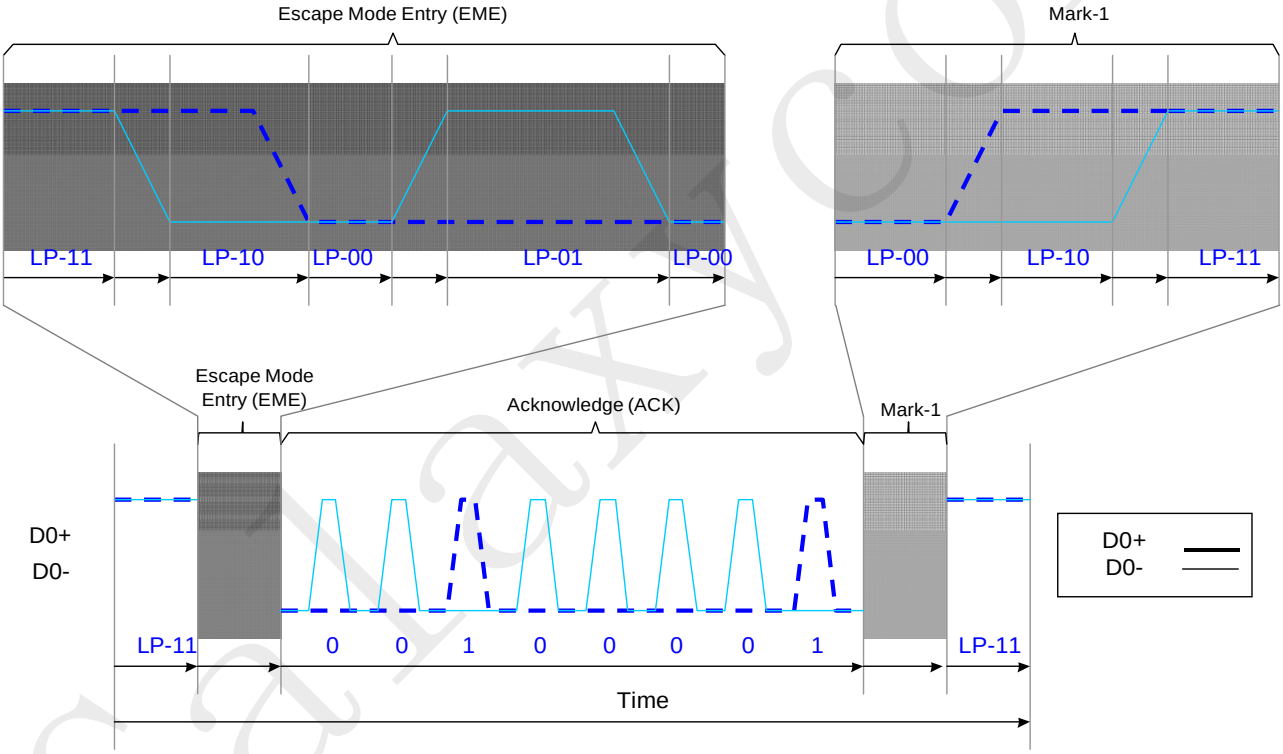


Figure 28 Acknowledge (ACK)

5.4.12 Entering High-Speed Data Transmission (TSOT of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MPU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

Start: LP-11

HS-Request: LP-01

HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

Rx Synchronization: 011101 (Tx (= MPU) Synchronization: 0001 1101)

End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below

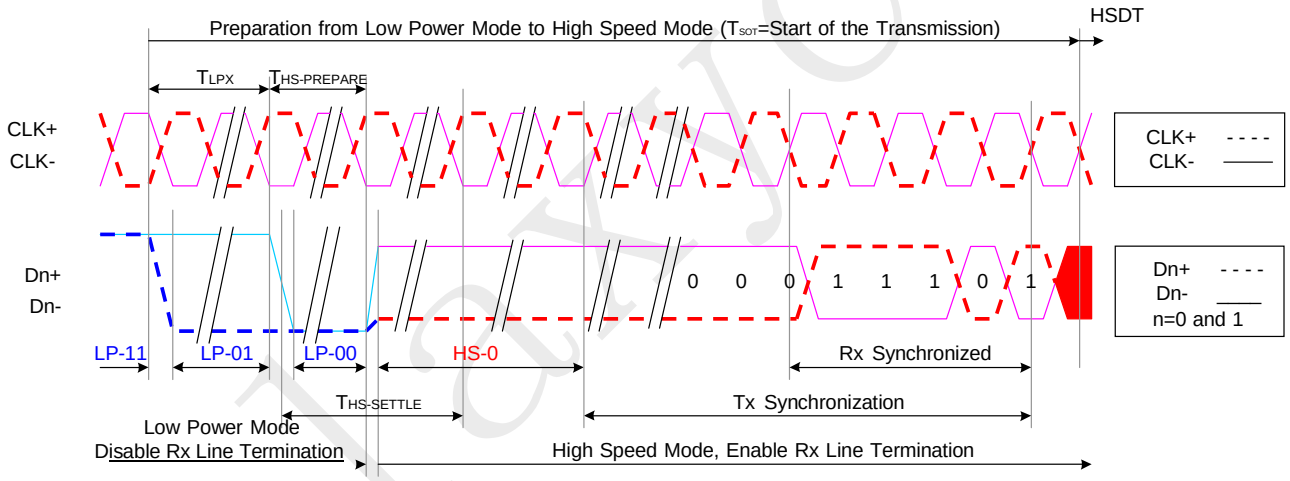


Figure 29 Entering High-Speed Data Transmission (TSOT of HSDT)

5.4.13 Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MPU and this HSCM is kept until data lanes DSI-D1+/- and DSI-D0+/- are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

Start: High-Speed Data Transmission (HSDT)

Stops High-Speed Data Transmission

o MPU changes to HS-1, if the last load bit is HS-0 o MPU changes to HS-0, if the last load bit is HS-1

End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

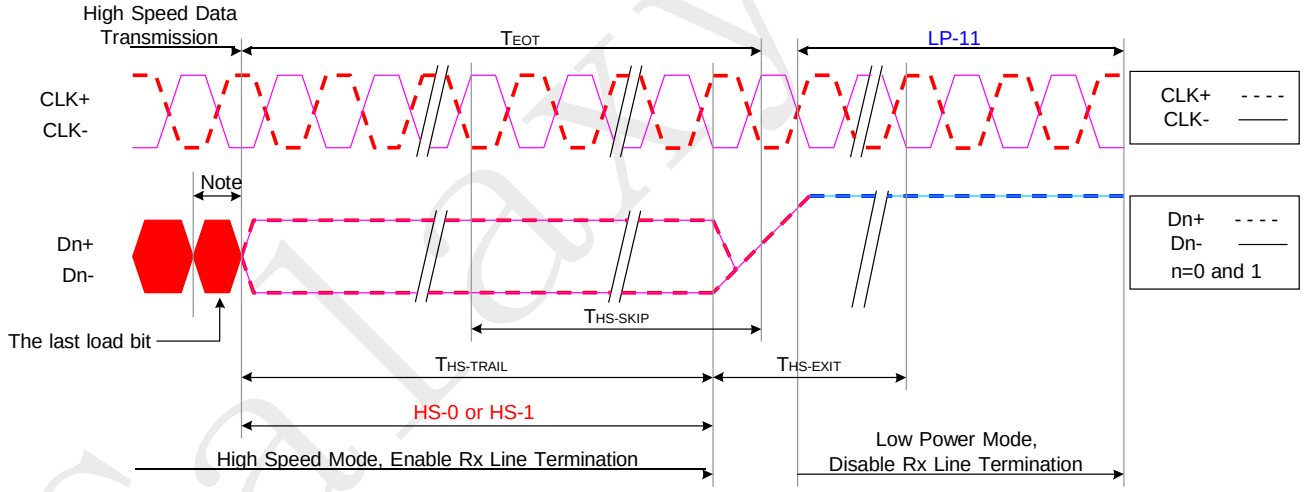


Figure 30 Leaving High-Speed Data Transmission (T_{EOT} of HSDT)[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

5.4.14 Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

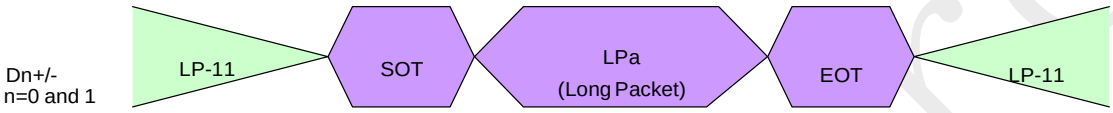
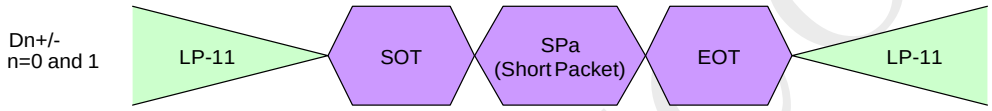


Figure 31 Single Packet in High-Speed Data Transmissions



The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:

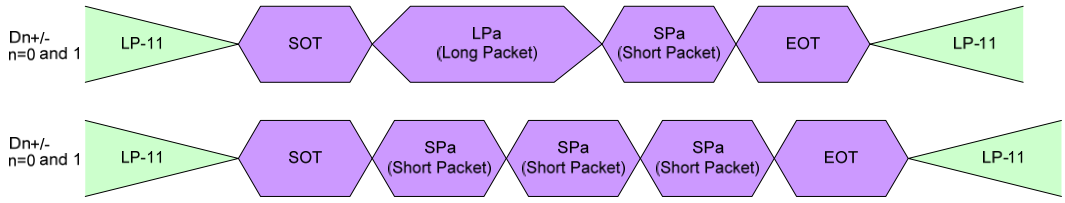


Figure 32 Multiple Packets in High-Speed Data Transmission – Examples

Table 13 Abbreviations

Abbreviatio	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet is in High-Speed Data Transmission (HSDT) as follows.

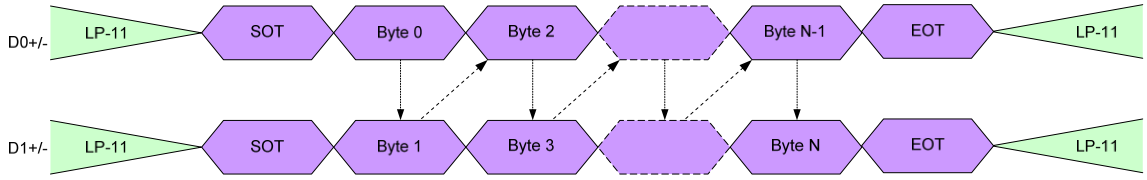


Figure 33 Single Packet in HSDT – Even Number of Bytes

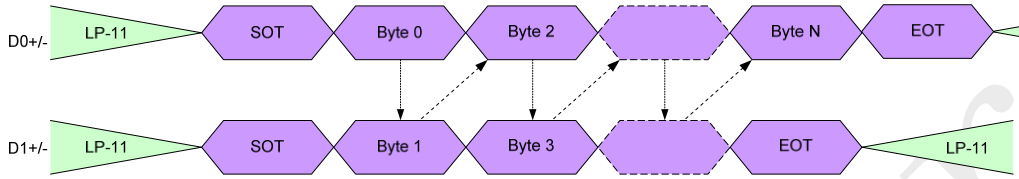


Figure 34 Single Packet in HSDT – Odd Number of Byte

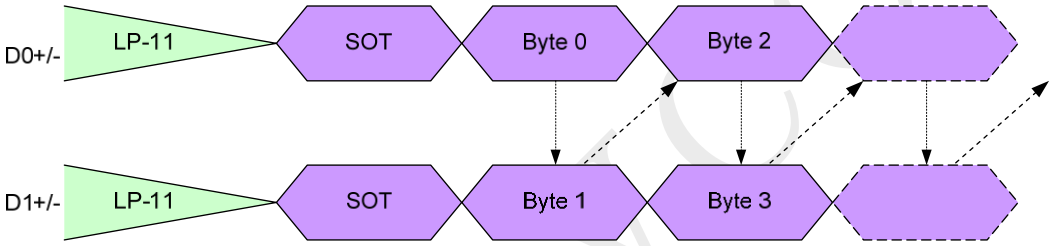


Figure 35 Start of Transmission (SoT) in HSDT for Multiple Packets

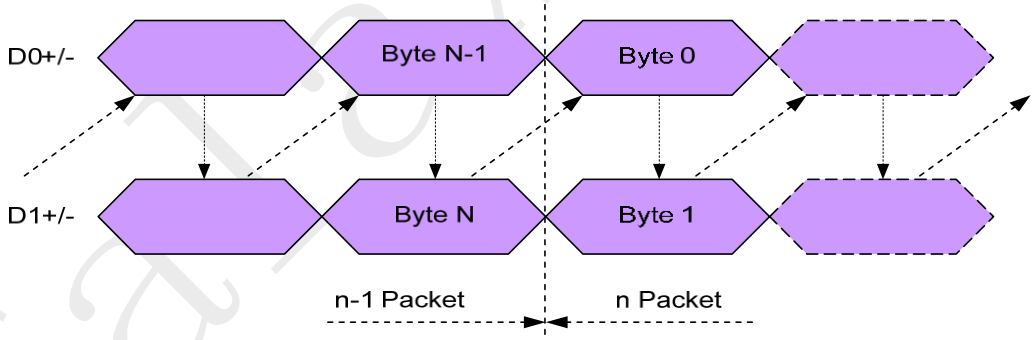


Figure 36 Continue Multiple Packets in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

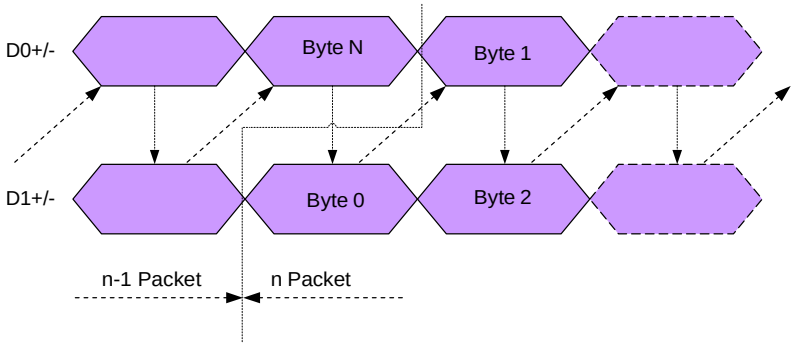


Figure 37 Continue Multiple Packets in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet

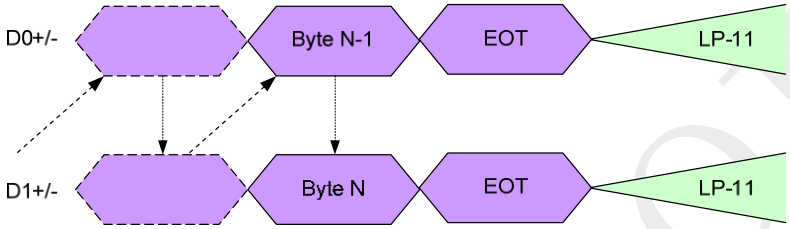


Figure 38 End of Transmission (EoT) in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

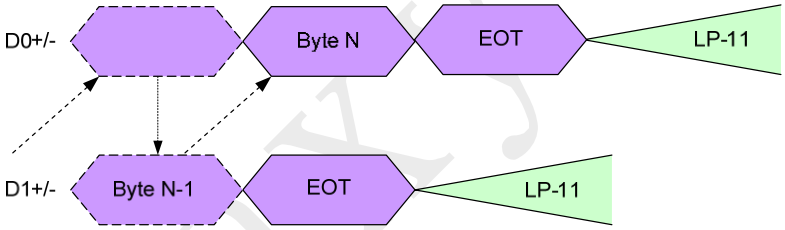


Figure 39 End of Transmission (EoT) in HSDT when Number of Bytes is not Equal on Both Data Lanes at cthe End of the Packet

5.4.15 Bus Turnaround (BTA)

The MPU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MPU or display module.

The MPU and display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MPU wants to do the bus turnaround procedure to the display module, as follows.

Start (MPU): LP-11

Turnaround Request (MPU): LP-11 =>LP-10 =>LP-00 => LP-10 => LP-00

The MPU waits until the display module is starting to control DSI-D0+/- data lanes and the MPU stops to control DSI-D0+/- data lanes (= High-Z)

The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MPU to the display module) is illustrated below

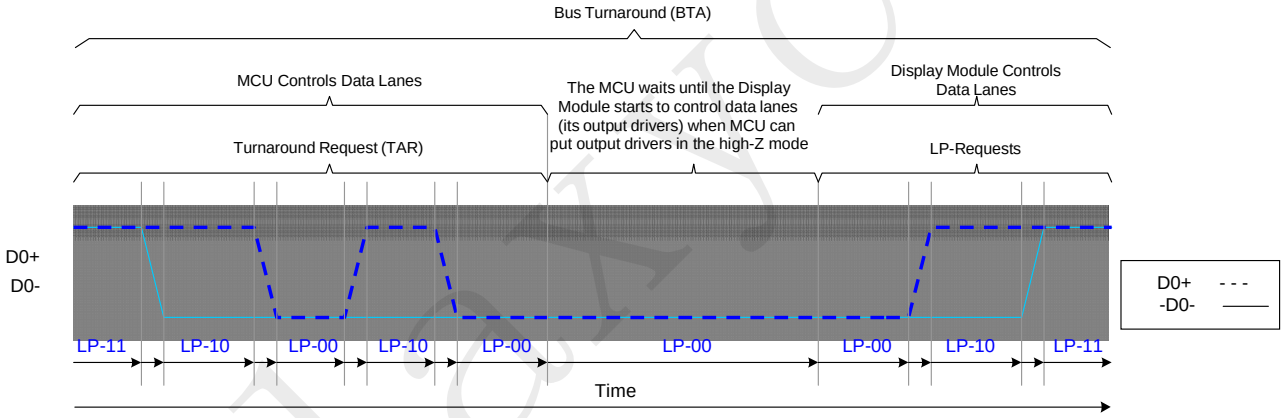


Figure 40 Bus Turnaround Procedure

MPU and display module terms are switched on the Figure 40, if the Bus Turnaround (BTA) is from the display module to the MPU.

5.4.16 Packet Level Communication

5.4.17 Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes[Note].

The lengths of the packets are

Short Packet (SPa): 4 bytes

Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

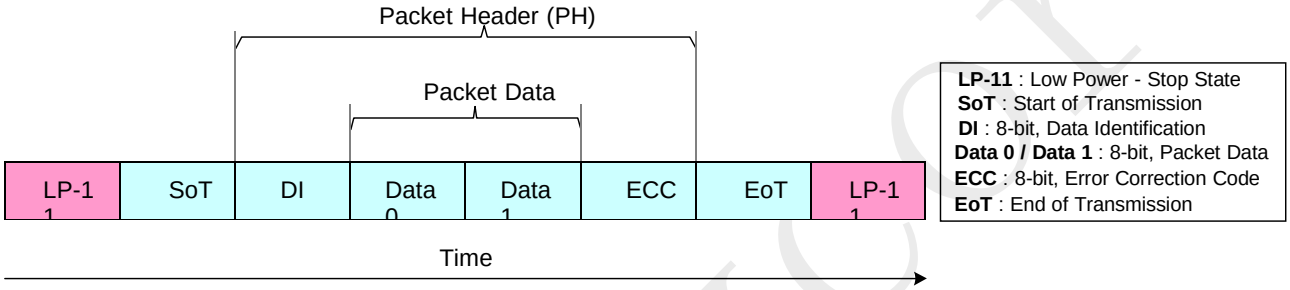


Figure 41 Short Packet (SPa) Structure

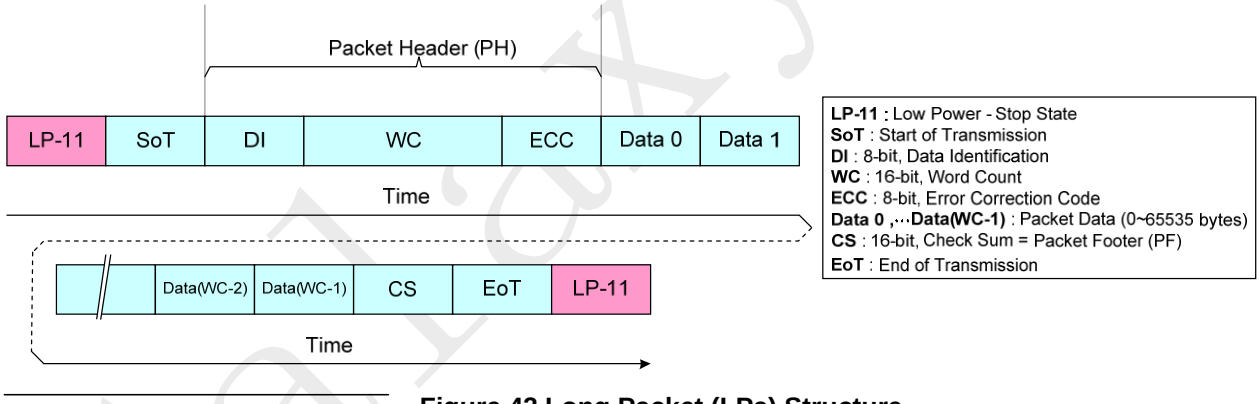


Figure 42 Long Packet (LPa) Structure

Note Short Packet (SPa) and Long Packet (LPa) are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

5.4.18 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last. This same order is illustrated for reference purposes below.

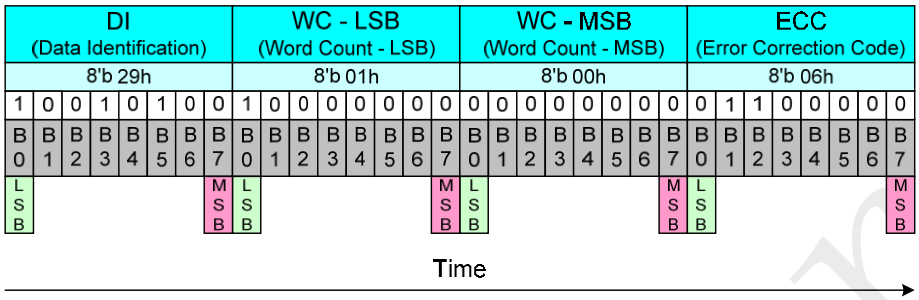


Figure 43 Bit Order of the Byte on Packets

5.4.19 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last

e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

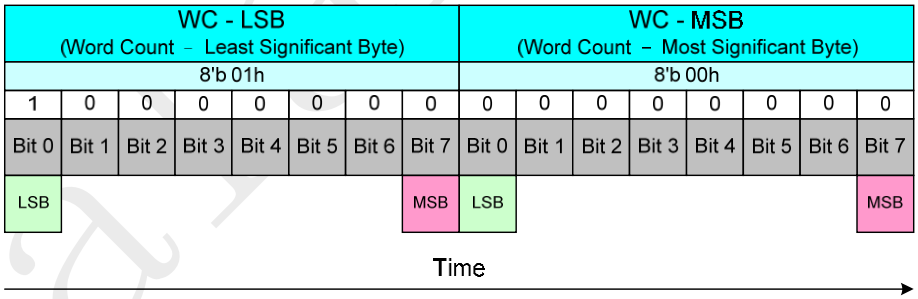


Figure 44 Byte Order of the Multiple Byte Information on Packets

5.4.20 Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

4th byte: Error Correction Code (ECC)

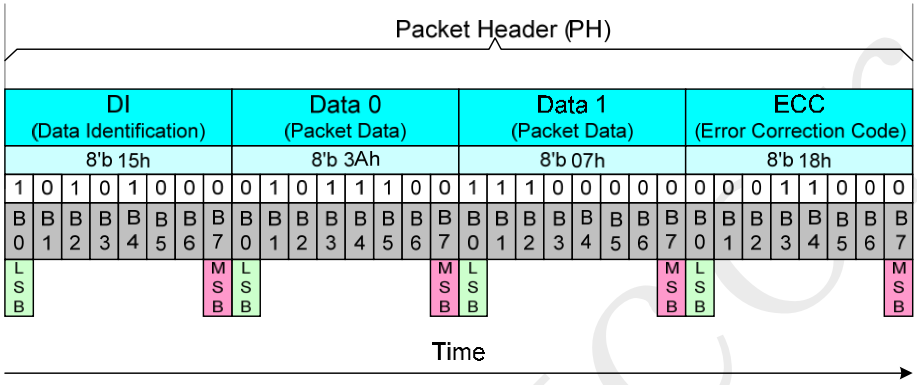


Figure 45 Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):

1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

2nd and 3rd bytes: Word Count (WC)

4th byte: Error Correction Code (ECC)

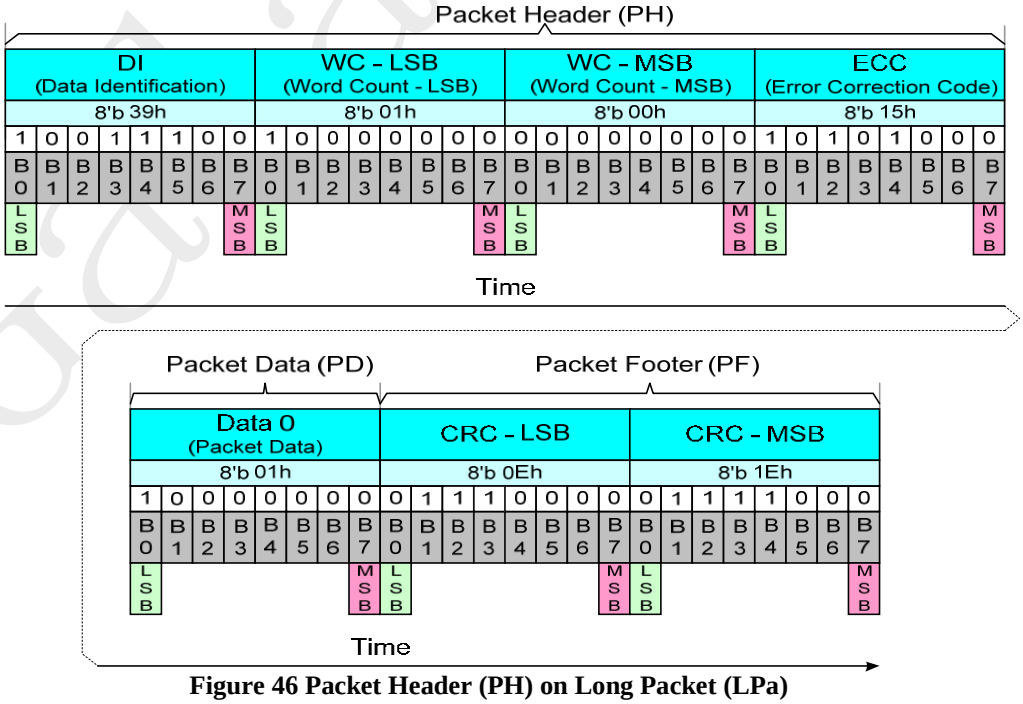


Figure 46 Packet Header (PH) on Long Packet (LPa)

5.4.21 Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

Virtual Channel (VC), 2 bits, DI[7...6]

Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated, see figure below.

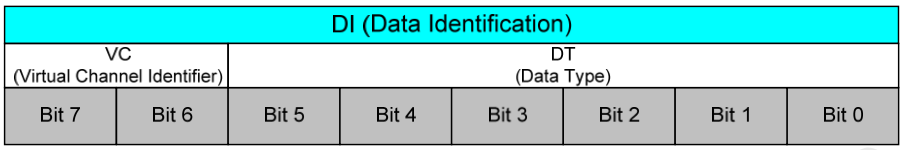


Figure 47 Data Identification (DI) Structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

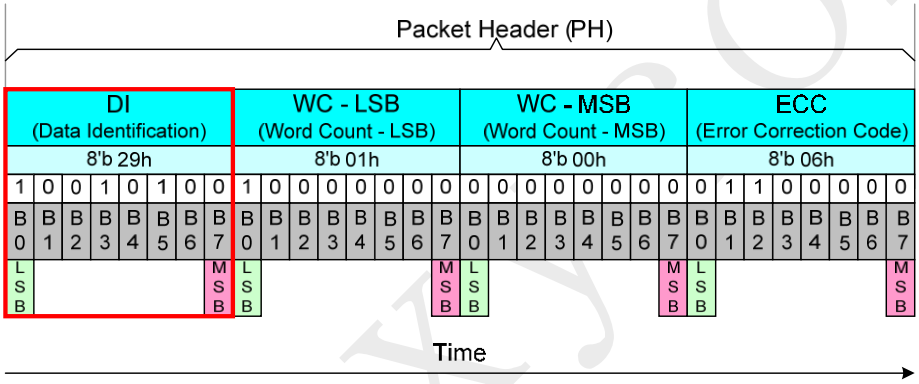


Figure 48 Data Identification (DI) on the Packet Header (PH)

5.4.22 Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MPU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

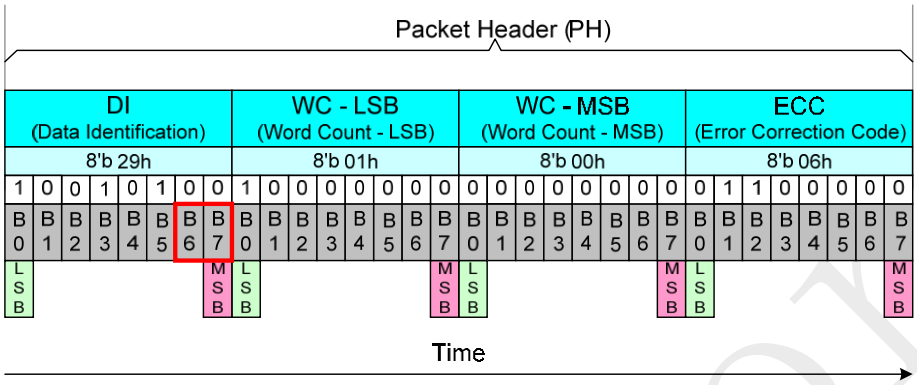


Figure 49 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MPU is using to send packets to them e.g.

The MPU is using the virtual channel 0 when it sends packets to this display module This display module is also using the virtual channel 0 when it sends packets to the MPU This functionality is illustrated below.

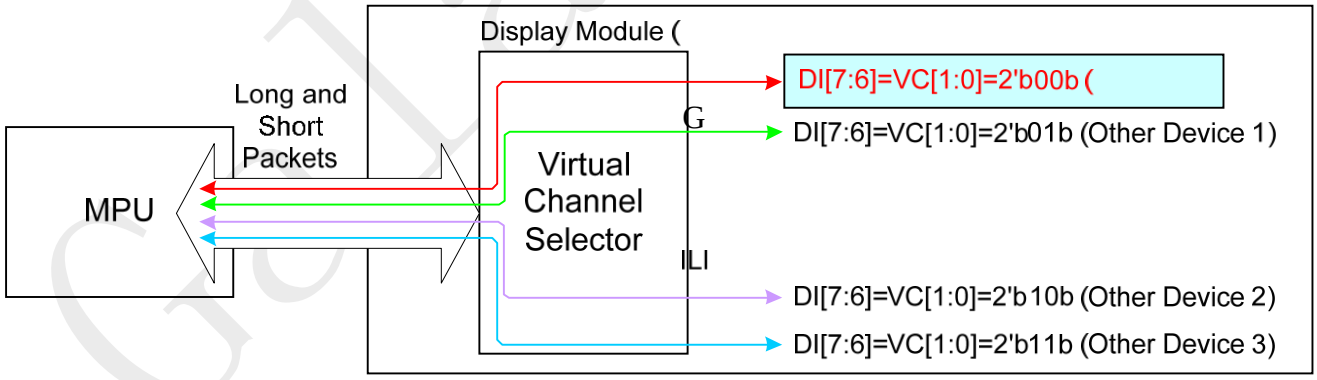


Figure 50 Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00_b) when the MPU is sending “End of Transmission Packet” to the display module. See chapter “End of Transmission Packet (EoTP)”.

This display module is not supporting the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC[1..0]) is 00b for this display module.

5.4.23 Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

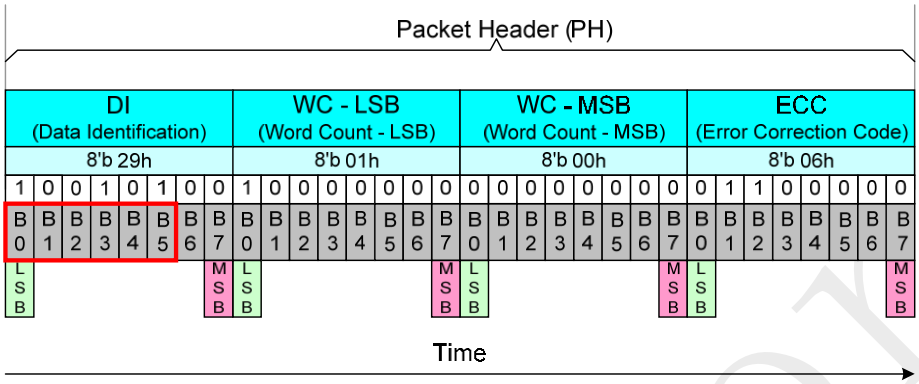


Figure 51 Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MPU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

Table 14 Data Type (DT) from the MPU to the Display Module (GC9503V)

From the MPU to the Display Module (**GC9503V**)									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long	Abbreviatio
0	0	1	0	0	0	08	End of Transmission Packet, Note	SPa (Short Packet)	EoTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, Note 2	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Note 1 This can be used when the MPU wants to secure that there is the end of the transmission in High Speed Data Transferring (HSDT) mode.

Note 2 This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.

Table 15 Data Type (DT) from the Display Module (GC9503V) to the MPU

From the Display Module (**GC9503V**) to the MPU									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviatio
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

The receiver is ignored other Data Type (DT) if they are not defined on tables: “ Table 14 Data Type (DT) from the MPU to the Display Module (or Other Devices)” or “ Table 15 Data Type (DT) from the Display Module (or Other Devices) to the MPU”.

5.4.24 Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

Data 1: 01hex (DCS's parameter)

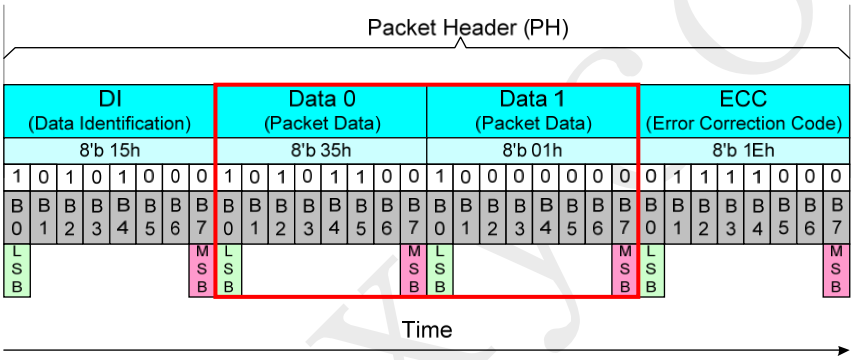


Figure 52 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

Data 1: 00hex (Null)

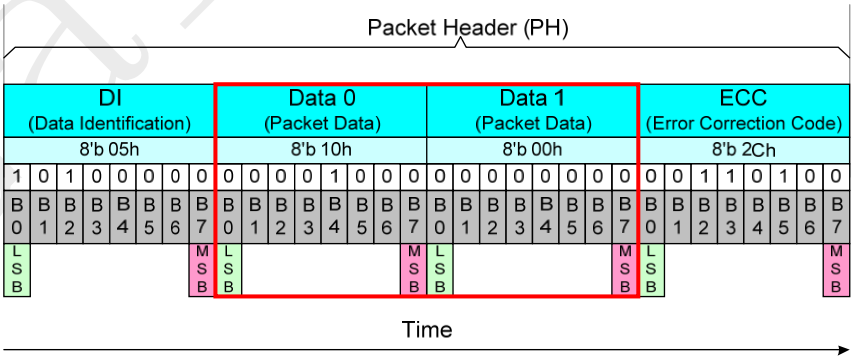


Figure 53 Packet Data (PD) for Short Packet (SPa), 1 Byte Information

5.4.25 Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH). Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

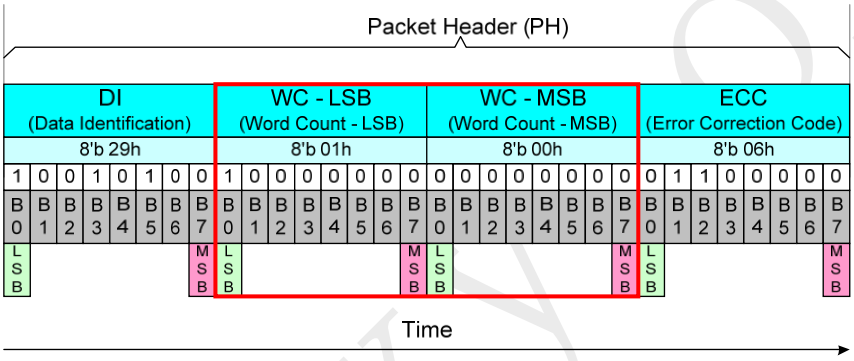


Figure 54 Word Count (WC) on the Long Packet (LPa)

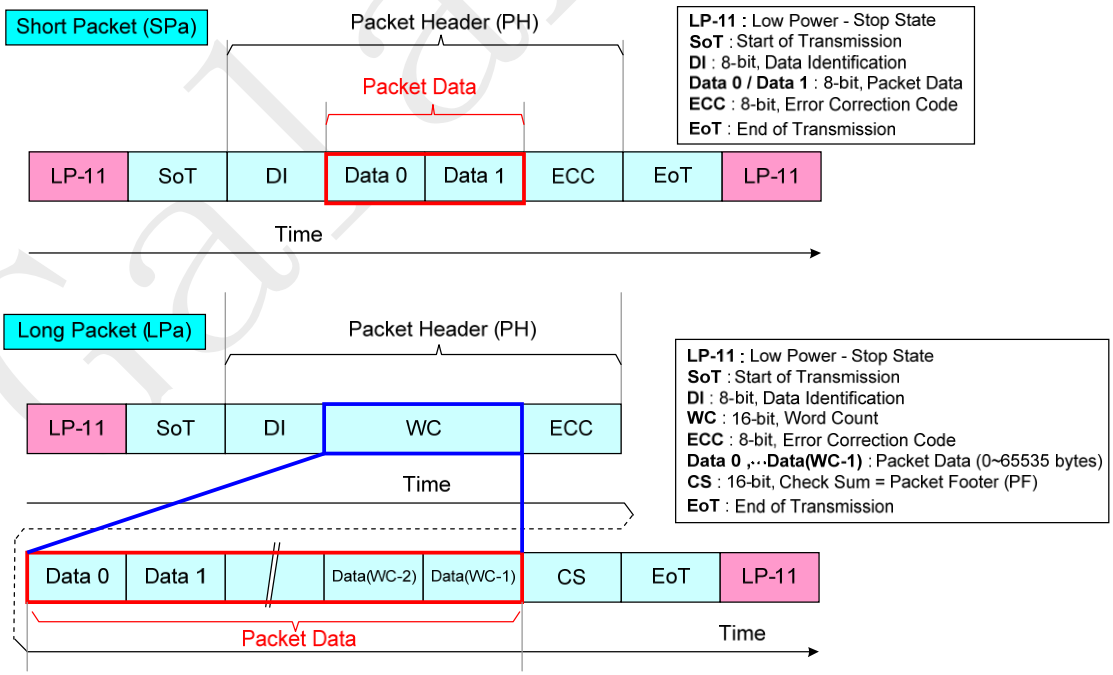


Figure 55 Packet Data in Short and Long Packets

5.4.26 Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

Short Packet (SPa): Data Identification (DI) byte (8 bits: D[0…7]), Packet Data (PD) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

Long Packet (LPa): Data Identification (DI) byte (8 bits: D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

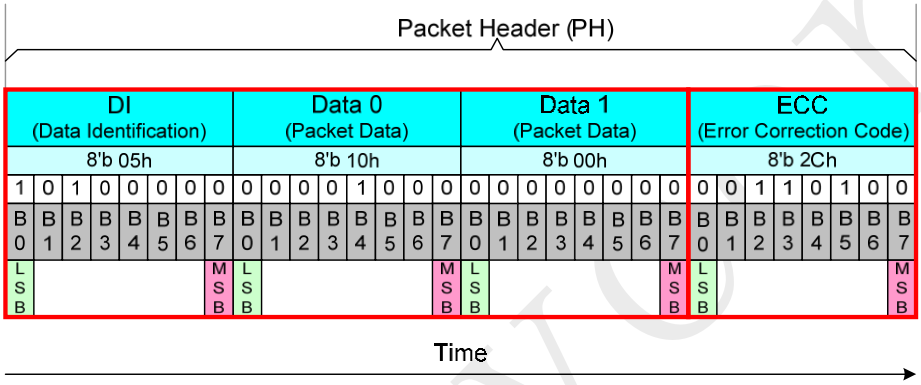


Figure 56 D[23…0] and P[7…0] on the Short Packet (SPa)

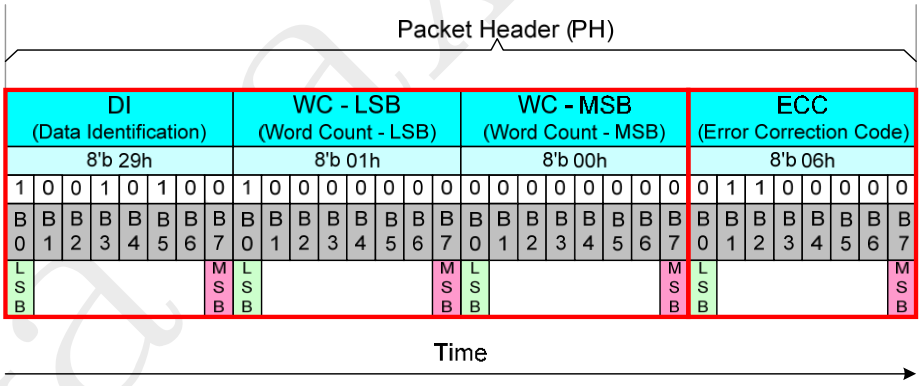


Figure 57 D[23…0] and P[7…0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

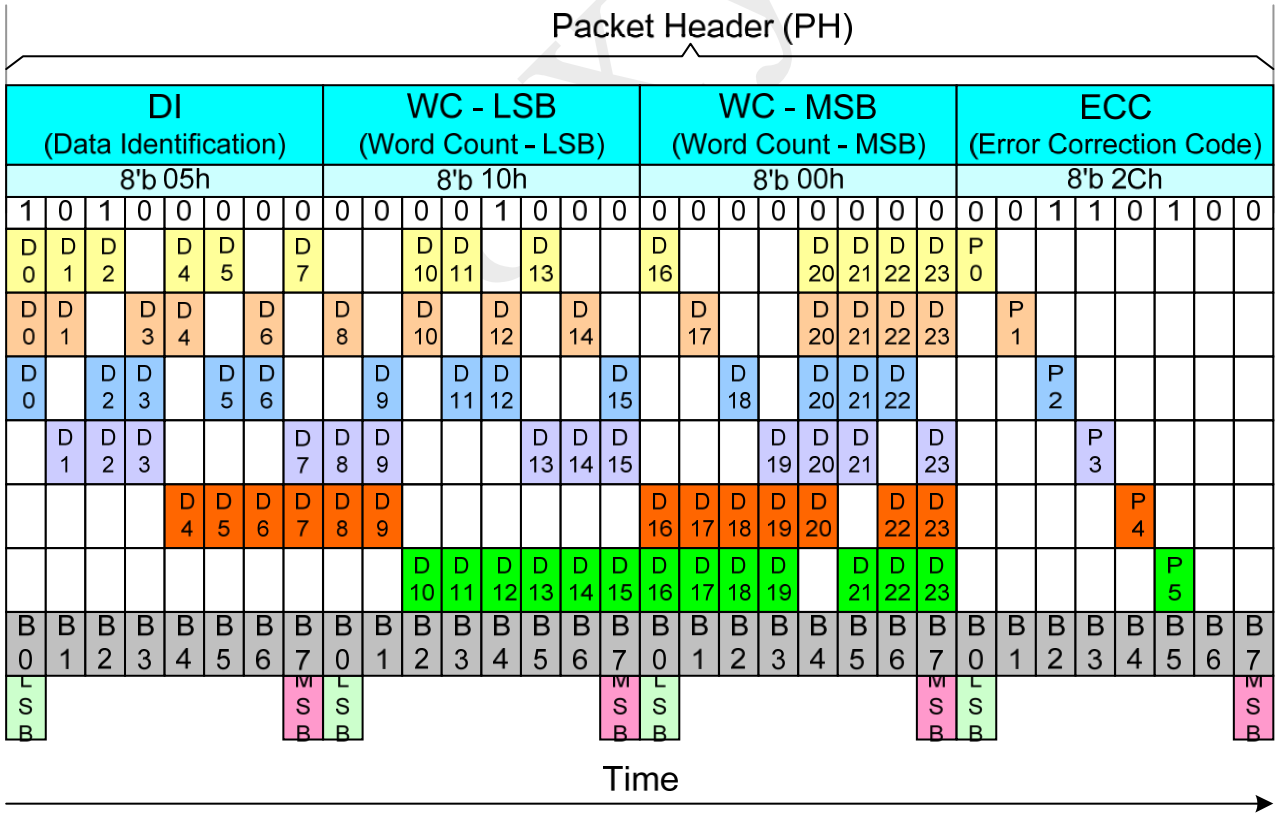


Figure 58 XOR Functionality on the Short Packet (SPa)

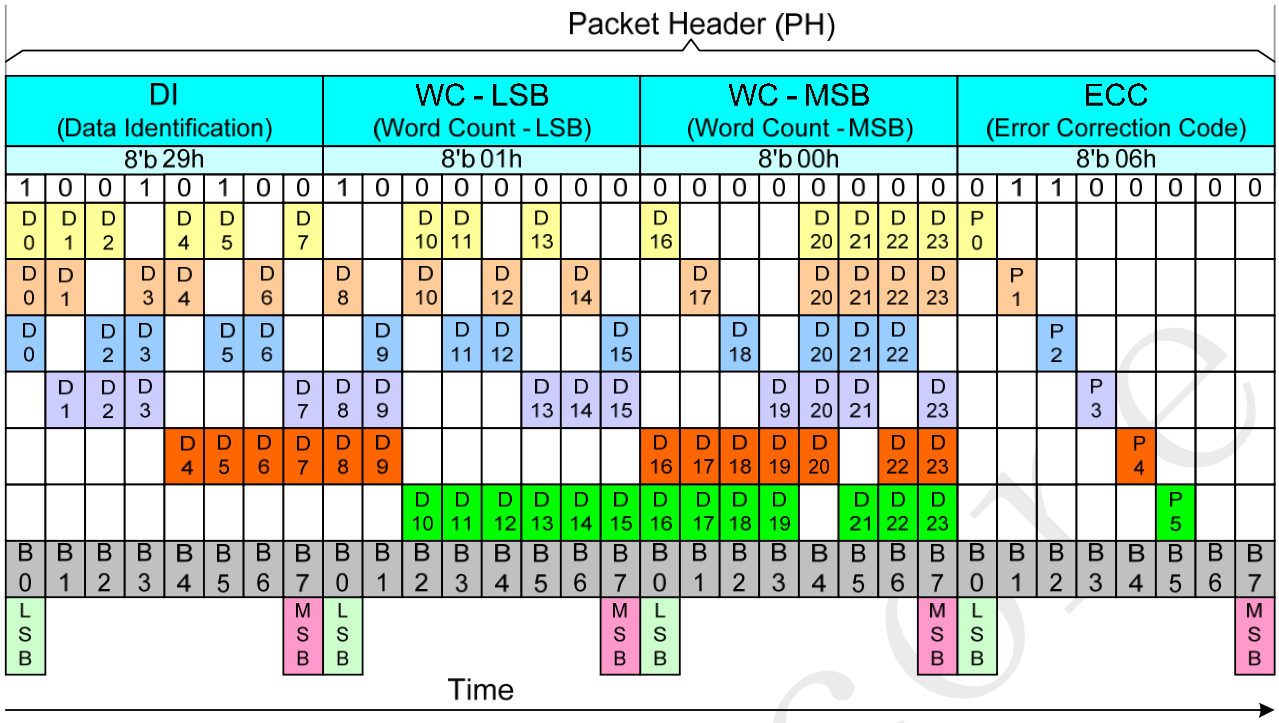


Figure 59 XOR Functionality on the Long Packet (LPa)

The transmitter (The MPU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MPU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MPU and the receiver is the display module, is illustrated for reference purposes below.

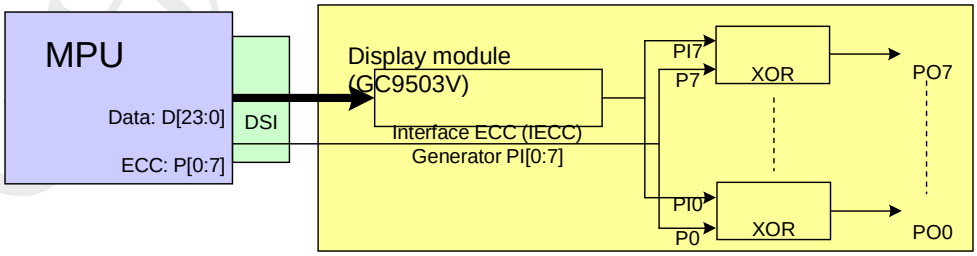


Figure 60 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 61 Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 62 Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.
The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Table 16 One Bit Error Value of the Error Correction Code (ECC)

Data	PO	PO	PO	PO	PO	PO	PO	PO	He
D[0]	0	0	0	0	0	1	1	1	07
D[1]	0	0	0	0	1	0	1	1	0B
D[2]	0	0	0	0	1	1	0	1	0D
D[3]	0	0	0	0	1	1	1	0	0E
D[4]	0	0	0	1	0	0	1	1	13
D[5]	0	0	0	1	0	1	0	1	15
D[6]	0	0	0	1	0	1	1	0	16
D[7]	0	0	0	1	1	0	0	1	19
D[8]	0	0	0	1	1	0	1	0	1A
D[9]	0	0	0	1	1	1	0	0	1C
D[10]	0	0	1	0	0	0	1	1	23
D[11]	0	0	1	0	0	1	0	1	25
D[12]	0	0	1	0	0	1	1	0	26
D[13]	0	0	1	0	1	0	0	1	29
D[14]	0	0	1	0	1	0	1	0	2A
D[15]	0	0	1	0	1	1	0	0	2C
D[16]	0	0	1	1	0	0	0	1	31
D[17]	0	0	1	1	0	0	1	0	32
D[18]	0	0	1	1	0	1	0	0	34
D[19]	0	0	1	1	1	0	0	0	38
D[20]	0	0	0	1	1	1	1	1	1F
D[21]	0	0	1	0	1	1	1	1	2F
D[22]	0	0	1	1	0	1	1	1	37
D[23]	0	0	1	1	1	0	1	1	3B

One error is detected if the value of the PO[7…0] is on Table 25: One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on Table 25: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

5.4.27 Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

5.4.28 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

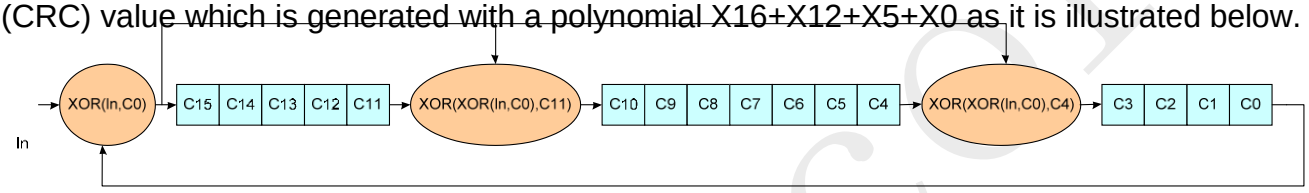
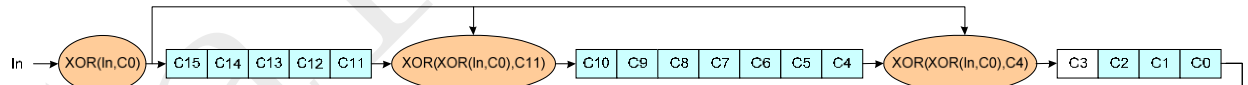


Figure 63 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

Figure 64 CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

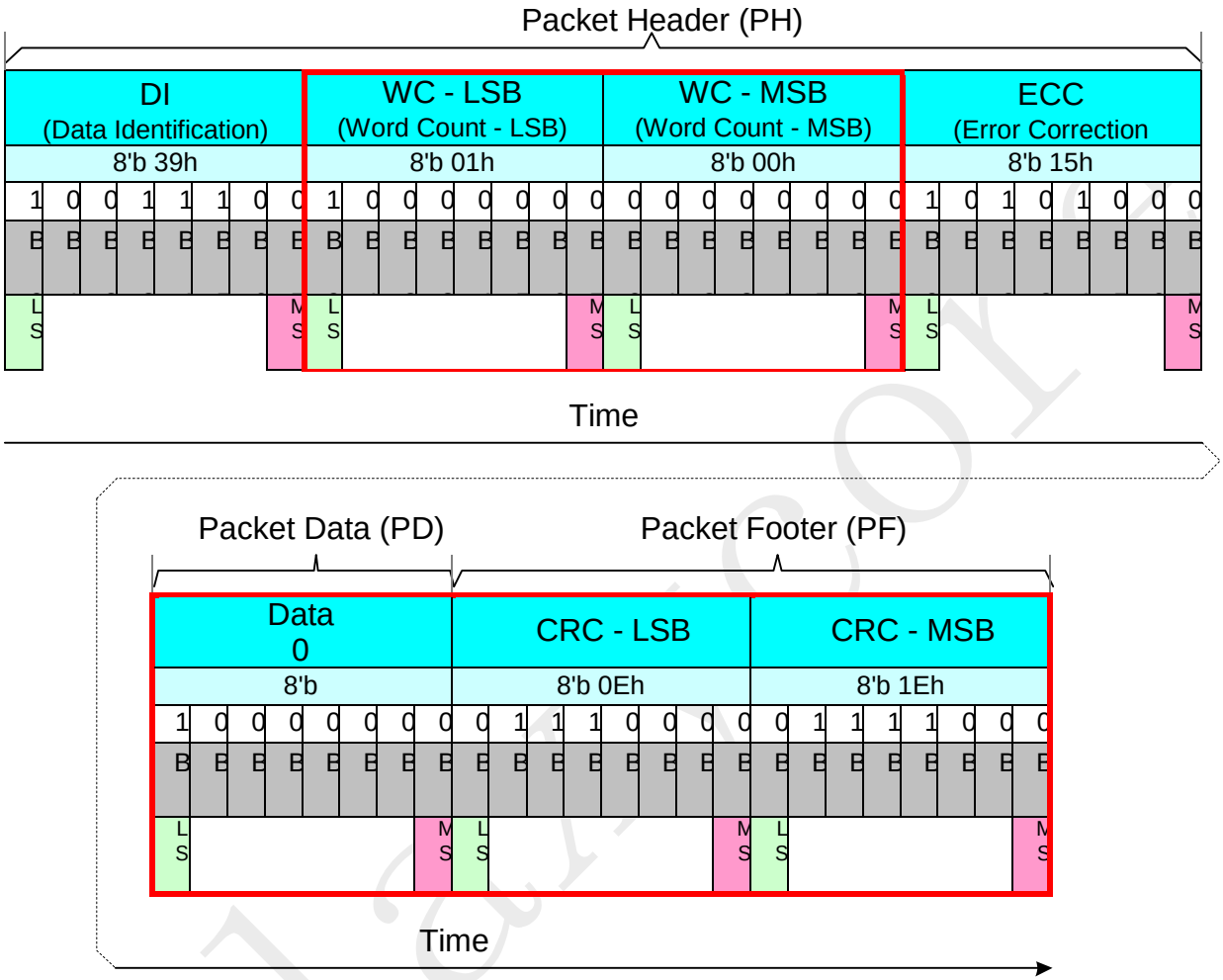


Figure 65 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.4.29 Packet Transmissions

5.4.30 Packet from the MPU to the Display Module

5.4.31 Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “5.2. Command Description” is used from the MPU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

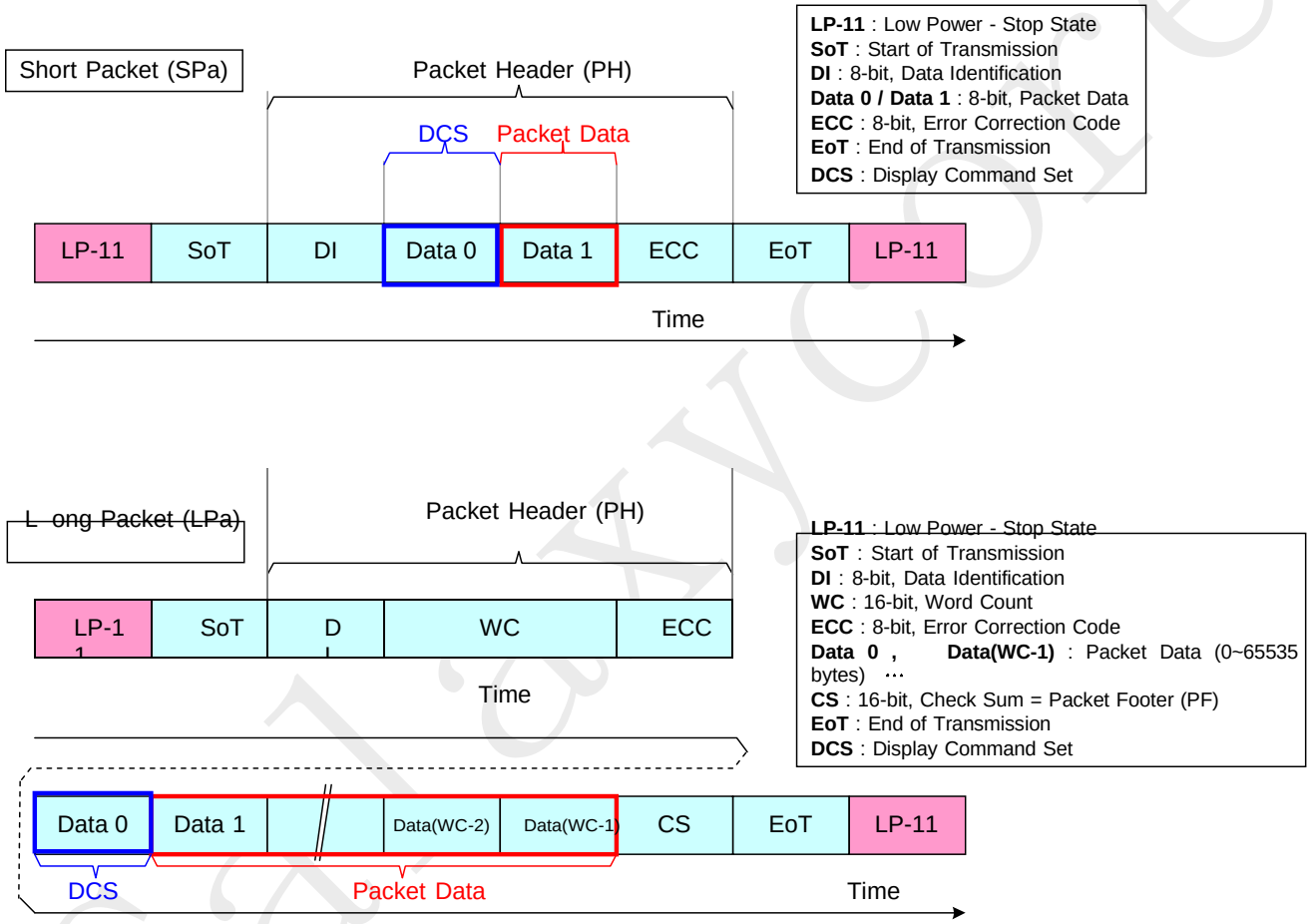


Figure 66 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

5.4.32 Display Command Set (DCS) Write, No Parameter (DCSWN-S)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MPU to the display module. These commands are defined on a table below. (See chapter "Command Description")

Table 17 Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Page 0 Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On (13h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)

Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b o Data Type (DT, DI[5…0]): 00 0101b

Packet Data (PD)

o Data 0: "Sleep In (10h)", Display Command Set (DCS) o Data 1: Always 00hex

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

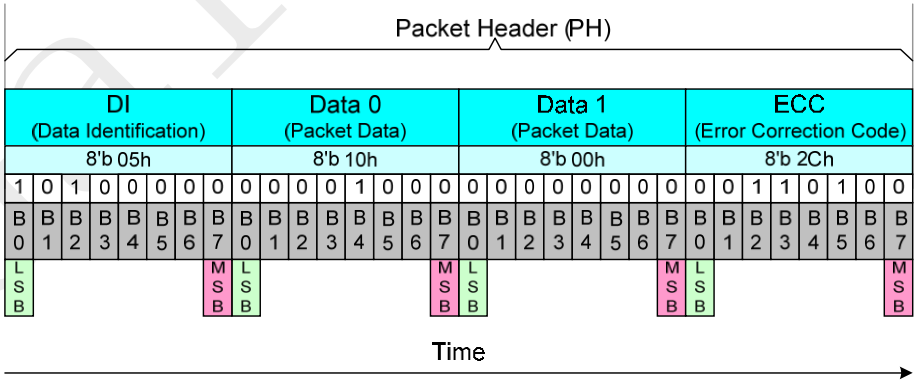


Figure 67 Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

5.4.33 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MPU to the display module. These commands are defined on a table (See chapter “Command Description”) below.

Table 18 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Page 0 Command
Gamma Set (26h)
Interface Pixel Format (3Ah)
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Content Adaptive Brightness control
Write CABC Minimum Brightness (5Eh)

Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC,

DI[7…6]): 00b o Data Type (DT,

DI[5…0]): 01 0101b

Packet Data (PD)

o Data 0: “Gamma Set (26h)”, Display Command

Set (DCS) o Data 1: 01hex, Parameter of the DCS

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

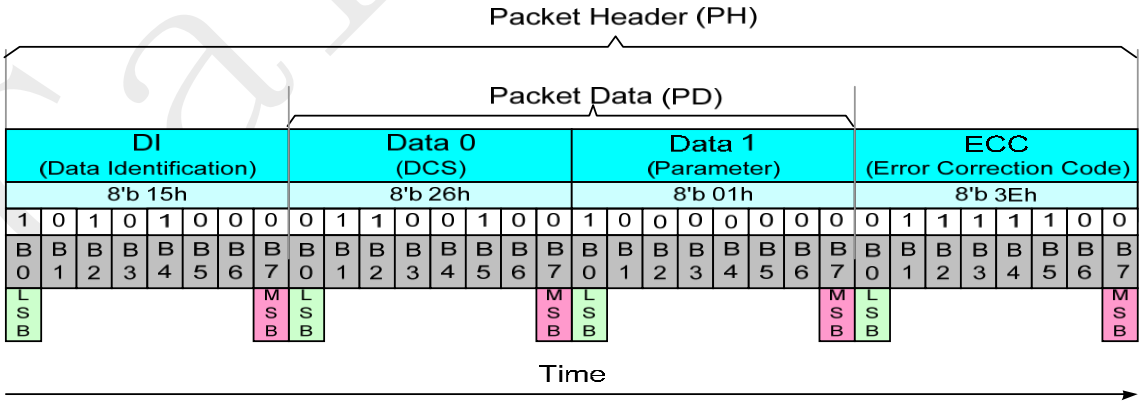


Figure 68 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

5.4.34 Display Command Set (DCS) Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MPU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "Command Description") below.

Table 19 Display Command Set (DCS) Write Long (DCSW-L)

Page 0 Command
NOP (00h) , Note 1
Software Reset (01h) , Note 1
Sleep In(10h) , Note 1
Sleep Out (11h) , Note 1
Normal Display Mode On (13h) , Note 1
All Pixel Off (22h)
All Pixel On (23h)
Gamma Set (26h), Note 2
Display Off (28h) , Note 1
Display ON (29h) , Note 1
Interface Pixel Format (3Ah)
Write Display Brightness (51h) , Note 2
Write CTRL Display (53h) , Note 2
Write Content Adaptive Brightness control (55h) , Note 2
Write CABC Minimum Brightness (5Eh)

Note 1 Also Short Packet (SPa) can be used; See chapter "Display Command Set (DCS) Write, No Parameter"

Note 2 Also Short Packet (SPa) can be used; See chapter "Display Command Set (DCS) Write, 1 Parameter"

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC,

DI[7…6]): 00b o Data Type (DT,

DI[5…0]): 11 1001b

Word Count (WC)

o Word Count (WC): 0001h

Error Correction Code (ECC)

Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

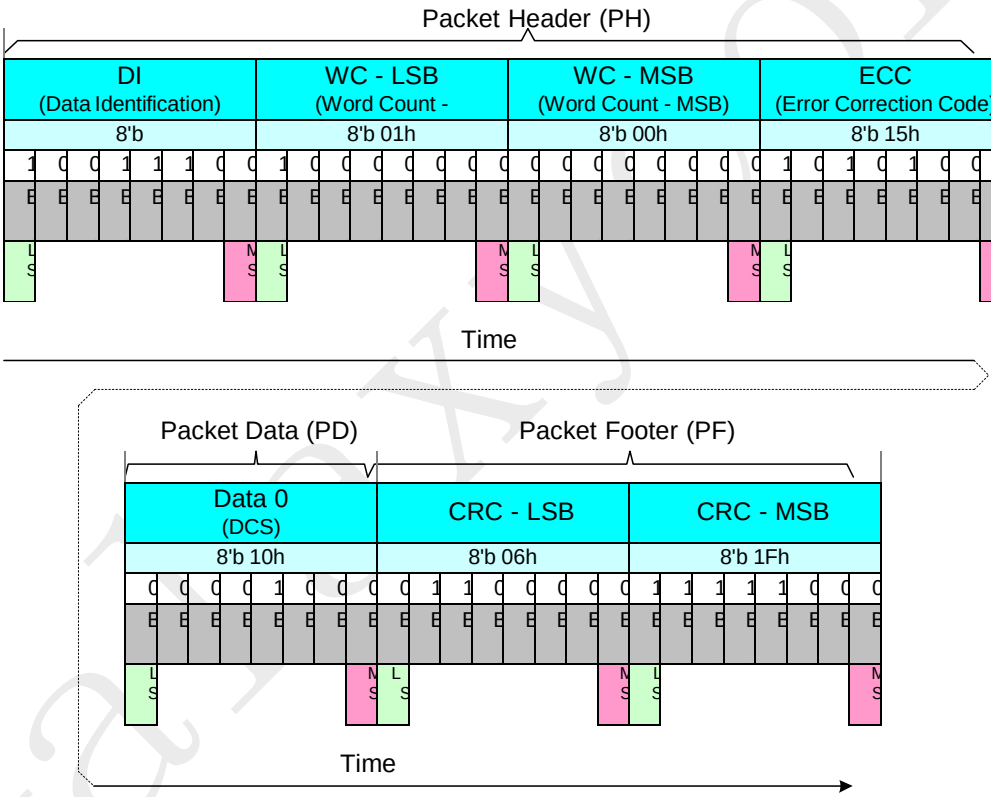


Figure 69 Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC,

DI[7…6]): 00b o Data Type (DT,

DI[5…0]): 11 1001b

Word Count (WC)

o Word Count (WC): 0002h

Error Correction Code (ECC)

Packet Data (PD):

o Data 0: “Gamma Set (26h)”, Display Command

Set (DCS) o Data 1: 01hex, Parameter of the DCS

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

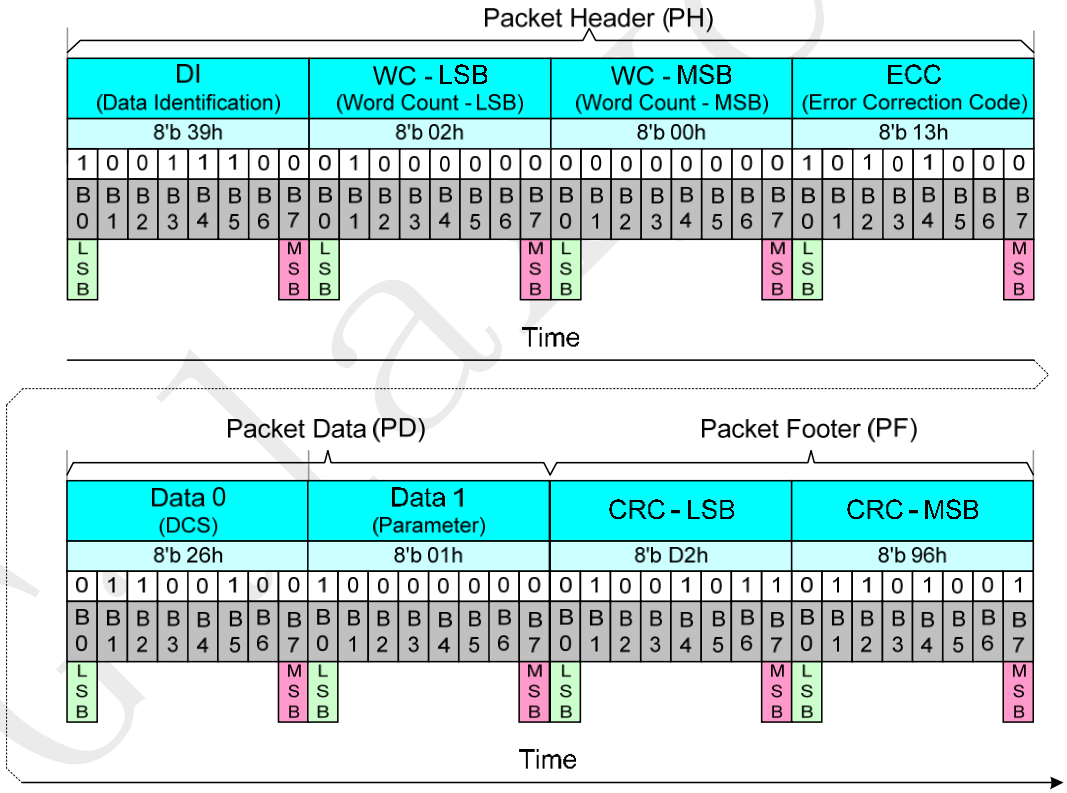


Figure 70 Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC,

DI[7…6]): 00b o Data Type (DT,

DI[5…0]): 11 1001b

Word Count (WC)

o Word Count (WC): 0005h

Error Correction Code (ECC)

Packet Data (PD):

o Data 0: “Column Address Set (2Ah)”, Display Command

Set (DCS) o Data 1: 00hex, 1st Parameter of the DCS,

Start Column SC[15…8] o Data 2: 12hex, 2nd Parameter

of the DCS, Start Column SC[7…0] o Data 3: 01hex, 3rd

Parameter of the DCS, End Column EC[15…8] o Data 4:

EFhex, 4th Parameter of the DCS, End Column EC[7…0]

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

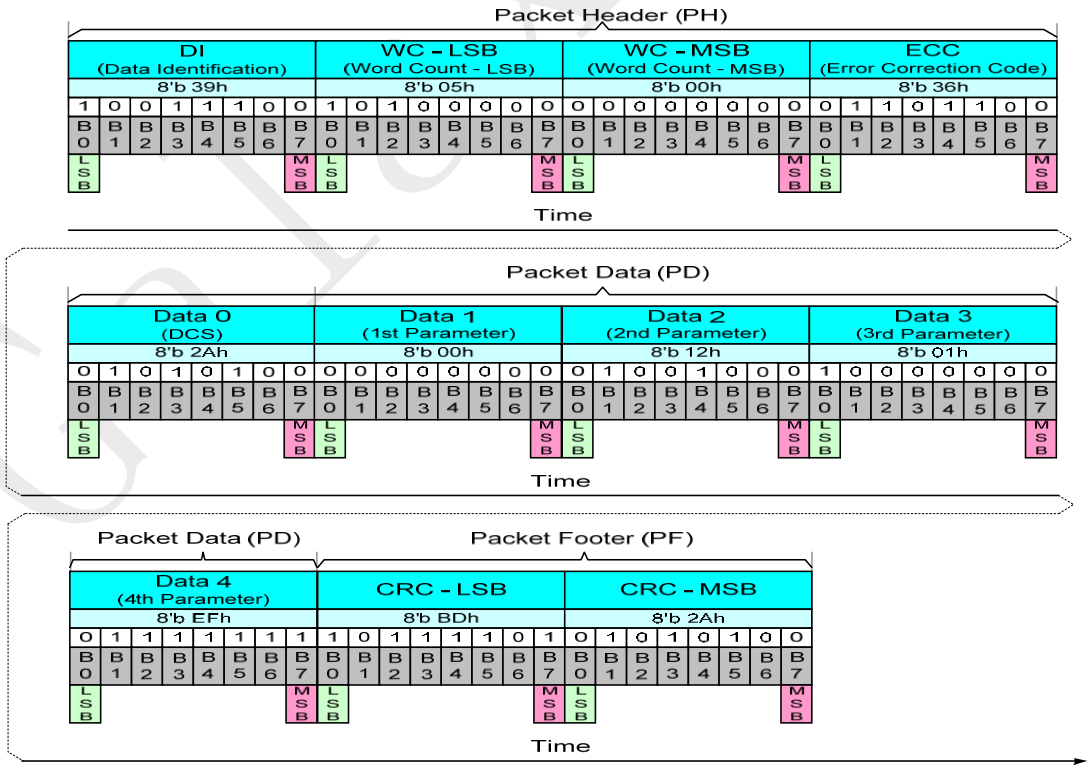


Figure 71 Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

5.4.35 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MPU to the display module. These commands are defined on a table (See chapter "5.2. Command Description") below.

Table 20 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Page 0 Command
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Content Adaptive Brightness Control (56h)
Read CABC Minimum Brightness (5Fh)
Read ID1
Read ID2
Read ID3 (DCh)

The MPU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MPU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

The MPU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

Data Identification (DI)

o Virtual Channel (VC,

DI[7…6]): 00b o Data Type (DT,

DI[5…0]): 11 0111b

Maximum Return Packet Size

(MRPS) o Data 0: 01hex

o Data 1: 00hex

Error Correction Code (ECC)

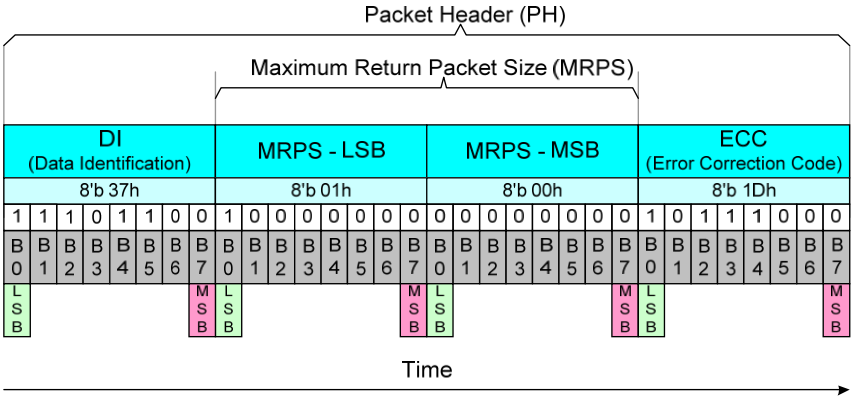


Figure 72 Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

The MPU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MPU sends “Display Command Set (DCS) Read, No Parameter” to the display module

Data Identification (DI)

o Virtual Channel (VC,

DI[7…6]): 00b o Data Type (DT,

DI[5…0]): 00 0110b

Packet Data (PD)

o Data 0: “Read ID1 (DAh)”, Display Command

Set (DCS) o Data 1: Always 00hex

Error Correction Code (ECC)

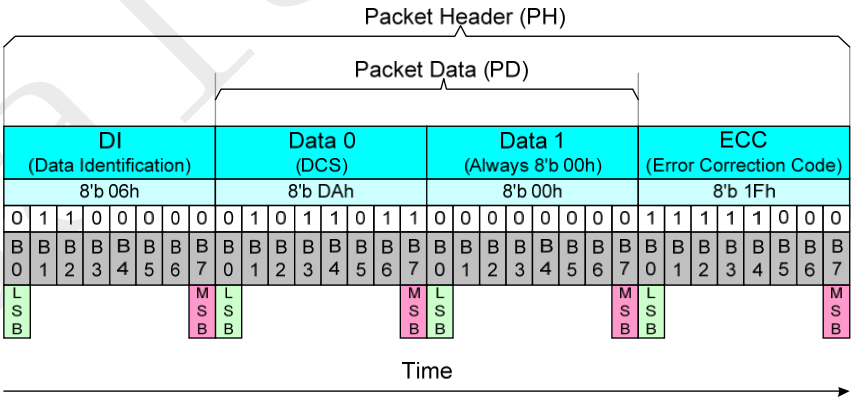


Figure 73 Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3: The display module can send 2 different information to the MPU after Bus Turnaround (BTA)

An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there

is an error to receive a

command, See chapter “Acknowledge with Error Report (AwER)”

Information of the received command. Short Packet (SPa) or Long Packet (LPa)

5.4.36 Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MPU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed.

The display module is ignored Packet Data (PD) what the MPU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

Data Identification (DI)

- o Virtual Channel (VC, DI[7…6]): 00b o Data Type (DT, DI[5…0]): 00 1001b

Word Count (WC)

- o Word Count (WC): 0005hex

Error Correction Code (ECC)

Packet Data (PD):

- o Data 0: 89hex (Random data) o Data 1: 23hex (Random data) o Data 2: 12hex (Random data) o Data 3: A2hex (Random data) o Data 4: E2hex (Random data)

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

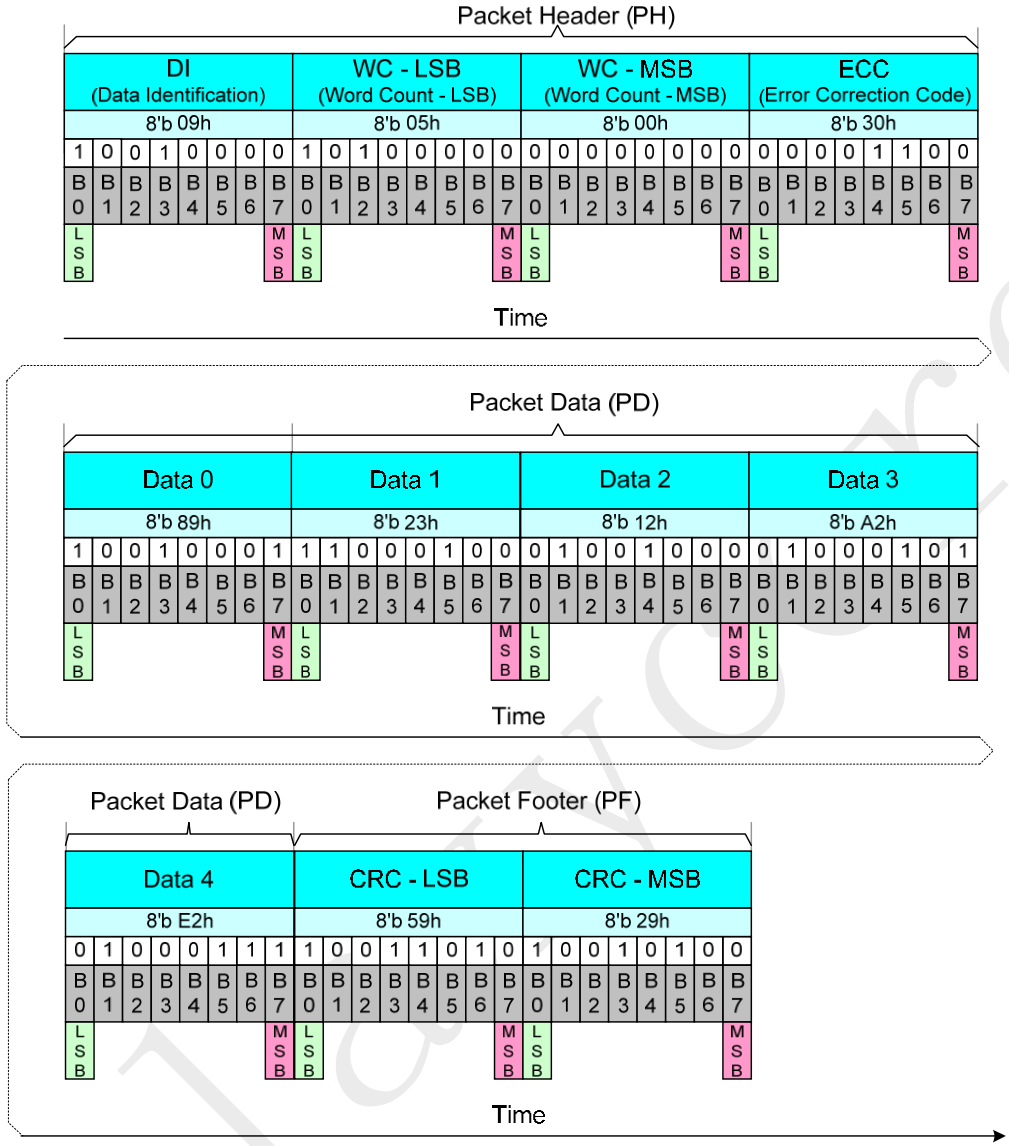


Figure 74 Null Packet, No Data (NP-L) - Example

End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MPU to the display module. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before “End of Transmission” (EoT), which is an interface level functionality.

The MPU can decide if it wants to use the “End of Transmission Packet” (EoTP) or not. The display shall have the capability to support both: i.e. If the MPU applies the EoTP, it shall report the “DSI Protocol Violation Error” when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module is or isn’t receiving “End of Transmission Packet” (EoTP) from the MPU during the Low Power Data Transmission (LPDT) mode before “Mark-1” (= Leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send “End of Transmission Packet” (EoTP) to the MPU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Table 21 Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MPU => Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module => MPU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

Short Packet (SPa) is using a fixed format as follows

Data Identification (DI)

- o Virtual Channel (VC, DI[7…6]): 00b
- o Data Type (DT, DI[5…0]): 00 1000b

Packet Data (PD)

- o Data 0: 0Fhex
- o Data 1: 0Fhex

Error Correction Code

(ECC) o ECC: 01hex

This is defined on the Short Packet (SPa) as follows.

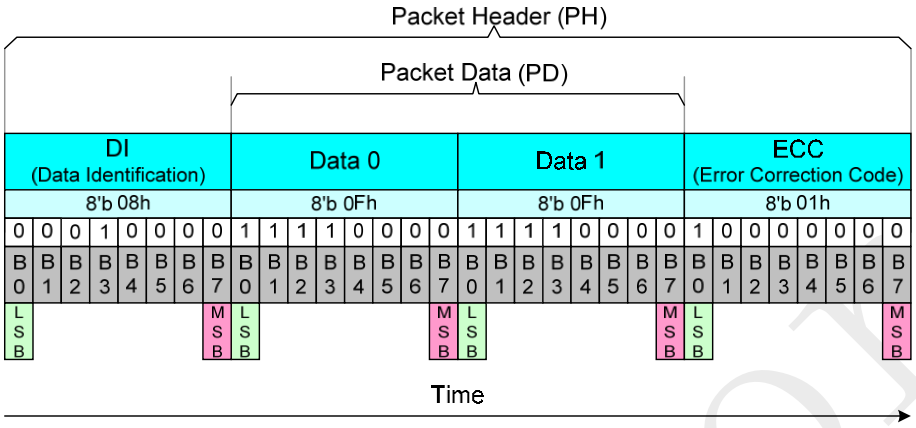


Figure 75 End of Transmission Packet (EoTP)

Some use cases of the “End of Transmission Packet” (EoTP) are illustrated only for reference purposes below.

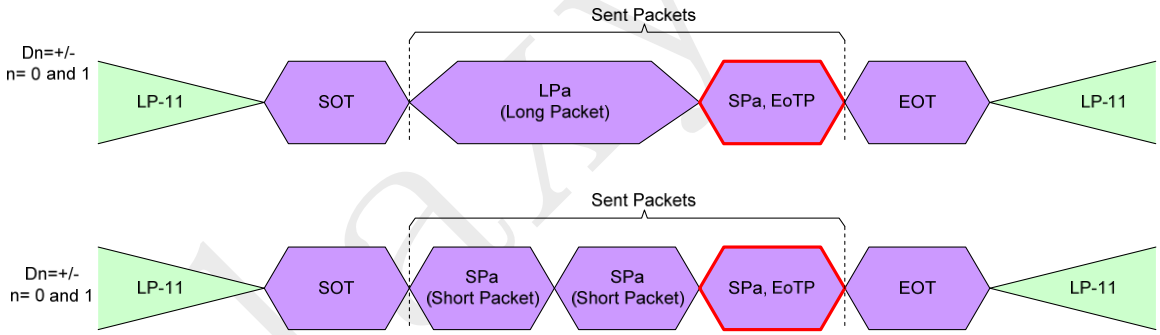


Figure 76 End of Transmission Packet (EoTP)-Examples

5.4.37 Packet from the Display Module to the MPU

5.4.38 Used Packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MPU after the MPU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “Data Type (DT)”. It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.

Both cases are illustrated for reference purposes below.

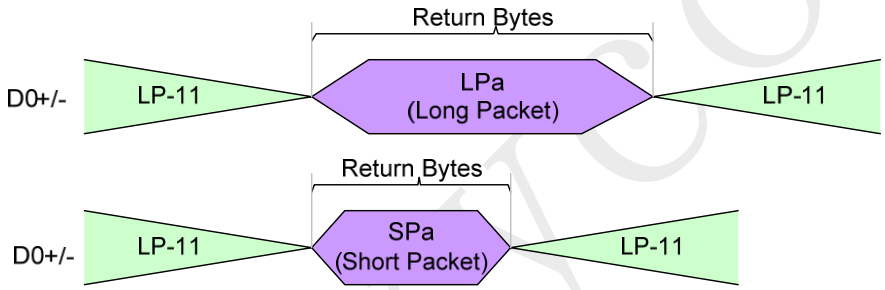


Figure 77 Return Bytes on Single Packet

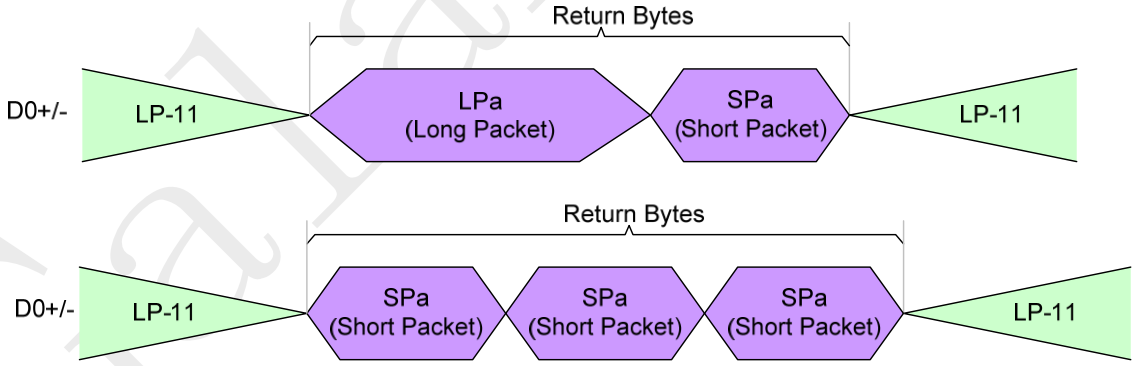


Figure 78 Return Bytes on Several Packets – Not Possible

Exception:

The display module is returning 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MPU when the display module has received a read command (See chapter "Display Command Set (DCS) Read, No Parameter (DCSRN-S)") where has been detected and corrected a single bit error by the EEC (See bit 8 on "Table 22: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response").

These return packets are illustrated for reference purposes below.

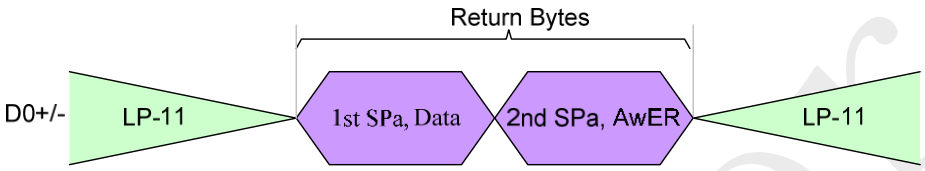


Figure 79 Exception when Return Bytes on Several Packets

AwER = Acknowledge with Error Report

5.4.39 Acknowledge with Error Report (AwER)

“Acknowledge with Error Report” (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MPU. The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to ‘1’, as they are defined on the following table.

Table 22 Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

B	Description
0	SoT Error
1	SoT Sync
2	EoT Sync
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

Table 23 Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

B	Description
0	SoT Error
1	SoT Sync
2	EoT Sync
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Reserved, Set to ‘0’ internally Set to ‘0’ internally (Only for Long Packet (LP)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

These errors are included from all packages what has been received from the MPU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors. Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b o Data Type (DT, DI[5…0]): 00 0010b

Packet Data (PD)

o Bit 8: ECC Error, single-bit (detected and corrected) o AwER: 0100h

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

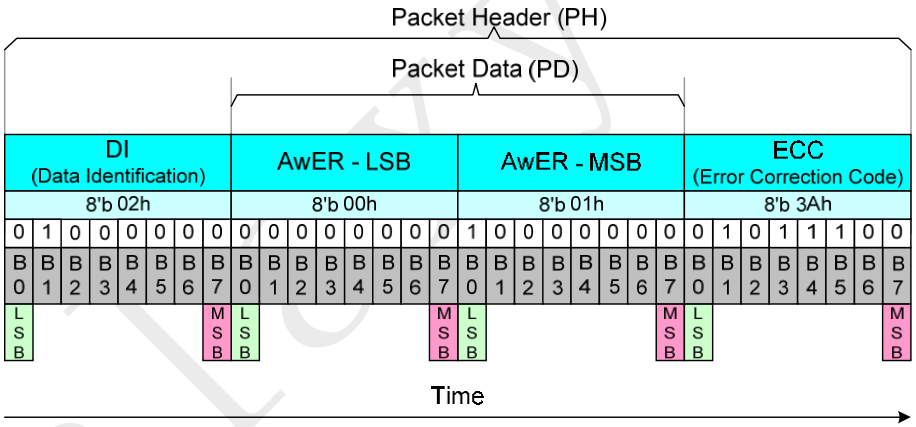


Figure 80 Acknowledge with Error Report (AwER) – Example

It is possible that the display module has received several packets, which have included errors, from the MPU before the MPU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

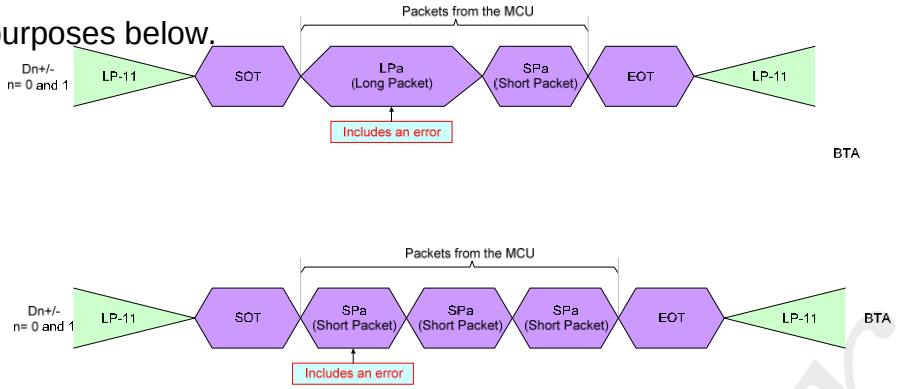


Figure 81 Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ***ECC or CRC*** error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MPU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.

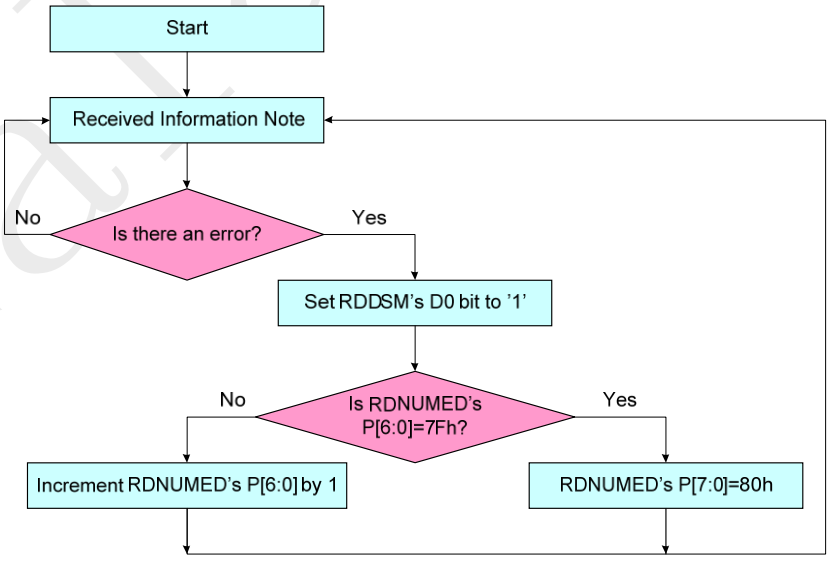


Figure 82 Flow Chart for Errors on DSI[Note]

Note *1. This information can be Interface or Packet Level Communication but it is always from the MPU to the display module in this case.*

2. CRC or ECC error

5.4.40 DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 011100b), from the display module to the MPU.“DCS Read Long Response” (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module. Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

Data Identification (DI)

o Virtual Channel (VC,

DI[7…6]): 00b o Data Type (DT,

DI[5…0]): 01 1100b

Word Count (WC)

o Word Count (WC): 0005hex

Error Correction Code (ECC)

Packet Data (PD):

o Data 0: 89hex

o Data 1:

23hex o Data

2: 12hex o

Data 3:

A2hex o Data

4: E2hex

Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.

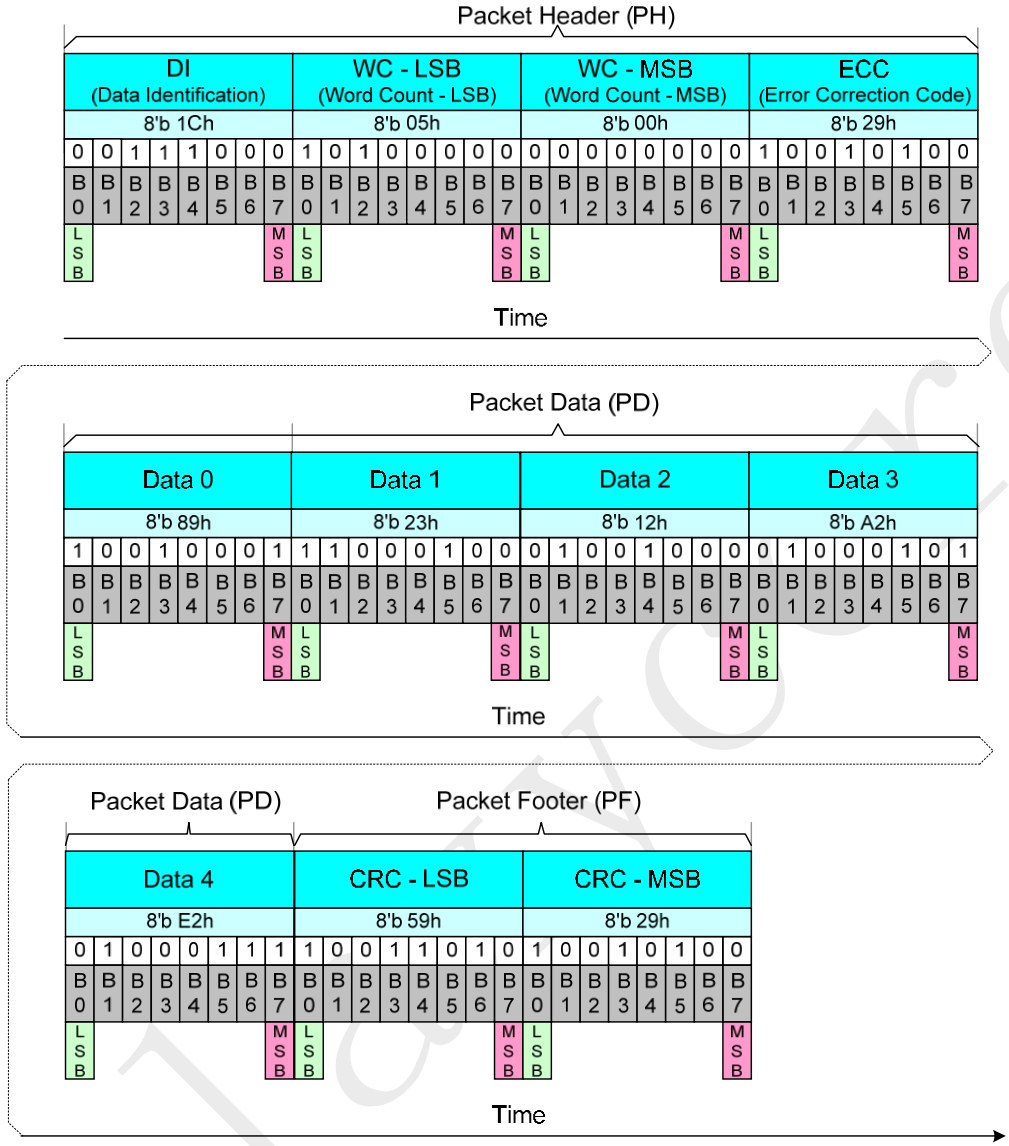


Figure 83 DCS Read Long Response (DCSRR-L) - Example

5.4.41 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MPU.“DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module.

Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC,

DI[7…6]): 00b o Data Type (DT,

DI[5…0]): 10 0001b

Packet Data (PD)

o Data 0: 45hex

o Data 1: 00hex (Always)

Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

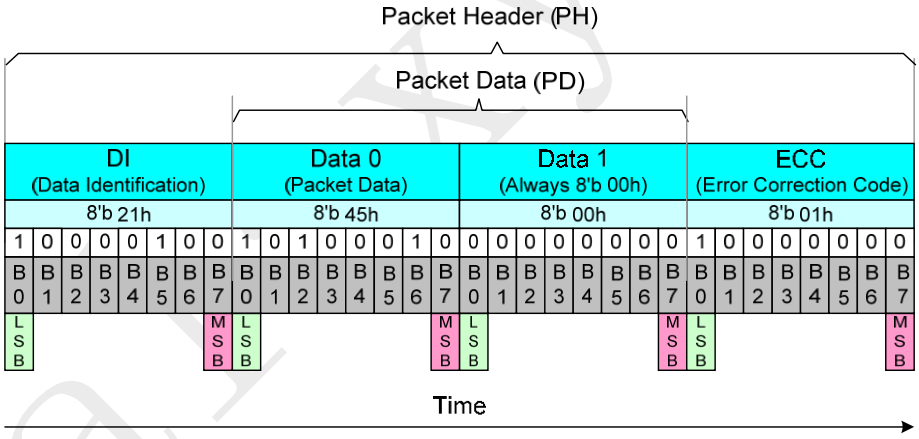


Figure 84 DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

5.4.42 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MPU.“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module.

Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC,

DI[7…6]): 00b o Data Type (DT,

DI[5…0]): 10 0010b

Packet Data (PD)

o Data 0: 45hex

o Data 1: 32hex

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

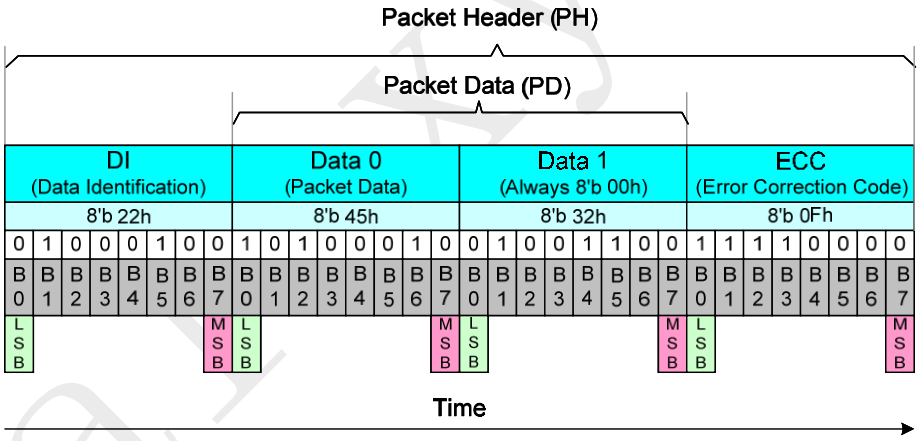


Figure 85 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

5.4.43 Communication Sequences

The communication sequences can be done on interface or packet levels between the MPU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes (DSI-D0+/- and DSI-D1+/-) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically. See chapter “DSI-CLK Lanes”.

Functions of the interface level communication is described on the following table.

Table 24 Interface Level Communication

Interface	Abbreviatio	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data

Functions of the packet level communication are described on the following table.

Table 25 Packet Level Communication

Interface	Abbreviatio	Packet	Interface Action Description
MPU	DCSW1-	Short	DCS Write, 1 Parameter
	DCSWN-	Short	DCS Write, No Parameter
	DCSW-L	Long	DCS Write Long
	DCSRN-S	Short	DCS Read, No Parameter
	SMRPS-S	Short	Set Maximum Return Packet
	NP-L	Long	Null Packet, No Data
	EoTP	Short	End of Transmission Packet
Display Module (GC9503	AwER	Short	Acknowledge with Error Packet
	DCSRR-L	Long	DCS Read Long Response
	DCSRR1-	Short	DCS Read Short Response
	DCSRR2-	Short	DCS Read Short Response

5.4.44 Sequences

5.4.45 DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

Table 26 DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**GC9503V**)		Comment
	Packet	Interface Mode Control		Interface Mode	Packet	
1	-	LP-	–	-	-	Start
2	DCSW1-	LPDT	–	-	-	
3	-	LP-	–	-	-	End

Table 27 DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**GC9503V**)		Comment
	Packet	Interface Mode Control		Interface Mode	Packet	
1	-	LP-	–	-	-	St
2	DCSW1-	HS	–	-	--	
3	EoTP	HS	–	-	--	End of Transmission Packet
4	-	LP-	–	-	-	E

5.4.46 DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

Table 29 DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	M		Information Direction	Display Module (**GC9503V**)		Comment
	Packet Sender	Interface Mode		Interface Mode	Packet Sender	
1	-	LP-	−	-	-	St
2	DCSWN-	LPDT	−+	--	--	
3	-	LP-	−	-	-	E

Table 30 DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	M		Information Direction	Display Module (**GC9503V**)		Comment
	Packet Sender	Interface Mode		Interface Mode	Packet Sender	
1	-	LP-	−	-	-	St
2	DCSWN-	HS	−	-	-	
3	EoTP	HS	−	--	--	End of Transmission Packet
4	-	LP-	−	-	-	E

Table 31 DCS Write, No Parameter Sequence – Example 3

5.4.47 DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

Table 32 DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**GC9503V**)		Comment
	Packet	Interface Mode		Interface Mode	Packet Sender	
1	-	LP-11	−	-	-	Start
2	DCSW-L	LPDT	−+	-	-	
3	-	LP-11	−	-	-	End

Table 33 DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**GC9503V**)		Comment
	Packet	Interface Mode		Interface Mode	Packet Sender	
1	-	LP-11	−	-	-	Start
2	DCSRN-	HSDT	−	-	-	
3	EoTP	HSDT	−	-	--	End of Transmission Packet
4	-	LP-11	−	-	-	End

5.4.48 DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

5.4.49 Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and an example sequence, how this packet is used, is described on the following table.

Table 37 Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	M		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	–	-	-	St
2	NP-	HSDT	–	-	-	Only High Speed Data Transmission is
3	EoT	HSDT	–	-	-	End of Transmission Packet
4	-	LP-11	–	-	-	E

5.4.50 End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined on chapter “8.1.3.2.1.7 End of Transmission Packet (EoTP)” and an example sequence, how this packet is used, is described on the following table.

Table 38 End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	M		Information Direction	Display Module		Comment
	Packet	Interface Mode		Interface Mode Control	Packet Sender	
1	-	LP-11	–	-	-	St
2	NP-	HSDT	–	-	-	Only High Speed Data Transmission is
3	EoT	HSDT	–	-	-	End of Transmission Packet
4	-	LP-11	–	-	-	E

5.5 Display Data Format

5.5.1 DPI (RGB) Interface

5.5.2 16-bit / pixel 65K colors order on the DPI Interface

The 16-bit RGB interface is selected by setting the DPI[2:0] bits to “101”. The display operation is synchronized with VS, HS and PCLK signals.

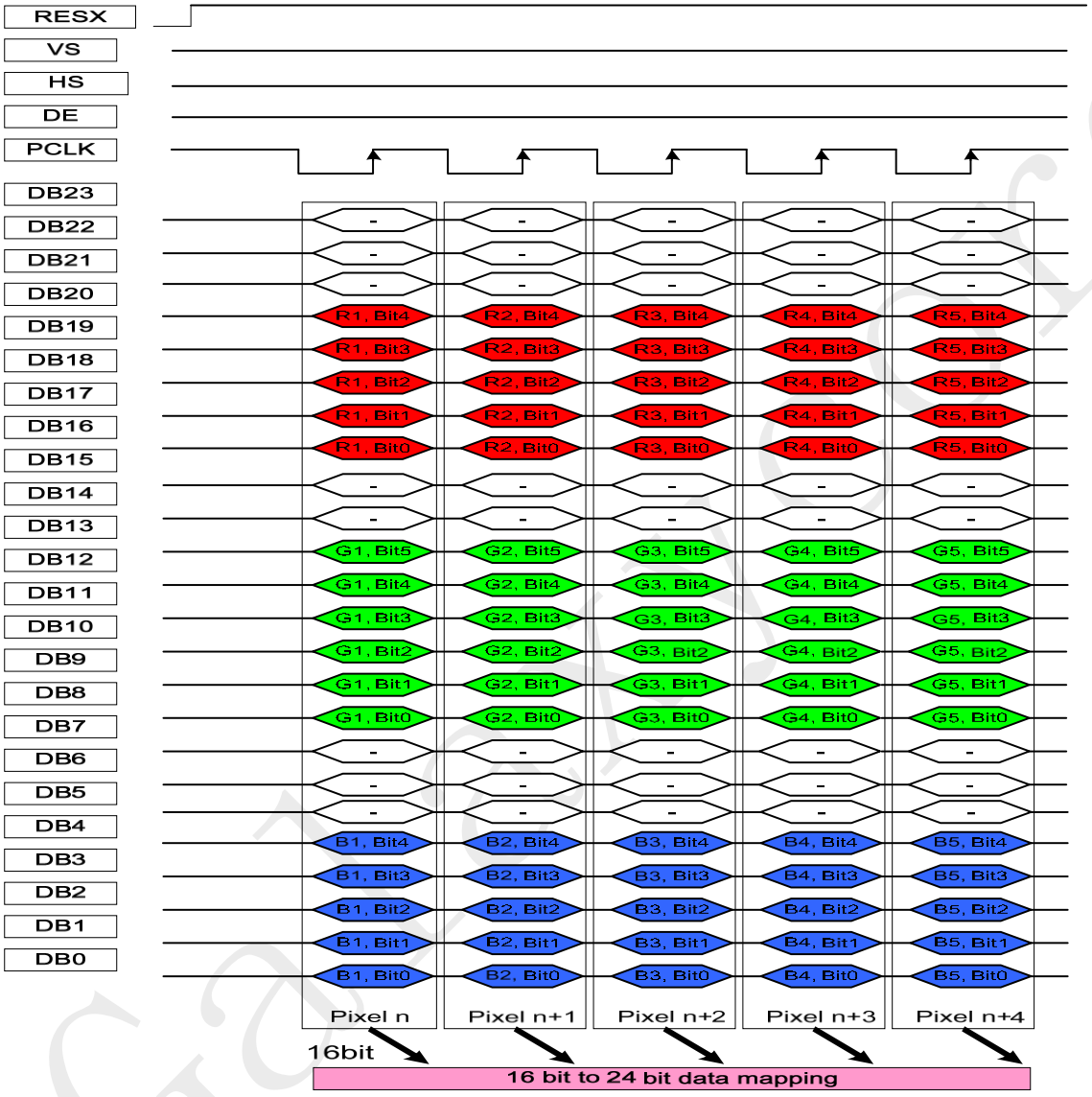


Figure 86 16-bit / pixel 65K colors order on the DPI Interface

Not
e:

The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

1-times transfer is used to transmit 1 pixel data to the 16-bit color depth information.

‘-‘= void

5.5.3 18-bit / pixel 262K colors order on the DPI Interface

The 18-bit RGB interface is selected by setting the DPI[2:0] bits to “110”. The display operation is synchronized with VS, HS and PCLK signals.

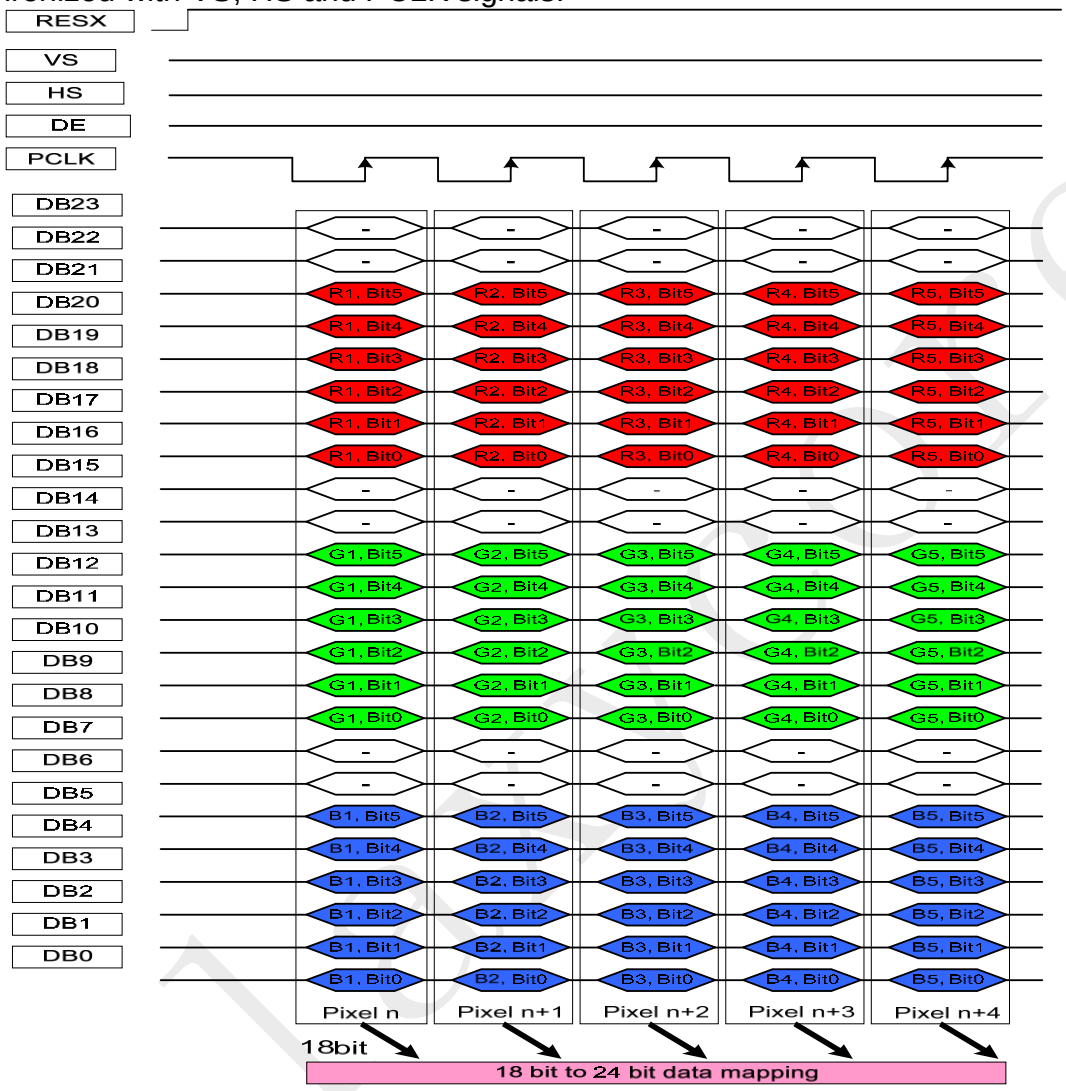


Figure 87 18-bit / pixel 262K colors order on the DPI Interface

Note:

The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

1-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.

‘-‘= void

5.5.4 24-bit / pixel 16.7M colors order on the DPI Interface

The 24-bit RGB interface is selected by setting the DPI[2:0] bits to “111”. The display operation is synchronized with VS, HS and PCLK signals.

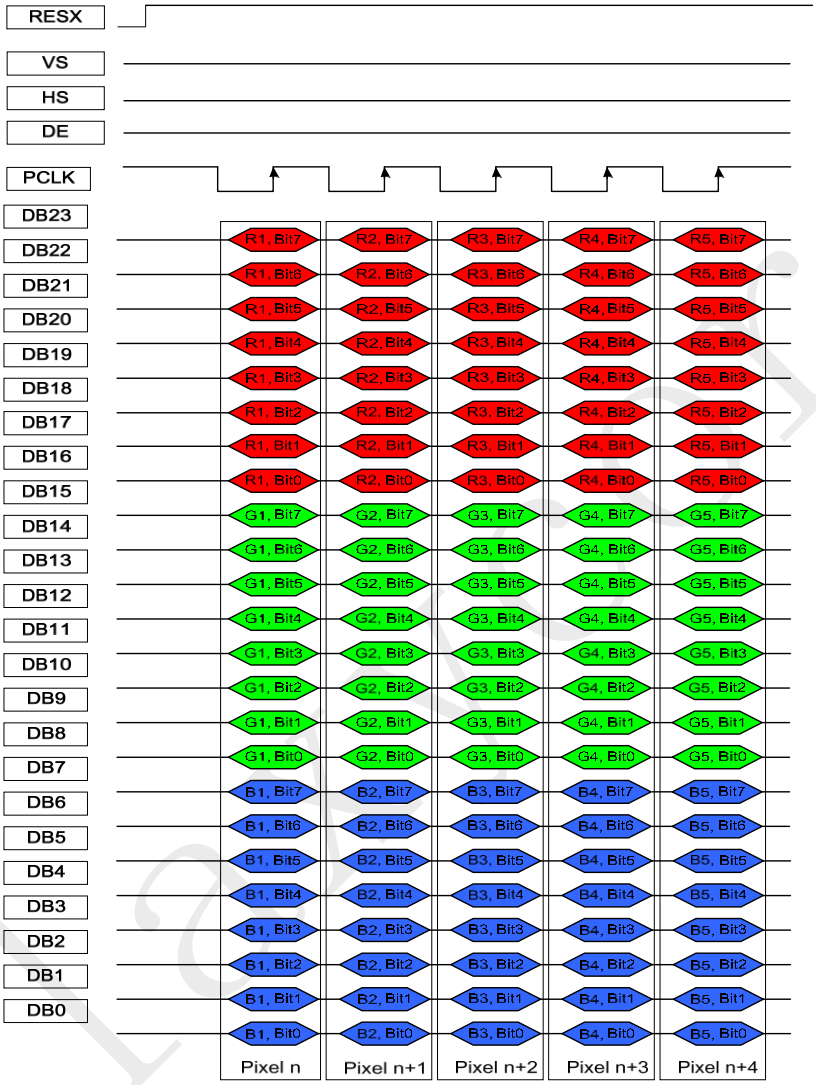


Figure 88 24-bit / pixel 16.7M colors order on the DPI Interface

Note:

The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 7, LSB=Bit 0 for Green, Red and Blue data.

1-times transfer is used to transmit 1 pixel data to the 24-bit color depth information.

5.5.5 DSI transmission data format

5.5.6 16-bit per Pixel, Long packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long Packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, GC9503V has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifice.

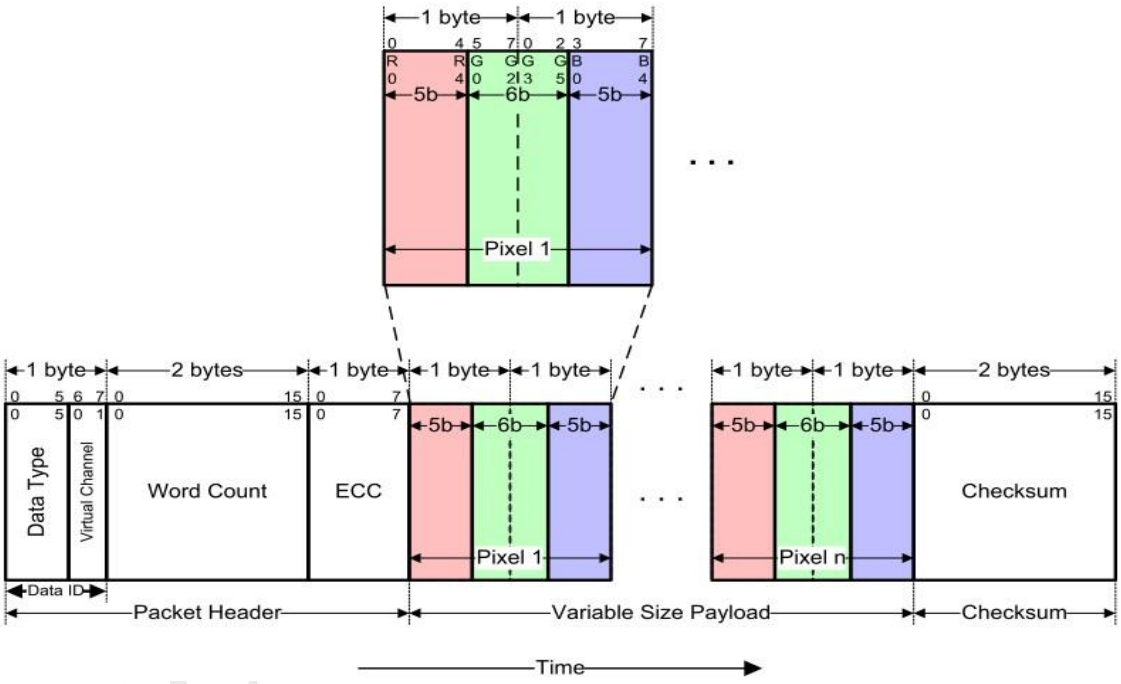


Figure 89 16-bit per Pixel, Data Type 00 1110 (0Eh)

5.5.7 18-bit per Pixel, Long packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four 1246 pixels (nine bytes).

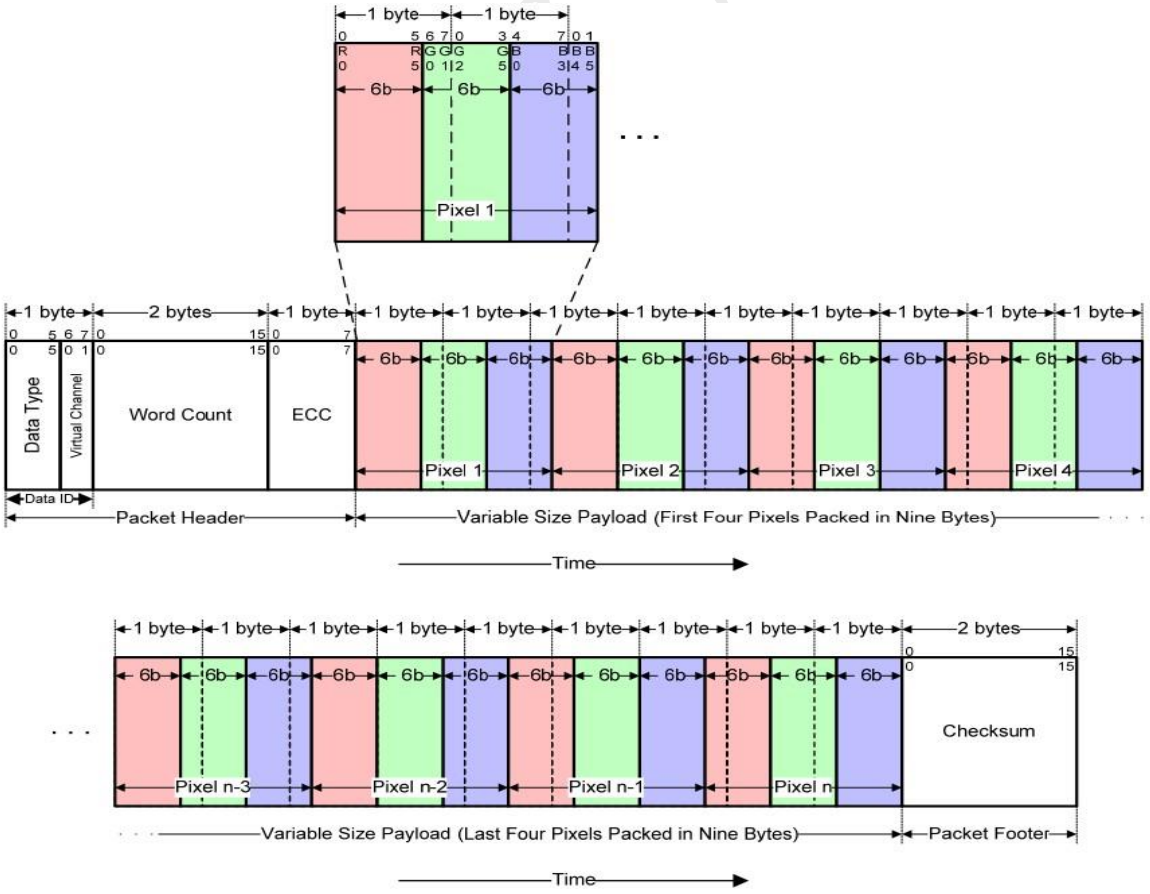


Figure 90 18-bit per Pixel, Data Type = 01 1110 (1Eh)

18-bit per Pixel, Long packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

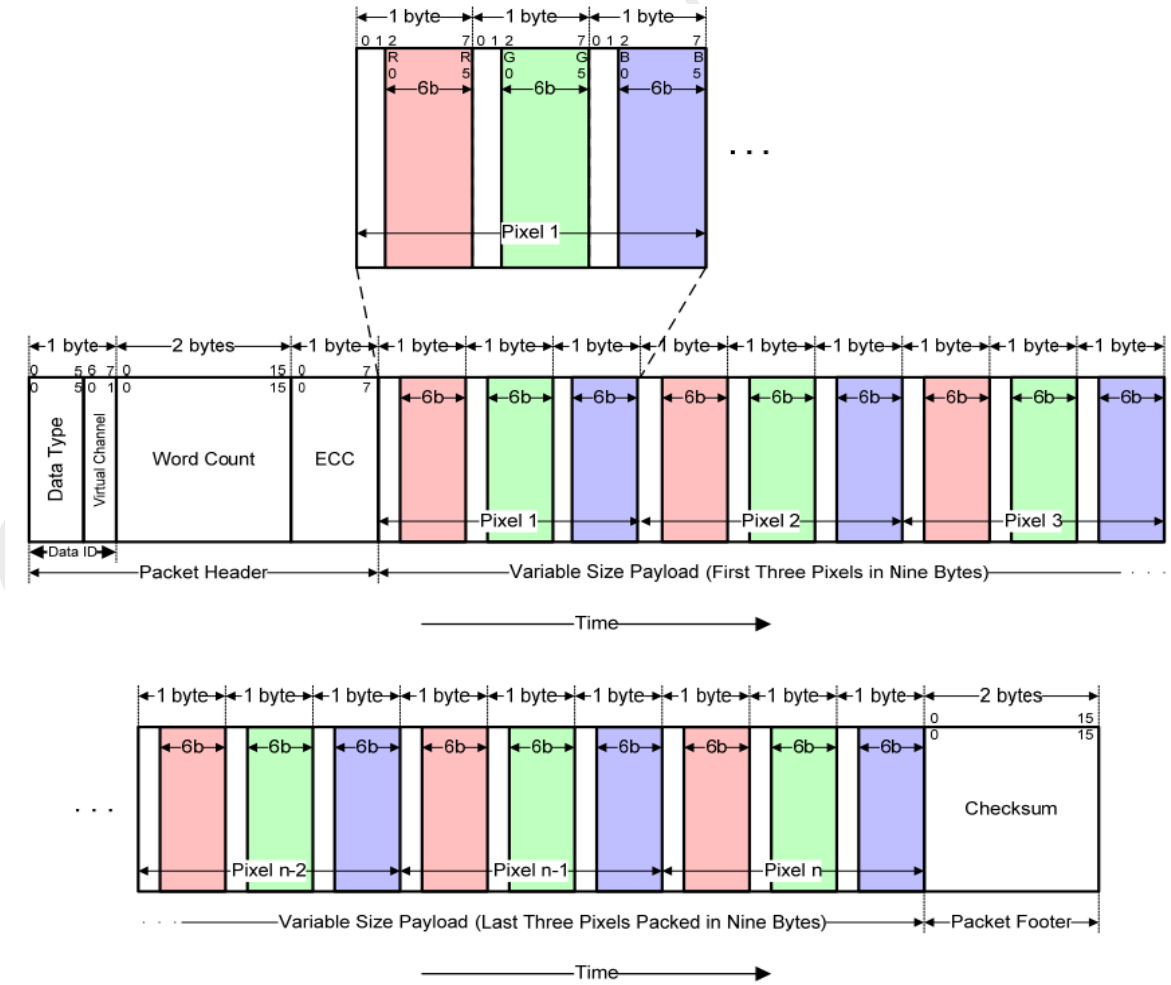


Figure 91 18-bit per Pixel, Data Type = 10 1110 (2Eh)

5.5.8 24-bit per Pixel, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

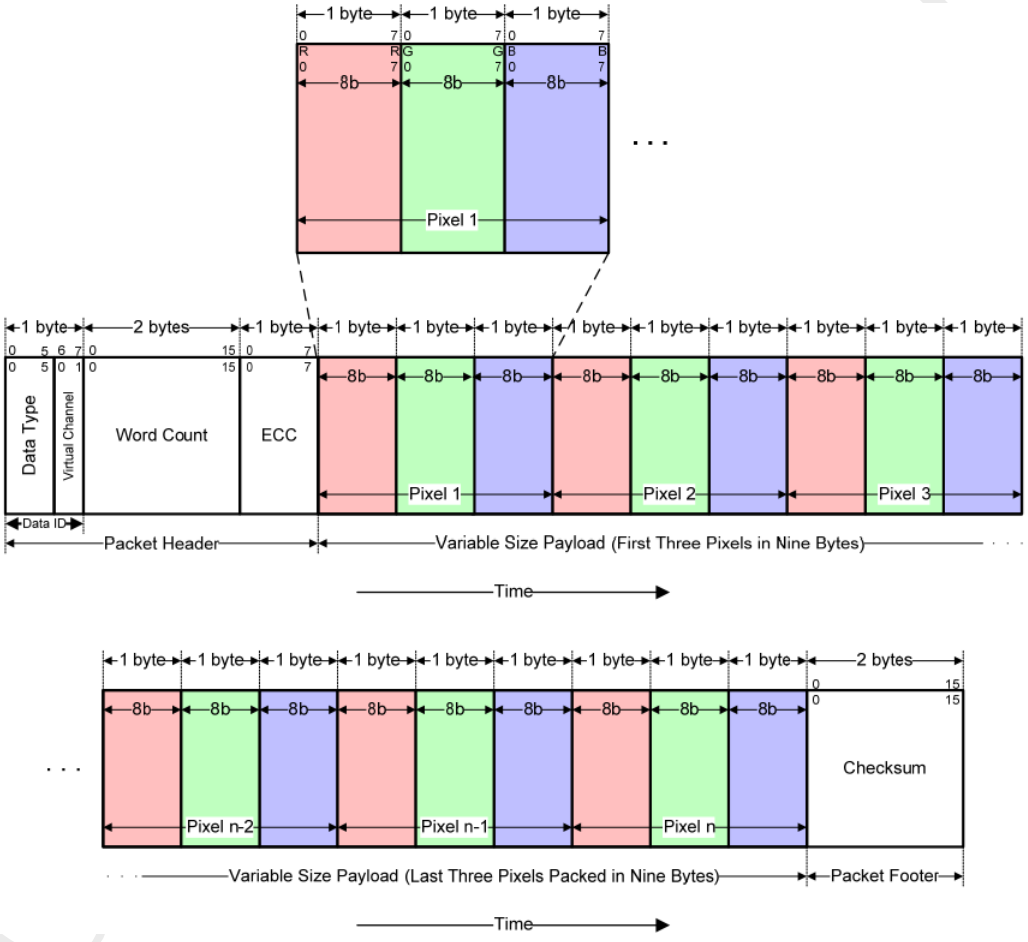


Figure 92 24-bit per Pixel, Data Type = 11 1110 (3Eh)

6. Command

6.1 User Command Set

Table 6.1.1 User Command Set

R/W	Address		Parameter									Function
	MIPI/spi8/9	Spi-16	D[15:8] (Non-MIPI/spi8/9)	D7	D6	D5	D4	D3	D2	D1	D0	
R	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read display ID
		0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
		0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
R	05h	0500h	00h	dsi_error[7:0]								RDNUMED
		0501h	00h	dsi_error[15:8]								
R	0Ah	0A00h	00h	sleep_out	idle	partial_on	sleep_out	normal_on	disp_on			Read Display Power Mode
R	0Bh	0B00h	00h				gs	bgr	ss			Read Display MADCTR
R	0Ch	0C00h	00h		vipf[2:0]							Read Display Pixel Format
R	0Dh	0D00h	00h			inv_on	pixel_on	pixel_off	gcs			Read Display Image Mode
W	10h	1000h	No Argument									Sleep in & booster off
W	11h	1100h	No Argument									Sleep out & booster on
W	12h	1200h	No Argument									Partial mode on
W	13h	1300h	No Argument									Normal display mode on
W	22h	2200h	No Argument									ALLPOFF
W	23h	2300h	No Argument									ALLPON
W	28h	2800h	No Argument									Display off
W	29h	2900h	No Argument									Display on
W	30h	3000h	00h							PSL9	PSL8	Partial start/end address set PSL[15:0]: partial start address PEL[15:0]: partial end address
		3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
		3002h	00h							PEL9	PEL8	
		3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	
W	38h	3800h	No Argument									Idle mode off
W	39h	3900h	No Argument									Idle mode on
W	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0					Interface pixel format
W	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Write display brightness
W	B0h	B000h	00h	rgb_mode	0	0	0	PCKP	DEP	HSP	VSP	RGB_MODE
		B001h	00h	VBP[7:0]								
		B002h	00h	VFP[7:0]								
		B003h	00h	HBP[7:0]								
		B004h	00h	HFP[7:0]								
W	B1h	B100h	00h	REV	0	BGR	NLA[2:0](dinv)			GS	SS	Display_CTL
W	F6h	F600h	00h	otp_reload_en_tmp[15:8]								OTP_CTL
		F601h	00h	otp_reload_en_tmp[7:0]								
R	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
R	DBh	DB00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID2

R	DCh	DC00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID3
W	F0h	F000h	00h	0	1	0	1	0	1	0	1	Manufacture command enable
		F001h	00h	1	0	1	0	1	0	1	0	
		F002h	00h	0	1	0	1	0	0	1	0	
		F003h	00h	0	0	0	0	MAUNC	0	0	0	
		F004h	00h	0	0	0	0	0	0	0	PAGE	

Notes:
In MIPI interface, parameters of the command are stores onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. See more information on the section "DATA TRANSFER RECOVERY". This note is valid when a number of the parameters is equal or less than 32.
The 8-bit address code for "MIPI" in above table and following command description means include 3-wire 9-bit

Read Display ID (04h)

User Command Set		04h : RDNUMED (Read Display ID)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	0	04h
1st Parameter	Read	ID1[7:0]								00h
2st Parameter	Read	ID2[7:0]								95h
3st Parameter	Read	ID3[7:0]								04h
Description	This read byte returns 24-bit display identification information. (the module's manufacture ID). And it is equal to returns value of Dah,DBh,DCh command.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h009503V
S/W Reset	24'h009503V
H/W Reset	24'h009503V

Read DSI ERROR (05h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">04h : RDNUMED (Read Display ID)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>05h</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">DSU_ERRO[7:0]</td><td>00h</td></tr>
<tr><td>2st Parameter</td><td>Read</td><td colspan="8">DSU_ERRO[15:8]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command returns an error report when DSI is used.
DSU_ERRO[15:8] is In accordance with Acknowledge with Error Report as followed.
<table>
<tr><th>DSU_ERRO</th><th>Description</th></tr>
<tr><td>0</td><td>SoT Error</td></tr>
<tr><td>1</td><td>SoT Sync Error</td></tr>
<tr><td>2</td><td>EoT Sync Error</td></tr>
<tr><td>3</td><td>Escape Mode Entry Command Error Y</td></tr>
<tr><td>4</td><td>Low-Power Transmit Sync Error Y</td></tr>
<tr><td>5</td><td>HS Receive Timeout Error</td></tr>
<tr><td>6</td><td>False Control Error</td></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>8</td><td>ECC Error, single-bit (detected, and corrected) Y</td></tr>
<tr><td>9</td><td>ECC Error, multi-bit (detected, not corrected) Y</td></tr>
<tr><td>10</td><td>Checksum Error (Long packet only) Y</td></tr>
<tr><td>11</td><td>DSI Data Type Not Recognized Y</td></tr>
<tr><td>12</td><td>DSI VC ID Invalid Y</td></tr>
<tr><td>13</td><td>Invalid Transmission Length</td></tr>
<tr><td>14</td><td>Reserved</td></tr>
<tr><td>15</td><td>DSI Protocol Violation</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000</td></tr>
<tr><td>S/W Reset</td><td>16’h0000</td></tr>
<tr><td>H/W Reset</td><td>16’h0000</td></tr>
</table></td></tr>
</table>

Read Display Power Mode (0Ah)

User Command Set		0Ah : RDDPM (Read Display Power Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	0	0Ah
1st Parameter	Read	booster	idle	partial_ on	sleep_ out	normal_ on	disp_o n	0	0	00h

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D7	Booster Voltage Status	0	Booster Off or has a fault.
		1	Booster On and working OK
D6	IDEL MODE	0 1	IDEL MODE ON IDEL MODE OFF
D5	PARTIAL MODE	0 1	PARTIAL MODE ON PARTIAL MODE O
D4	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D3	Display Normal Mode On/Off	0	Display Normal Mode Off.
		1	Display Normal Mode On
D2	Display On/Off	0	Display is Off.
		1	Display is On
D1	AVDD POWER STATE	0 1	AVDD POWER GOOD AVDD POWER NOT GOOD
D0	AVEE POWER STATE	0 1	AVEE POWER GOOD AVEE POWER NOT GOOD

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

Read Display MADCTL (0Bh)

User Command Set		0Bh : RDDPM (Read Display Power Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	1	0Bh
1st Parameter	Read	0	0	0	GS	BGR	SS	0	0	00h

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D7	Reserved	0	Reserved, so it is set to '0'
D6	Reserved	0	Reserved, so it is set to '0'
D5	Reserved	0	Reserved, so it is set to '0'
D4	GS	0	Gate output Top to Bottom
		1	Gate output Bottom to Top
D3	BGR	0	RGB (When MADCTL D3='0')
		1	BGR (When MADCTL D3='1').
D2	SS	0	Source output Left to Right
		1	Source output Right to Left
D1	Reserved	0	Reserved, so it is set to '0'
D0	Reserved	0	Reserved, so it is set to '0'

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

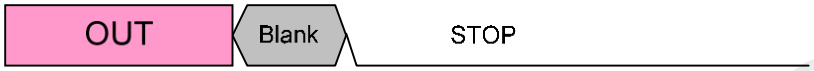
Read Display Pixel Format (0Ch)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="8">0Ch : RDDPM (Read Display Pixel Format)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0Ch</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td>VIPF2</td><td>VIPF1</td><td>VIFP0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below.
<table>
<tr><th colspan="3">VIPF[2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16-bit / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18-bit / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24-bit / pixel</td></tr>
<tr><td colspan="3">Others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>According to initial code</td></tr>
<tr><td>S/W Reset</td><td>8’h70</td></tr>
<tr><td>H/W Reset</td><td>8’h70</td></tr>
</table></td></tr>
</table>

Read Display Image Mode (0Dh)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="8">0Dh : RDDPM (Read Display Image Mode)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td>0</td><td>INVO</td><td>allpon</td><td>allpoff</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td rowspan="2">D5</td><td rowspan="2">Inversion On/Off</td><td>0</td><td>Inversion is Off.</td></tr>
<tr><td>1</td><td>Inversion is On.</td></tr>
<tr><td rowspan="2">D4</td><td rowspan="2">All Pixels On</td><td>0</td><td>Normal Display</td></tr>
<tr><td>1</td><td>White Display</td></tr>
<tr><td rowspan="2">D3</td><td rowspan="2">All Pixels Off</td><td>0</td><td>Normal Display</td></tr>
<tr><td>1</td><td>Black Display</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>According to initial code</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

Sleep In (10h)

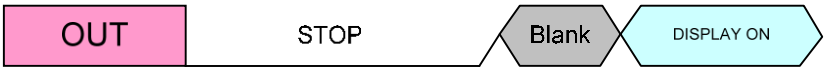
User Command Set		10h : CLOMD(Sleep In)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	0	10h
1st Parameter	-	XX								XXh
Description	This command causes the GC9503V to enter the minimum power consumption mode. 									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep out mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Sleep Out (11h)

User Command Set		11h : CLOMD(Sleep Out)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	1	11h
1st Parameter	-	XX								XXh
Description	This command causes the GC9503V to enter the Sleep Out mode 									
Restriction	This command has no effect when module is already in Sleep Out mode. Sleep Out mode can be left by the Sleep In command (10h) or H/W reset. It is necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The GC9503V loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the GC9503V is already Sleep Out mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep out mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

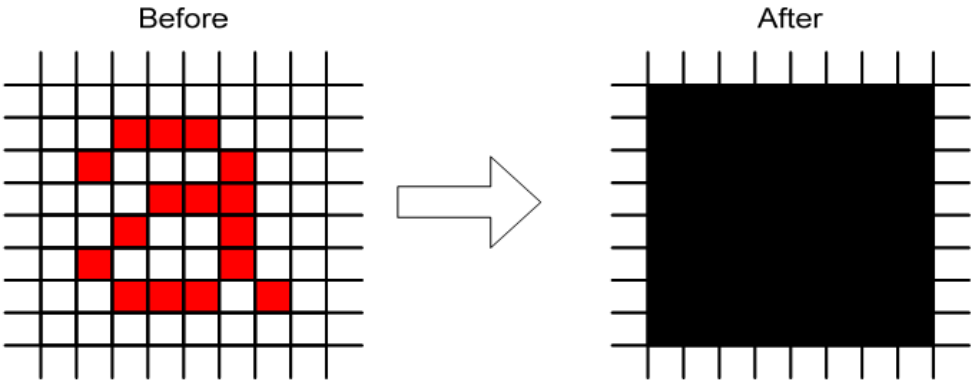
Partial Mode On (12h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">13h :CLOMD(Partial Mode On)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>1st Parameter</td><td>-</td><td colspan="8">XX</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H)
To leave Partial mode, the Normal Display Mode On command (13H) should be written.
There is no abnormal visual effect during mode change between Normal mode On to Partial mode On.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when Normal Display Mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal display mode on</td></tr><tr><td>S/W Reset</td><td>Normal display mode on</td></tr><tr><td>H/W Reset</td><td>Normal display mode on</td></tr></table></td></tr>
</table>

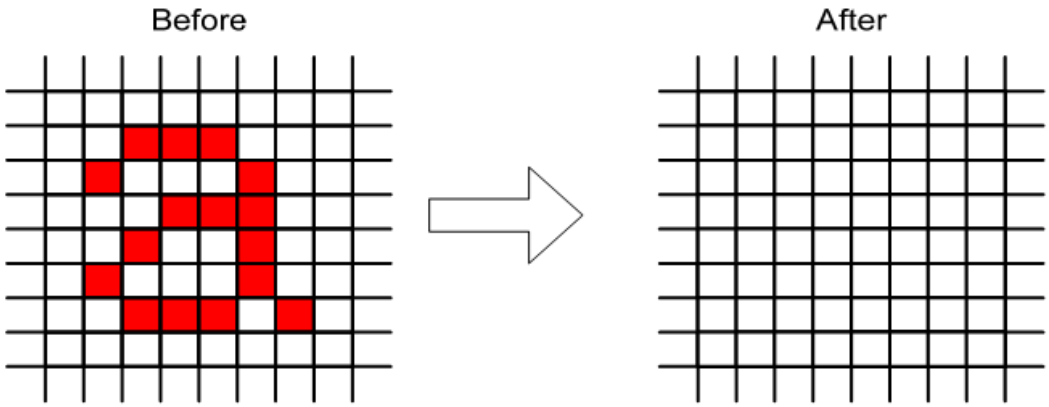
Normal Display Mode On (13h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">13h :CLOMD(Normal Display Mode On)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">XX</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command returns the display to Normal Display</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when Normal Display Mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal display mode on</td></tr><tr><td>S/W Reset</td><td>Normal display mode on</td></tr><tr><td>H/W Reset</td><td>Normal display mode on</td></tr></table></td></tr>
</table>

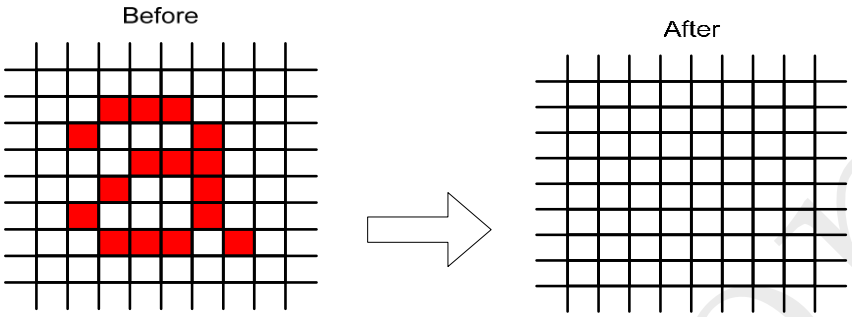
All Pixel Off (22h)

User Command Set		20h : CLOMD(Display Inversion Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	0	22h
1st Parameter	-	XX								XXh
Description	This command turns the display panel black in 'Sleep Out' mode and a status of the' Display On/Off' register can be 'on' or 'off'. This command does not change any other status 'All Pixels On', 'Normal Display Mode On' commands are used to leave this mode. 									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table>									

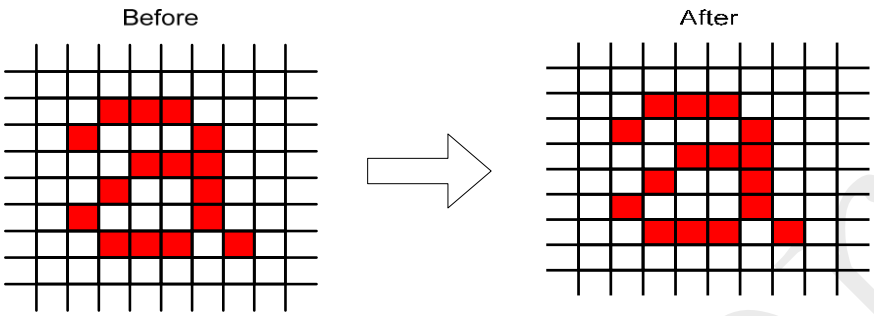
All Pixel On (23h)

User Command Set		21h : CLOMD(Display Inversion On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	1	23h
1st Parameter	Read	XX								XXh
Description	This command turns the display panel white in 'Sleep Out ' mode and a status of the 'Display On/Off' register can be 'on' or 'off'. This command does not change any other status. 'All Pixels Off', 'Normal Display Mode On'– commands are used to leave this mode. 									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table>									

Display Off (28h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="8">28h : CLOMD(Display Off)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28h</td></tr>
<tr><td>1st Parameter</td><td>-</td><td colspan="8">XX</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into Display Off mode. In this mode, the output data is disabled and blank page inserted. This command makes no change any other status.
There will be no abnormal visible effect on the display.
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Display Off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>display on mode</td></tr><tr><td>S/W Reset</td><td>display off mode</td></tr><tr><td>H/W Reset</td><td>display off mode</td></tr></table></td></tr>
</table>

Display ON (29h)

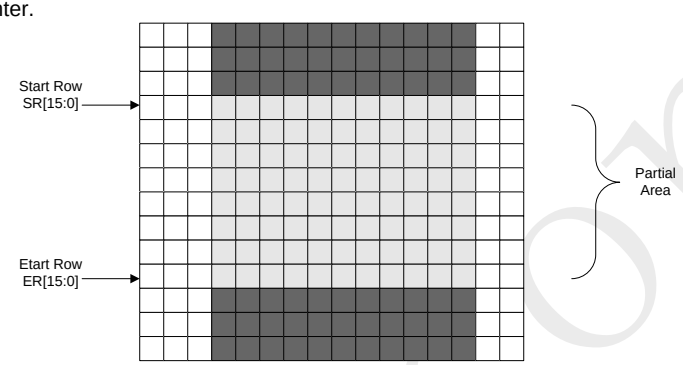
<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">29h : CLOMD(Display On)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>1st Parameter</td><td>-</td><td colspan="8">XX</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from Display Off mode. Output data is enabled. This command does not change any other status.
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the GC9503V is already in Display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>display on mode</td></tr><tr><td>S/W Reset</td><td>display off mode</td></tr><tr><td>H/W Reset</td><td>display off mode</td></tr></table></td></tr>
</table>

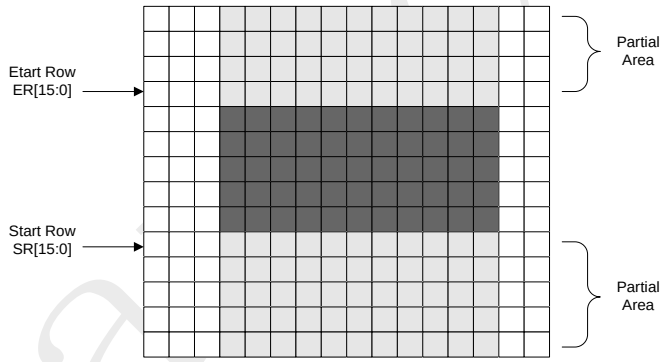
Partial Area (30h)

User Command Set		30h : CLOMD(Partial Area)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	0	0	0	30h
1st Parameter	Write							PSL9	PSL8	00h
2st Parameter	Write	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	00h
3st Parameter	Write							PEL9	PEL8	00h
4st Parameter	Write	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	00h
Description	This command returns the display to Normal Display									

Restriction

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.





If End Row = Start Row then the Partial Area will be one row deep.
X = Don't care.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

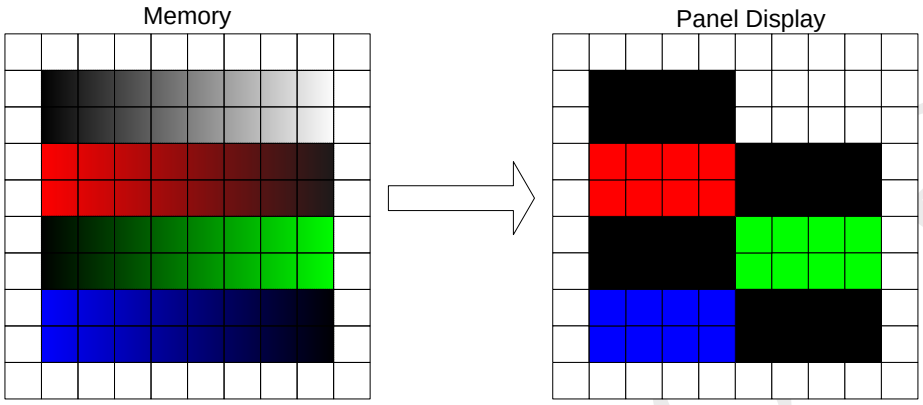
Default

Status	Default Value
Power On Sequence	32'h00000000
S/W Reset	32'h00000000
H/W Reset	32'h00000000

Idle Mode Off (38h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">38h : CLOMD(Idle Mode Off)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>1st Parameter</td><td>-</td><td colspan="8">xx</td><td>xxh</td></tr>
<tr><td>Description</td><td colspan="10">This command returns the display to Normal Display</td></tr>
<tr><td>Restriction</td><td colspan="10">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 16.7M colors.
X = Don’t care.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>S/W Reset</td><td>Idle mode OFF</td></tr><tr><td>H/W Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
</table>

Idle Mode On (39h)

User Command Set		39h : CLOMD(Idle Mode On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	1	0	0	1	39h
1st Parameter	Write	xx								xxh
Description	This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed. 									
Restriction	This command has no effect when module is already in idle off mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
S/W Reset	Idle mode OFF
H/W Reset	Idle mode OFF

Interface Pixel Format (3Ah)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">3Ah : COLMOD (Interface Pixel Format)</th></tr>
<tr><td></td><td>Write /</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3</td></tr>
<tr><td>1st Parameter</td><td>W</td><td>0</td><td colspan="4">VIPF[2:0]</td><td>0</td><td>0</td><td>0</td><td>70h</td></tr>
<tr><td>Description</td><td colspan="10">This command sets the pixel format. VIPF[2:0] selects the pixel format of RGB interface.
<table>
<tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16-bit / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18-bit / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24-bit / pixel</td></tr>
<tr><td colspan="3">Others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h70</td></tr>
<tr><td>S/W Reset</td><td>8’h70</td></tr>
<tr><td>H/W Reset</td><td>8’h70</td></tr>
</table></td></tr>
</table>

Write Display Brightness Value (51h)

User Command Set		3Ah : COLMOD (Interface Pixel Format)								
	Write /	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	W	0	0	1	1	1	0	1	0	51h
1st Parameter	W	0	DBV[7:0]							00h
Description	The command is used to adjust the brightness value of the display. DBV[7:0]: 8 bit, for display brightness of manual brightness setting in the GC9503V. There is a PWM output signal, LEDPWM pin, to control the LED driver IC in order to control display brightness.									
Restriction										

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

RGB Interface Signals Control(B0h)

User Command Set		B0h : RGB Interface Signals Control								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	D7	D6	D5	D4	D3	D2	D1	D0	B0h
1st Parameter	Write	CMRC				PCKP	DEP	HSP	VSP	00h
2th Parameter	Write	VBP[7:0]								0Eh
3th Parameter	Write	VFP[7:0]								0Eh
4th Parameter	Write	HBP[7:0]								14h
5th Parameter	Write	HFP[7:0]								04h

Description

Bit	Description	Value
CRCM	Select the RGB mode1/mode 2	"0" = RGB mode 1(DE mode)
		"1" = RGB mode 2(Sync mode)
PCKP	PCLK Fetch Polarity	"0" = Data latched at the rising edge of PCLK
		"1" = Data latched at the falling edge of PCLK
DEP	DE Enable Polarity	"0" = High enable for RGB interface
		"1" = Low enable for RGB interface
HSP	H-Sync Pulse Level	"0" = Low pulse level sync clock
		"1" = High pulse level sync clock
VSP	V-Sync Pulse Level	"0" = Low pulse level sync clock
		"1" = High pulse level sync clock
VBP[7:0]	V-Sync Back Porch	"05h" to "FFh" = 5 to 255 H-Sync clocks
VFP[7:0]	V-Sync Front Porch	"02h" to "FFh" = 2 to 255 H-Sync clocks
HBP[7:0]	H-Sync Back Porch	"05h" to "FFh" = 5 to 255 PCLK clocks
HFP[7:0]	H-Sync Front Porch	"02h" to "FFh" = 2 to 255 PCLK clocks

The registers VBP[7:0], VFP[7:0], HBP[7:0] and HFP[7:0] for vertical and horizontal porch control are used in RGB interface mode 2 only. The setting value "00h" is invalid for all of these four register s.

RGB IF Mode	PCLK	DE	D[23:0]	VS	HS	VBP[7:0], VFP[7:0], HBP[7:0], HFP[7:0]
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	B000h	B001h	B002h	B003h	B004h
Power On Sequence	00h	0Eh	0Eh	14h	04h
S/W Reset	00h	0Eh	0Eh	14h	04h
H/W Reset	00h	0Eh	0Eh	14h	04h

DISPLAY_CTL (B1h)

User Command Set		BCh : COLMOD (Display Inversion Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	D7	D6	D5	D4	D3	D2	D1	D0	B1h
1st Parameter	Write	REV	0	BGR	NLA[2:0](dinv)			GS	SS	10h

Description

REV=0
recover from Display Inversion On mode

REV=1
enter into Display Inversion On mode

BGR=0
BGR color filter panel

BGR=1
RGB color filter panel

GS: Select the Gate driver scan direction on panel module
SS:Select the Source driver scan direction on panel module

NLA[2:0]	Inersion Mode for Source Driver
000	1-Dot inversion
001	2-Dot inversion
010	3-Dot inversion
011	4-Dot inversion
100	Column inversion
101-111	reserved

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h10
S/W Reset	8'h10
H/W Reset	8'h10

Read ID1 (DAh)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="8">DAh : RDDPM (Read ID1)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>DAh</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">ID1[7:0]</td><td>8h’00</td></tr>
<tr><td>Description</td><td colspan="10">This read byte returns 8-bit display identification information. (the module’s manufacture ID). And it is equal to returns 1rst parameter of 04h command.
The ID1 is programmed by OTP function.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0h’00</td></tr><tr><td>S/W Reset</td><td>0h’00</td></tr><tr><td>H/W Reset</td><td>0h’00</td></tr></table></td></tr>
<tr><td></td><td colspan="10"></td></tr>
</table>

Read ID2 (DBh)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="8">DBh : RDDPM (Read ID2)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DBh</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">ID2[7:0]</td><td>8'h95</td></tr>
<tr><td>Description</td><td colspan="10">This read byte returns 8-bit display identification information. (the module's manufacture ID). And it is equal to returns 2th parameter of 04h command.
The ID2 is programmed by OTP function.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0'h95</td></tr><tr><td>S/W Reset</td><td>0'h95</td></tr><tr><td>H/W Reset</td><td>0'h95</td></tr></table></td></tr>
</table>

Read ID3 (DCh)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="8">DCh : RDDPM (Read ID3)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>DCh</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">ID3[7:0]</td><td>8’h04</td></tr>
<tr><td>Description</td><td colspan="10">This read byte returns 8-bit display identification information. (the module’s manufacture ID). And it is equal to returns 3th parameter of 04h command.
The ID3 is programmed by OTP function.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h04</td></tr><tr><td>S/W Reset</td><td>8’h04</td></tr><tr><td>H/W Reset</td><td>8’h04</td></tr></table></td></tr>
</table>

EXTC Command Set enable register (F0h)

User Command Set		F0h : COLMOD (EXTC Command Set enable register)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	1	0	0	0	0	F0h
1st Parameter	Write	0	1	0	1	0	1	0	1	55h
2st Parameter	Write	1	0	1	0	1	0	1	0	aah
3st Parameter	Write	0	1	0	1	0	0	1	0	52h
4st Parameter	Write	0	0	0	0	MAUNC	0	0	0	08h
5st Parameter	Write	0	0	0	0	0	0	0	PAGE	00h

Description

Bit	Description	Value
MAUC	Manufacture Command Set enable/ disable	"0": Manufacture Command Set disable "1": Manufacture Command Set enable
PAGE	Manufacture Command Set selection	"0": Page 0
		"1": Page 1

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	40h'55aa520800
S/W Reset	40h'55aa520800
H/W Reset	40h'55aa520800

OTP_CTL (F6h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="8">F0h : COLMOD (EXTC Command Set enable register)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>F6h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">otp_reload_en_tmp[15:8]</td><td>5ah</td></tr>
<tr><td>2th Parameter</td><td>Write</td><td colspan="8">otp_reload_en_tmp[7:0]</td><td>87h</td></tr>
<tr><td>Description</td><td colspan="10">If otp_reload_en_tmp[15:0]!=16’h5a87, then IC will reload OTP automatically.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>16’h5a87</td></tr><tr><td>S/W Reset</td><td>16’h5a87</td></tr><tr><td>H/W Reset</td><td>16’h5a87</td></tr></table></td></tr>
</table>

6.2 Page 0 Command Set

Table 6.1.2 Page 0 Command Set

R/W	Address		Parameter									Function
	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
W	80h	8000h	00h	D2D_VOFFSET[7:0]								VREG_CTL0
W	82h	8200h	00h	D2D_VGSPN_AD_TMP1[7:0]								VREG_CTL1
		8201h	00h	D2D_VGSPN_AD_TMP2[7:0]								
W	86h	8600h	00h	0x99								CHP_CTL1
		8601h	00h	0Xa3								
		8602h	00h	0xa3								
		8603h	00h	0	D2A_VGL_AD[2:0]			0	0	0	1	
W	89h	8900h	00h	0	D2A_AVEE_AD[2:0]			0	D2A_AVDD_AD[2:0]			CHP_CTL2
W	90h	9000h	00h	0	1	0	1	0	D2A_BVDD1_AD[2:0]			CHP_CTL3
W	91h	9100h	00h	0	1	0	1	0	D2A_BVEE1_AD[2:0]			CHP_CTL4
W	98h	9800h	00h	D2D_VREG_VGMP_AD_TMP1[7:0]								VREG_CTL2
W	99h	9900h	00h	D2D_VREG_VGMN_AD_TMP1[7:0]								VREG_CTL3
W	9Ah	9A00h	00h	D2D_VREG_VGMP_AD_TMP2[7:0]								VREG_CTL4
W	9Bh	9B00h	00h	D2D_VREG_VGMN_AD_TMP2[7:0]								VREG_CTL5
W	A0h	A000h	00h	D2D_VGHS[3:0]_TMP1				D2D_VGHS[3:0]_TMP2				CHP_CTL5
W	C4h	C400h	00h	1	reg_en_86 (0)	0	1	1	reg_en_82 (1)	1	reg_en_80 (1)	REG_CTL1
W	C5h	C500h	00h	0	0	0	0	0	0	reg_en_89 (0)	1	REG_CTL2
W	C6h	C600h	00h	0	1	1	1	1	1	reg_en_91 (0)	reg_en_90 (0)	REG_CTL3
W	C7h	C700h	00h	0	0	1	1	reg_en_9B (1)	reg_en_9A (1)	reg_en_99 (0)	reg_en_98 (0)	REG_CTL4
W	C8h	C800h	00h	1	1	0	0	1	0	reg_en_a1 (0)	reg_en_a0 (0)	REG_CTL5

VREG_CTL0 (80h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9"></th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>80h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VOFFSET[7:0]</td><td>8’h00</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VOFFSET is the offset of VGMP and VGSPN and VGMN together, which is used to dispel the flicker.

<table>
<tr><th>D2D_VOFFSET[7:0]</th><th>Offset of VREG</th><th>D2D_VOFFSET[7:0]</th><th>Offset of VREG</th></tr>
<tr><td>0</td><td>+0</td><td>128</td><td>-127</td></tr>
<tr><td>1</td><td>+1</td><td>129</td><td>-126</td></tr>
<tr><td>..</td><td>…</td><td>..</td><td>..</td></tr>
<tr><td>..</td><td>…</td><td>..</td><td>..</td></tr>
<tr><td>126</td><td>+126</td><td>254</td><td>-1</td></tr>
<tr><td>127</td><td>+127</td><td>255</td><td>-0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (C4h)” b0” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

VREG_CTL1 (82h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9"></th></tr>
<tr><th></th><th>Write / Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default (Hex)</th></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>82h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VGSPN_AD_TMP1[7:0]</td><td>8'h4f</td></tr>
<tr><td>2th Parameter</td><td>Write</td><td colspan="8">D2D_VGSPN_AD_TMP2[7:0]</td><td>8'h4f</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VGSPN_AD_TMP 1 is the adjustment register of VGSPN in low-temperature environment.
D2D_VGSPN_AD_TMP 2 is the adjustment register of VGSPN in normal-temperature environment.
<table>
<tr><th>D2D_VGSPN_AD_TMP 1[7:0]</th><th>VGSPN(V)</th><th>D2D_VGSPN_AD_TMP 2[7:0]</th><th>VGSPN(V)</th></tr>
<tr><td>0</td><td>0.125</td><td>0</td><td>0.125</td></tr>
<tr><td>1</td><td>0.250</td><td>1</td><td>0.250</td></tr>
<tr><td>2</td><td>0.375</td><td>2</td><td>0.375</td></tr>
<tr><td>..</td><td>…</td><td>..</td><td>…</td></tr>
<tr><td>n</td><td>(n+1)*0.125</td><td>n</td><td>(n+1)*0.125</td></tr>
<tr><td>..</td><td>…</td><td>..</td><td>…</td></tr>
<tr><td>199</td><td>2.5</td><td>199</td><td>2.5</td></tr>
<tr><td>200</td><td>inhibited</td><td>200</td><td>inhibited</td></tr>
<tr><td>…</td><td>inhibited</td><td>…</td><td>inhibited</td></tr>
<tr><td>255</td><td>inhibited</td><td>255</td><td>inhibited</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (C4h)” b2” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>16'h4f4f</td></tr>
<tr><td>S/W Reset</td><td>16'h4f4f</td></tr>
<tr><td>H/W Reset</td><td>16'h4f4f</td></tr>
</table></td></tr>
</table>

CHP_CTL1 (86h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">CHP_CTL1</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>86h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">0x99</td><td>0x99</td></tr>
<tr><td>2th Parameter</td><td>Write</td><td colspan="8">0Xa3</td><td>0Xa3</td></tr>
<tr><td>3th Parameter</td><td>Write</td><td colspan="8">0xa3</td><td>0xa3</td></tr>
<tr><td>4th Parameter</td><td>Write</td><td>0</td><td colspan="3">D2A_VGL_AD[2:0]</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0x21</td></tr>
<tr><td>Description</td><td colspan="10">D2A_VGL_AD the adjustment register of VGL amplitude.

<table>
<tr><th>D2A_VGL_AD[2:0]</th><th>VGL(V)</th></tr>
<tr><td>0</td><td>-8.0</td></tr>
<tr><td>1</td><td>-8.5</td></tr>
<tr><td>2</td><td>-9.0</td></tr>
<tr><td>3</td><td>-9.5</td></tr>
<tr><td>4</td><td>-10.0</td></tr>
<tr><td>5</td><td>-10.5</td></tr>
<tr><td>6</td><td>-11.0</td></tr>
<tr><td>7</td><td>-11.5</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (C4h)” b6” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>32’h99a3a321</td></tr>
<tr><td>S/W Reset</td><td>32’h99a3a321</td></tr>
<tr><td>H/W Reset</td><td>32’h99a3a321</td></tr>
</table></td></tr>
</table>

CHP_CTL2(89h)

User Command Set										
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	D7	D6	D5	D4	D3	D2	D1	D0	89h
1st Parameter	Write	0	D2A_AVEE_AD[2:0]			0	D2A_AVDD_AD[2:0]			8'h33

Description

Adjust AVDD/AVEE Clamp Voltage

AVDD_AD[2:0]	AVDD(V)	AVEE_AD[2:0]	AVEE(V)
0	6.88	0	-4.92
1	6.76	1	-4.8
2	6.64	2	-4.68
3	6.52	3	-4.56
4	6.4	4	-4.44
5	6.28	5	-4.32
6	6.16	6	-4.2
7	6.04	7	-4.08

Restriction

To enable this command, "Page 0 Command Set enable register (F0h) " must set first.
And enable register (C5h)" b6" must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h33
S/W Reset	8'h33
H/W Reset	8'h33

CHP_CTL3 (90h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9"></th></tr>
<tr><th></th><th>Write / Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default (Hex)</th></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>90h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td colspan="3">D2A_BVDD1_AD[2:0]</td><td>8’h55</td></tr>
<tr><td>Description</td><td colspan="10">Adjust BVDD Clamp Voltage
<table>
<tr><th>D2A_BVDD1_AD[2:0]</th><th>BVDD(V)</th></tr>
<tr><td>0</td><td>7.0</td></tr>
<tr><td>1</td><td>6.9</td></tr>
<tr><td>2</td><td>6.8</td></tr>
<tr><td>3</td><td>6.7</td></tr>
<tr><td>4</td><td>6.6</td></tr>
<tr><td>5</td><td>6.5</td></tr>
<tr><td>6</td><td>6.4</td></tr>
<tr><td>7</td><td>6.3</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (C6h)” b0” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h55</td></tr>
<tr><td>S/W Reset</td><td>8’h55</td></tr>
<tr><td>H/W Reset</td><td>8’h55</td></tr>
</table></td></tr>
</table>

CHP_CTL4 (91h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9"></th></tr>
<tr><th></th><th>Write / Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default (Hex)</th></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>91h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td colspan="3">D2A_BVEE1_AD[2:0]</td><td>8’h55</td></tr>
<tr><td>Description</td><td colspan="10">Adjust BVEE Clamp Voltage
<table>
<tr><th>D2A_BVEE1_AD[2:0]</th><th>BVEE(V)</th></tr>
<tr><td>0</td><td>-5.0</td></tr>
<tr><td>1</td><td>-4.9</td></tr>
<tr><td>2</td><td>-4.8</td></tr>
<tr><td>3</td><td>-4.7</td></tr>
<tr><td>4</td><td>-4.6</td></tr>
<tr><td>5</td><td>-4.5</td></tr>
<tr><td>6</td><td>-4.4</td></tr>
<tr><td>7</td><td>-4.3</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (C6h)” b1” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h55</td></tr>
<tr><td>S/W Reset</td><td>8’h55</td></tr>
<tr><td>H/W Reset</td><td>8’h55</td></tr>
</table></td></tr>
</table>

VREG_CTL2 (98h)

<table>
<tr><td colspan="2">User Command Set</td><td colspan="9"></td></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>98h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VREG_VGMP_AD_TMP1[7:0]</td><td>8’Hc2</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VGMP_AD_TMP 1 is the adjustment register of VGMP in low-temperature environment.

<table>
<tr><th>D2D_VREG_VGMP_AD_TMP1[7:0]</th><th>VGMP(V)</th></tr>
<tr><td>0</td><td>3.575</td></tr>
<tr><td>1</td><td>3.5875</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>N</td><td>3.575+0.0125*N</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>229</td><td>6.4375</td></tr>
<tr><td>…</td><td>inhibited</td></tr>
<tr><td>255</td><td>inhibited</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (C7h)” b0” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’hc2</td></tr>
<tr><td>S/W Reset</td><td>8’hc2</td></tr>
<tr><td>H/W Reset</td><td>8’hc2</td></tr>
</table></td></tr>
</table>

VREG_CTL3 (99h)

<table>
<tr><td colspan="2">User Command Set</td><td colspan="9"></td></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>99h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VREG_VGMN_AD_TMP1[7:0]</td><td>8’H4a</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VGMN_AD_TMP1 is the adjustment register of VGMN in low-temperature environment.

<table>
<tr><th>D2D_VREG_VGMN_AD_TMP1[7:0]</th><th>VGMN(V)</th></tr>
<tr><td>0</td><td>inhibited</td></tr>
<tr><td>..</td><td>inhibited</td></tr>
<tr><td>10</td><td>-4.8</td></tr>
<tr><td>11</td><td>-4.7875</td></tr>
<tr><td>..</td><td>...</td></tr>
<tr><td>N</td><td>-4.8+N*0.0125</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>255</td><td>-1.7375</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (C7h)” b1” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h4a</td></tr>
<tr><td>S/W Reset</td><td>8’h4a</td></tr>
<tr><td>H/W Reset</td><td>8’h4a</td></tr>
</table></td></tr>
</table>

VREG_CTL4 (9Ah)

<table>
<tr><td colspan="2">User Command Set</td><td colspan="9"></td></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>9Ah</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VREG_VGMP_AD_TMP2[7:0]</td><td>8’Hc2</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VGMP_AD_TMP 2 is the adjustment register of VGMP in normal-temperature environment.

<table>
<tr><th>D2D_VREG_VGMP_AD_TMP2[7:0]</th><th>VGMP(V)</th></tr>
<tr><td>0</td><td>3.575</td></tr>
<tr><td>1</td><td>3.5875</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>N</td><td>3.575+0.0125*N</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>229</td><td>6.4375</td></tr>
<tr><td>…</td><td>inhibited</td></tr>
<tr><td>255</td><td>inhibited</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (C7h)” b2” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’hc2</td></tr>
<tr><td>S/W Reset</td><td>8’hc2</td></tr>
<tr><td>H/W Reset</td><td>8’hc2</td></tr>
</table></td></tr>
</table>

VREG_CTL5 (9Bh)

<table>
<tr><td colspan="2">User Command Set</td><td colspan="9"></td></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>9Bh</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VREG_VGMN_AD_TMP2[7:0]</td><td>8’H4a</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VGMN_AD_TMP2 is the adjustment register of VGMN in normal-temperature environment.

<table>
<tr><th>D2D_VREG_VGMN_AD_TMP2[7:0]</th><th>VGMN(V)</th></tr>
<tr><td>0</td><td>inhibited</td></tr>
<tr><td>..</td><td>inhibited</td></tr>
<tr><td>10</td><td>-4.8</td></tr>
<tr><td>11</td><td>-4.7875</td></tr>
<tr><td>..</td><td>...</td></tr>
<tr><td>N</td><td>-4.8+N*0.0125</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>255</td><td>-1.7375</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
Andenable register (C7h)” b3” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h4a</td></tr>
<tr><td>S/W Reset</td><td>8’h4a</td></tr>
<tr><td>H/W Reset</td><td>8’h4a</td></tr>
</table></td></tr>
</table>

CHP_CTL5(A0h)

User Command Set		7Fh : CHP_CTL6								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	D7	D6	D5	D4	D3	D2	D1	D0	A0h
1st Parameter	Write	D2D_VGHS_TMP1[3:0]				D2D_VGHS_TMP2[3:0]				8'h77

Description

D2D_ VGHS _TMP1 is the adjustment register of VGH in low-temperature environment.
D2D_ VGHS _TMP2 is the adjustment register of VGH in normal-temperature environment.

D2D_VGHS_TMP1[3:0]	VGH(V)	D2D_VGHS_TMP2[3:0]]	VGH(V)
0	8.47	0	8.47
1	9.00	1	9.00
2	9.47	2	9.47
3	10.00	3	10.00
4	10.43	4	10.43
5	11.07	5	11.07
6	11.43	6	11.43
7	12.00	7	12.00
8	12.41	8	12.41
9	13.09	9	13.09
10	13.58	10	13.58
11	14.12	11	14.12
12	14.40	12	14.40
13	15.00	13	15.00
14	15.65	14	15.65
15	16.00	15	16.00

Restriction

To enable this command, "Page 0 Command Set enable register (F0h) " must set first.
Andenable register (C8h)" b1" must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

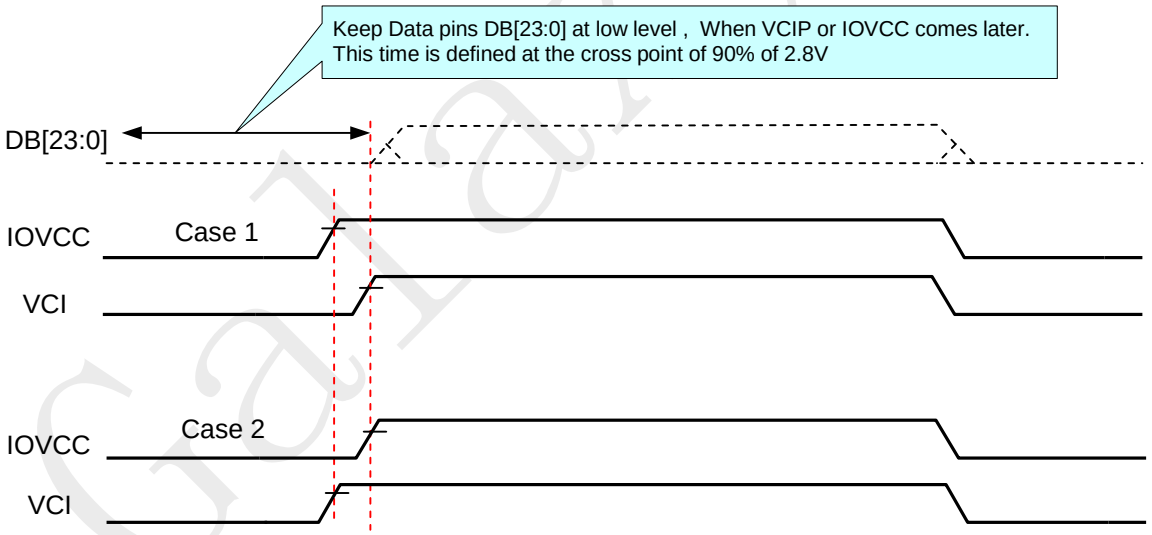
Status	Default Value
Power On Sequence	8'h77
S/W Reset	8'h77
H/W Reset	8'h77

7. Power ON/OFF Sequence

IOVCC and VCI can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VCI and IOVCC can be powered down with minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

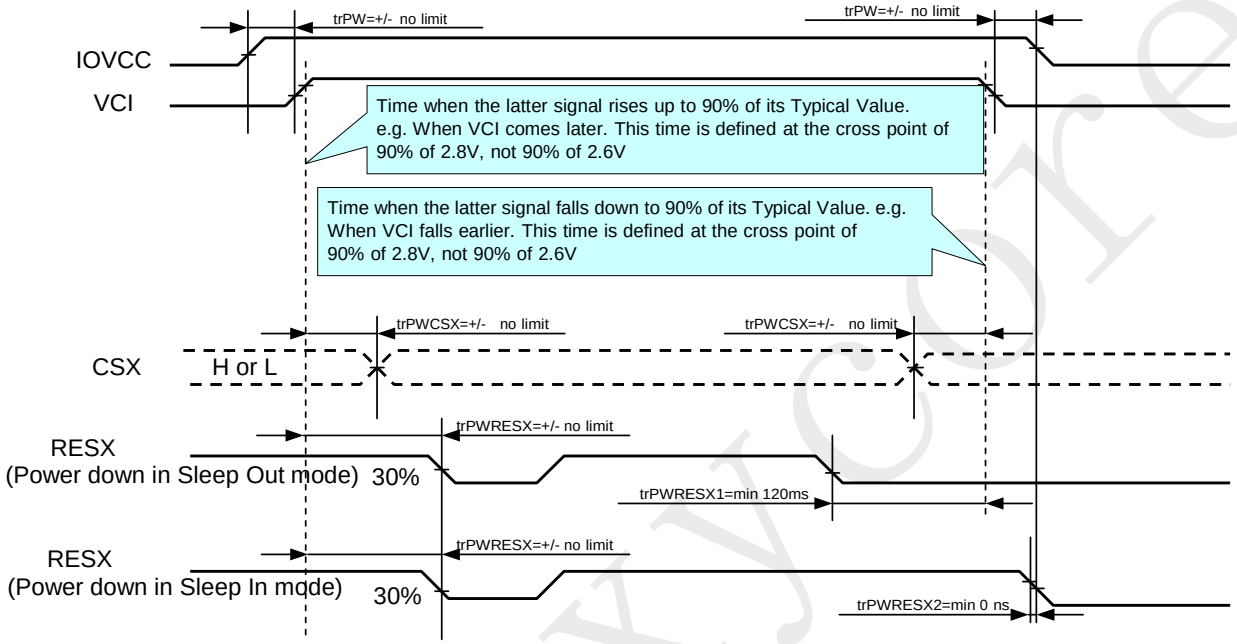
Note:

1. There will be no damage to GC9503V if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.1 and 7.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. Keep data pins DB[23:0] at low level, when VCIP or IOVCC comes later



7.1. Case 1 –RESX line is held High or Unstable by Host at Power ON

If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

7.2. Case 2 – RESX line is held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.

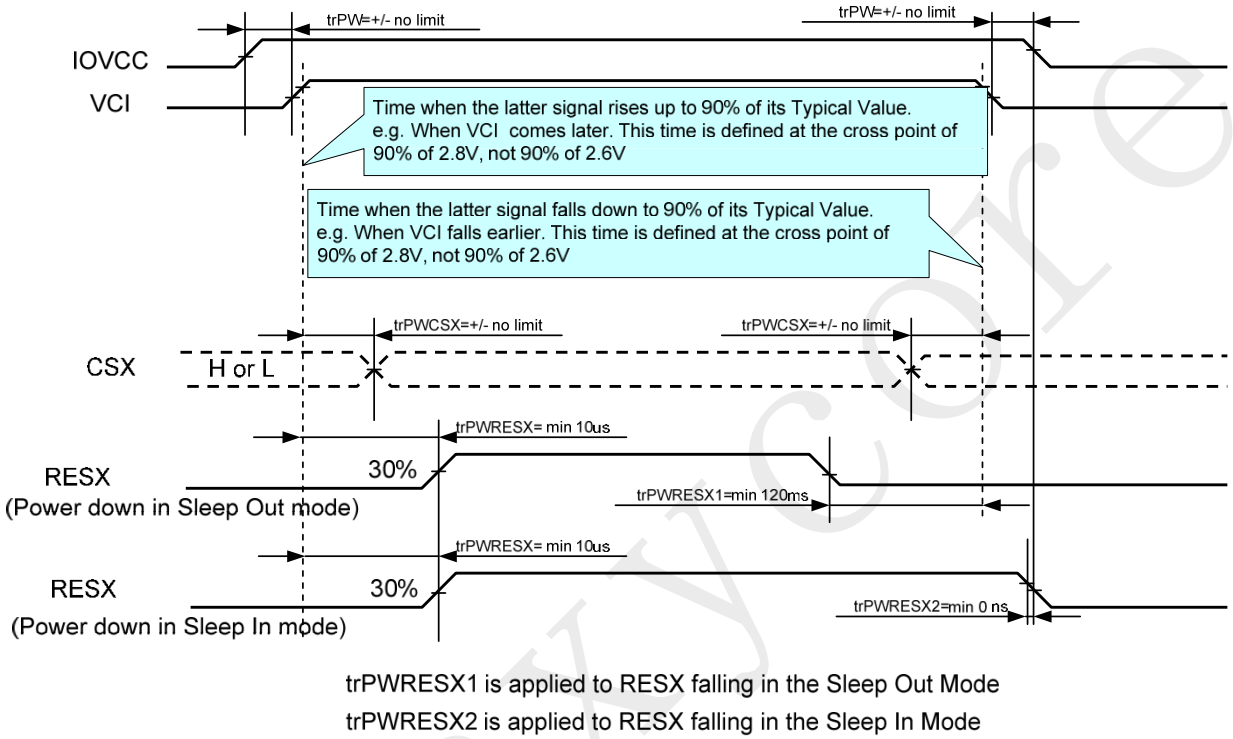


Figure 99 Case 2 – RESX line is held Low by Host at Power ON

Note: 1. Unless otherwise specified, timings herein show cross point at 50% of signal power level.

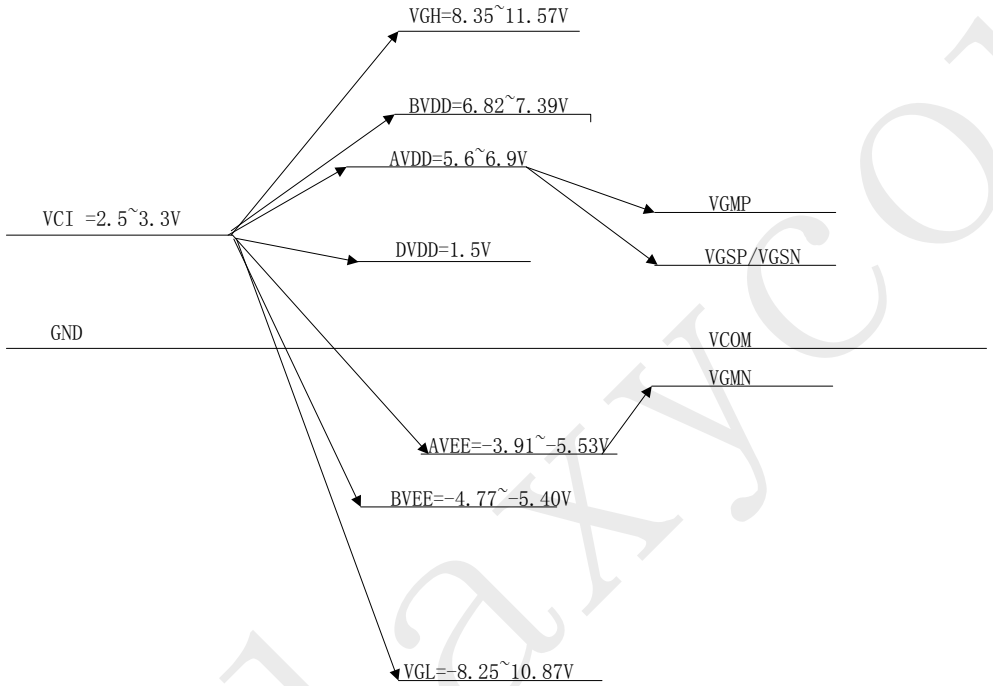
7.3. Abnormal Power Off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, GC9503V will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it up

8. Power Level Definition

8.1. LCM Voltage Generation

Note: 1. The AVDD，AVEE，BVDD，BVEE, VGH, VGL output voltage levels may be fewer different from their theoretical levels due to different panel loading.



9. Electrical Characteristics

9.1. Absolute Maximum Ratings

The absolute maximum rating is listed on Table 42. When the GC9503V is used out of the absolute maximum ratings, it may be permanently damaged. To use the GC9503V within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the GC9503V will malfunction and cause poor reliability.

Table 43 Absolute Maximum Ratings

Item	Symbol	Unit	Value
Supply voltage(Analog)	VCI ~ AGND	V	-0.3 ~ +4.6
Supply voltage(Analog)	VCIP ~ CGND	V	-0.3 ~ +4.6
Supply voltage(Analog)	VCIR ~ VSSR1	V	-0.3 ~ +4.6
Supply voltage (I/O)	IOVCC ~ DGND	V	-0.3 ~ +4.6
OTP Supply voltage	VPP ~ AGND	V	-0.3 ~ +6.6
Supply voltage	AVDD ~ AGND	V	-0.3 ~ +6.6
Supply voltage	AVEE ~ AGND	V	0.3 ~ -6.6
Supply voltage	BVDD ~ AGND	V	-0.3 ~ +6.6
Supply voltage	BVEE ~ AGND	V	0.3 ~ -6.6
Supply voltage	VGH ~ AGND	V	-0.3 ~ +25
Supply voltage	VGL ~ AGND	V	0.3 ~ -16
Driver supply voltage	AVDD – AVEE	V	≦13.2V
Driver supply voltage	VGH – VGL	V	≦ 32.0V
Input voltage	V_{IN}	V	-0.3 ~ IOVCC + 0.3
HS Input voltage	V_{HSIN}	V	-0.3 ~ + 2
Operating temperature	Topr	℃	-30 ~ +70
Storage temperature	Tstg	℃	-55 ~ +110

Note:

Even if the one of the above parameters is exceeded momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the exceeding values which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

9.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Operating voltage	VCI VCIP VCIR	-	2.5	2.8	3.3	V	
Operating voltage	IOVCC	-	1.65	1.8	3.3	V	Note1,2
OTP Supply voltage	VPP	-		5.0		V	Note1
Logic High level input voltage	V_{IH}	-	0.7*IOVCC		IOVCC	V	Note1
Logic Low level input voltage	V_{IL}	-	-0.3		0.3*IOVCC	V	Note1
Logic High level output voltage TE, SDO (SDA) , LEDPWM	V_{OH}	IOH = -1.0mA	0.8*IOVCC		IOVCC	V	Note1
Logic Low level output voltage TE, SDO (SDA) , LEDPWM	V_{OL}	IOL = +1.0mA	0		0.2*IOVCC	V	Note1
Gate Driver High Voltage	VGH	-	10.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	
Driver Supply Voltage	-	|VGH-VGL|	16	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.0	-	0	V	Note3
Source Driver							
Source Output Range	V_{SOUT}	-	VREG2OUT +0.1	-	VREG1OUT -0.1	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	3.0	-	6.1875	V	Note5
Negative Gamma Reference Voltage	VREG2OUT	-	-6.1875	-	-3.0	V	Note5
Source Output Setting Time	Tr	Below with 99% precision	-	15	20	us	Note3.4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	30	mV	Note3
		4.2V>Sout>0.8V	-	-	20	mV	-
Output Offset Voltage	V_{OFFSET}	-	-	-	35	mV	Note3
Booster Operation							
Booster Voltage	DDVDH	-			6.5	V	
Booster Voltage	DDVDL	-	-6.5			V	
Booster Drop Voltage	DDVDH drop	loading=1mA	-	-	5	%	
Gate Driver High Voltage	VGH	-	10.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	
Standby mode current consumption							
Sleep In mode	$I_{(IOVCC\ SLP\ IN)}$	Ta = 25 °C VCI=2.8V IOVCC=1.8V	-	10		uA	
	$I_{(VCI\ SLP\ IN)}$		-	10		uA	
Deep Standby mode	$I_{(IOVCC\ DSTB)}$		-	1		uA	
	$I_{(VCI\ DSTB)}$		-	1		uA	

Note:

1. Ta = -30 to 70 °C (to 85 °C no damage), IOVCC=1.65V to 3.3V, VCIP=2.5V to 3.3V.
2. Supply digital IOVCC voltage equal or less than analog VCIP voltage.
3. Source channel loading = 10pF/channel
4. The Max. Value is between with Note 3 measure point and Gamma setting value
5. VREG1OUT≦DDVDH-0.3V and VREG2OUT≧DDVDL+0.3V.

9.3. DSI DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	Low (LP)

Note: Ta=-30℃ to 70℃ (to +85℃ no damage)

9.4 DC characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage	VCI	Operating voltage	2.5	2.8	3.3	V
Digital power supply voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Analog power supply voltage noise	V_{VCI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV
		Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV
I/O power supply voltage noise	V_{IOVCC_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. These values are not symmetric amplitude, which centersm3g points are IOVCC or VCI. See examples as reference purposes, when V_{VCI_NOISE} and V_{IOVCC_NOISE} are maximums, below.

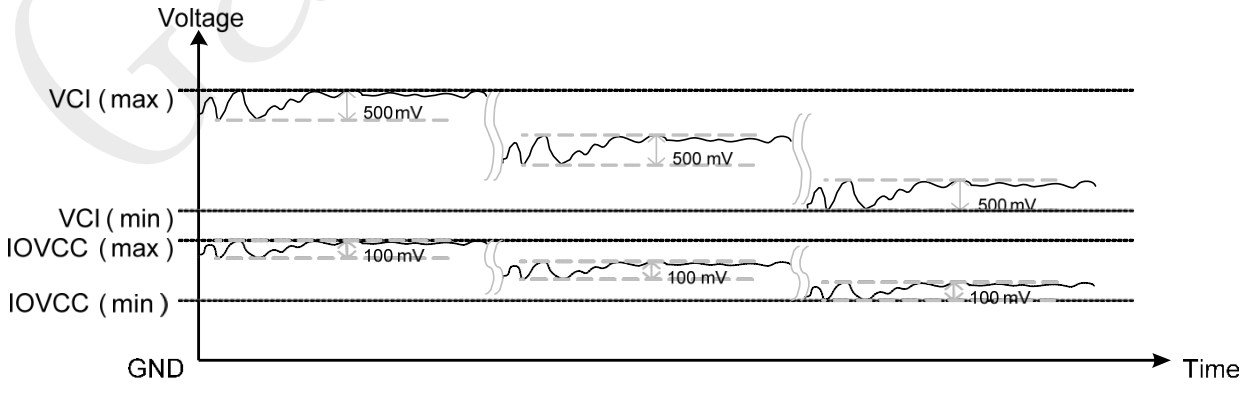


Figure 109 Noise on Power Supply Lines

9.5. DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MPU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA, Note 2	0.8 V_{VCI}	-	V_{VCI}	V
Logic Low level output voltage	V_{OL}	I_{OUT}=1mA, Note 2	0.0	-	0.2V_{VCI}	V
Logic High level input voltage	V_{IHLPCD}	LP-CD, Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD, Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1), Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1), Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (D0), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. LEDPWM
3. DSI High Speed mode is off

9.6. Spike / Glitch Rejection

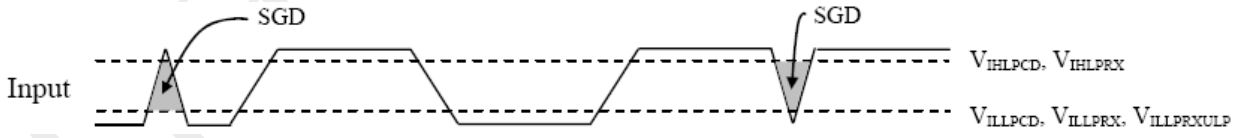


Figure 110 Spike / Glitch Rejection

Note:

1. Peak Interference Amplitude max. 200mV and Interference Frequency min. 450MHz.
2. n = 0 and 1.

Table 44 Spike / Glitch Rejection

Spike / Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-, DSI-Dn+/-	SGD	Input pulse rejection for DSI	-	300	Vps

9.7. DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLK+/- Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-Dn+/- Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLK+/- Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-Dn+/- Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLK+/-	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-Dn+/- Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLK+/-	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-Dn+/- Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLK+/-	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-Dn+/- Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/- Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6	-	-	60	pF

Note:

1. Ta = -30℃ to 70℃ (to +85℃ no damage), IOVCC = 1.65 to 1.95V.
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without VCMRCLKM450/VCMRDATAM450.
4. Without 50mV (-50mV to 50mV) ground difference.
5. n = 0 and 1.
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) is understanding that there is logical ‘1’ (HS-1) when a differential voltage is more than V_{THH} (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical ‘0’ (HS-0) when a differential voltage is more than V_{THL} (CLK-/DATA-). There is undefined state if the differential voltage is less than V_{THH} (CLK+/DATA+) and less than V_{THL} (CLK-/DATA-). A reference figure is below.

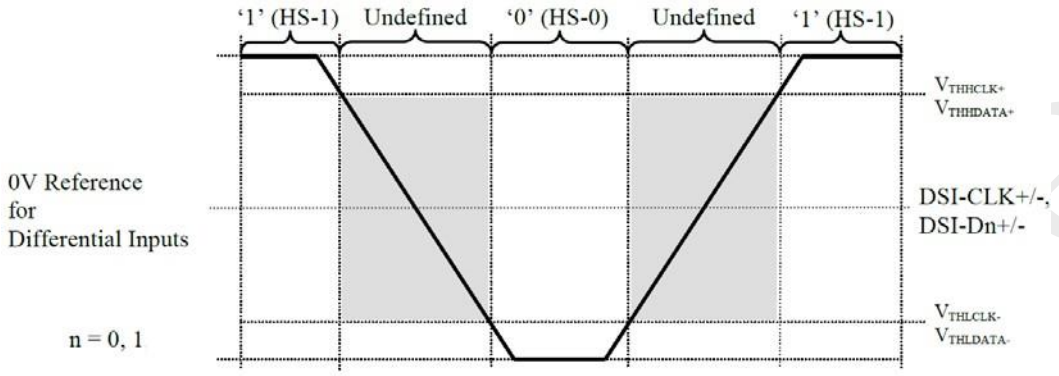
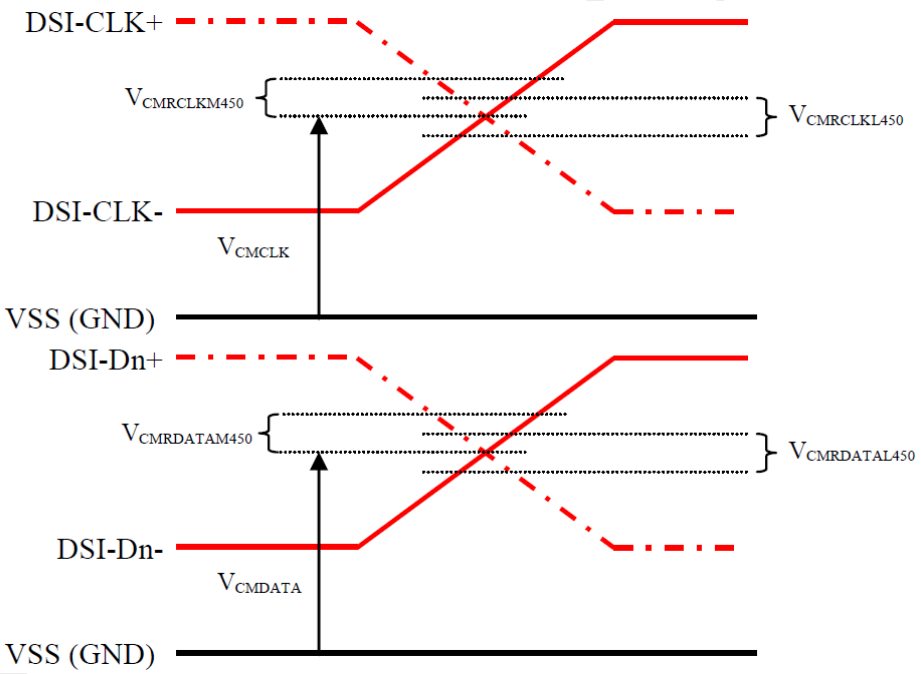


Figure 111 Differential Inputs Logical ‘0’s and ‘1’s, Threshold High/Low, Differential Voltage Range



Note: n = 0 and 1

Figure 112 Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs
  (DSI-CLK+ ∪ DSI-CLK- or DSI-D0+ ∪ DSI-D0- or DSI-D1+ ∪ DSI-D1-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs
  (DSI-CLK+ ∪ DSI-CLK- or DSI-D0+ ∪ DSI-D0- or DSI-D1+ ∪ DSI-D1-)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

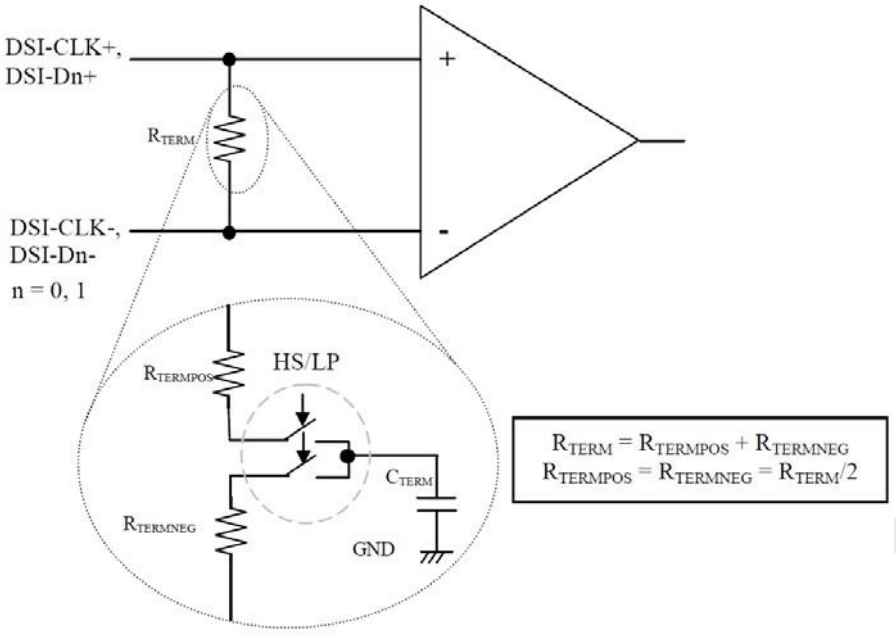
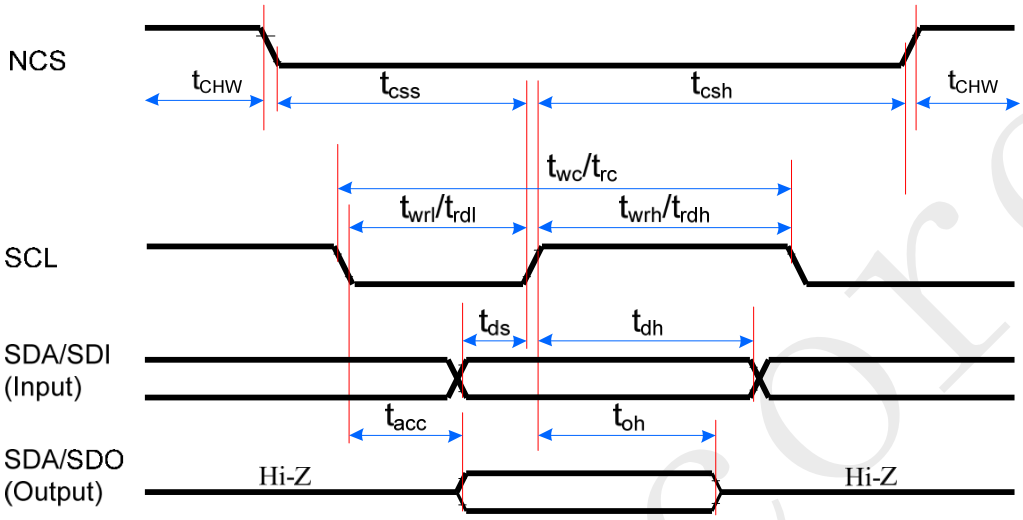


Figure 113 Differential Pair Termination Resistor on the Receiver Side

9.8. AC Characteristics

9.8.1. Display Serial Interface Timing Characteristics (3-line SPI system)

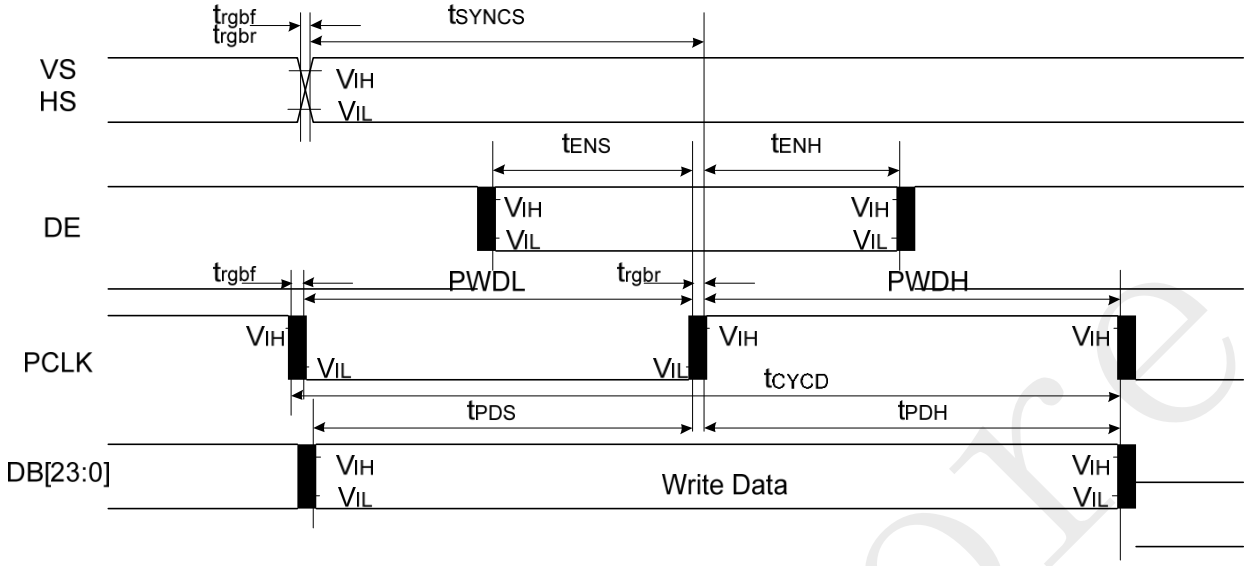


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS “H” pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL “H” pulse width (Write)	10	-	ns	
	twrl	SCL “L” pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	100	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	

Note:

1. Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, T=10+/-0.5ns.
2. Does not include signal rise and fall times.

9.8.2. Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
DB[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, DGND=0V

9.8.3. DSI Timing Characteristics

9.8.4. High Speed Mode – Clock Channel Timing

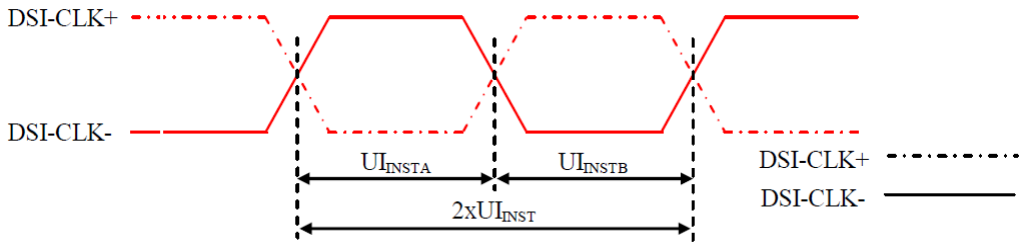


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: UI = UI_{INSTA} = UI_{INSTB}

9.8.5. High Speed Mode – Data Clock Channel Timing

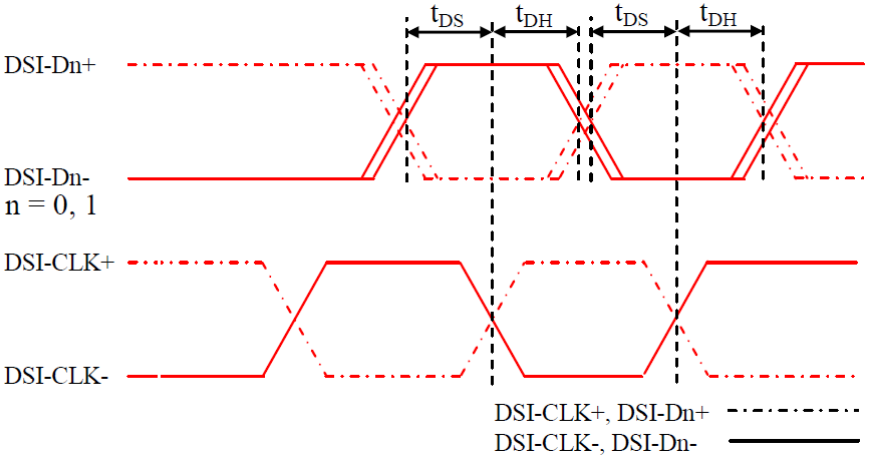


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

9.8.6 High Speed Mode – Rise and Fall Timings

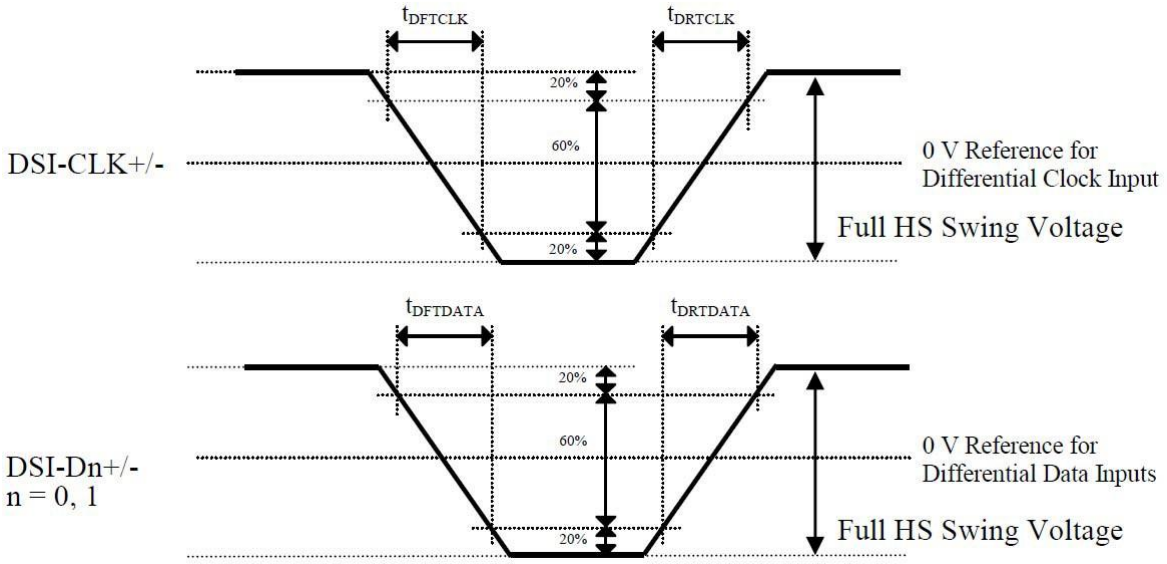


Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps

Note:The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard

9.8.7. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (GC9503V) sequence below.

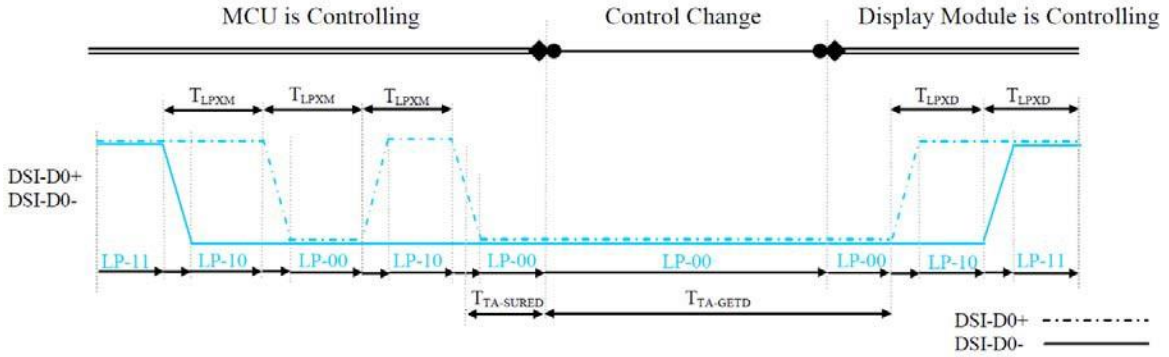


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (GC9503V) to the MPU sequence below.

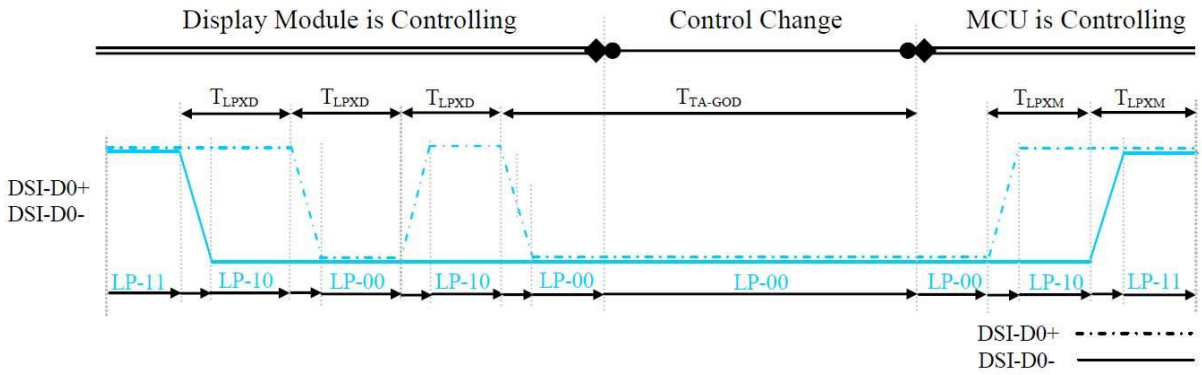


Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU ⇑ Display Module (GC9503V)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (GC9503V) ⇑ MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (GC9503V) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (GC9503V)	$5 \times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4 \times T_{LPXD}$	ns

9.8.8. Data Lanes from Low Power Mode to High Speed Mode

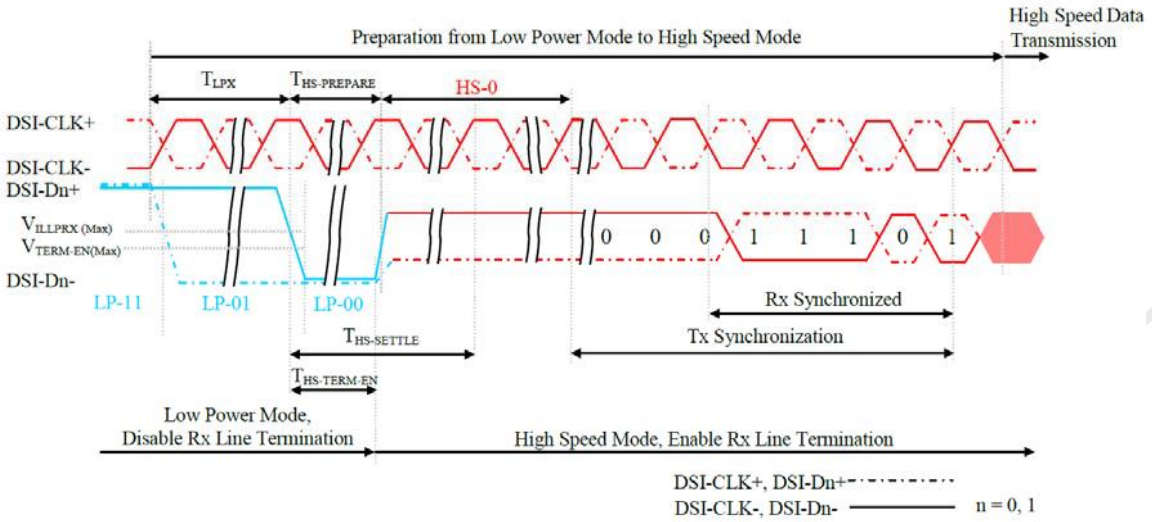


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

9.8.9. Data Lanes from High Speed Mode to Low Power Mode

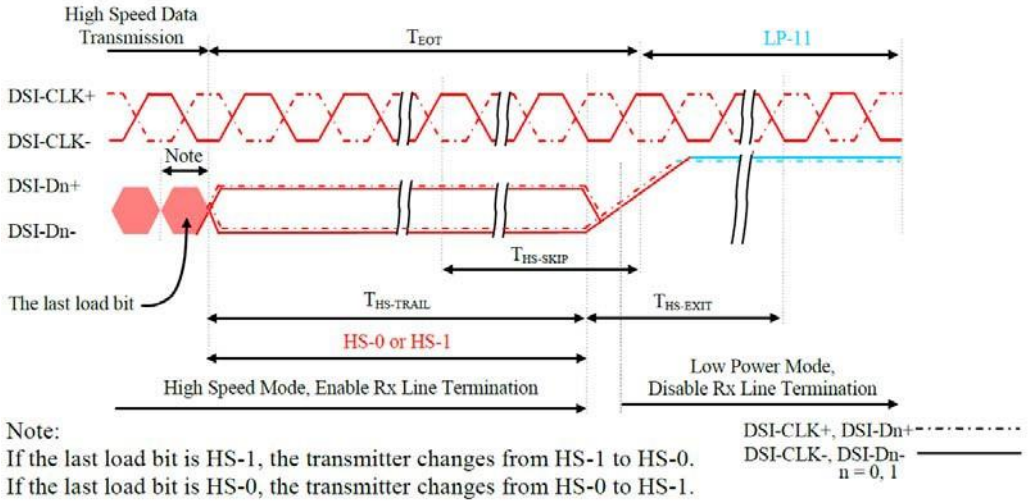


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (GC9503V) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

9.8.10. DSI Clock Burst – High Speed Mode to/from Low Power Mode

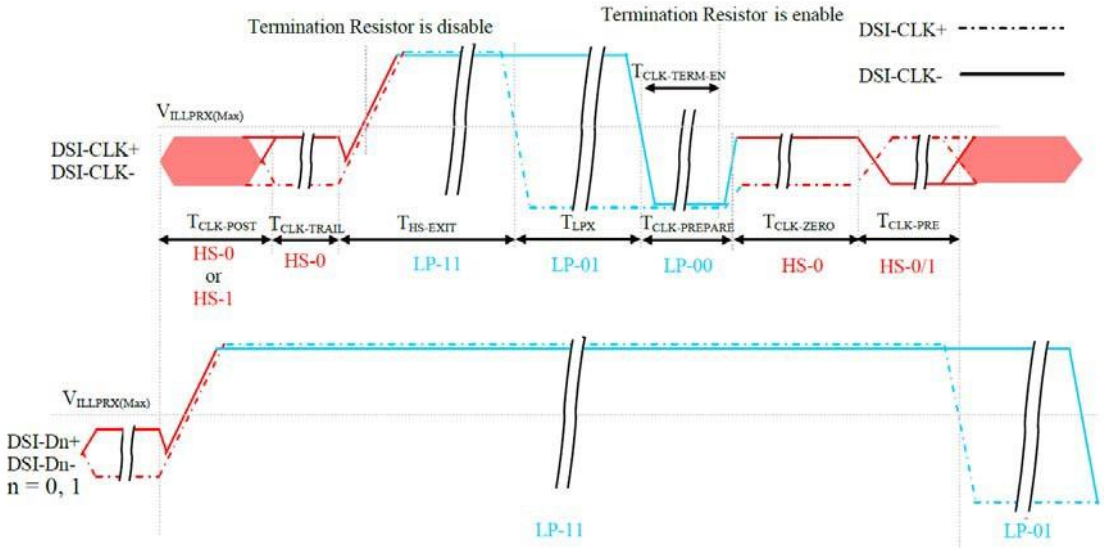


Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

10. Revision History

Version No.	Date	Page	Description
V1.00	2017/03/30	All	New created.