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JD79686AB

Data Sheet

All-in-one driver with
TCON for Color application

Version 1.0.5
2022/01/17

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All-in-one driver with TCON for Color application

1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 1-bit white/black and 1-bit red resolution output per pixel. The timing controller provides control signals for the source driver and gate drivers.

The DC-DC controller allows to generate the source output voltage VSH/VSL (+/-2.4V~+/-15V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial.

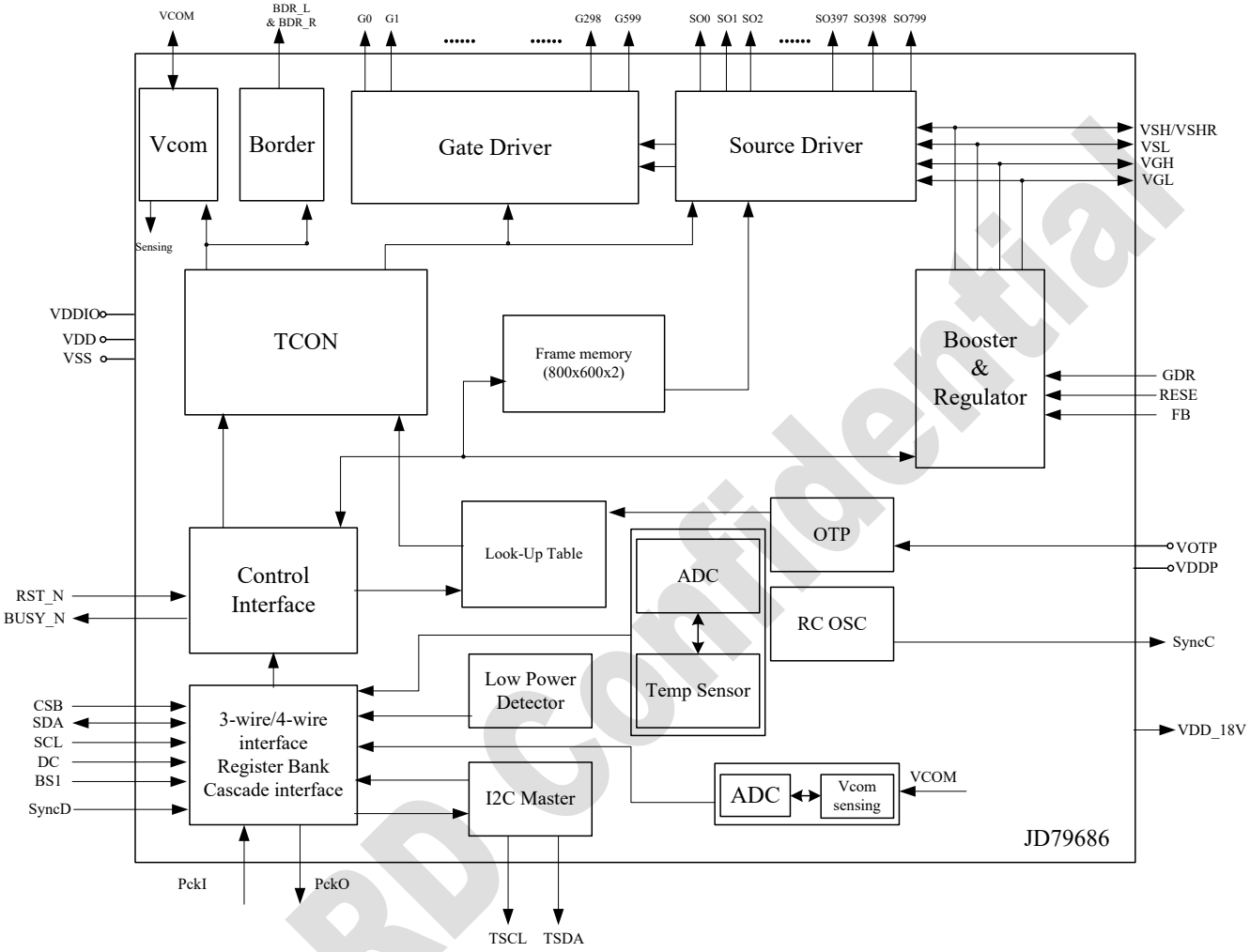
2. FEATURES

- System-on-chip (SOC) for color application
- Timing controller support several all resolution (maximum resolution 800x600)
- Support source & gate driver function:
  - 800 Outputs source driver with 1-bit white/black & 1-bit red per pixel:
    - Output dynamic range: VSH (+2.4~+15V)& VSL (-2.4~-15V) (programmable, black/white)

      VSHR: +2.4~+11V (programmable, red)
    - Output deviation: 0.1V
    - Left and Right shift capability
  - 600 Output gate driver:
    - Output dynamic range: VGH and VGL: +20V, -20V
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (6-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: (800 x 600 x 1 bit) x 2 SRAM
- Built in temperature sensor:
  - On-Chip: On-Chip: -25~50 ^{o}C ± 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}< 2.2V~2.5V)
- OCS : On-chip RC oscillator

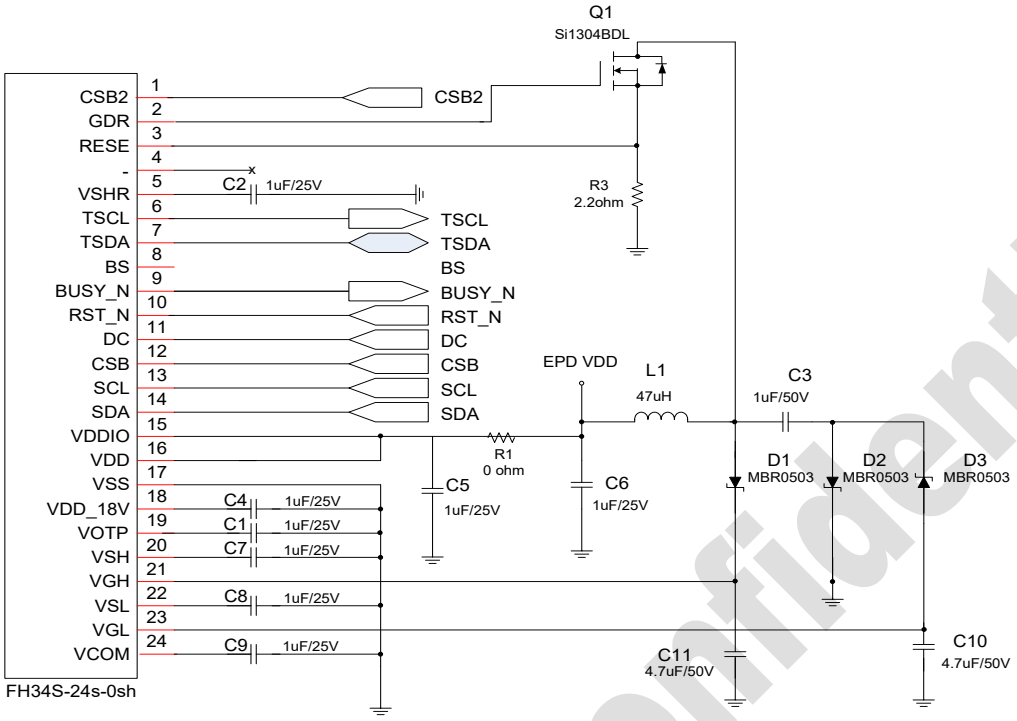
- 3-wire/4-wire (SPI) serial interface for system configuration
- Digital supply voltage: 2.3~3.6V
- OTP: 6K-byte OTP for LUT
- cascade
- Partial update
- Package-COG

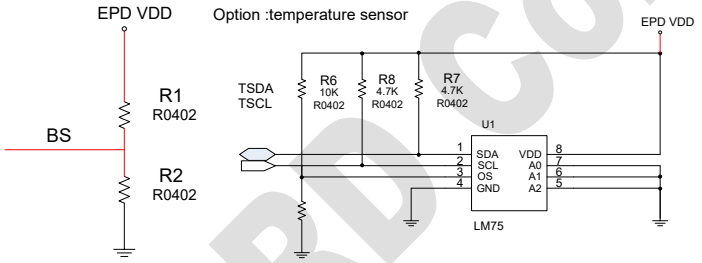
3. BLOCK DIAGRAM



4. APPLICATION CIRCUIT

4.1 power board circuit



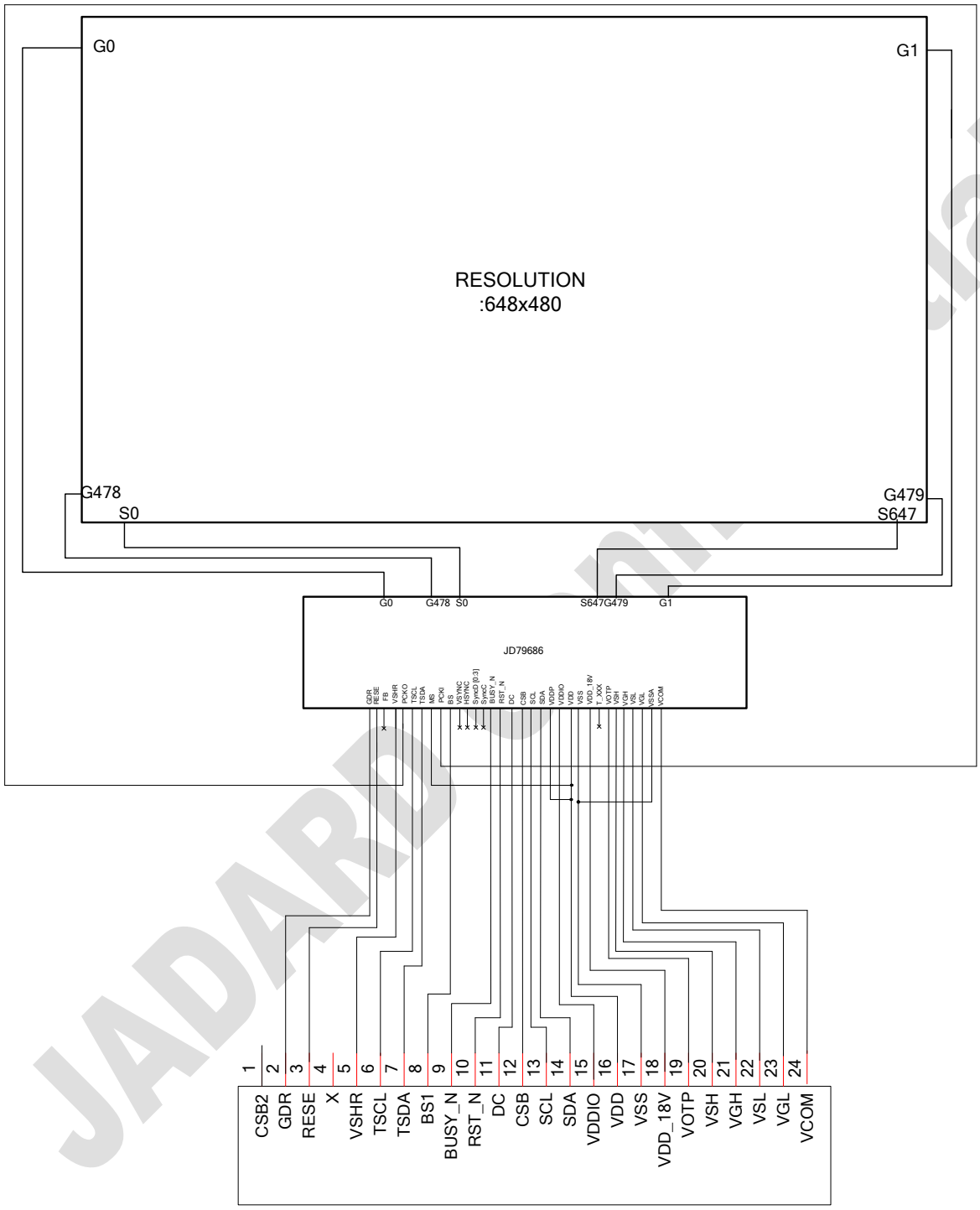


	R1	R2
3- wire SPI (CS#, SDA, SCL)	10K	NC
4-wire SPI (D/C#, CS#, SDA, SCL)	NC	10K

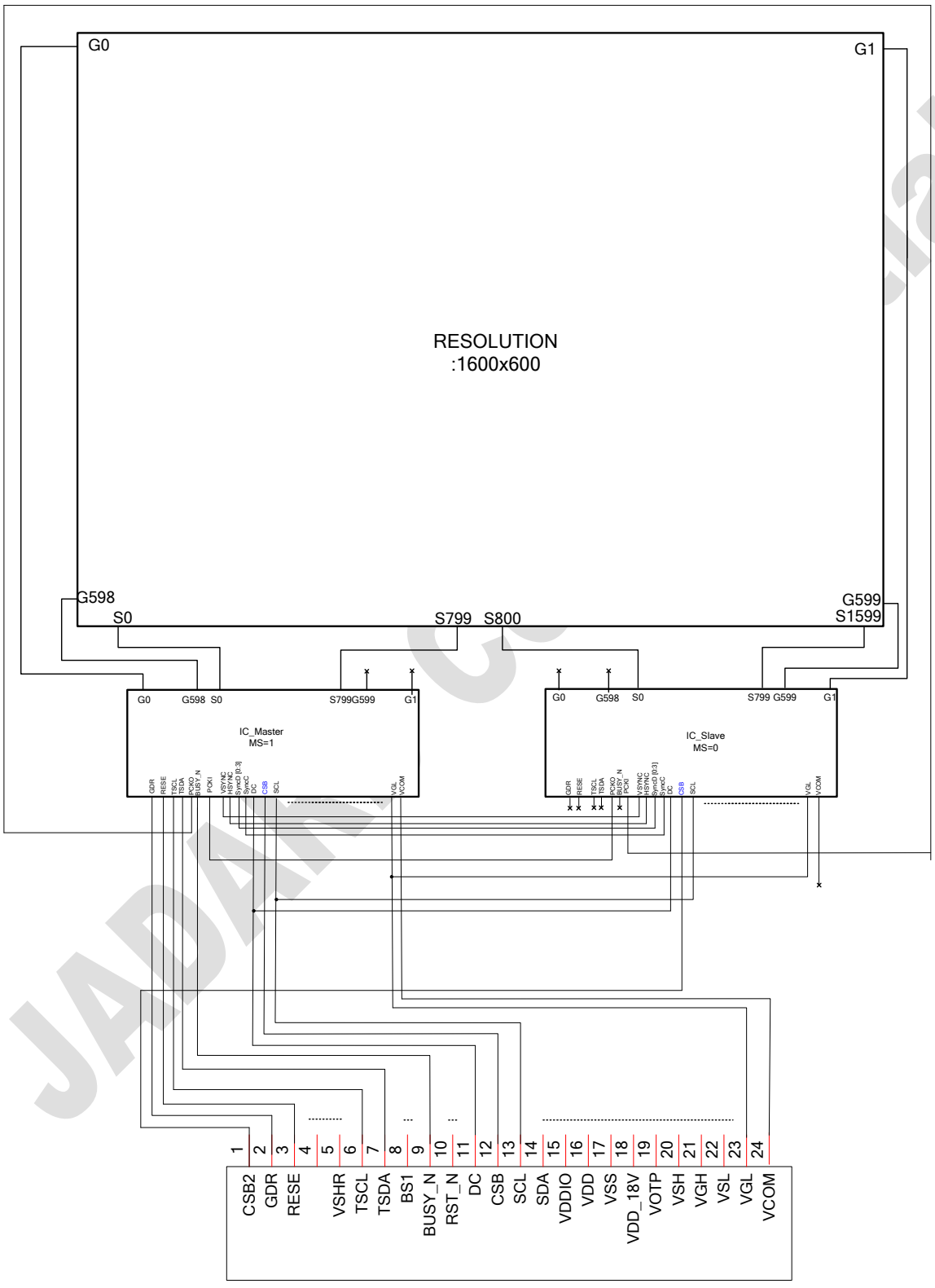
Note:

Part name	Value / Type	Requirement / Reference part
C1, C2, C4-C9	1uF	0603, X5R/X7R, Voltage Rating:25V
C3	1uF	0603, X5R/X7R, Voltage Rating:50V
C10,C11	4.7uF	0805, X5R/X7R, Voltage Rating:50V
R2	2.2Ω	0603; 1% variation
D1-D3	Diode	MBR0530 1. Reverse DC voltage ≧ 30V 2. Forward current ≧ 500mA 3. Forward voltage ≦ 430mV
Q1	NMOS	Si1308EDL / Si1304BDL 1. Drain-source break volatage ≧ 30V 2. Gate-source threshold voltage ≦ 1.5V 3. Drain-source on-state resistance < 400mΩ
L1	47uH	CDRH2D18 / LDNP-470NC 1. Maximum DC current~420Ma 2. Maximum DC resistance~650mΩ

4.2 single chip (648x480)

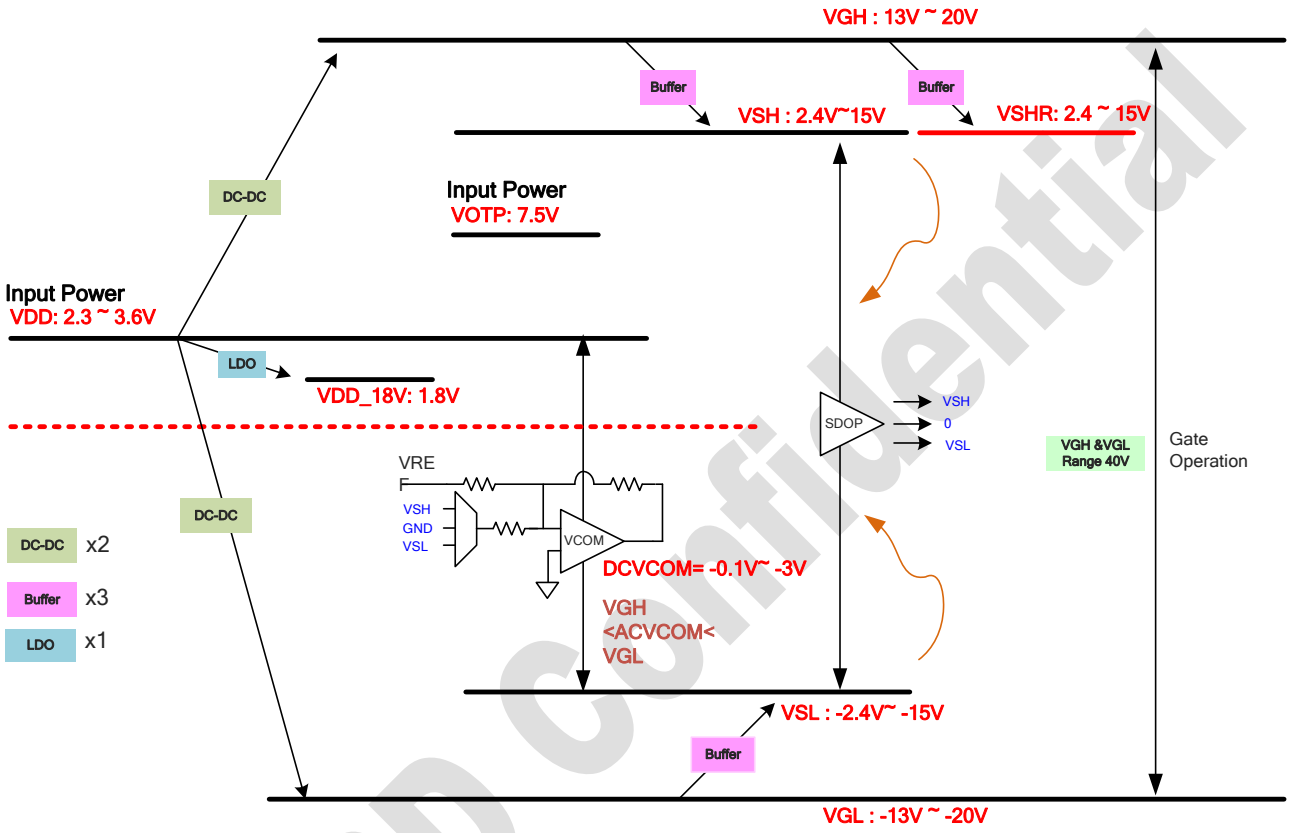


4.3 cascade mode



5. APPLICATION POWER CIRCUIT

5.1 Power Generation



6. PIN DESCRIPTION

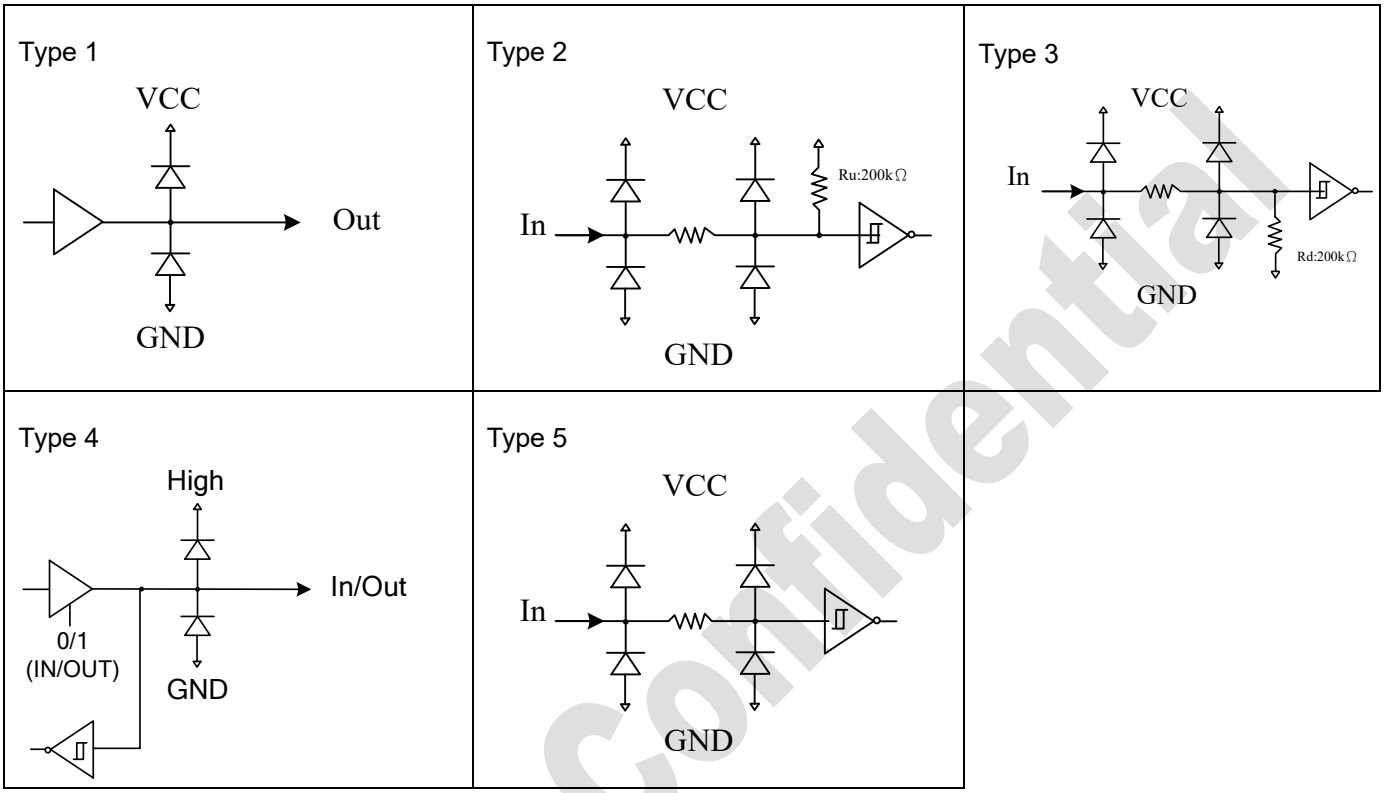
6.1 Pin define

Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 5	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 5	Serial communication clock input.
DC	I	Type 5	Serial communication Command/Data input L: Command H: data (default) Connect to VDD if BS=High.
Control Interface			
RST_N	I	Type 5	Global reset pin. Low reset. **(normal pull high)** When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will be released to floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= ”0” : Driver is busy, data/VCOM is transforming. BUSY_N= ”1” : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF(Default)
TSCL	O	Type1	I2C serial communication clock input. (I2C interface need external pull high resistance.) Must pull high or low if not used.
TSDA	I/O	Type 4	I_2C serial communication data input. (I2C interface need external pull high resistance.) Must pull high or low if not used.
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
Output Driver			
S[799:0]	O	-	Source driver output signals.
G[599:0]	O	-	Gate driver output signals..
Border			
VBD[2:1]	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (-VCM_DC) v 2. (VSH-VCM_DC) 3. (VSL-VCM_DC) v. 4. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.
FB	P	-	Keep open

Pin Name	Pin Type	I/O Structure	Description
VGH	P	Type 4	Positive gate voltage
VGL	P	Type 4	Negative gate voltage.
VSH	P	Type 4	Positive source voltage
VSL	P	Type 4	Negative source voltage.
VSHR	P	Type 4	Positive source voltage for Red
Power Supply			
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power.
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_18V	P	-	1.8V voltage input &output
VOTP	P	-	OTP program power (7.5V)
Reserved Pins			
TP [39 :0]	I/O	-	Test pin. Leave open or pull gnd if it is not used.
SyncD [3 :0]	I/O	Type 4	Cascade data signal. Leave open or pull gnd if it is not used.
SyncC	I/O	Type 4	Cascade clock signal. Leave open or pull gnd if it is not used.
PckI	I	Type 3	Break panel check input. Leave open or pull gnd if it is not used.
PckO	O	Type 1	Break panel check output. Leave open or pull gnd if it is not used.
HSYNC	I/O	Type 4	Cascade signal. Leave open or pull gnd if it is not used.
VSYNC	I/O	Type 4	Cascade signal. Leave open or pull gnd if it is not used.
m2m1_sync	I/O	Type 4	2+2 cascade Sync signal. Leave open or pull gnd if it is not used.
m1m2_sync	I/O	Type 4	2+2 cascade Sync signal. Leave open or pull gnd if it is not used.
Lsync	I/O	Type 4	2+2 cascade Sync signal. Leave open or pull gnd if it is not used.
MM	I	Type 3	2+2 cascade define pin. Leave open or pull gnd if it is not used.
T_OSCO	I/O	Type 4	Ocilator output pin. Leave open or pull gnd if it is not used.

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6.2 I/O Pin Structure



6.3 Value of wiring resistance to each pin

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VCOM	5ohm	TSDA	100ohm
VGL	5ohm	TSCL	100ohm
VSHR	5ohm	BUSY_N	100ohm
VGH	5ohm	BS	100ohm
VSH	5ohm	RESE	5ohm
VOTP	5ohm	GDR	5ohm
VDD_18V	5ohm	SDA	100ohm
VSSA	5ohm	SCL	100ohm
VDDIO	5ohm	CSB	100ohm
VSS	5ohm	DC	100ohm
VDDP	5ohm	RST_N	100ohm
VDD	5ohm	SyncD	100ohm
VSL	5ohm	SyncC	100ohm
MS	100ohm	PckI	100ohm
TP [39 :0]	100ohm	PckO	100ohm
m2m1_sync	10ohm	Lsync	10ohm
m1m2_sync	10ohm	MM	100ohm
T_OSCO	10ohm	HSYNC	10ohm
VSYNC	10ohm		

Note: Resistance of theses pins marked in yellow should be considered preferentially.

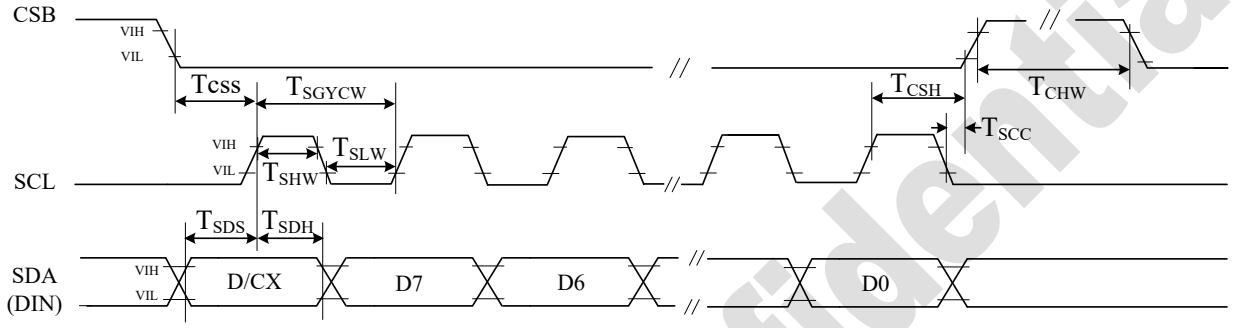
7. SPI COMMAND DESCRIPTION

7.1 "3-Wire" Serial Port Interface

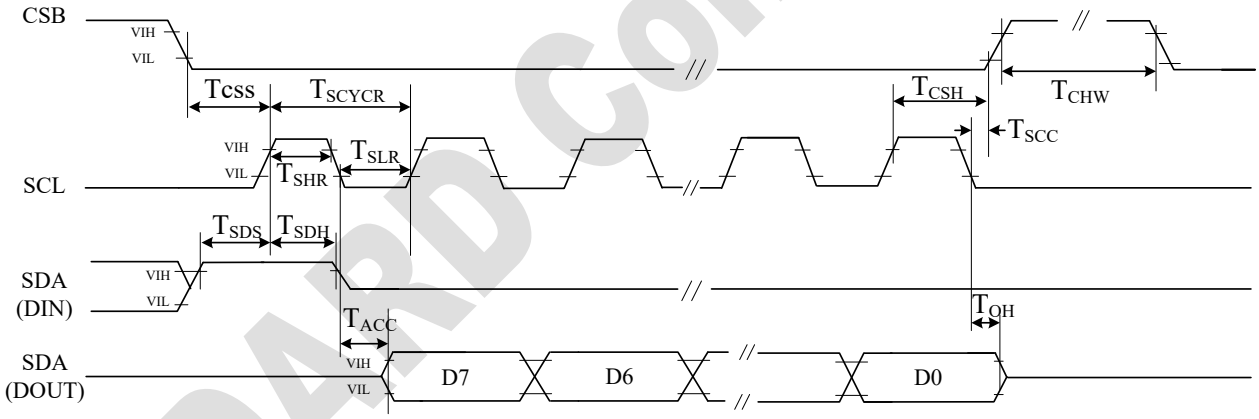
JD79686 use the 3-wire serial port as communication interface for all the function and command setting.

3-Wire communication can be bi-directional controlled by the "R/W" bit in address field. JD79686 3-Wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-Wire bus itself.

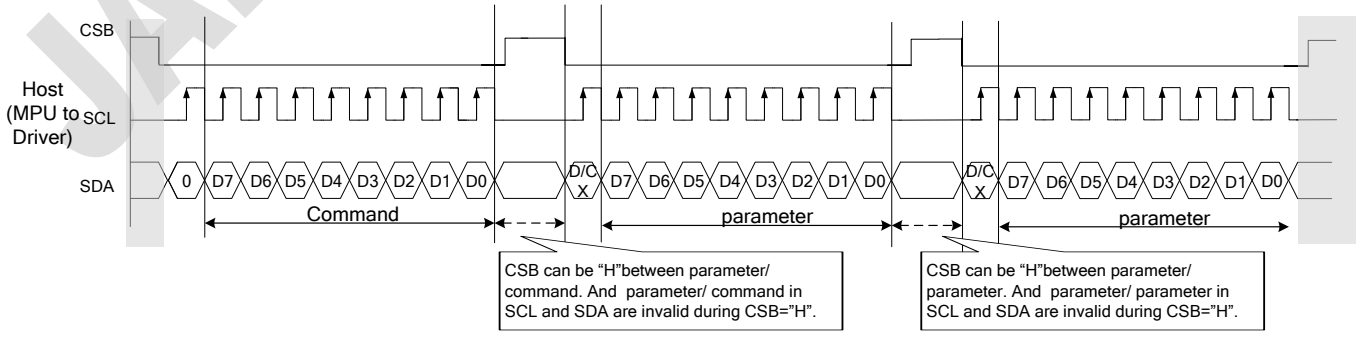
Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".



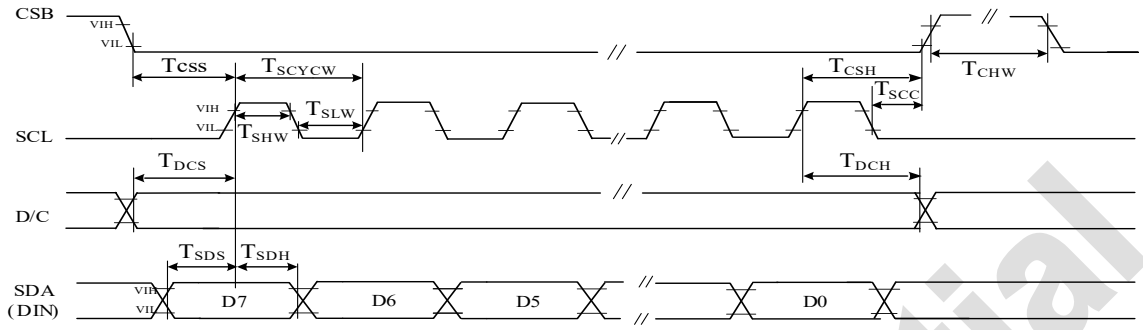
3 pin serial interface characteristics (write mode)



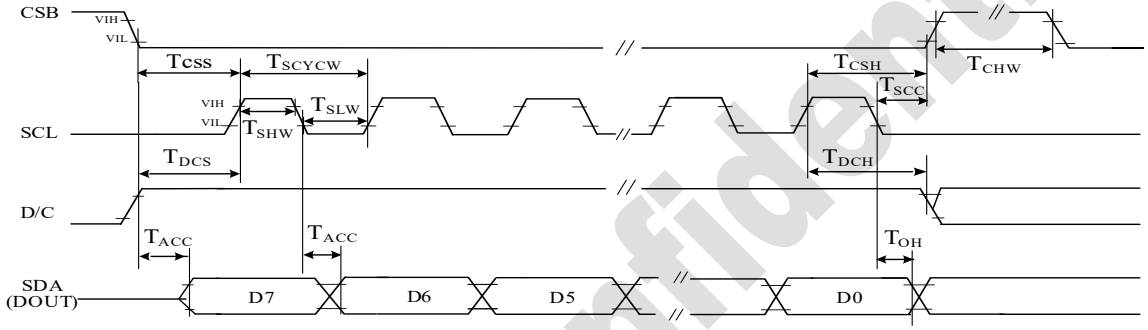
3 pin serial interface characteristics (read mode)



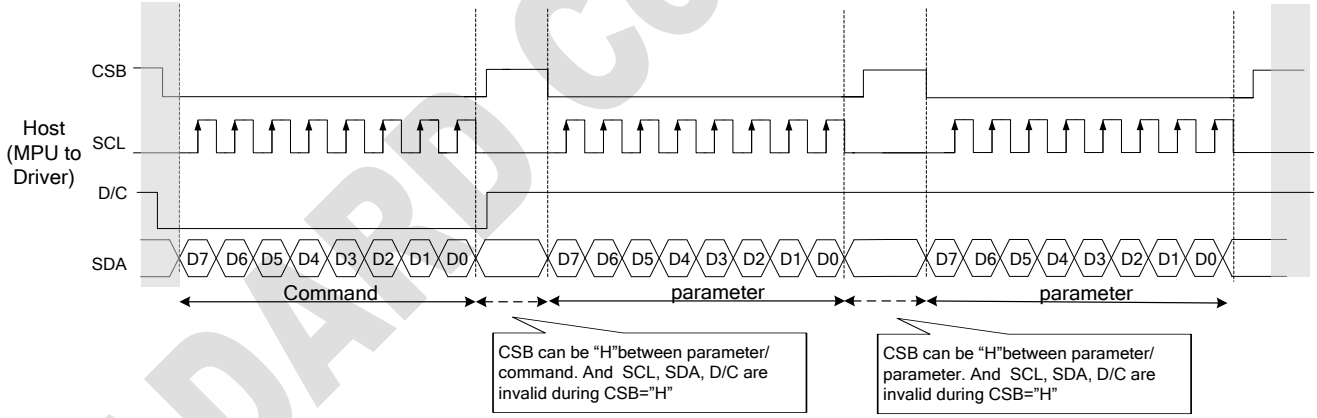
7.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics (write mode)



4 pin serial interface characteristics (read mode)



8. SPI CONTROL REGISTERS:

8.1 Register Table

Following table list all the SPI control registers and bit name definition for JD79686. Refer to the next section for detail register function description.

Address	command	Bit										
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	-00H
		W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8Fh
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
		W	1			-	-	VCOM_HV	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	00h
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	3Fh
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	3Fh
		W	1		VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	0Fh
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-	-	T_VDS_OFF [1]	T_VDS_OFF[0]					00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R05H	Power ON Measure (PMES)	W	0	0	0	0	0	0	1	0	1	05H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
		W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
		W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission1 (DTM1)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
R13H	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	1	1	13H
		W	1	#	#	#	#	#	#	#	#	00h
R14H	Partial Data Start transmission1 (PDTM1)	W	0	0	0	0	1	0	1	0	0	14H
		W	1	#	#	#	#	#	#	#	#	00h
R15H	Partial Data Start transmission 2 (PDTM2)	W	0	0	0	0	1	0	1	0	1	15H
		W	1	#	#	#	#	#	#	#	#	00h
R16H	Partial Display Refresh(PDRF)	W	0	0	0	0	1	0	1	1	0	16H
		W	1	#	#	#	#	#	#	#	#	00h
R20H	LUT for VCOM (LUT1)	W	0	0	0	1	0	0	0	0	0	20H
		W	1	#	#	#	#	#	#	#	#	00h
R21H	White to White LUT (LUTWW)	W	0	0	0	1	0	0	0	0	1	21H
		W	1	#	#	#	#	#	#	#	#	00h
R22H	Black to White LUT (LUTBW/LUTR)	W	0	0	0	1	0	0	0	1	0	22H
		W	1	#	#	#	#	#	#	#	#	00h
R23H	White to Black LUT (LUTWB/LUTW)	W	0	0	0	1	0	0	0	1	1	23H
		W	1	#	#	#	#	#	#	#	#	00h
R24H	Black to Black LUT	W	0	0	0	1	0	0	1	0	0	24H

	(LUTBB/LUTB)	W	1	#	#	#	#	#	#	#	#	00h
R25H	LUTC option	W	0	0	0	1	0	0	1	0	1	25H
		W	1							XON [9:8]		00h
		W	1	XON [7:0]								00h
		W	1							ST_CHV [9:8]		00h
		W	1	ST_CHV [7:0]								00h
R26H	Set Vcom/Red states	W	0	0	0	1	0	0	1	1	0	26H
		W	1	0	0			vcom_stg_sel[1:0]		b2w_stg_sel[1:0]		00h
R30H	OSC control (OSC)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-		M[2:0]			N[2:0]			3Ah
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	--
		R	1	D2	D1	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	-
R60H	TCON setting (TCON)	W	0	0	1	1	0	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h
		W	1	-	-	-	-	-	-	-	VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R62H	Source & gate start setting	W	0	0	1	1	0	0	0	1	0	62H
		W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	-	-	-	00h
		W	1				gscan				G_start [8]	00h
		W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	-
		R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV10]	REV[09]	REV[08]	-
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	-	PTL_flag	I^2C_ERR	I^2C_ BUSYN	Data_flag	PON	POF	BUSY_N	-
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	-
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	-	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	1Fh
RA0H	Program Mode (PGM)	W	0	1	0	1	0	0	0	0	0	A0H
		W	1	1	0	1	0	0	1	0	1	A5h
RA1H	Active program(APG)	W	0	1	0	1	0	0	0	0	1	A1H
RA2H	Read OTP Data	W	0	1	0	1	0	0	0	1	0	A2H

	(ROTP)	R	1	#	#	#	#	#	#	#	#	-
RE5H	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h
RE6H	LVD voltage Select	W	0	1	1	1	0	0	1	1	0	E6H
		W	1	-	-	-	-	-	-	LVD_SEL[1]	LVD_SEL[0]	11h
RE7H	Panel Break Check	W	0	1	1	1	0	0	1	1	1	E7H
		R	1	-	-	-		-	-	-	PSTA	-
RE8H	Power saving	W	0	1	1	1	0	1	0	0	0	E8H
		W	1	VCOM_W[3]	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00h
RE9H	AUTO sequence	W	0	1	1	1	0	1	0	0	1	E9H
		W	1	1	0	1	0	0	1	0	1	00h
REBH	OTP LUT backup1 program	W	0	1	1	1	0	1	0	1	1	EBH
RECH	Read OTP LUT backup1	W	0	1	1	1	0	1	1	0	0	ECH
		R	1	#	#	#	#	#	#	#	#	--
REDH	OTP LUT backup2 program	W	0	1	1	1	0	1	1	0	1	EDH
		R	1	#	#	#	#	#	#	#	#	--
REEH	Read OTP LUT backup2	W	0	1	1	1	0	1	1	1	0	EEH
REFH	Checksum Program to OTP	W	0	1	1	1	0	1	1	1	1	EFH
RF0H	Remap LUT	W	0	1	1	1	1	0	0	0	0	F0H
		W	1	-	-	-	bkup_lut_2_en	rmp2_table_sel[3]	rmp2_table_sel[2]	rmp2_table_sel[1]	rmp2_table_sel[0]	1Fh
		W	1	-	-	-	bkup_lut_1_en	rmp1_table_sel[3]	rmp1_table_sel[2]	rmp1_table_sel[1]	rmp1_table_sel[0]	1Fh
RF1H	Set OTP program	W	0	1	1	1	1	0	0	0	1	F1H
		W	1	-	-	-	-	-	-	LUT_bank	reg_bank	03h
RF2H	Read checksum	W	0	1	1	1	1	0	0	1	0	F2H
		R	1	#	#	#	#	#	#	#	#	00h
RF3H	Calculate Checksum	W	0	1	1	1	1	0	0	1	1	F3H

8.2 Register Description

8.2.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

Bit	Name	Description
0	RST_N	RST_N function 1 : no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. **(default)**
2	SHL	SHL function 0: Shift left; First data=Sn →Sn-1 → …→S2 →Last data=S1. 1: Shift right: First data=S1→ S2 → …→Sn-1 → Last data=Sn. **(default)**
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→ G2 → Last line=G1. 1:Scan up; First line=G1 →G2 →…→Gn-1 →Last line=Gn. **(default)**
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. **(default)** 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP**(default)** 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 00: Display resolution is 600x448 01: Display resolution is 640x480 10: Display resolution is 720x540 11: Display resolution is 800x600 (default)

Notes:

1. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.

2. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.

8.2.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
2nd Parameter	W	1	-	-	-	-	VCOM_HV	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	00h
3rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	3Fh
4th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	3Fh
5th Parameter	W	1	-	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	0Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	**Gate power selection.** 0 : External VDNS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL. (default)
1	VDS_EN	**Source power selection.** 0 : External source power from VSH/VSL pins. 1 : Internal DC/DC function for generate VSH/VSL. (default)

2nd Parameter:

Bit	Name	Description
2-0	VGHL_LV	**VGHL_LV Voltage Level.** 000: VGH=20 v, VGL=-20v (default) 001: VGH=19 v, VGL=-19v 010: VGH=18 v, VGL=-18v 011: VGH=17 v, VGL=-17v 100: VGH=16 v, VGL=-16v 101: VGH=15 v, VGL=-15v 110: VGH=14 v, VGL=-14v 111: VGH=13 v, VGL=-13v
3	VCOM_HV	**VCOM Voltage Level** 0: VCOMH=VSH+VCOMDC,VCOML=VSL+VCOMDC(default) 1: VCOMH=VGH, VCOML=VGL

3rd Parameter: Internal VSH power selection for B/W LUT. **(Default value: 111111b)**

Bit	Name	Description
5-0	**VSH**	**Internal VSH power selection.** 000000: 2.4 v 000001: 2.6 v 000010: 2.8 v 000011: 3.0 v …. 010111: 7.0V

		011000: 7.2 V 011001: 7.4 V …. 111010: 14.0V 111011: 14.2 V 111100: 14.4V 111101: 14.6V 111110: 14.8V 111111: 15.0V

4th Parameter: Internal VSL power selection for B/W LUT. **(Default value: 111111b)**

Bit	Name	Description
5-0	**VSL**	**Internal VSL power selection.** 000000: -2.4 v 000001: -2.6 v 000010: -2.8 v 000011: -3.0 v …. 010111: -7.0V 011000: -7.2 V 011001: -7.4 V …. 111010 :-14.0V 111011: -14.2 V 111100: -14.4 V 111101: -14.6V 111110: -14.8V 111111: -15.0V

5th Parameter: Internal VSHR power selection for Red LUT. **(Default value: 00001111b)**

Bit	Name	Description
6-0	**VSHR**	**Internal VSL power selection.** 0000000: 2.4 v 0000001: 2.5 v 0000010: 2.6 v 0000011: 2.7 v …. 0101110: 7.0 V 0101111: 7.1 V 0110000: 7.2 V …. 1010001: 10.5V 1010010: 10.6 V 1010011: 10.7 V 1010100: 10.8V 1010101: 10.9V 1010110: 11.0V

Note:
1.VSH>VSHR

Restriction	

8.2.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will keep floating.
Restriction	

8.2.4 R03H (PFS): Power off Sequence Setting Register

R03H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PFS	W	0	0	0	0	0	0	0	1	1	03H
1st Parameter	W	1	-	-	Vsh_off[1]	Vsh_off [0]	Vsl_off[1]	vsl_off[0]	vshr_off[1]	vshr_off[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :
1st Parameter:

Bit	Name	Description
1-0	**vshr_off**	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
3-2	**vsl_off**	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms
5-4	**vsh_off**	00: 5ms. (default) 01: 10ms 10: 20ms 11: 40ms

Restriction

8.2.5 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power off sequence, BUSY_N signal will rise from low to high.
Restriction	

8.2.6 R05H (PMES): Power ON Measure Command

R05H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PMES	W	0	0	0	0	0	0	1	0	1	05H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).
Restriction	

8.2.7 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17h
2nd Parameter	W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17h
3rd Parameter	W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
2-0	**Driving strength of phase A**	000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase A**	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

2nd Parameter:

Bit	Name	Description
2-0	**Driving strength of phase B**	000: period1 001: period2 010: period3 011: period4 100: period5 101: period6 110: period7 111: period8
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase B**	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

<table>
<tr><td>Description</td><td>3rd Parameter:

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>2-0</td><td>Minimum OFF time setting of GDR in phase C</td><td>000: period1
001: period2
010: period3
011: period4
100: period5
101: period6
110: period7
111: period8</td></tr>
<tr><td>5-3</td><td>Driving strength of phase C</td><td>000: Strength 1
001: Strength 2
010: Strength 3 (default)
011: Strength 4
100: Strength 5
101: Strength 6
110: Strength 7
111: Strength 8</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

8.2.8 R07H (DSLP): Deep Sleep

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	

8.2.9 R10H (DTM1): Data Start transmission 1 Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
...	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. In Program mode, this command writes "OTP" data to SRAM for programming.
Restriction	

8.2.10 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter: Bit / Name / Description 7 / -- / 0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data. After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = "1".

8.2.11 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0".
Restriction	This command only actives when BUSY_N = "1".

8.2.12 R13H (DTM2): Data Start transmission 2 Register

R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
...	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

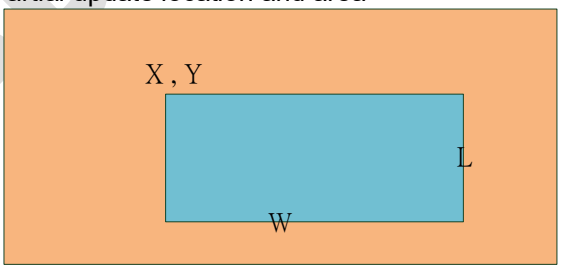
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM.
Restriction	

8.2.13 R14H (PDTM1): Partial Data Start transmission 1 Register

R14H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM1	W	0	0	0	0	1	0	1	0	0	14H
1st Parameter									X[9]	X[8]	
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter									Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	00h
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

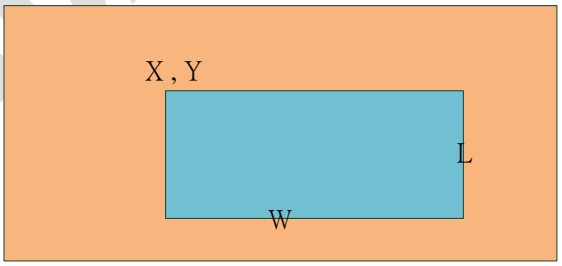
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

8.2.14 R15H (PDTM2): Partial Data Start transmission 2 Register

R15H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM2	W	0	0	0	0	1	0	1	0	0	15H
1st Parameter									X[9]	X[8]	
2nd Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter									Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	00h
8th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
9th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

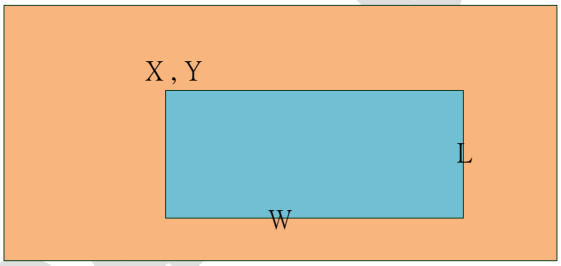
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM. Partial update location and area  Note: X and W should be the multiple of 8.
Restriction	

8.2.15 R16H (PDRF): Partial Display Refresh Command

R16H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDRF	W	0	0	0	0	1	0	1	1	0	16H
1st Parameter	W	1	DFV_EN						X[9]	X[8]	00h
2nd Parameter			X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
3rd Parameter	W	1							Y[9]	Y[8]	00h
4th Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
5th Parameter									W[9]	W[8]	00h
6th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
7th Parameter									L[9]	L[8]	
8th Parameter			L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: While user sent this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. Only the area (X,Y, W, L) would update, the others pixel output would follow VCOM LUT After display refresh command, BUSY_N signal will become "0".  Note: X and W should be the multiple of 8. DFV_EN: data follow VCOM function on display area. DFV_EN=1: Only effective in B/W mode, if pixel from "New data" SRAM equal to "Old data" SRAM on display area, this pixel output would follow VCOM LUT. DFV_EN=0: Data doesn't follow VCOM LUT.
Restriction	this command only active when BUSY_N = "1".

8.2.16 R20H (LUTC): LUT for Vcom

R20H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~13th Parameter	W	1	2nd state								00h
….	W	1	3rd ~9th state								00h
55th ~60h Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This register is set for VCOM LUT. This command stores VCOM Look-Up Table with 10 states of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat. If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG) If BWR=1 (BW mode), only 7 groups are used.
Restriction	- This command only actives when BUSY_N = "1".

define	description
Level selection [1:0]	00: -VCM_DC 01: VSH+VCM_DC. 10: VSL+VCM_DC. 11: Floating.
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame … 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 00000001: 1 … 11111110: 254 11111111: 255

8.2.17 R21H (LUTWW): White to White LUT Register

R21H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWW	W	0	0	0	1	0	0	0	0	1	21H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	- This command only actives when BUSY_N = "1".

8.2.18 R22H (LUTBW/LUTR): Black to White LUT or Red LUT Register

R22H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBW/LUTR	W	0	0	0	1	0	0	0	1	0	22H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~9th state								00h
55th ~60th Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

- The command defines as:

This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG)
If BWR=1 (BW mode), only 7 groups are used.

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction

- This command only actives when BUSY_N = "1".

8.2.19 R23H (LUTWB/LUTW): White to Black LUT or White LUT Register

R23H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWB/LUTW	W	0	0	0	1	0	0	0	1	1	23H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	- This command only actives when BUSY_N = "1".

8.2.20 R24H (LUTBB/LUTB): Black to Black LUT or Black LUT Register

R24H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBB/LUTB	W	0	0	0	1	0	0	1	0	0	24H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

define	description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	- This command only actives when BUSY_N = "1".

8.2.21 R25H (LUTC Option): LUTC option

R25H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC option	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1							XON [9:8]		00h
2nd Parameter	W	1	XON [7:0]								00h
3rd Parameter	W	1							VCOM_H [9:8]		00h
4th Parameter	W	1	VCOM_H [7:0]								00h

NOTE: "-" Don't care, can be set to VDD or GND level

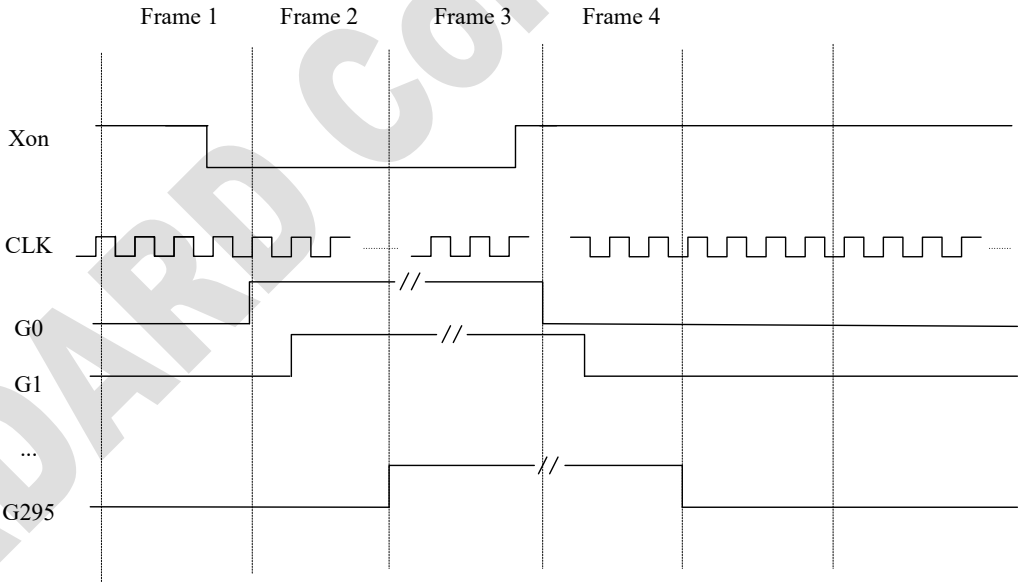
Description

-The command defines as:

This register is set for VCOM LUT.

XON[9:0]	All Gate ON 0000000000: No all gate on. 0000000001: State1 gate power on 1111111111: State1~10 all gate power on
VCOM_H[9:0]	Control VCOM Power as High 0000000000: No VCOM High voltage 0000000001: State1 VCOM High voltage …. 1111111111: State1~10 VCOM High voltage

Xon function:



Restriction

- This command only actives when BUSY_N = "1".

8.2.22 R26H (SET_STG): Set VCOM/Red States

R26H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_STG	W	0	0	0	1	0	0	1	1	0	H
1st Parameter	W	1			-	-	vcom_stg_sel[1:0]		b2w_stg_sel[1:0]		00h

Description	This command is used to set VCOM/Red LUT states Function of vcom_stg_sel [1:0]/ b2w_stg_sel[1:0] are shown below Value / Stages 00 / 7 01 / 8 10 / 9 11 / 10 Default is set as 7 stages.
Restriction	These settings are valid for BWR mode.

8.2.22 R30H (OSC): OSC control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
OSC	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	M[2:0]			N[2:0]			3Ch

NOTE: "-" Don't care, can be set to VDD or GND level

Description

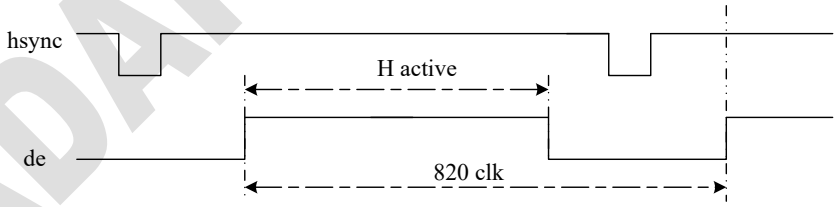
-The command defines as:

The command controls the OSC clock frequency. The OSC structure must support the following frame rates:

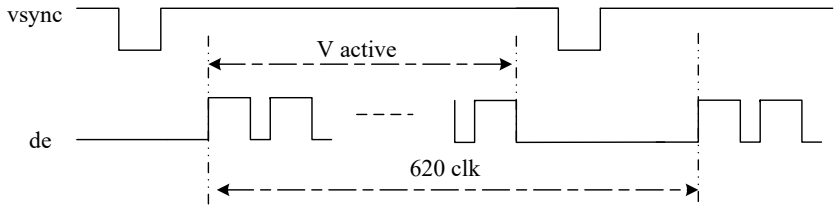
M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ (default)
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

remark

-Horizental



-Vertical



Restriction

8.2.23 R40H (TSC): Temperature Sensor Command

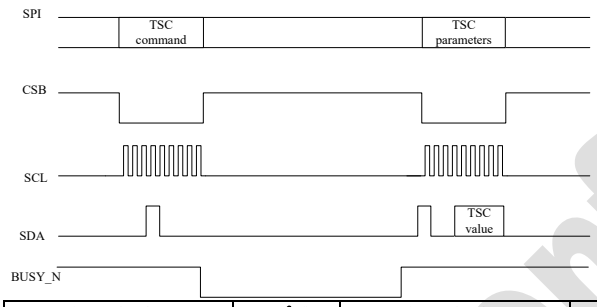
R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2	D1	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:
This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.
If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.24 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the driver IC temperature sensor enable and calibration function. **Bit** / **temperature** 2-0: mean temperature offset value 000:0℃ 001:1℃ 010:2℃ …. 111:7℃ 3: Positive and negative value 0:"+" 1: "-" 7: **Internal temperature sensor enable** 0: Internal temperature sensor enable.(**default)** 1: Internal temperature sensor disable, using external temperature sensor. For example: 1100: - 4 degree c 0111: + 7 degree c
Restriction	This command only actives after R04H(PON) or R05H(PMES)

8.2.25 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	temperature
2-0	Pointer setting
5-3	User-defined address bits (A2, A1, A0)
7-6	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	temperature
7-0	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	temperature
7-0	LSByte of write-data to external temperature sensor

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.26 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

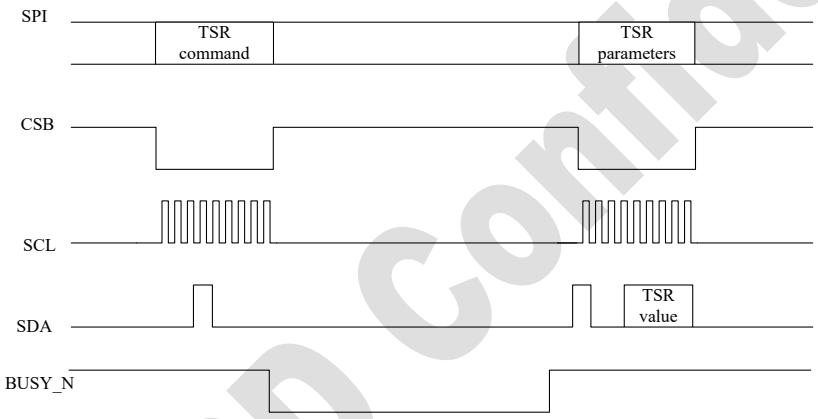
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	temperature
7-0	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	temperature
7-0	LSByte of write-data from external temperature sensor



Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.27 R50H (CDI): VCOM and DATA interval setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h

NOTE: "-" Don't care, can be set to VDD or GND level

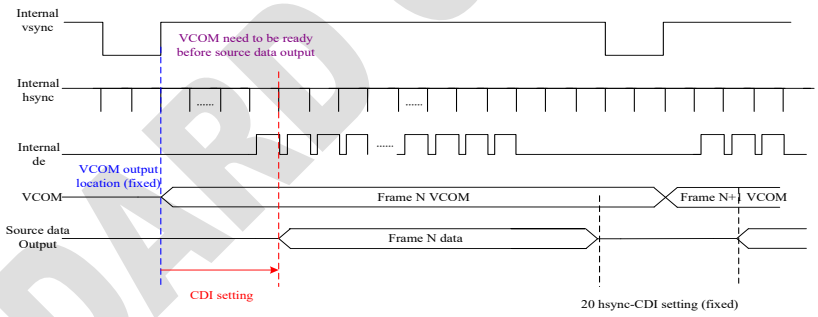
Description

-The command defines as:

1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit	
3-0	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[1:0] Border data selection.

B/W/Red mode(BWR=0)

Bit 5-4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11 (default)	Floating

B/W mode (BWR=1)

Bit 5-4	Bit7-6	description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
1 (default)	00	Floating
	01	LUTWB (1->0)
	10	LUTBW (0->1)
	11	Floating

DDX[1:0]: Data polarity
1. DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
2. DDX[0] for B/W mode

B/W/Red mode(BWR=0)

Bit 5-4	Description	
DDX[1:0]	Data (Red, B/W)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

Bit 5-4	Description	
DDX[0]	Data (New,Old)	LUT
0	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
1 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

8.2.28 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE6H (LVSEL)). 1st Parameter: Bit 0 | LPD 0 | Low power input. 1 | Normal status.
Restriction	

8.2.29 R60H (TCON): TCON setting

R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	00h

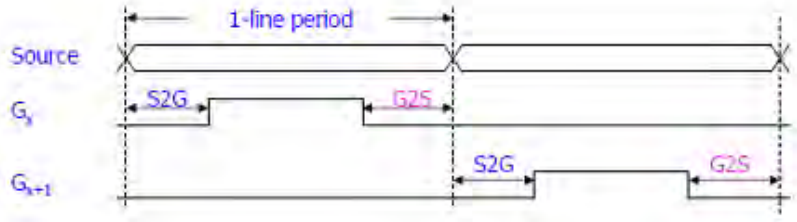
NOTE: "-" Don't care, can be set to VDD or GND level

Description

- The command define Non-overlap period of gate and source as below:
  1st Parameter:

Bit	Period
S2G[3:0]/G2S[3:0]	0000: 2 clock(default) 0001: 4 clock 0010: 6 clock 0011:8 clock 0100: 10 clock 0101: 12 clock 0110: 14 clock 0111: 16 clock 1000: 18 clock 1001: 20 clock 1010: 22 clock 1011: 24 clock 1100: 26 clock 1101: 28 clock 1110: 40 clock 1111: 32 clock

Period=660ns



1 line times=1 frame times/620 line(max.gate(600 lines)+fix blanking(20 lines)
Gate on time= 1 line times-gate off time(S2G+G2S times)

Restriction

8.2.30 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1							HRES(9)	HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h
3th Parameter	W	1							VRES(9)	VRES(8)	ooh
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution = HRES Vertical display resolution = VRES Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]*8-1 EX :128X272 GD: First G active = G0 LAST active GD= 0+272-1= 271; (G271) SD : First active channel: =S0 LAST active SD=0+16*8-1=127; (S127)
Restriction	

8.2.31 R62H (TSGS): Source & gate start setting

R62H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSGS	W	0	0	1	1	0	0	0	1	0	62H
1st Parameter	W	1							S_Start (9)	S_Start (8)	00h
2nd Parameter	W	1	S_Start (7)	S_Start (6)	S_Start (5)	S_Start (4)	S_Start (3)	-	-	-	00h
3th Parameter	W	1				gscan			G_Start (9)	G_Start (8)	ooh
4th Parameter	W	1	G_Start (7)	G_Start (6)	G_Start (5)	G_Start (4)	G_Start (3)	G_Start (2)	G_Start (1)	G_Start (0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line 3. gscan :Gate scan select 0: Normal scan 1: Cascade type 2 scan
Restriction	S_Start should be the multiple of 8

8.2.32 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	-
2nd Parameter	R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: The LUT_REV is read from OTP address = 0x001.& 0x002
Restriction	- This command only actives when BUSY_N = "1".

8.2.33 R71H (FLG): Status register

R71H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
FLG	W	0	0	1	1	1	0	0	0	1	71H
1st Parameter	R	1	-		I2C_ERR	II2C_BUSYN	Data_flag	PON	POF	BUSY_N	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the IC status. Host can read this data to understand the IC status. 1st Parameter:

Bit	Function
5	I2C master error status
4	I2C master busy status (low active)
3	Driver has already received one frame data
2	PON 0: Not in PON mode 1: In PON mode
1	POF 0: Not in POF mode(default) 1: In POF mode
0	Driver busy status(low active)

Restriction	User can send this command in any time. It doesn't have restriction of BUSY_N.

8.2.34 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80 H
1st Parameter	W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Function
0	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSHR during Auto Measure VCOM period.
3	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	The sensing time of VCOM detection 00: 3s 01: 5s (default) 10: 8s 11: 10s

Restriction

This command only actives when BUSY_N = "1".

8.2.35 R81H (VV): Vcom Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	(81H)
1st Parameter	R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command could get the Vcom value 1st Parameter: Bit: 5-0 — Function: Vcom value 000000: -0.1V 000001:-0.15V 000010:-0.2V …. 111000:-2.9V 111001:-2.95V 111010:-3.0V
Restriction	This command only actives when BUSY_N = "1".

8.2.36 R82H (VDCS): Vcom_DC Setting register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	-	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	1Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command set the VCOM DC value. Driver will base on this value for VCM_DC. 1st Parameter:

Bit	Function
5-0	**VCOM value** 000000: -0.1V 000001:-0.15V 000010:-0.2V …. 111000:-2.9V 111001:-2.95V 111010:-3.0V

Restriction	This command only actives when BUSY_N = "1".

8.2.37 RA0H (PGM): Program Mode

RA0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	1	0	0	0	0	0	A0H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset. The only one parameter is a check code, the command would be executed if check code = 0xA5.
Restriction	This command only actives when BUSY_N = "1".

8.2.38 RA1H (APG): Active Program

RA1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	1	0	0	0	0	1	A1H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

8.2.39 RA2H (ROTP): Read OTP Data

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
ROTP	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the OTP								-
3rd Parameter	R	1	The data of address 0x001 in the OTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the OTP								-
6th~ (m-1)th Parameter	R	1	.....								-
mth Parameter	R	1	The data of address (n) in the OTP								-

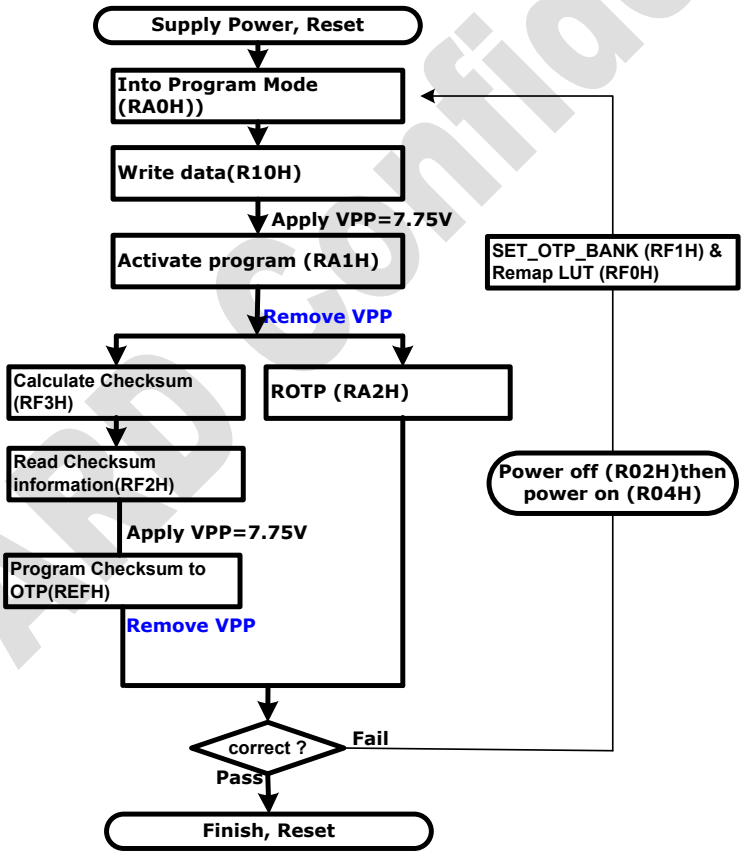
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.



The sequence of programming OTP

Restriction

This command only actives when BUSY_N = "1".

8.2.40 RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade. 1st Parameter: **Bit** 0: Output clock enable/disable. 0: Output 0V at CL pin. (default) 1: Output clock at CL pin for slave chip. 1: Let the value of slave's temperature is same as the master's. 0: Temperature value is defined by internal temperature sensor / external LM75. (default) 1: Temperature value is defined by TS_SET [7:0] registers.
Restriction	This command only actives when BUSY_N = "1".

8.2.41 RE5H (TSSET): Force Temperature

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command is used to fix the temperature value of master and salve
Restriction	

8.2.42 RE6H (LVSEL): LVD voltage Select

RE6H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Select LVD Voltage	W	0	1	1	1	0	0	1	1	0	E6H
1st Parameter	W	1							LVD_SEL[1]	LVD_SEL[0]	11h

Description	LVD_SEL[1:0]: Low power Voltage selection LVD_SEL[1:0] / LVD value 00 / < 2.2 V 01 / < 2.3 V 10 / < 2.4 V 11 / < 2.5 V
Restriction	

8.2.43 RE7H (PBC): Panel Break Check

RE7H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Select LVD Voltage	W	0	1	1	1	0	0	1	1	1	E7H
1st Parameter	R	1								PSTA	-

Description	This command is used to enable panel check, and to disable after reading result. 1st Parameter:
Restriction	

Bit	PSTA
0	Panel check fail (panel broken).
1	Panel check pass

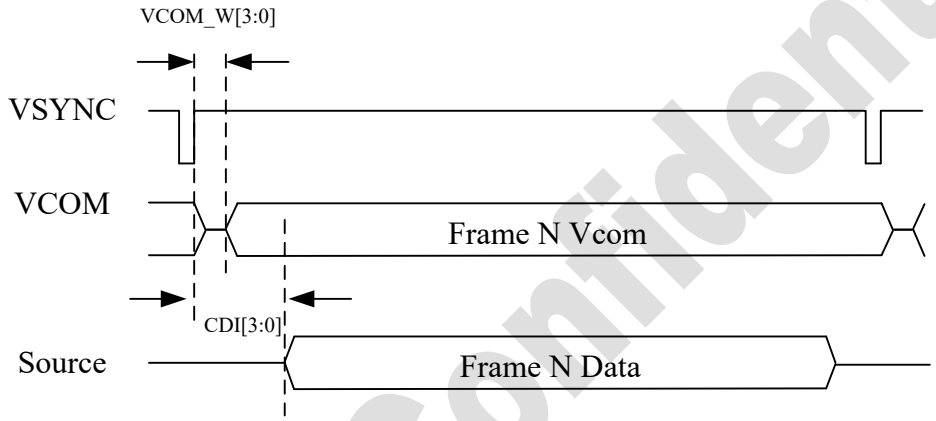
8.2.44 RE8H (PWS): Power Saving

RE8H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Power Saving	W	0	1	1	1	0	1	0	0	0	E8H
1st Parameter	W	1	VCOM_W[3]	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00h

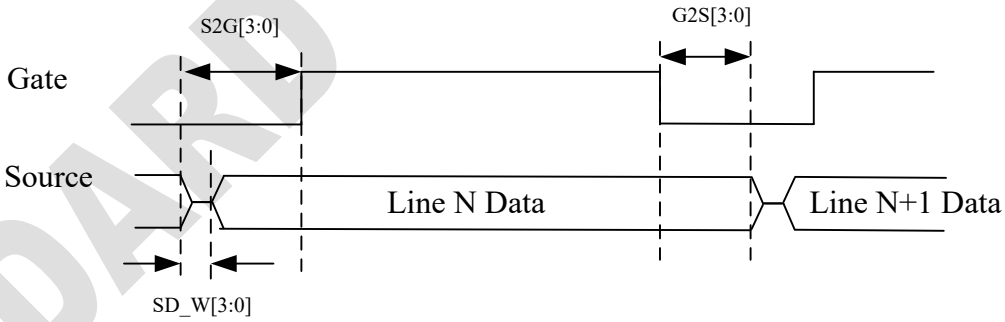
Description

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.1st Parameter:

Vcom_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



Restriction

8.2.45 RE9H (AUTO): AUTO Sequence

RE9H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AUTO Sequence	W	0	1	1	1	0	1	0	0	1	E9H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	00h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0xE9) + Code(0xA5) = (PON->DRF->POF) AUTO (0xE9) + Code(0xA7) = (PON->DRF->POF->DSLP)
Restriction	

`

8.2.46 REBH (LUT_BACKUP1_PG): OTP LUT backup1 program

REBH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP1_PG	W	0	1	1	1	0	1	0	1	1	EBH

NOTE: "-" Don't care, can be set to VDD or GND level

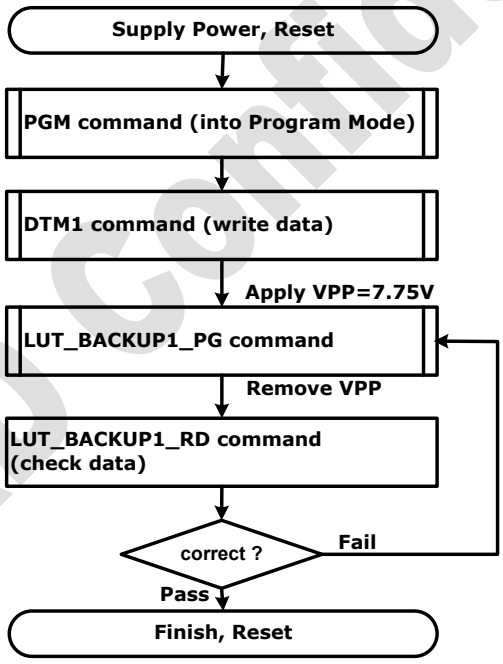
Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

8.2.47 RECH (LUT_BACKUP1_RD): Read OTP LUT backup1

RECH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP1_RD	W	0	1	1	1	0	1	1	0	0	ECH
1st Parameter	R	1	Dummy								
2nd Parameter	R	1	The data of address 0xA00/0x1600 in the OTP								
3rd Parameter	R	1	The data of address 0xA01/0x1601 in the OTP								
4th Parameter	R	1	The data of address 0xA02/0x1602 in the OTP								
5th Parameter	R	1	The data of address 0xA03/0x1603 in the OTP								
6th~ 256th Parameter	R	1	…..								
257th Parameter	R	1	The data of address 0xAFF/0x16FF in the OTP								

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFF.
Restriction	This command only actives when BUSY_N = "1".



The sequence of programming OTP LUT backup1

8.2.48 REDH (LUT_BACKUP2_PG): OTP LUT backup2 program

REDH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP2_PG	W	0	1	1	1	0	1	1	0	1	EDH

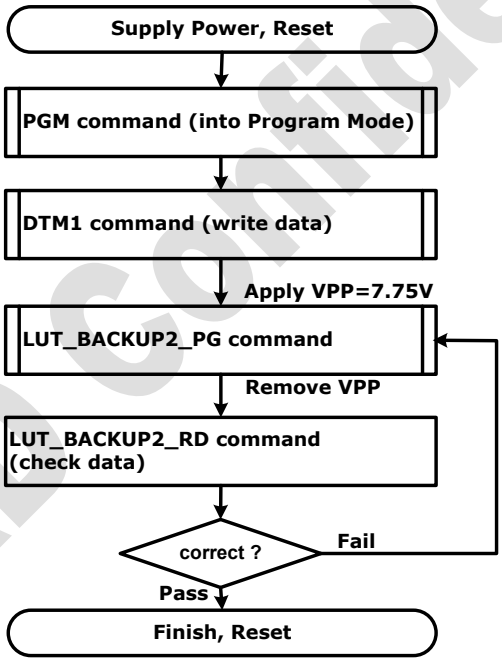
NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	-- The BUSY flag would fall to 0 while the programming is completed.

8.2.49 REEH (LUT_BACKUP2_RD): Read OTP LUT backup2

REEH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT_BACKUP2_RD	W	0	1	1	1	0	1	1	1	0	EEH
1st Parameter	R	1	Dummy								
2nd Parameter	R	1	The data of address 0xB00/0x1700 in the OTP								
3rd Parameter	R	1	The data of address 0xB01/0x1701 in the OTP								
4th Parameter	R	1	The data of address 0xB02/0x1702 in the OTP								
5th Parameter	R	1	The data of address 0xB03/0x1703 in the OTP								
6th~ 256th Parameter	R	1	.....								
257th Parameter	R	1	The data of address 0xBFF/0x17FF in the OTP								

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFF.  The sequence of programming OTP LUT backup2
Restriction	This command only actives when BUSY_N = "1".

8.2.50 REFH (CHKSUM_PG): Checksum Program to OTP

REFH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CHKSUM_PG	W	0	1	1	1	0	1	0	1	1	EFH

Description	This command is used to Program Checksum of LUT Table
Restriction	Apply VPP to OTP before use this command

8.2.51 RF0H (RM_LUT_CMD): Remap LUT command

RF0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RM_LUT_CMD	W	0	1	1	1	1	0	0	0	0	F0H
1st Parameter	W	1	-	-	-	tr10_lut_en	rmp2_table_sel[3]	rmp2_table_sel[2]	rmp2_table_sel[1]	rmp2_table_sel[0]	1Fh
2nd Parameter	W	1	-	-	-	tr9_lut_en	rmp1_table_sel[3]	rmp1_table_sel[2]	rmp1_table_sel[1]	rmp1_table_sel[0]	1Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description

The command is used for indicating backup OTP blocks to remap for LUTs

Addr (hex)	OTP Bank 0 (3K Bytes)	Addr (hex)	OTP Bank 1 (3K Bytes)
00h~0Fh	Temp. segment	C00h~C0Fh	Temp. segment
20h~60h	Default setting	C20h~C60h	Default setting
100h	TR0 WF	D00h	TR0 WF
200h	TR1 WF	E00h	TR1 WF
300h	TR2 WF	F00h	TR2 WF
400h	TR3 WF	1000h	TR3 WF
500h	TR4 WF	1100h	TR4 WF
600h	TR5 WF	1200h	TR5 WF
700h	TR6 WF	1300h	TR6 WF
800h	TR7 WF	1400h	TR7 WF
900h	TR8 WF	1500h	TR8 WF
A00h	TR9 WF / Backup 1	1600h	TR9 WF / Backup 1
B00h	TR10 WF / Backup 2	1700h	TR10 WF / Backup 2

1st Parameter:

tr10_lut_en :

Value	Function
1	OTP Address B00h~BFFh is used as "TR10 WF"
0	OTP Address B00h~BFFh is used as "Backup 2", And you can replace one of TR0 ~TR9.

rmp2_tab_sel [3:0] :

Only be functional when tr10_lut_en is set "0", target LUTs to be replaced is shown below

Value	Target LUTs
0001	TR0
0010	TR1
0011	TR2
0100	TR3
0101	TR4
0110	TR5
0111	TR6
1000	TR7
1001	TR8
1010	TR9

	1011~1111 | None 2nd Parameter tr9_lut_en : Value | Function 1 | OTP Address B00h~BFFh is used as "TR9 WF" 0 | OTP Address B00h~BFFh is used as "Backup 1", And you can replace one of TR0 ~TR8. rmp1_tab_sel[3:0] Only be functional when tr9_lut_en is set "0", target LUTs to be replaced is shown below Value | Target LUTs 0001 | TR0 0010 | TR1 0011 | TR2 0100 | TR3 0101 | TR4 0110 | TR5 0111 | TR6 1000 | TR7 1001 | TR8 1010~1111 | None Notice : If rmp1_tab_sel = rmp2_tab_sel , the control hardware will reload "backup 1" block to replace target LUT.
Restriction	

8.2.52 RF1H (SET_OTP_BANK): Set OTP program bank

RF1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_OTP_BANK	W	0	1	1	1	1	0	0	0	1	F1H
1st Parameter	W	1			-	-	-	-	LUT_bank0	reg_bank0	03h

Description

This command is used to set program bank for registers and LUTs

Addr (hex)	OTP Bank 0 (3K Bytes)	Addr (hex)	OTP Bank 1 (3K Bytes)
00h~0Fh	Temp. segment	C00h~C0Fh	Temp. segment
20h~60h	Default setting	C20h~C60h	Default setting
100h~BFFh	LUTs	D00h~17FFh	LUTs

reg_bank :

Value	Function
1	Program “Temp. segment” and “Default Setting” in bank 0
0	Program “Temp. segment” and “Default Setting” in bank 1

LUT_bank :

Value	Function
1	Program “LUTs” in bank 0
0	Program “LUTs” in bank 1

Restriction

8.2.53 RF2H (RD_CHKSUM): Read checksum information

RF2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RD_CHKSUM	W	0	1	1	1	1	0	0	1	0	F2H
1st ~9th Parameter	R	1	Checksum from “TR0 WF” to “TR8 WF”								-
10th Parameter	R	1	Checksum of “TR9 WF / backup 1”								-
11th Parameter	R	1	Checksum of “TR10 WF / backup 2”								-
12th Parameter	R	1	Checksum comparison result from “TR0 WF” to “TR7 WF”								-
13th Parameter	R	1	Checksum comparison result from “TR8” and “TR10 WF / backup 2”								-

Description

This command is to read checksum information from OTP.
1st to 11th Parameter : Checksum from “TR0 WF” to “TR10 WF / backup 2”
12th Parameter

D7	D6	D5	D4	D3	D2	D1	D0
fault_TR7	fault_TR6	fault_TR5	fault_TR4	fault_TR3	fault_TR2	fault_TR1	fault_TR0

13th Parameter

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	fault_TR10 / fault_backup2	fault_TR9 / fault_backup1	fault_TR9

definition of fault_TRx / fault_backup_x

Value	Function
0	Checksum comparison : Equal
1	Checksum comparison : Not Equal

Restriction

8.2.54 RF3H (CAL_CHKSUM): Calculate Checksum

RF3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CAL_CHKSUM	W	0	1	1	1	1	0	0	1	1	F3H

Description	This command is used to Calculate Checksum of LUT Table
Restriction	

8.3 Register Restriction

Following table will indicate the register restriction:

Register	Refresh restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R03H(PFS)	X	No action
R04H(PON)	X	Flag
R05H(PMES)	X	No action
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM1)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R13H(DTM2)	X	No action
R14H(PDTM1)	X	No action
R15H(PDTM2)	X	No action
R16H(PDRF)	X	Flag
R20H(LUTC)	X	No action
R21H(LUTWW)	X	No action
R22H(LUTBW/LUTR)	X	No action
R23H(LUTWB/LUTW)	X	No action
R24H(LUTBB/LUTB)	X	No action
R25H(LUTC Option)	X	No action
R26H(SET_STG)	Valid in BWR mode	No action
R30H(OSC)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R60H(TCON)	X	No action
R61H(TRES)	X	No action
R62H(TSGS)	X	No action
R70H(REV)	Valid only read	No action
R71H(FLG)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
RA0H(PGM)	X	No action
RA1H(APG)	X	Flag
RA2H(ROTP)	X	Flag
RE5H(TSSET)	X	No action
RE6H(LVSEL)	X	No action
RE7H (PBC)	Valid (only read)	Flag
RE8H (PWS)	X	No action
RE9H (AUTO):	Valid in standby	Flag
REBH	X	No action
RECH	X	Flag
REEH	X	No action
REFH	X	Flag
REFH (CHKSUM_PG)	X	No action
RF0H (RM_LUT_CMD)	X	No action
RF1H (SET_OTP_BANK)	X	No action
RF2H (RD_CHKSUM)	Valid only read	No action
RF3H (CAL_CHKSUM)	X	Flag

9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power on Sequence

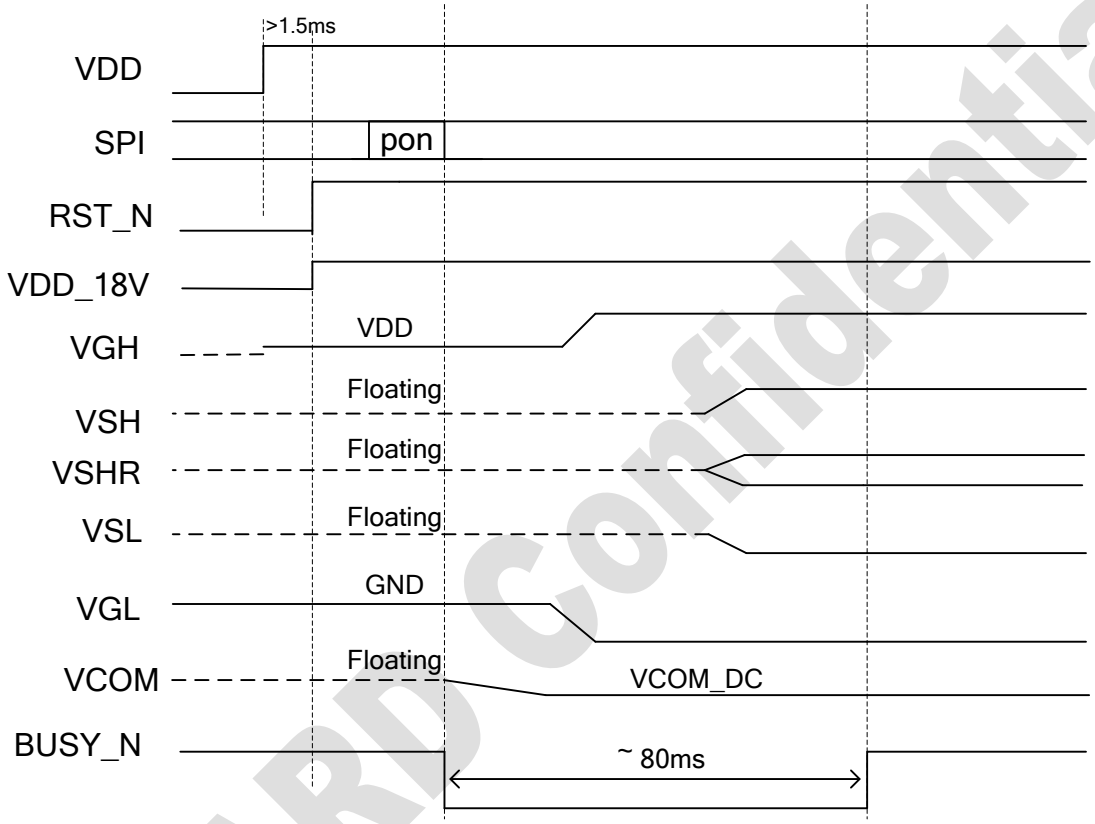


Figure 1: Power on sequence

Power off Sequence

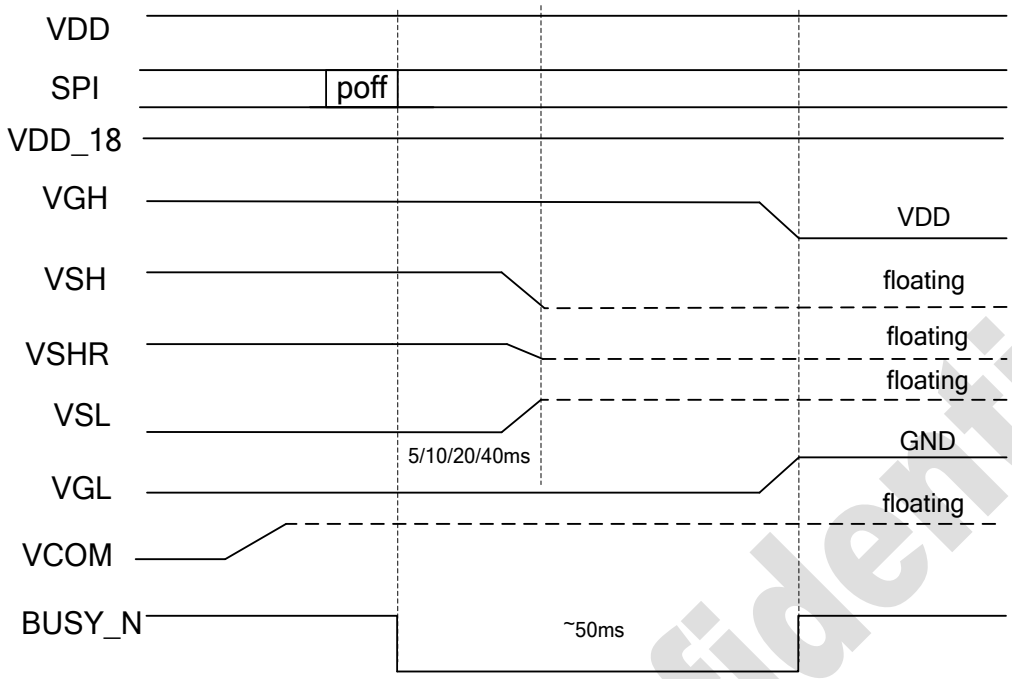


Figure 2: Power off sequence

DSLP sequence

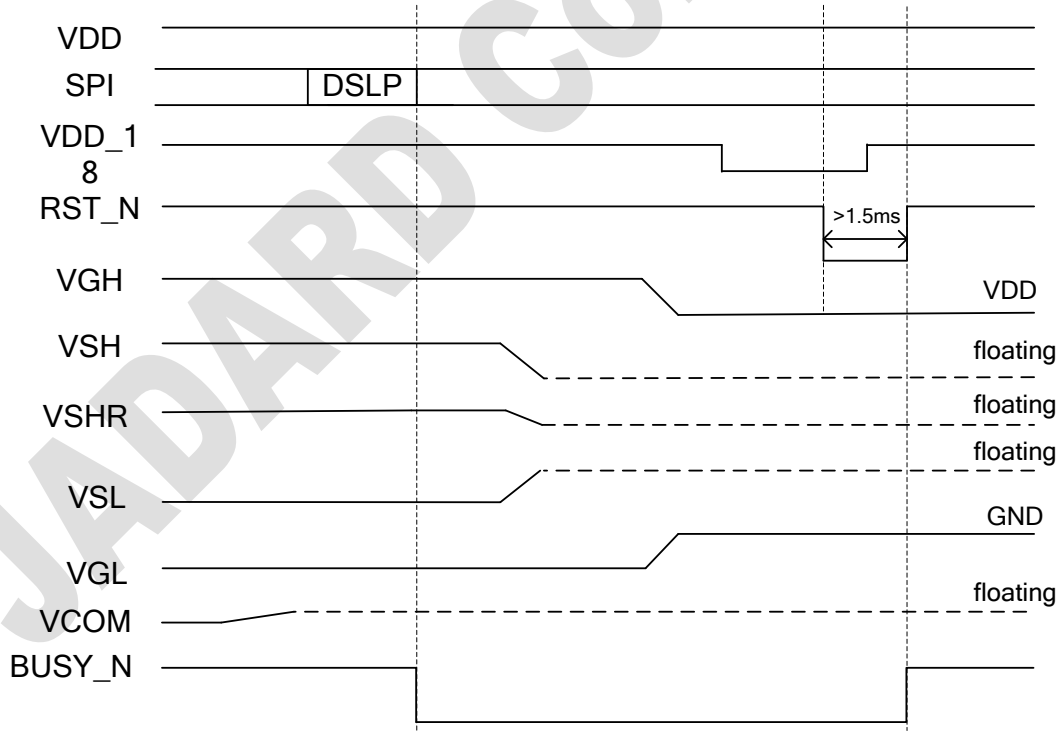


Figure 3: DSLP sequence

9.2 OTP LUT Definition

The OTP size would be 6144 Byte included temperature segment setting and 11 set waveform (maximum).

If TEMP<Boundary 0, use TR0 WF

If Boundary 0 ≦TEMP<Boundary1, use TR1

If Boundary 1 ≦TEMP<Boundary2, use TR2

.....

	OTP bank 0 (3K bytes)	Addr (hex)	OTP bank 1 (3K bytes)
00h~1Fh	Temp. segment	C00h~C1Fh	Temp. segment
20h~5Fh	Default setting	C20h~C5Fh	Default setting
60h~FFh	FIti command	C60h~CFFh	FIti command
100h	TR0 WF	D00h	TR0 WF
200h	TR1 WF	E00h	TR1 WF
300h	TR2 WF	F00h	TR2 WF
400h	TR3 WF	1000h	TR3 WF
500h	TR4 WF	1100h	TR4 WF
600h	TR5 WF	1200h	TR5 WF
700h	TR6 WF	1300h	TR6 WF
800h	TR7 WF	1400h	TR7 WF
900h	TR8 WF	1500h	TR8 WF
A00h	TR9 WF / Backup 1	1600h	TR9 WF / Backup 1
B00h	TR10 WF / Backup 2	1700h	TR10 WF / Backup 2

Temperature segment:

Command	Addr (dec)	Addr (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	0	000	otp_chk (A5)							
	1	001	otp_ver [7:0]							
	2	002	otp_ver [15:8]							
	3	003	otp_temp0							
	4	004	otp_temp1							
	5	005	otp_temp2							
	6	006	otp_temp3							
	7	007	otp_temp4							
	8	008	otp_temp5							
	9	009	otp_temp6							
	10	00A	otp_temp7							
	11	00B	otp_temp8 (optional)							
	12	00C	otp_temp9 (optional)							
	13 ~ 31	00D ~ 01F	Reserved							

Default setting

	32	020	Enable OTP Setting (0xA5)							
R00H	33	021	res[1:0]		reg_en	bwr	ud	shl	shd_n	rst_n
R01H	34	022							Vdg_en	Vds_en
	35	023						Vghl_lv[2:0]		
	36	024			Vsh[5:0]					
	37	025			Vsl[5:0]					
	38	026		VSHr[6:0]						
R03H	39	027			Vsh_off[1:0]		Vsl_off[1:0]		vshr_off[1:0]	
R06H	40	028	bt_pha[7:0]							
	41	029	bt_phb[7:0]							
	42	02A			bt_phc[5:0]					
R16H	43	02B	DFV_EN	Reserved						
--	44	02C	Reserved							
RE6H	45	02D							LVD_SEL[1:0]	
RE8H	46	02E			VCOM_W[2:0]			SD_W[2:0]		
--	47 ~ 50	02F ~ 032	Reserved							
R30H	51	033			M[2:0]			N[2:0]		
R41H	52	034	tse				To[3:0]			
R42H	53	035	Wattr[7:0]							
	54	036	Wmsb[7:0]							
	55	037	Wlsb[7:0]							
R50H	56	038	vbd[1:0]		ddx[1:0]		cdi[3:0]			
R60H	57	039	s2g[3:0]				g2s[3:0]			
R61H	58	03A	Reserved						hres[9]	hres[8]
	59	03B	hres[7:3]							
	60	03C							vres[9]	vres[8]
	61	03D	vres[7:0]							
R80H	62	03E			amvt[1:0]		xon	amvs	amv	
R82H	63	03F		vdcs[6:0]						
RE0H	64	040					cce_sel	cce_lr	tsfix	ccein
RE5H	65	041	ts_set[7:0]							
R62H	66	042	Reserved						sstart[9]	sstart[8]
	67	043	sstart[7:3]							
	68	044				gscan			gstart[9]	gstart[8]
	69	045	gstart[7:0]							
RF0H	70	046				tr10_lut_en	rmp2_table_sel			
	71	047				tr9_lut_en	rmp1_table_sel			
RF1H	72	048							LUT_bank0	reg_bank0

Slave setting									
R00H	73	049	slv_res[1:0]	slv_reg_en	slv_bwr	slv_ud	slv_shl		slv_rst_n
R62H	74	04A	Reserved						
	75	04B	slv_sstart[7:3]						
	76	04C				slv_gscan			slv_gstart[9]	slv_gstart[8]
	77	04D	slv_gstart[7:0]						
--	78	04E	Reserved						
R26H	79	04F				vcom_stg_sel[1:0]		b2w_stg_sel[1:0]	

TR0~10 WF is the same as TR0 defined as below:

	Discription	Addr (dec)	Addr (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	PS1
TR0 WF	Voltage	256	100			M[2:0]			N[2:0]			
		257	101			vsh[5:0]						
		258	102			vsl[5:0]						
		259	103		vshr[6:0]							
		260	104			vdcs[5:0]						
		261	105		vghl_lv[2:0]					XON[9:8]		
		262	106	XON[7:0]								
		263	107							VCOMH[9:8]		
		264	108	VCOMH[7:0]								
	LUTC	265	109	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		266	10A	1st Frame number[7:0]								
		267	10B	2nd Frame number[7:0]								
		268	10C	3rd Frame number[7:0]								
		269	10D	4th Frame number[7:0]								
		270	10E	Repeat number[7:0]								
		271	10F	Stage 2 ~ Stage 10								
		324	144									
	LUTWW	325	145	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		326	146	1st Frame number[7:0]								
		327	147	2nd Frame number[7:0]								
		328	148	3rd Frame number[7:0]								
		329	149	4th Frame number[7:0]								
		330	14A	Repeat number[7:0]								
		331	14B	Stage 2 ~ Stage 7								
		366	16E									
	LUTBW / LUTR	367	16F	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		368	170	1st Frame number[7:0]								
		369	171	2nd Frame number[7:0]								
		370	172	3rd Frame number[7:0]								
		371	173	4th Frame number[7:0]								
		372	174	Repeat number[7:0]								
		373	175	Stage 2 ~ Stage 10								
		426	1AA									
	LUTWB / LUTW	427	1AB	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		428	1AC	1st Frame number[7:0]								
		429	1AD	2nd Frame number[7:0]								
		430	1AE	3rd Frame number[7:0]								
		431	1AF	4th Frame number[7:0]								
		432	1B0	Repeat number[7:0]								
		433	1B1	Stage 2 ~ Stage 7								
		468	1D4									
	LUTBB / LUTB	469	1D5	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		470	1D6	1st Frame number[7:0]								
		471	1D7	2nd Frame number[7:0]								
		472	1D8	3rd Frame number[7:0]								
		473	1D9	4th Frame number[7:0]								
		474	1DA	Repeat number[7:0]								
		475	1DB	Stage 2 ~ Stage 7								
		510	1FE									

9.3 Data transmission waveform

Example1: LUT all states (7 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 v.

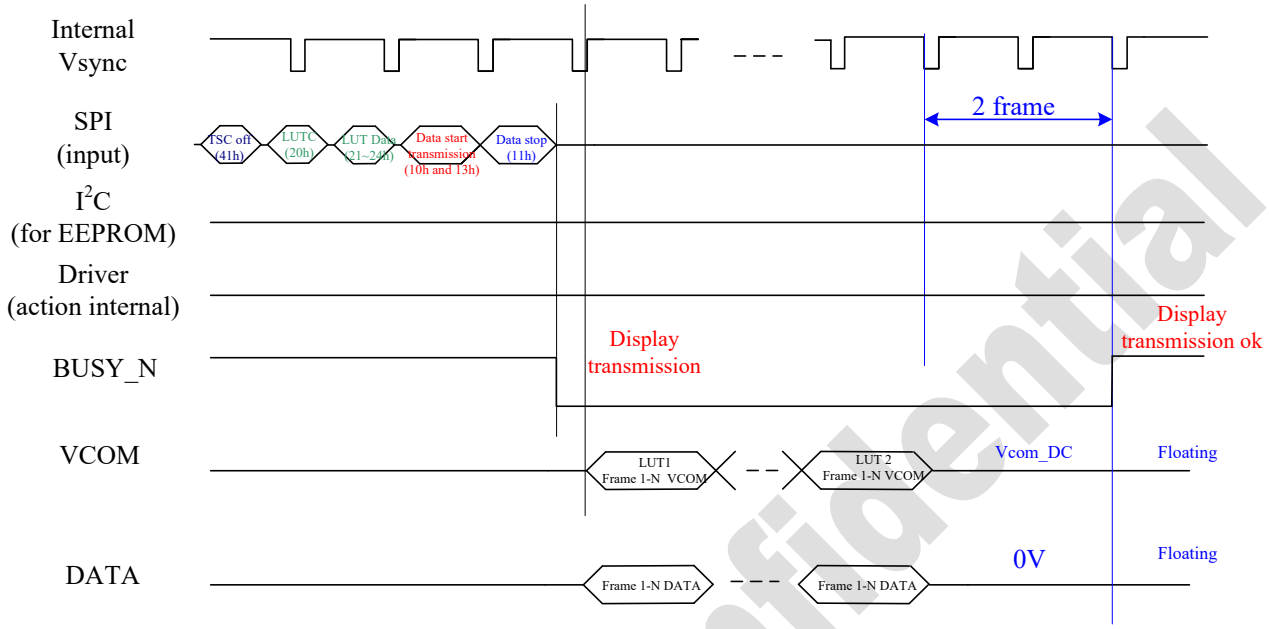


Figure 3: Data transmission example1 waveform

Example2: While level selection in LUT is “11”, the driver will float VCOM and data.

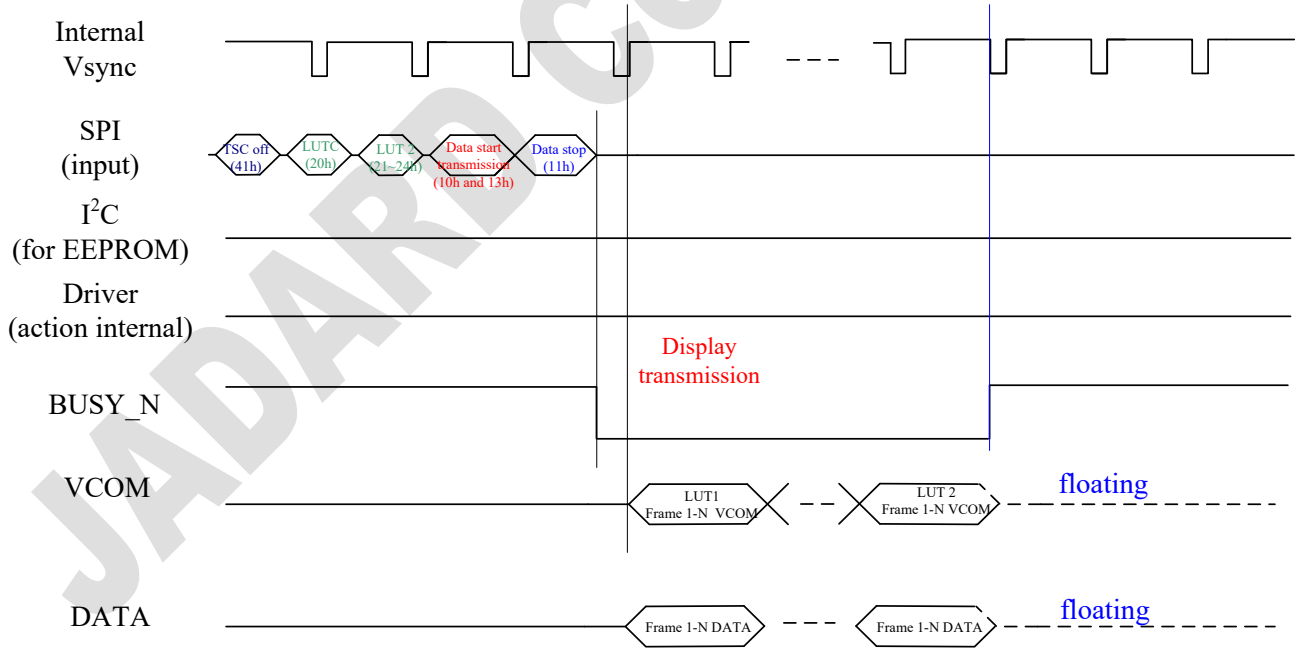


Figure 4: Data transmission example 2 waveform

9.4 Display refresh waveform

Example1: LUT all states (7 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 v.

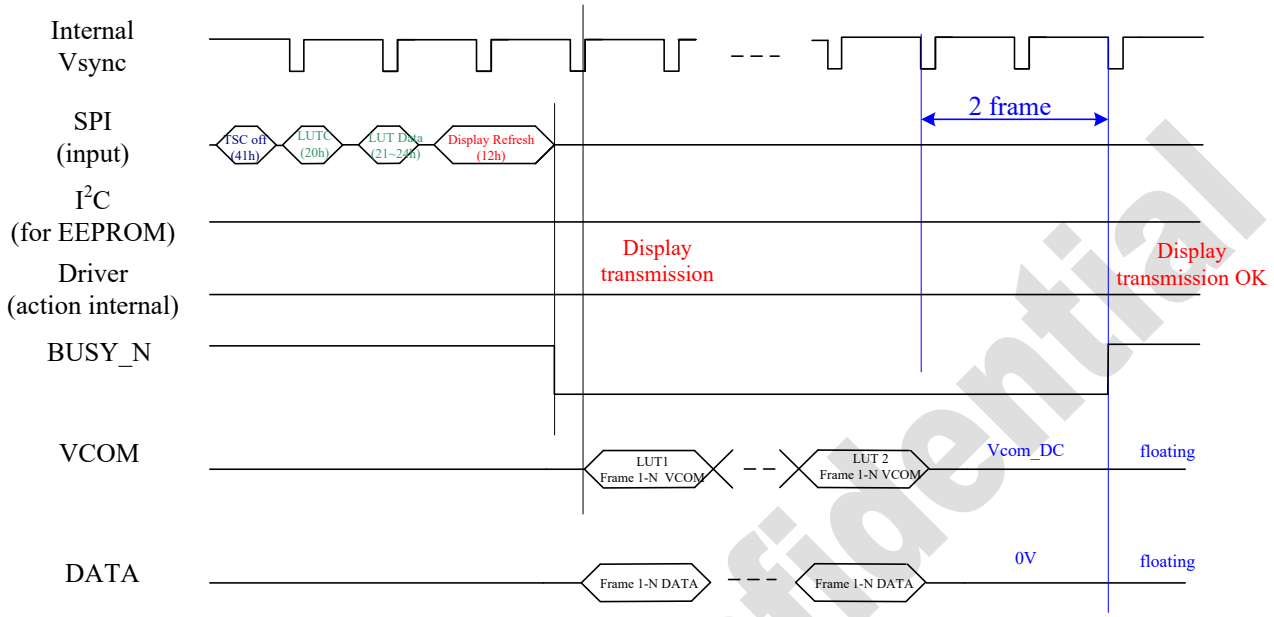


Figure 5: Display refresh example1 waveform

Example2: While level selection in LUT is “11”, the driver will float VCOM and data.

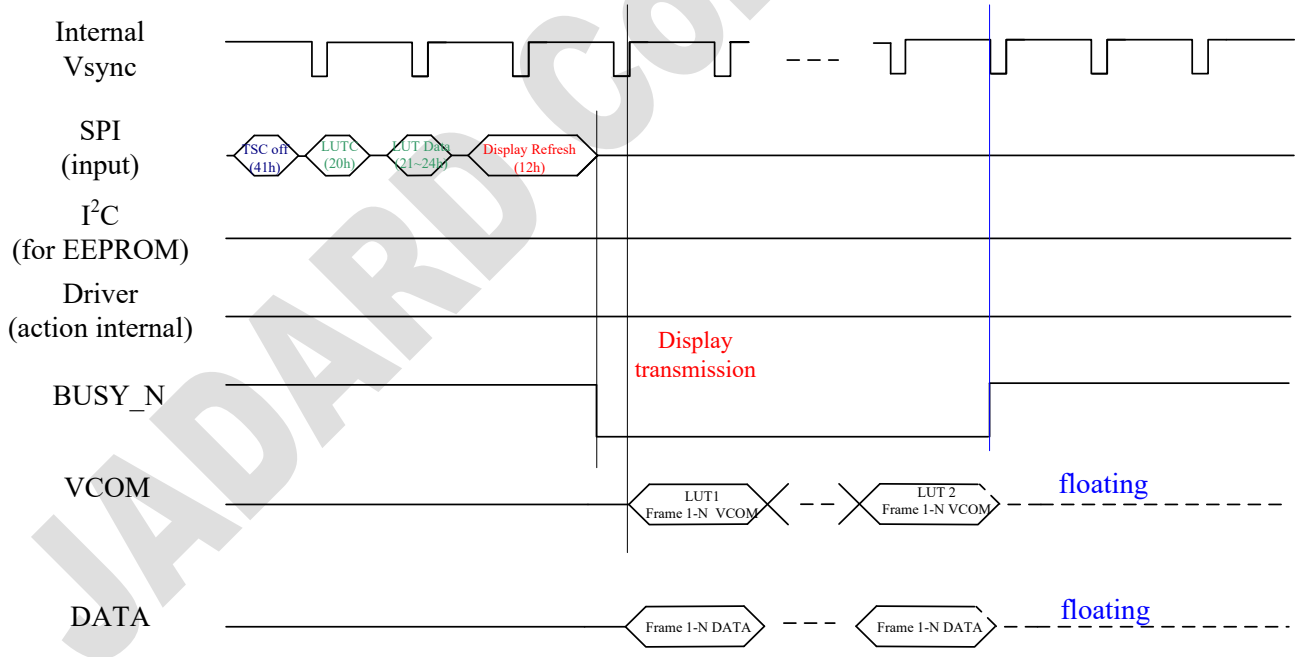


Figure 6: Display refresh example2 waveform

10. ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	TBD	V
Supply range	VGH-VGL	VGL-0.3	VGH+0.3	V
Analog supply	VSH	+2.4	+15	V
Analog supply	VSL	-15	-2.4	V
Analog supply	VSHR	-15	+15	
Supply voltage	VGH	-	+20	V
Supply voltage	VGL	-20	-	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

10.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.8V output voltage	VDD_18	1.62	1.8	1.98		
1.8V input voltage	VDD_18	1.62	1.8	1.98		
OTP program power	VOTP	7.25	7.5	7.75		
Digital ground	VSS		0			
DCDC ground	VSSP		0			
Low Level Input Voltage	Vil	GND	-	0.3xVDD	V	Digital input pins
High Level Input Voltage	Vih	0.7xVIO	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400μA
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400μA DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL = -400μA
Input Leakage Current	Iin	-1.0	-	+1.0	uA	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Deep sleep Current	IdpVDD*	-	0	1	uA	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	mA	
IO Stand-by Current (power off mode)	IstVDDIO*	-	0.4	1.0	uA	All stopped
IO Operating Current	IVDDIO*	-	-	0.2	mA	No load
DCDC Stand-by Current (power off mode)	IstVDD1*	-	0	1	uA	All stopped
DCDC Operating Current	IVDD1*	-	-	1.5	mA	fdcdc=250kHz, No load
DCDC Operating Current	IVDD1*	-	10	20	mA	fdcdc=250kHz, External cap: PMOS=415pF, NMOS=340pF
Operating temperature	T_{op}	-30	-	85	℃	

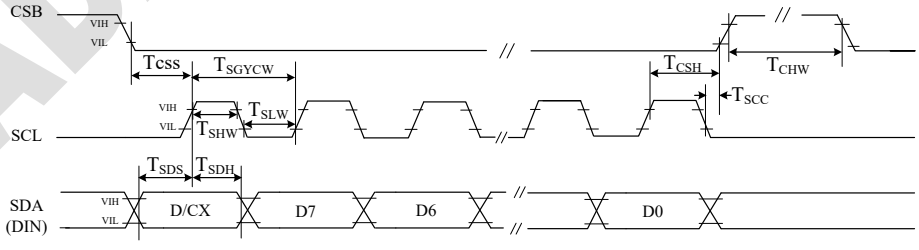
NOTE: typ. and max. values to be confirmed by design

10.3 Analog DC Characteristics

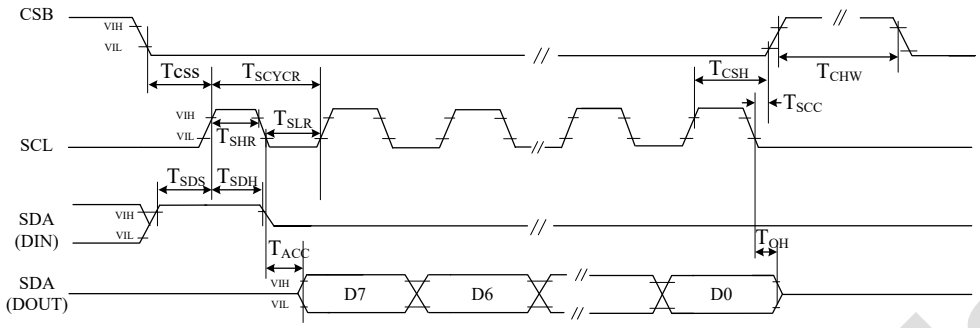
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSH		10		V	For source driver/VCOM
Positive Source voltage dev	d VSH	-300	0	+300	mV	
Negative Source voltage	VSL		-10		V	For source driver/VCOM
Negative Source voltage dev	d VSL	-300	-	+300	mV	
Positive Source voltage for Red	VSHR					
Negative Source voltage for Red	VSLR					
Analog Operating Current	Idd		TBD		mA	No load,
Dynamic Range of Output	Vdr	0.1	-	VSH-0.1	V	
Voltage Range of VGH - VGL	VGH-VGL	4.8	-	31	V	
Negative Source voltage	VGL	-15	-	-12	V	For gate driver
Negative Source voltage dev	dVGL	-400	0	+400	mV	
Positive Source voltage	VGH	13		16	V	For gate driver
Positive Source voltage dev	dVGH	-400	0	+400	mV	
Positive HV Stand-by Current (power off mode)	IstVGH*	-	0	0.2	uA	Include VSH power With load
Positive HV Operating Current	IVGH*	-	0.7	1.1	mA	Include VSH power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVGH*	-	0.8	1.2	mA	Include VSH power With load all SD=H VCOM external resistor divider not included
Negative HV Stand-by Current (power off mode)	IstVGL*	-	0	0.2	µA	Include VSH power With load
Negative HV Operating Current	IVGL*	-	0.8	1.2	mA	Include VSL power With load all SD=L
Negative HV Operating Current	IVGL*	-	0.9-	1.3	mA	Include VSL power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*		0	0.01	µA	
VINT1 Operating Current	IVINT1*			0.3	mA	

10.4 AC Characteristics

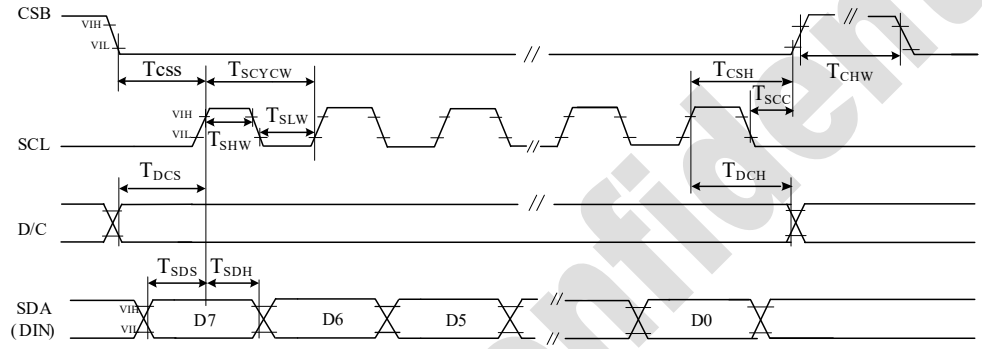
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	100			ns	Chip select setup time
	T_{CSH}	100			ns	Chip select hold time
	T_{SCC}	50			ns	Chip select CSB setup time
	T_{CHW}	500			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35	-		ns	SCL “H” pulse width (Write)
	T_{SLW}	35	-		ns	SCL “L” pulse width (Write)
	T_{SCYCR}	200	-		ns	Serial clock cycle (Read)
	T_{SHR}	85			ns	SCL “H” pulse width (Read)
	T_{SLR}	85			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}	10			ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time
RC loading						
Source driver output loading	RL_S	-	11.95k		Ω	
	CL_S	-	42		pf	
Gate driver output loading	RL_S		37.3k		Ω	
	CL_S		170pf		pf	
VCOM output loading	RL_com		2.85 k		Ω	
	CL_com		2300		pf	
Driver						
Source driver rise time	trS		5		us	99% final value
Source driver fall time	tFS		5		us	
Gate driver rise time	TrG		5		us	99% final value
Gate driver fall time	tFG		5		us	
VCOM rise time	trCOM		1		ms	99% final value
VCOM fall time	tFCOM		1		ms	



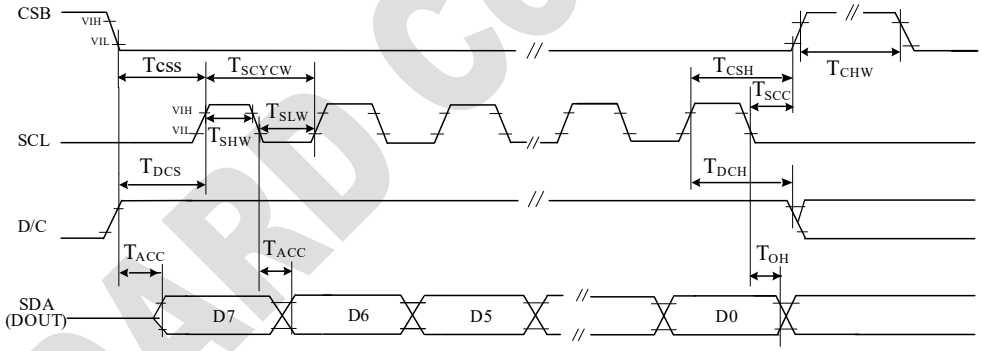
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics (write mode)



4 pin serial interface characteristics (read mode)

Figure 8: SPI interface timing

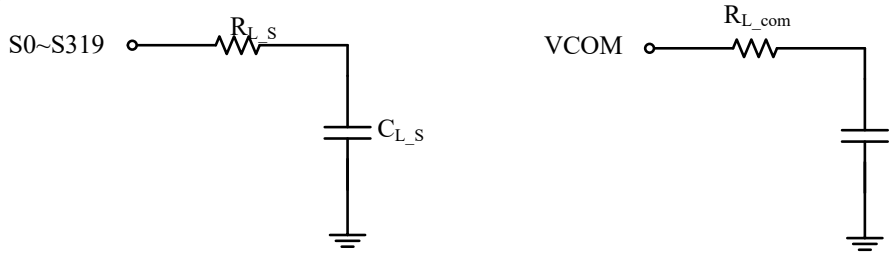
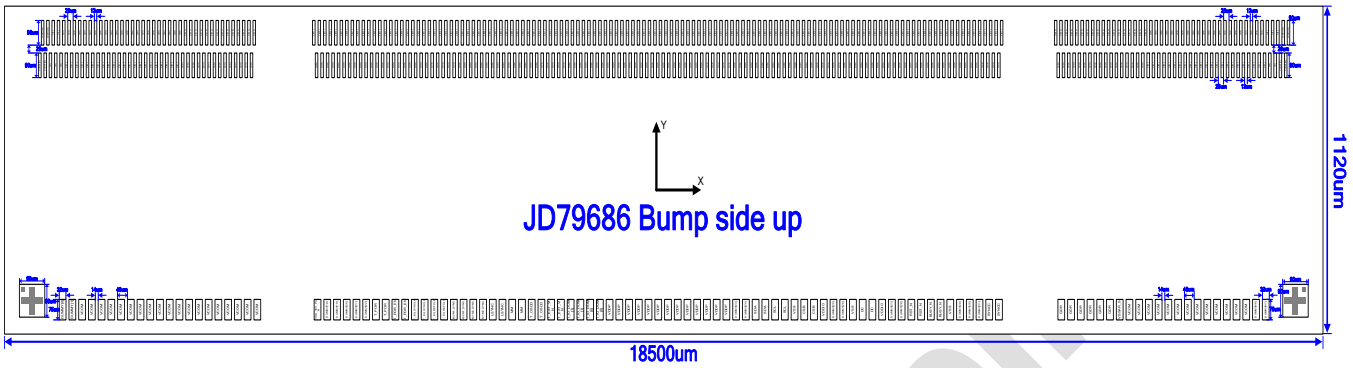


Figure 9: RC loading

11. CHIP OUTLINE DIMENSIONS

11.1 Circuit/Bump View



Die Size: 18500 um(+20um) x1120 um(+20um)

Die Thickness: 330 μm ± 20μm

Die TTV: (D_{MAX} – D_{MIN}) within die ≤ 2μm

Bump Height: 9 μm ± 3μm

(H_{MAX} – H_{MIN}) within die ≤ 2μm

Bump Size: 12 μm x 90 um ± 2μm

Bump area: 1080um^2

Bump pitch: 25um ± 3μm

Bump Gap: 13 um ± 3μm

Hardness:75 Hv ± 25Hv

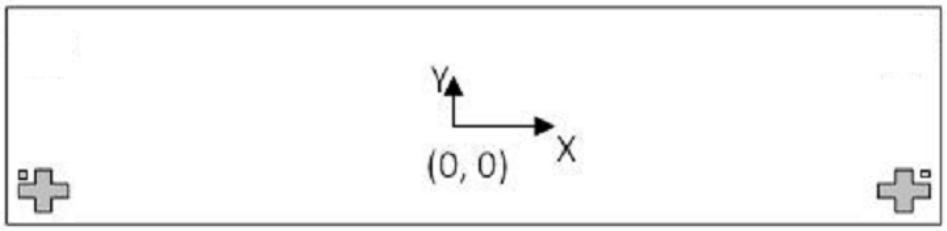
Coordinate origin: Chip center

Note: the tolerance of others' dimension shown in drawing is ± **3μm**

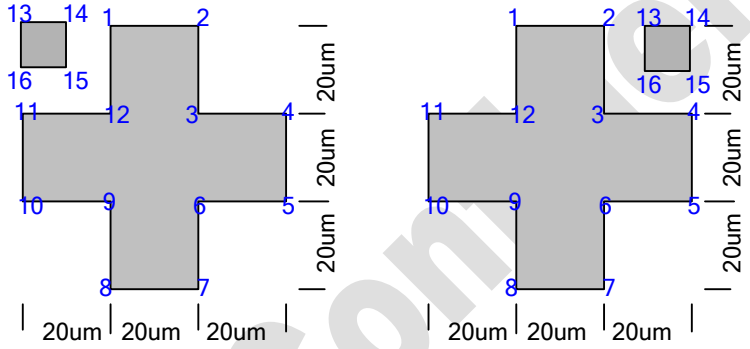
12. ALIGNMENT MARK INFORMATION

12.1 Location:

Upper-Left Mark Upper-Right Mark



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-9183	-498	9183	-498
1	-9193	-468	9173	-468
2	-9173	-468	9193	-468
3	-9173	-488	9193	-488
4	-9153	-488	9213	-488
5	-9153	-508	9213	-508
6	-9173	-508	9193	-508
7	-9173	-528	9193	-528
8	-9193	-528	9173	-528
9	-9193	-508	9173	-508
10	-9213	-508	9153	-508
11	-9213	-488	9153	-488
12	-9193	-488	9173	-488
13	-9213	-468	9203	-468
14	-9203	-468	9213	-468
15	-9203	-478	9213	-478
16	-9213	-478	9203	-478

12.2 Pad coordinates:

No.	Name	X-axis	Y-axis	W	H
1	DUMMY[0]	-9062	-512.5	32	75
2	DUMMY[1]	-9016	-512.5	32	75
3	VCOM	-8970	-512.5	32	75
4	VCOM	-8924	-512.5	32	75
5	VCOM	-8878	-512.5	32	75
6	VCOM	-8832	-512.5	32	75
7	VCOM	-8786	-512.5	32	75
8	VCOM	-8740	-512.5	32	75
9	VCOM	-8694	-512.5	32	75
10	VCOM	-8648	-512.5	32	75
11	VCOM	-8602	-512.5	32	75
12	VCOM	-8556	-512.5	32	75
13	VCOM	-8510	-512.5	32	75
14	VCOM	-8464	-512.5	32	75
15	VCOM	-8418	-512.5	32	75
16	VCOM	-8372	-512.5	32	75
17	VCOM	-8326	-512.5	32	75
18	VCOM	-8280	-512.5	32	75
19	VCOM	-8234	-512.5	32	75
20	VCOM	-8188	-512.5	32	75
21	VCOM	-8142	-512.5	32	75
22	VSSA	-8096	-512.5	32	75
23	VGL	-8050	-512.5	32	75
24	VGL	-8004	-512.5	32	75
25	VGL	-7958	-512.5	32	75
26	VGL	-7912	-512.5	32	75
27	VGL	-7866	-512.5	32	75
28	VGL	-7820	-512.5	32	75
29	VGL	-7774	-512.5	32	75
30	VGL	-7728	-512.5	32	75
31	VGL	-7682	-512.5	32	75
32	VGL	-7636	-512.5	32	75
33	VGL	-7590	-512.5	32	75
34	VGL	-7544	-512.5	32	75
35	VGL	-7498	-512.5	32	75
36	VGL	-7452	-512.5	32	75
37	VSSAL_VSL	-7406	-512.5	32	75
38	VSL	-7360	-512.5	32	75
39	VSL	-7314	-512.5	32	75
40	VSL	-7268	-512.5	32	75
41	VSL	-7222	-512.5	32	75
42	VSL	-7176	-512.5	32	75
43	VSL	-7130	-512.5	32	75
44	VSL	-7084	-512.5	32	75
45	VSL	-7038	-512.5	32	75
46	VSL	-6992	-512.5	32	75
47	VSL	-6946	-512.5	32	75
48	VSL	-6900	-512.5	32	75
49	VSL	-6854	-512.5	32	75
50	VSSA	-6808	-512.5	32	75
51	VGH	-6762	-512.5	32	75
52	VGH	-6716	-512.5	32	75
53	VGH	-6670	-512.5	32	75
54	VGH	-6624	-512.5	32	75
55	VGH	-6578	-512.5	32	75
56	VGH	-6532	-512.5	32	75
57	VGH	-6486	-512.5	32	75
58	VGH	-6440	-512.5	32	75
59	VGH	-6394	-512.5	32	75
60	VGH	-6348	-512.5	32	75

No.	Name	X-axis	Y-axis	W	H
61	VGH	-6302	-512.5	32	75
62	VGH	-6256	-512.5	32	75
63	VGH	-6210	-512.5	32	75
64	VGH	-6164	-512.5	32	75
65	VSSA	-6118	-512.5	32	75
66	VSH	-6072	-512.5	32	75
67	VSH	-6026	-512.5	32	75
68	VSH	-5980	-512.5	32	75
69	VSH	-5934	-512.5	32	75
70	VSH	-5888	-512.5	32	75
71	VSH	-5842	-512.5	32	75
72	VSH	-5796	-512.5	32	75
73	VSH	-5750	-512.5	32	75
74	VSH	-5704	-512.5	32	75
75	VSH	-5658	-512.5	32	75
76	VSH	-5612	-512.5	32	75
77	VSH	-5566	-512.5	32	75
78	VSSA	-5520	-512.5	32	75
79	VOTP	-5474	-512.5	32	75
80	VOTP	-5428	-512.5	32	75
81	VOTP	-5382	-512.5	32	75
82	VOTP	-5336	-512.5	32	75
83	VOTP	-5290	-512.5	32	75
84	VOTP	-5244	-512.5	32	75
85	VOTP	-5198	-512.5	32	75
86	VOTP	-5152	-512.5	32	75
87	VOTP	-5106	-512.5	32	75
88	VOTP	-5060	-512.5	32	75
89	T_LDON5V	-5014	-512.5	32	75
90	T_LDON5V	-4968	-512.5	32	75
91	T_VCOM	-4922	-512.5	32	75
92	T_VCOM	-4876	-512.5	32	75
93	T_N18V	-4830	-512.5	32	75
94	T_N18V	-4784	-512.5	32	75
95	T_VSLREF	-4738	-512.5	32	75
96	T_VSLREF	-4692	-512.5	32	75
97	T_VSLOK	-4646	-512.5	32	75
98	T_VSLOK	-4600	-512.5	32	75
99	T_VSHREF	-4554	-512.5	32	75
100	T_VSHREF	-4508	-512.5	32	75
101	T_VSHRREF	-4462	-512.5	32	75
102	T_VSHRREF	-4416	-512.5	32	75
103	VDD_18V	-4370	-512.5	32	75
104	VDD_18V	-4324	-512.5	32	75
105	VDD_18V	-4278	-512.5	32	75
106	VDD_18V	-4232	-512.5	32	75
107	VDD_18V	-4186	-512.5	32	75
108	VDD_18V	-4140	-512.5	32	75
109	VDD_18V	-4094	-512.5	32	75
110	VDD_18V	-4048	-512.5	32	75
111	VDD_18V	-4002	-512.5	32	75
112	VDD_18V	-3956	-512.5	32	75
113	VDD_18V	-3910	-512.5	32	75
114	VDD_18V	-3864	-512.5	32	75
115	VDD_18V	-3818	-512.5	32	75
116	VDD_18V	-3772	-512.5	32	75
117	VDD_18V	-3726	-512.5	32	75
118	VDD_18V	-3680	-512.5	32	75
119	VSSA	-3634	-512.5	32	75
120	VSSA	-3588	-512.5	32	75

No.	Name	X-axis	Y-axis	W	H
121	VSSA	-3542	-512.5	32	75
122	VSSA	-3496	-512.5	32	75
123	VSSA	-3450	-512.5	32	75
124	VSSA	-3404	-512.5	32	75
125	VSSA	-3358	-512.5	32	75
126	VSSA	-3312	-512.5	32	75
127	VSSA	-3266	-512.5	32	75
128	VSSA	-3220	-512.5	32	75
129	VSSA	-3174	-512.5	32	75
130	VSSA	-3128	-512.5	32	75
131	VSS	-3082	-512.5	32	75
132	VSS	-3036	-512.5	32	75
133	VSS	-2990	-512.5	32	75
134	VSS	-2944	-512.5	32	75
135	VSS	-2898	-512.5	32	75
136	VSS	-2852	-512.5	32	75
137	VSS	-2806	-512.5	32	75
138	VSS	-2760	-512.5	32	75
139	VSS	-2714	-512.5	32	75
140	VSS	-2668	-512.5	32	75
141	VSS	-2622	-512.5	32	75
142	VSS	-2576	-512.5	32	75
143	VDD	-2530	-512.5	32	75
144	VDD	-2484	-512.5	32	75
145	VDD	-2438	-512.5	32	75
146	VDD	-2392	-512.5	32	75
147	VDD	-2346	-512.5	32	75
148	VDD	-2300	-512.5	32	75
149	VDD	-2254	-512.5	32	75
150	VDD	-2208	-512.5	32	75
151	VDD	-2162	-512.5	32	75
152	VDD	-2116	-512.5	32	75
153	VDDIO	-2070	-512.5	32	75
154	VDDIO	-2024	-512.5	32	75
155	VDDIO	-1978	-512.5	32	75
156	VDDIO	-1932	-512.5	32	75
157	VDDIO	-1886	-512.5	32	75
158	VDDIO	-1840	-512.5	32	75
159	VDDIO	-1794	-512.5	32	75
160	VDDIO	-1748	-512.5	32	75
161	VDDIO	-1702	-512.5	32	75
162	VDDIO	-1656	-512.5	32	75
163	VDDIO	-1610	-512.5	32	75
164	DUMMY[2]	-1564	-512.5	32	75
165	DUMMY[3]	-1518	-512.5	32	75
166	DUMMY[4]	-1472	-512.5	32	75
167	DUMMY[5]	-1426	-512.5	32	75
168	DUMMY[6]	-1380	-512.5	32	75
169	DUMMY[7]	-1334	-512.5	32	75
170	DUMMY[8]	-1288	-512.5	32	75
171	DUMMY[9]	-1242	-512.5	32	75
172	DUMMY[10]	-1196	-512.5	32	75
173	DUMMY[11]	-1150	-512.5	32	75
174	DUMMY[12]	-1104	-512.5	32	75
175	DUMMY[13]	-1058	-512.5	32	75
176	DUMMY[14]	-1012	-512.5	32	75
177	DUMMY[15]	-966	-512.5	32	75
178	DUMMY[16]	-920	-512.5	32	75
179	DUMMY[17]	-874	-512.5	32	75
180	VDD_18V_POR	-828	-512.5	32	75

No.	Name	X-axis	Y-axis	W	H
181	VDD_18V_POR	-782	-512.5	32	75
182	DUMMY[18]	-736	-512.5	32	75
183	DUMMY[19]	-690	-512.5	32	75
184	DUMMY[20]	-644	-512.5	32	75
185	DUMMY[21]	-598	-512.5	32	75
186	DUMMY[22]	-552	-512.5	32	75
187	T_POR	-506	-512.5	32	75
188	T_POR	-460	-512.5	32	75
189	T_POR_EN	-414	-512.5	32	75
190	T_POR_EN	-368	-512.5	32	75
191	T_EX_SYSCLK	-322	-512.5	32	75
192	T_EX_SYSCLK	-276	-512.5	32	75
193	T_EX_REFCLK	-230	-512.5	32	75
194	T_EX_REFCLK	-184	-512.5	32	75
195	M2M1_SYNC	-138	-512.5	32	75
196	M2M1_SYNC	-92	-512.5	32	75
197	M1M2_SYNC	-46	-512.5	32	75
198	M1M2_SYNC	0	-512.5	32	75
199	LSYNC	46	-512.5	32	75
200	LSYNC	92	-512.5	32	75
201	MM	138	-512.5	32	75
202	MM	184	-512.5	32	75
203	T_OSCO	230	-512.5	32	75
204	T_OSCO	276	-512.5	32	75
205	T_EXT_VIN	322	-512.5	32	75
206	T_EXT_VIN	368	-512.5	32	75
207	T_IO_DUM[1]	414	-512.5	32	75
208	T_IO_DUM[1]	460	-512.5	32	75
209	T_IO_DUM[0]	506	-512.5	32	75
210	T_IO_DUM[0]	552	-512.5	32	75
211	VDDP	598	-512.5	32	75
212	VDDP	644	-512.5	32	75
213	VDDP	690	-512.5	32	75
214	VDDP	736	-512.5	32	75
215	VDDP	782	-512.5	32	75
216	VDDP	828	-512.5	32	75
217	VDDP	874	-512.5	32	75
218	VDDP	920	-512.5	32	75
219	VDDP	966	-512.5	32	75
220	VDDP	1012	-512.5	32	75
221	VDDP	1058	-512.5	32	75
222	VDDP	1104	-512.5	32	75
223	VDDP	1150	-512.5	32	75
224	DUMMY[23]	1196	-512.5	32	75
225	DUMMY[24]	1242	-512.5	32	75
226	SDA	1288	-512.5	32	75
227	SDA	1334	-512.5	32	75
228	SCL	1380	-512.5	32	75
229	SCL	1426	-512.5	32	75
230	VSS	1472	-512.5	32	75
231	CSB	1518	-512.5	32	75
232	CSB	1564	-512.5	32	75
233	VDDIO	1610	-512.5	32	75
234	DUMMY[25]	1656	-512.5	32	75
235	DUMMY[26]	1702	-512.5	32	75
236	VSS	1748	-512.5	32	75
237	DC	1794	-512.5	32	75
238	DC	1840	-512.5	32	75
239	VDDIO	1886	-512.5	32	75
240	DUMMY[27]	1932	-512.5	32	75

No.	Name	X-axis	Y-axis	W	H
241	DUMMY[28]	1978	-512.5	32	75
242	RST_N	2024	-512.5	32	75
243	RST_N	2070	-512.5	32	75
244	BUSY_N	2116	-512.5	32	75
245	BUSY_N	2162	-512.5	32	75
246	VSS	2208	-512.5	32	75
247	DUMMY[29]	2254	-512.5	32	75
248	DUMMY[30]	2300	-512.5	32	75
249	DUMMY[31]	2346	-512.5	32	75
250	SYNCC	2392	-512.5	32	75
251	SYNCC	2438	-512.5	32	75
252	SYNCD[3]	2484	-512.5	32	75
253	SYNCD[3]	2530	-512.5	32	75
254	SYNCD[2]	2576	-512.5	32	75
255	SYNCD[2]	2622	-512.5	32	75
256	SYNCD[1]	2668	-512.5	32	75
257	SYNCD[1]	2714	-512.5	32	75
258	SYNCD[0]	2760	-512.5	32	75
259	SYNCD[0]	2806	-512.5	32	75
260	VSS	2852	-512.5	32	75
261	HSYNC	2898	-512.5	32	75
262	HSYNC	2944	-512.5	32	75
263	VDDIO	2990	-512.5	32	75
264	VSYNC	3036	-512.5	32	75
265	VSYNC	3082	-512.5	32	75
266	VSS	3128	-512.5	32	75
267	DUMMY[32]	3174	-512.5	32	75
268	VDDIO	3220	-512.5	32	75
269	BS	3266	-512.5	32	75
270	BS	3312	-512.5	32	75
271	VSS	3358	-512.5	32	75
272	DUMMY[33]	3404	-512.5	32	75
273	VDDIO	3450	-512.5	32	75
274	PCKI	3496	-512.5	32	75
275	PCKI	3542	-512.5	32	75
276	VSS	3588	-512.5	32	75
277	MS	3634	-512.5	32	75
278	MS	3680	-512.5	32	75
279	VDDIO	3726	-512.5	32	75
280	VSS	3772	-512.5	32	75
281	TSDA	3818	-512.5	32	75
282	TSDA	3864	-512.5	32	75
283	VDDIO	3910	-512.5	32	75
284	TSCL	3956	-512.5	32	75
285	TSCL	4002	-512.5	32	75
286	VSS	4048	-512.5	32	75
287	PCKO	4094	-512.5	32	75
288	PCKO	4140	-512.5	32	75
289	T_EN_DIG	4186	-512.5	32	75
290	T_EN_DIG	4232	-512.5	32	75
291	T_IN[1]	4278	-512.5	32	75
292	T_IN[1]	4324	-512.5	32	75
293	T_IN[0]	4370	-512.5	32	75
294	T_IN[0]	4416	-512.5	32	75
295	T_DEBUG[9]	4462	-512.5	32	75
296	T_DEBUG[9]	4508	-512.5	32	75
297	T_DEBUG[8]	4554	-512.5	32	75
298	T_DEBUG[8]	4600	-512.5	32	75
299	T_DEBUG[7]	4646	-512.5	32	75
300	T_DEBUG[7]	4692	-512.5	32	75

No.	Name	X-axis	Y-axis	W	H
301	T_DEBUG[6]	4738	-512.5	32	75
302	T_DEBUG[6]	4784	-512.5	32	75
303	T_DEBUG[5]	4830	-512.5	32	75
304	T_DEBUG[5]	4876	-512.5	32	75
305	T_DEBUG[4]	4922	-512.5	32	75
306	T_DEBUG[4]	4968	-512.5	32	75
307	T_DEBUG[3]	5014	-512.5	32	75
308	T_DEBUG[3]	5060	-512.5	32	75
309	T_DEBUG[2]	5106	-512.5	32	75
310	T_DEBUG[2]	5152	-512.5	32	75
311	T_DEBUG[1]	5198	-512.5	32	75
312	T_DEBUG[1]	5244	-512.5	32	75
313	T_DEBUG[0]	5290	-512.5	32	75
314	T_DEBUG[0]	5336	-512.5	32	75
315	T_SRAM	5382	-512.5	32	75
316	T_SRAM	5428	-512.5	32	75
317	DUMMY[34]	5474	-512.5	32	75
318	DUMMY[35]	5520	-512.5	32	75
319	T_EN_LSH	5566	-512.5	32	75
320	T_EN_LSH	5612	-512.5	32	75
321	T_VREF	5658	-512.5	32	75
322	T_VREF	5704	-512.5	32	75
323	T_IBIAS	5750	-512.5	32	75
324	T_IBIAS	5796	-512.5	32	75
325	T_TSEN_EXTIN	5842	-512.5	32	75
326	T_TSEN_EXTIN	5888	-512.5	32	75
327	T_VTSEN	5934	-512.5	32	75
328	T_VTSEN	5980	-512.5	32	75
329	T_ITSEN	6026	-512.5	32	75
330	T_ITSEN	6072	-512.5	32	75
331	DUMMY[36]	6118	-512.5	32	75
332	DUMMY[37]	6164	-512.5	32	75
333	DUMMY[38]	6210	-512.5	32	75
334	DUMMY[39]	6256	-512.5	32	75
335	VSHR	6302	-512.5	32	75
336	VSHR	6348	-512.5	32	75
337	VSHR	6394	-512.5	32	75
338	VSHR	6440	-512.5	32	75
339	VSHR	6486	-512.5	32	75
340	VSHR	6532	-512.5	32	75
341	VSHR	6578	-512.5	32	75
342	VSHR	6624	-512.5	32	75
343	VSHR	6670	-512.5	32	75
344	VSHR	6716	-512.5	32	75
345	VSHR	6762	-512.5	32	75
346	VSHR	6808	-512.5	32	75
347	VSHR	6854	-512.5	32	75
348	VSHR	6900	-512.5	32	75
349	VSHR	6946	-512.5	32	75
350	VSHR	6992	-512.5	32	75
351	DUMMY[40]	7038	-512.5	32	75
352	DUMMY[41]	7084	-512.5	32	75
353	DUMMY[42]	7130	-512.5	32	75
354	DUMMY[43]	7176	-512.5	32	75
355	DUMMY[44]	7222	-512.5	32	75
356	DUMMY[45]	7268	-512.5	32	75
357	VSSAR_S	7314	-512.5	32	75
358	FB	7360	-512.5	32	75
359	FB	7406	-512.5	32	75
360	VSSAR_S	7452	-512.5	32	75

No.	Name	X-axis	Y-axis	W	H
361	RESE	7498	-512.5	32	75
362	RESE	7544	-512.5	32	75
363	RESE	7590	-512.5	32	75
364	RESE	7636	-512.5	32	75
365	VSSAR_S	7682	-512.5	32	75
366	GDR	7728	-512.5	32	75
367	GDR	7774	-512.5	32	75
368	GDR	7820	-512.5	32	75
369	GDR	7866	-512.5	32	75
370	GDR	7912	-512.5	32	75
371	GDR	7958	-512.5	32	75
372	GDR	8004	-512.5	32	75
373	GDR	8050	-512.5	32	75
374	GDR	8096	-512.5	32	75
375	GDR	8142	-512.5	32	75
376	GDR	8188	-512.5	32	75
377	GDR	8234	-512.5	32	75
378	GDR	8280	-512.5	32	75
379	GDR	8326	-512.5	32	75
380	VSSAR_S	8372	-512.5	32	75
381	VCOM	8418	-512.5	32	75
382	VCOM	8464	-512.5	32	75
383	VCOM	8510	-512.5	32	75
384	VCOM	8556	-512.5	32	75
385	VCOM	8602	-512.5	32	75
386	VCOM	8648	-512.5	32	75
387	VCOM	8694	-512.5	32	75
388	VCOM	8740	-512.5	32	75
389	VCOM	8786	-512.5	32	75
390	VCOM	8832	-512.5	32	75
391	VCOM	8878	-512.5	32	75
392	VCOM	8924	-512.5	32	75
393	VCOM	8970	-512.5	32	75
394	DUMMY[46]	9016	-512.5	32	75
395	DUMMY[47]	9062	-512.5	32	75
396	DUMMY[48]	9169.5	500	12	90
397	DUMMY[49]	9156.5	381	12	90
398	DUMMY[50]	9144.5	500	12	90
399	DUMMY[51]	9131.5	381	12	90
400	G[0]	9119.5	500	12	90
401	G[2]	9106.5	381	12	90
402	G[4]	9094.5	500	12	90
403	G[6]	9081.5	381	12	90
404	G[8]	9069.5	500	12	90
405	G[10]	9056.5	381	12	90
406	G[12]	9044.5	500	12	90
407	G[14]	9031.5	381	12	90
408	G[16]	9019.5	500	12	90
409	G[18]	9006.5	381	12	90
410	G[20]	8994.5	500	12	90
411	G[22]	8981.5	381	12	90
412	G[24]	8969.5	500	12	90
413	G[26]	8956.5	381	12	90
414	G[28]	8944.5	500	12	90
415	G[30]	8931.5	381	12	90
416	G[32]	8919.5	500	12	90
417	G[34]	8906.5	381	12	90
418	G[36]	8894.5	500	12	90
419	G[38]	8881.5	381	12	90
420	G[40]	8869.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
421	G[42]	8856.5	381	12	90
422	G[44]	8844.5	500	12	90
423	G[46]	8831.5	381	12	90
424	G[48]	8819.5	500	12	90
425	G[50]	8806.5	381	12	90
426	G[52]	8794.5	500	12	90
427	G[54]	8781.5	381	12	90
428	G[56]	8769.5	500	12	90
429	G[58]	8756.5	381	12	90
430	G[60]	8744.5	500	12	90
431	G[62]	8731.5	381	12	90
432	G[64]	8719.5	500	12	90
433	G[66]	8706.5	381	12	90
434	G[68]	8694.5	500	12	90
435	G[70]	8681.5	381	12	90
436	G[72]	8669.5	500	12	90
437	G[74]	8656.5	381	12	90
438	G[76]	8644.5	500	12	90
439	G[78]	8631.5	381	12	90
440	G[80]	8619.5	500	12	90
441	G[82]	8606.5	381	12	90
442	G[84]	8594.5	500	12	90
443	G[86]	8581.5	381	12	90
444	G[88]	8569.5	500	12	90
445	G[90]	8556.5	381	12	90
446	G[92]	8544.5	500	12	90
447	G[94]	8531.5	381	12	90
448	G[96]	8519.5	500	12	90
449	G[98]	8506.5	381	12	90
450	G[100]	8494.5	500	12	90
451	G[102]	8481.5	381	12	90
452	G[104]	8469.5	500	12	90
453	G[106]	8456.5	381	12	90
454	G[108]	8444.5	500	12	90
455	G[110]	8431.5	381	12	90
456	G[112]	8419.5	500	12	90
457	G[114]	8406.5	381	12	90
458	G[116]	8394.5	500	12	90
459	G[118]	8381.5	381	12	90
460	G[120]	8369.5	500	12	90
461	G[122]	8356.5	381	12	90
462	G[124]	8344.5	500	12	90
463	G[126]	8331.5	381	12	90
464	G[128]	8319.5	500	12	90
465	G[130]	8306.5	381	12	90
466	G[132]	8294.5	500	12	90
467	G[134]	8281.5	381	12	90
468	G[136]	8269.5	500	12	90
469	G[138]	8256.5	381	12	90
470	G[140]	8244.5	500	12	90
471	G[142]	8231.5	381	12	90
472	G[144]	8219.5	500	12	90
473	G[146]	8206.5	381	12	90
474	G[148]	8194.5	500	12	90
475	G[150]	8181.5	381	12	90
476	G[152]	8169.5	500	12	90
477	G[154]	8156.5	381	12	90
478	G[156]	8144.5	500	12	90
479	G[158]	8131.5	381	12	90
480	G[160]	8119.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
481	G[162]	8106.5	381	12	90
482	G[164]	8094.5	500	12	90
483	G[166]	8081.5	381	12	90
484	G[168]	8069.5	500	12	90
485	G[170]	8056.5	381	12	90
486	G[172]	8044.5	500	12	90
487	G[174]	8031.5	381	12	90
488	G[176]	8019.5	500	12	90
489	G[178]	8006.5	381	12	90
490	G[180]	7994.5	500	12	90
491	G[182]	7981.5	381	12	90
492	G[184]	7969.5	500	12	90
493	G[186]	7956.5	381	12	90
494	G[188]	7944.5	500	12	90
495	G[190]	7931.5	381	12	90
496	G[192]	7919.5	500	12	90
497	G[194]	7906.5	381	12	90
498	G[196]	7894.5	500	12	90
499	G[198]	7881.5	381	12	90
500	G[200]	7869.5	500	12	90
501	G[202]	7856.5	381	12	90
502	G[204]	7844.5	500	12	90
503	G[206]	7831.5	381	12	90
504	G[208]	7819.5	500	12	90
505	G[210]	7806.5	381	12	90
506	G[212]	7794.5	500	12	90
507	G[214]	7781.5	381	12	90
508	G[216]	7769.5	500	12	90
509	G[218]	7756.5	381	12	90
510	G[220]	7744.5	500	12	90
511	G[222]	7731.5	381	12	90
512	G[224]	7719.5	500	12	90
513	G[226]	7706.5	381	12	90
514	G[228]	7694.5	500	12	90
515	G[230]	7681.5	381	12	90
516	G[232]	7669.5	500	12	90
517	G[234]	7656.5	381	12	90
518	G[236]	7644.5	500	12	90
519	G[238]	7631.5	381	12	90
520	G[240]	7619.5	500	12	90
521	G[242]	7606.5	381	12	90
522	G[244]	7594.5	500	12	90
523	G[246]	7581.5	381	12	90
524	G[248]	7569.5	500	12	90
525	G[250]	7556.5	381	12	90
526	G[252]	7544.5	500	12	90
527	G[254]	7531.5	381	12	90
528	G[256]	7519.5	500	12	90
529	G[258]	7506.5	381	12	90
530	G[260]	7494.5	500	12	90
531	G[262]	7481.5	381	12	90
532	G[264]	7469.5	500	12	90
533	G[266]	7456.5	381	12	90
534	G[268]	7444.5	500	12	90
535	G[270]	7431.5	381	12	90
536	G[272]	7419.5	500	12	90
537	G[274]	7406.5	381	12	90
538	G[276]	7394.5	500	12	90
539	G[278]	7381.5	381	12	90
540	G[280]	7369.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
541	G[282]	7356.5	381	12	90
542	G[284]	7344.5	500	12	90
543	G[286]	7331.5	381	12	90
544	G[288]	7319.5	500	12	90
545	G[290]	7306.5	381	12	90
546	G[292]	7294.5	500	12	90
547	G[294]	7281.5	381	12	90
548	G[296]	7269.5	500	12	90
549	G[298]	7256.5	381	12	90
550	G[300]	7244.5	500	12	90
551	G[302]	7231.5	381	12	90
552	G[304]	7219.5	500	12	90
553	G[306]	7206.5	381	12	90
554	G[308]	7194.5	500	12	90
555	G[310]	7181.5	381	12	90
556	G[312]	7169.5	500	12	90
557	G[314]	7156.5	381	12	90
558	G[316]	7144.5	500	12	90
559	G[318]	7131.5	381	12	90
560	G[320]	7119.5	500	12	90
561	G[322]	7106.5	381	12	90
562	G[324]	7094.5	500	12	90
563	G[326]	7081.5	381	12	90
564	G[328]	7069.5	500	12	90
565	G[330]	7056.5	381	12	90
566	G[332]	7044.5	500	12	90
567	G[334]	7031.5	381	12	90
568	G[336]	7019.5	500	12	90
569	G[338]	7006.5	381	12	90
570	G[340]	6994.5	500	12	90
571	G[342]	6981.5	381	12	90
572	G[344]	6969.5	500	12	90
573	G[346]	6956.5	381	12	90
574	G[348]	6944.5	500	12	90
575	G[350]	6931.5	381	12	90
576	G[352]	6919.5	500	12	90
577	G[354]	6906.5	381	12	90
578	G[356]	6894.5	500	12	90
579	G[358]	6881.5	381	12	90
580	G[360]	6869.5	500	12	90
581	G[362]	6856.5	381	12	90
582	G[364]	6844.5	500	12	90
583	G[366]	6831.5	381	12	90
584	G[368]	6819.5	500	12	90
585	G[370]	6806.5	381	12	90
586	G[372]	6794.5	500	12	90
587	G[374]	6781.5	381	12	90
588	G[376]	6769.5	500	12	90
589	G[378]	6756.5	381	12	90
590	G[380]	6744.5	500	12	90
591	G[382]	6731.5	381	12	90
592	G[384]	6719.5	500	12	90
593	G[386]	6706.5	381	12	90
594	G[388]	6694.5	500	12	90
595	G[390]	6681.5	381	12	90
596	G[392]	6669.5	500	12	90
597	G[394]	6656.5	381	12	90
598	G[396]	6644.5	500	12	90
599	G[398]	6631.5	381	12	90
600	G[400]	6619.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
601	G[402]	6606.5	381	12	90
602	G[404]	6594.5	500	12	90
603	G[406]	6581.5	381	12	90
604	G[408]	6569.5	500	12	90
605	G[410]	6556.5	381	12	90
606	G[412]	6544.5	500	12	90
607	G[414]	6531.5	381	12	90
608	G[416]	6519.5	500	12	90
609	G[418]	6506.5	381	12	90
610	G[420]	6494.5	500	12	90
611	G[422]	6481.5	381	12	90
612	G[424]	6469.5	500	12	90
613	G[426]	6456.5	381	12	90
614	G[428]	6444.5	500	12	90
615	G[430]	6431.5	381	12	90
616	G[432]	6419.5	500	12	90
617	G[434]	6406.5	381	12	90
618	G[436]	6394.5	500	12	90
619	G[438]	6381.5	381	12	90
620	G[440]	6369.5	500	12	90
621	G[442]	6356.5	381	12	90
622	G[444]	6344.5	500	12	90
623	G[446]	6331.5	381	12	90
624	G[448]	6319.5	500	12	90
625	G[450]	6306.5	381	12	90
626	G[452]	6294.5	500	12	90
627	G[454]	6281.5	381	12	90
628	G[456]	6269.5	500	12	90
629	G[458]	6256.5	381	12	90
630	G[460]	6244.5	500	12	90
631	G[462]	6231.5	381	12	90
632	G[464]	6219.5	500	12	90
633	G[466]	6206.5	381	12	90
634	G[468]	6194.5	500	12	90
635	G[470]	6181.5	381	12	90
636	G[472]	6169.5	500	12	90
637	G[474]	6156.5	381	12	90
638	G[476]	6144.5	500	12	90
639	G[478]	6131.5	381	12	90
640	G[480]	6119.5	500	12	90
641	G[482]	6106.5	381	12	90
642	G[484]	6094.5	500	12	90
643	G[486]	6081.5	381	12	90
644	G[488]	6069.5	500	12	90
645	G[490]	6056.5	381	12	90
646	G[492]	6044.5	500	12	90
647	G[494]	6031.5	381	12	90
648	G[496]	6019.5	500	12	90
649	G[498]	6006.5	381	12	90
650	G[500]	5994.5	500	12	90
651	G[502]	5981.5	381	12	90
652	G[504]	5969.5	500	12	90
653	G[506]	5956.5	381	12	90
654	G[508]	5944.5	500	12	90
655	G[510]	5931.5	381	12	90
656	G[512]	5919.5	500	12	90
657	G[514]	5906.5	381	12	90
658	G[516]	5894.5	500	12	90
659	G[518]	5881.5	381	12	90
660	G[520]	5869.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
661	G[522]	5856.5	381	12	90
662	G[524]	5844.5	500	12	90
663	G[526]	5831.5	381	12	90
664	G[528]	5819.5	500	12	90
665	G[530]	5806.5	381	12	90
666	G[532]	5794.5	500	12	90
667	G[534]	5781.5	381	12	90
668	G[536]	5769.5	500	12	90
669	G[538]	5756.5	381	12	90
670	G[540]	5744.5	500	12	90
671	G[542]	5731.5	381	12	90
672	G[544]	5719.5	500	12	90
673	G[546]	5706.5	381	12	90
674	G[548]	5694.5	500	12	90
675	G[550]	5681.5	381	12	90
676	G[552]	5669.5	500	12	90
677	G[554]	5656.5	381	12	90
678	G[556]	5644.5	500	12	90
679	G[558]	5631.5	381	12	90
680	G[560]	5619.5	500	12	90
681	G[562]	5606.5	381	12	90
682	G[564]	5594.5	500	12	90
683	G[566]	5581.5	381	12	90
684	G[568]	5569.5	500	12	90
685	G[570]	5556.5	381	12	90
686	G[572]	5544.5	500	12	90
687	G[574]	5531.5	381	12	90
688	G[576]	5519.5	500	12	90
689	G[578]	5506.5	381	12	90
690	G[580]	5494.5	500	12	90
691	G[582]	5481.5	381	12	90
692	G[584]	5469.5	500	12	90
693	G[586]	5456.5	381	12	90
694	G[588]	5444.5	500	12	90
695	G[590]	5431.5	381	12	90
696	G[592]	5419.5	500	12	90
697	G[594]	5406.5	381	12	90
698	G[596]	5394.5	500	12	90
699	G[598]	5381.5	381	12	90
700	DUMMY[52]	5369.5	500	12	90
701	DUMMY[53]	5356.5	381	12	90
702	DUMMY[54]	5344.5	500	12	90
703	DUMMY[55]	5331.5	381	12	90
704	DUMMY[56]	5232.5	500	12	90
705	DUMMY[57]	5219.5	381	12	90
706	VBD[1]	5206.5	500	12	90
707	S[0]	5193.5	381	12	90
708	S[1]	5180.5	500	12	90
709	S[2]	5167.5	381	12	90
710	S[3]	5154.5	500	12	90
711	S[4]	5141.5	381	12	90
712	S[5]	5128.5	500	12	90
713	S[6]	5115.5	381	12	90
714	S[7]	5102.5	500	12	90
715	S[8]	5089.5	381	12	90
716	S[9]	5076.5	500	12	90
717	S[10]	5063.5	381	12	90
718	S[11]	5050.5	500	12	90
719	S[12]	5037.5	381	12	90
720	S[13]	5024.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
721	S[14]	5011.5	381	12	90
722	S[15]	4998.5	500	12	90
723	S[16]	4985.5	381	12	90
724	S[17]	4972.5	500	12	90
725	S[18]	4959.5	381	12	90
726	S[19]	4946.5	500	12	90
727	S[20]	4933.5	381	12	90
728	S[21]	4920.5	500	12	90
729	S[22]	4907.5	381	12	90
730	S[23]	4894.5	500	12	90
731	S[24]	4881.5	381	12	90
732	S[25]	4868.5	500	12	90
733	S[26]	4855.5	381	12	90
734	S[27]	4842.5	500	12	90
735	S[28]	4829.5	381	12	90
736	S[29]	4816.5	500	12	90
737	S[30]	4803.5	381	12	90
738	S[31]	4790.5	500	12	90
739	S[32]	4777.5	381	12	90
740	S[33]	4764.5	500	12	90
741	S[34]	4751.5	381	12	90
742	S[35]	4738.5	500	12	90
743	S[36]	4725.5	381	12	90
744	S[37]	4712.5	500	12	90
745	S[38]	4699.5	381	12	90
746	S[39]	4686.5	500	12	90
747	S[40]	4673.5	381	12	90
748	S[41]	4660.5	500	12	90
749	S[42]	4647.5	381	12	90
750	S[43]	4634.5	500	12	90
751	S[44]	4621.5	381	12	90
752	S[45]	4608.5	500	12	90
753	S[46]	4595.5	381	12	90
754	S[47]	4582.5	500	12	90
755	S[48]	4569.5	381	12	90
756	S[49]	4556.5	500	12	90
757	S[50]	4543.5	381	12	90
758	S[51]	4530.5	500	12	90
759	S[52]	4517.5	381	12	90
760	S[53]	4504.5	500	12	90
761	S[54]	4491.5	381	12	90
762	S[55]	4478.5	500	12	90
763	S[56]	4465.5	381	12	90
764	S[57]	4452.5	500	12	90
765	S[58]	4439.5	381	12	90
766	S[59]	4426.5	500	12	90
767	S[60]	4413.5	381	12	90
768	S[61]	4400.5	500	12	90
769	S[62]	4387.5	381	12	90
770	S[63]	4374.5	500	12	90
771	S[64]	4361.5	381	12	90
772	S[65]	4348.5	500	12	90
773	S[66]	4335.5	381	12	90
774	S[67]	4322.5	500	12	90
775	S[68]	4309.5	381	12	90
776	S[69]	4296.5	500	12	90
777	S[70]	4283.5	381	12	90
778	S[71]	4270.5	500	12	90
779	S[72]	4257.5	381	12	90
780	S[73]	4244.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
781	S[74]	4231.5	381	12	90
782	S[75]	4218.5	500	12	90
783	S[76]	4205.5	381	12	90
784	S[77]	4192.5	500	12	90
785	S[78]	4179.5	381	12	90
786	S[79]	4166.5	500	12	90
787	S[80]	4153.5	381	12	90
788	S[81]	4140.5	500	12	90
789	S[82]	4127.5	381	12	90
790	S[83]	4114.5	500	12	90
791	S[84]	4101.5	381	12	90
792	S[85]	4088.5	500	12	90
793	S[86]	4075.5	381	12	90
794	S[87]	4062.5	500	12	90
795	S[88]	4049.5	381	12	90
796	S[89]	4036.5	500	12	90
797	S[90]	4023.5	381	12	90
798	S[91]	4010.5	500	12	90
799	S[92]	3997.5	381	12	90
800	S[93]	3984.5	500	12	90
801	S[94]	3971.5	381	12	90
802	S[95]	3958.5	500	12	90
803	S[96]	3945.5	381	12	90
804	S[97]	3932.5	500	12	90
805	S[98]	3919.5	381	12	90
806	S[99]	3906.5	500	12	90
807	S[100]	3893.5	381	12	90
808	S[101]	3880.5	500	12	90
809	S[102]	3867.5	381	12	90
810	S[103]	3854.5	500	12	90
811	S[104]	3841.5	381	12	90
812	S[105]	3828.5	500	12	90
813	S[106]	3815.5	381	12	90
814	S[107]	3802.5	500	12	90
815	S[108]	3789.5	381	12	90
816	S[109]	3776.5	500	12	90
817	S[110]	3763.5	381	12	90
818	S[111]	3750.5	500	12	90
819	S[112]	3737.5	381	12	90
820	S[113]	3724.5	500	12	90
821	S[114]	3711.5	381	12	90
822	S[115]	3698.5	500	12	90
823	S[116]	3685.5	381	12	90
824	S[117]	3672.5	500	12	90
825	S[118]	3659.5	381	12	90
826	S[119]	3646.5	500	12	90
827	S[120]	3633.5	381	12	90
828	S[121]	3620.5	500	12	90
829	S[122]	3607.5	381	12	90
830	S[123]	3594.5	500	12	90
831	S[124]	3581.5	381	12	90
832	S[125]	3568.5	500	12	90
833	S[126]	3555.5	381	12	90
834	S[127]	3542.5	500	12	90
835	S[128]	3529.5	381	12	90
836	S[129]	3516.5	500	12	90
837	S[130]	3503.5	381	12	90
838	S[131]	3490.5	500	12	90
839	S[132]	3477.5	381	12	90
840	S[133]	3464.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
841	S[134]	3451.5	381	12	90
842	S[135]	3438.5	500	12	90
843	S[136]	3425.5	381	12	90
844	S[137]	3412.5	500	12	90
845	S[138]	3399.5	381	12	90
846	S[139]	3386.5	500	12	90
847	S[140]	3373.5	381	12	90
848	S[141]	3360.5	500	12	90
849	S[142]	3347.5	381	12	90
850	S[143]	3334.5	500	12	90
851	S[144]	3321.5	381	12	90
852	S[145]	3308.5	500	12	90
853	S[146]	3295.5	381	12	90
854	S[147]	3282.5	500	12	90
855	S[148]	3269.5	381	12	90
856	S[149]	3256.5	500	12	90
857	S[150]	3243.5	381	12	90
858	S[151]	3230.5	500	12	90
859	S[152]	3217.5	381	12	90
860	S[153]	3204.5	500	12	90
861	S[154]	3191.5	381	12	90
862	S[155]	3178.5	500	12	90
863	S[156]	3165.5	381	12	90
864	S[157]	3152.5	500	12	90
865	S[158]	3139.5	381	12	90
866	S[159]	3126.5	500	12	90
867	S[160]	3113.5	381	12	90
868	S[161]	3100.5	500	12	90
869	S[162]	3087.5	381	12	90
870	S[163]	3074.5	500	12	90
871	S[164]	3061.5	381	12	90
872	S[165]	3048.5	500	12	90
873	S[166]	3035.5	381	12	90
874	S[167]	3022.5	500	12	90
875	S[168]	3009.5	381	12	90
876	S[169]	2996.5	500	12	90
877	S[170]	2983.5	381	12	90
878	S[171]	2970.5	500	12	90
879	S[172]	2957.5	381	12	90
880	S[173]	2944.5	500	12	90
881	S[174]	2931.5	381	12	90
882	S[175]	2918.5	500	12	90
883	S[176]	2905.5	381	12	90
884	S[177]	2892.5	500	12	90
885	S[178]	2879.5	381	12	90
886	S[179]	2866.5	500	12	90
887	S[180]	2853.5	381	12	90
888	S[181]	2840.5	500	12	90
889	S[182]	2827.5	381	12	90
890	S[183]	2814.5	500	12	90
891	S[184]	2801.5	381	12	90
892	S[185]	2788.5	500	12	90
893	S[186]	2775.5	381	12	90
894	S[187]	2762.5	500	12	90
895	S[188]	2749.5	381	12	90
896	S[189]	2736.5	500	12	90
897	S[190]	2723.5	381	12	90
898	S[191]	2710.5	500	12	90
899	S[192]	2697.5	381	12	90
900	S[193]	2684.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
901	S[194]	2671.5	381	12	90
902	S[195]	2658.5	500	12	90
903	S[196]	2645.5	381	12	90
904	S[197]	2632.5	500	12	90
905	S[198]	2619.5	381	12	90
906	S[199]	2606.5	500	12	90
907	S[200]	2593.5	381	12	90
908	S[201]	2580.5	500	12	90
909	S[202]	2567.5	381	12	90
910	S[203]	2554.5	500	12	90
911	S[204]	2541.5	381	12	90
912	S[205]	2528.5	500	12	90
913	S[206]	2515.5	381	12	90
914	S[207]	2502.5	500	12	90
915	S[208]	2489.5	381	12	90
916	S[209]	2476.5	500	12	90
917	S[210]	2463.5	381	12	90
918	S[211]	2450.5	500	12	90
919	S[212]	2437.5	381	12	90
920	S[213]	2424.5	500	12	90
921	S[214]	2411.5	381	12	90
922	S[215]	2398.5	500	12	90
923	S[216]	2385.5	381	12	90
924	S[217]	2372.5	500	12	90
925	S[218]	2359.5	381	12	90
926	S[219]	2346.5	500	12	90
927	S[220]	2333.5	381	12	90
928	S[221]	2320.5	500	12	90
929	S[222]	2307.5	381	12	90
930	S[223]	2294.5	500	12	90
931	S[224]	2281.5	381	12	90
932	S[225]	2268.5	500	12	90
933	S[226]	2255.5	381	12	90
934	S[227]	2242.5	500	12	90
935	S[228]	2229.5	381	12	90
936	S[229]	2216.5	500	12	90
937	S[230]	2203.5	381	12	90
938	S[231]	2190.5	500	12	90
939	S[232]	2177.5	381	12	90
940	S[233]	2164.5	500	12	90
941	S[234]	2151.5	381	12	90
942	S[235]	2138.5	500	12	90
943	S[236]	2125.5	381	12	90
944	S[237]	2112.5	500	12	90
945	S[238]	2099.5	381	12	90
946	S[239]	2086.5	500	12	90
947	S[240]	2073.5	381	12	90
948	S[241]	2060.5	500	12	90
949	S[242]	2047.5	381	12	90
950	S[243]	2034.5	500	12	90
951	S[244]	2021.5	381	12	90
952	S[245]	2008.5	500	12	90
953	S[246]	1995.5	381	12	90
954	S[247]	1982.5	500	12	90
955	S[248]	1969.5	381	12	90
956	S[249]	1956.5	500	12	90
957	S[250]	1943.5	381	12	90
958	S[251]	1930.5	500	12	90
959	S[252]	1917.5	381	12	90
960	S[253]	1904.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
961	S[254]	1891.5	381	12	90
962	S[255]	1878.5	500	12	90
963	S[256]	1865.5	381	12	90
964	S[257]	1852.5	500	12	90
965	S[258]	1839.5	381	12	90
966	S[259]	1826.5	500	12	90
967	S[260]	1813.5	381	12	90
968	S[261]	1800.5	500	12	90
969	S[262]	1787.5	381	12	90
970	S[263]	1774.5	500	12	90
971	S[264]	1761.5	381	12	90
972	S[265]	1748.5	500	12	90
973	S[266]	1735.5	381	12	90
974	S[267]	1722.5	500	12	90
975	S[268]	1709.5	381	12	90
976	S[269]	1696.5	500	12	90
977	S[270]	1683.5	381	12	90
978	S[271]	1670.5	500	12	90
979	S[272]	1657.5	381	12	90
980	S[273]	1644.5	500	12	90
981	S[274]	1631.5	381	12	90
982	S[275]	1618.5	500	12	90
983	S[276]	1605.5	381	12	90
984	S[277]	1592.5	500	12	90
985	S[278]	1579.5	381	12	90
986	S[279]	1566.5	500	12	90
987	S[280]	1553.5	381	12	90
988	S[281]	1540.5	500	12	90
989	S[282]	1527.5	381	12	90
990	S[283]	1514.5	500	12	90
991	S[284]	1501.5	381	12	90
992	S[285]	1488.5	500	12	90
993	S[286]	1475.5	381	12	90
994	S[287]	1462.5	500	12	90
995	S[288]	1449.5	381	12	90
996	S[289]	1436.5	500	12	90
997	S[290]	1423.5	381	12	90
998	S[291]	1410.5	500	12	90
999	S[292]	1397.5	381	12	90
1000	S[293]	1384.5	500	12	90
1001	S[294]	1371.5	381	12	90
1002	S[295]	1358.5	500	12	90
1003	S[296]	1345.5	381	12	90
1004	S[297]	1332.5	500	12	90
1005	S[298]	1319.5	381	12	90
1006	S[299]	1306.5	500	12	90
1007	S[300]	1293.5	381	12	90
1008	S[301]	1280.5	500	12	90
1009	S[302]	1267.5	381	12	90
1010	S[303]	1254.5	500	12	90
1011	S[304]	1241.5	381	12	90
1012	S[305]	1228.5	500	12	90
1013	S[306]	1215.5	381	12	90
1014	S[307]	1202.5	500	12	90
1015	S[308]	1189.5	381	12	90
1016	S[309]	1176.5	500	12	90
1017	S[310]	1163.5	381	12	90
1018	S[311]	1150.5	500	12	90
1019	S[312]	1137.5	381	12	90
1020	S[313]	1124.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1021	S[314]	1111.5	381	12	90
1022	S[315]	1098.5	500	12	90
1023	S[316]	1085.5	381	12	90
1024	S[317]	1072.5	500	12	90
1025	S[318]	1059.5	381	12	90
1026	S[319]	1046.5	500	12	90
1027	S[320]	1033.5	381	12	90
1028	S[321]	1020.5	500	12	90
1029	S[322]	1007.5	381	12	90
1030	S[323]	994.5	500	12	90
1031	S[324]	981.5	381	12	90
1032	S[325]	968.5	500	12	90
1033	S[326]	955.5	381	12	90
1034	S[327]	942.5	500	12	90
1035	S[328]	929.5	381	12	90
1036	S[329]	916.5	500	12	90
1037	S[330]	903.5	381	12	90
1038	S[331]	890.5	500	12	90
1039	S[332]	877.5	381	12	90
1040	S[333]	864.5	500	12	90
1041	S[334]	851.5	381	12	90
1042	S[335]	838.5	500	12	90
1043	S[336]	825.5	381	12	90
1044	S[337]	812.5	500	12	90
1045	S[338]	799.5	381	12	90
1046	S[339]	786.5	500	12	90
1047	S[340]	773.5	381	12	90
1048	S[341]	760.5	500	12	90
1049	S[342]	747.5	381	12	90
1050	S[343]	734.5	500	12	90
1051	S[344]	721.5	381	12	90
1052	S[345]	708.5	500	12	90
1053	S[346]	695.5	381	12	90
1054	S[347]	682.5	500	12	90
1055	S[348]	669.5	381	12	90
1056	S[349]	656.5	500	12	90
1057	S[350]	643.5	381	12	90
1058	S[351]	630.5	500	12	90
1059	S[352]	617.5	381	12	90
1060	S[353]	604.5	500	12	90
1061	S[354]	591.5	381	12	90
1062	S[355]	578.5	500	12	90
1063	S[356]	565.5	381	12	90
1064	S[357]	552.5	500	12	90
1065	S[358]	539.5	381	12	90
1066	S[359]	526.5	500	12	90
1067	S[360]	513.5	381	12	90
1068	S[361]	500.5	500	12	90
1069	S[362]	487.5	381	12	90
1070	S[363]	474.5	500	12	90
1071	S[364]	461.5	381	12	90
1072	S[365]	448.5	500	12	90
1073	S[366]	435.5	381	12	90
1074	S[367]	422.5	500	12	90
1075	S[368]	409.5	381	12	90
1076	S[369]	396.5	500	12	90
1077	S[370]	383.5	381	12	90
1078	S[371]	370.5	500	12	90
1079	S[372]	357.5	381	12	90
1080	S[373]	344.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1081	S[374]	331.5	381	12	90
1082	S[375]	318.5	500	12	90
1083	S[376]	305.5	381	12	90
1084	S[377]	292.5	500	12	90
1085	S[378]	279.5	381	12	90
1086	S[379]	266.5	500	12	90
1087	S[380]	253.5	381	12	90
1088	S[381]	240.5	500	12	90
1089	S[382]	227.5	381	12	90
1090	S[383]	214.5	500	12	90
1091	S[384]	201.5	381	12	90
1092	S[385]	188.5	500	12	90
1093	S[386]	175.5	381	12	90
1094	S[387]	162.5	500	12	90
1095	S[388]	149.5	381	12	90
1096	S[389]	136.5	500	12	90
1097	S[390]	123.5	381	12	90
1098	S[391]	110.5	500	12	90
1099	S[392]	97.5	381	12	90
1100	S[393]	84.5	500	12	90
1101	S[394]	71.5	381	12	90
1102	S[395]	58.5	500	12	90
1103	S[396]	45.5	381	12	90
1104	S[397]	32.5	500	12	90
1105	S[398]	19.5	381	12	90
1106	S[399]	6.5	500	12	90
1107	S[400]	-6.5	381	12	90
1108	S[401]	-19.5	500	12	90
1109	S[402]	-32.5	381	12	90
1110	S[403]	-45.5	500	12	90
1111	S[404]	-58.5	381	12	90
1112	S[405]	-71.5	500	12	90
1113	S[406]	-84.5	381	12	90
1114	S[407]	-97.5	500	12	90
1115	S[408]	-110.5	381	12	90
1116	S[409]	-123.5	500	12	90
1117	S[410]	-136.5	381	12	90
1118	S[411]	-149.5	500	12	90
1119	S[412]	-162.5	381	12	90
1120	S[413]	-175.5	500	12	90
1121	S[414]	-188.5	381	12	90
1122	S[415]	-201.5	500	12	90
1123	S[416]	-214.5	381	12	90
1124	S[417]	-227.5	500	12	90
1125	S[418]	-240.5	381	12	90
1126	S[419]	-253.5	500	12	90
1127	S[420]	-266.5	381	12	90
1128	S[421]	-279.5	500	12	90
1129	S[422]	-292.5	381	12	90
1130	S[423]	-305.5	500	12	90
1131	S[424]	-318.5	381	12	90
1132	S[425]	-331.5	500	12	90
1133	S[426]	-344.5	381	12	90
1134	S[427]	-357.5	500	12	90
1135	S[428]	-370.5	381	12	90
1136	S[429]	-383.5	500	12	90
1137	S[430]	-396.5	381	12	90
1138	S[431]	-409.5	500	12	90
1139	S[432]	-422.5	381	12	90
1140	S[433]	-435.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1141	S[434]	-448.5	381	12	90
1142	S[435]	-461.5	500	12	90
1143	S[436]	-474.5	381	12	90
1144	S[437]	-487.5	500	12	90
1145	S[438]	-500.5	381	12	90
1146	S[439]	-513.5	500	12	90
1147	S[440]	-526.5	381	12	90
1148	S[441]	-539.5	500	12	90
1149	S[442]	-552.5	381	12	90
1150	S[443]	-565.5	500	12	90
1151	S[444]	-578.5	381	12	90
1152	S[445]	-591.5	500	12	90
1153	S[446]	-604.5	381	12	90
1154	S[447]	-617.5	500	12	90
1155	S[448]	-630.5	381	12	90
1156	S[449]	-643.5	500	12	90
1157	S[450]	-656.5	381	12	90
1158	S[451]	-669.5	500	12	90
1159	S[452]	-682.5	381	12	90
1160	S[453]	-695.5	500	12	90
1161	S[454]	-708.5	381	12	90
1162	S[455]	-721.5	500	12	90
1163	S[456]	-734.5	381	12	90
1164	S[457]	-747.5	500	12	90
1165	S[458]	-760.5	381	12	90
1166	S[459]	-773.5	500	12	90
1167	S[460]	-786.5	381	12	90
1168	S[461]	-799.5	500	12	90
1169	S[462]	-812.5	381	12	90
1170	S[463]	-825.5	500	12	90
1171	S[464]	-838.5	381	12	90
1172	S[465]	-851.5	500	12	90
1173	S[466]	-864.5	381	12	90
1174	S[467]	-877.5	500	12	90
1175	S[468]	-890.5	381	12	90
1176	S[469]	-903.5	500	12	90
1177	S[470]	-916.5	381	12	90
1178	S[471]	-929.5	500	12	90
1179	S[472]	-942.5	381	12	90
1180	S[473]	-955.5	500	12	90
1181	S[474]	-968.5	381	12	90
1182	S[475]	-981.5	500	12	90
1183	S[476]	-994.5	381	12	90
1184	S[477]	-1007.5	500	12	90
1185	S[478]	-1020.5	381	12	90
1186	S[479]	-1033.5	500	12	90
1187	S[480]	-1046.5	381	12	90
1188	S[481]	-1059.5	500	12	90
1189	S[482]	-1072.5	381	12	90
1190	S[483]	-1085.5	500	12	90
1191	S[484]	-1098.5	381	12	90
1192	S[485]	-1111.5	500	12	90
1193	S[486]	-1124.5	381	12	90
1194	S[487]	-1137.5	500	12	90
1195	S[488]	-1150.5	381	12	90
1196	S[489]	-1163.5	500	12	90
1197	S[490]	-1176.5	381	12	90
1198	S[491]	-1189.5	500	12	90
1199	S[492]	-1202.5	381	12	90
1200	S[493]	-1215.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1201	S[494]	-1228.5	381	12	90
1202	S[495]	-1241.5	500	12	90
1203	S[496]	-1254.5	381	12	90
1204	S[497]	-1267.5	500	12	90
1205	S[498]	-1280.5	381	12	90
1206	S[499]	-1293.5	500	12	90
1207	S[500]	-1306.5	381	12	90
1208	S[501]	-1319.5	500	12	90
1209	S[502]	-1332.5	381	12	90
1210	S[503]	-1345.5	500	12	90
1211	S[504]	-1358.5	381	12	90
1212	S[505]	-1371.5	500	12	90
1213	S[506]	-1384.5	381	12	90
1214	S[507]	-1397.5	500	12	90
1215	S[508]	-1410.5	381	12	90
1216	S[509]	-1423.5	500	12	90
1217	S[510]	-1436.5	381	12	90
1218	S[511]	-1449.5	500	12	90
1219	S[512]	-1462.5	381	12	90
1220	S[513]	-1475.5	500	12	90
1221	S[514]	-1488.5	381	12	90
1222	S[515]	-1501.5	500	12	90
1223	S[516]	-1514.5	381	12	90
1224	S[517]	-1527.5	500	12	90
1225	S[518]	-1540.5	381	12	90
1226	S[519]	-1553.5	500	12	90
1227	S[520]	-1566.5	381	12	90
1228	S[521]	-1579.5	500	12	90
1229	S[522]	-1592.5	381	12	90
1230	S[523]	-1605.5	500	12	90
1231	S[524]	-1618.5	381	12	90
1232	S[525]	-1631.5	500	12	90
1233	S[526]	-1644.5	381	12	90
1234	S[527]	-1657.5	500	12	90
1235	S[528]	-1670.5	381	12	90
1236	S[529]	-1683.5	500	12	90
1237	S[530]	-1696.5	381	12	90
1238	S[531]	-1709.5	500	12	90
1239	S[532]	-1722.5	381	12	90
1240	S[533]	-1735.5	500	12	90
1241	S[534]	-1748.5	381	12	90
1242	S[535]	-1761.5	500	12	90
1243	S[536]	-1774.5	381	12	90
1244	S[537]	-1787.5	500	12	90
1245	S[538]	-1800.5	381	12	90
1246	S[539]	-1813.5	500	12	90
1247	S[540]	-1826.5	381	12	90
1248	S[541]	-1839.5	500	12	90
1249	S[542]	-1852.5	381	12	90
1250	S[543]	-1865.5	500	12	90
1251	S[544]	-1878.5	381	12	90
1252	S[545]	-1891.5	500	12	90
1253	S[546]	-1904.5	381	12	90
1254	S[547]	-1917.5	500	12	90
1255	S[548]	-1930.5	381	12	90
1256	S[549]	-1943.5	500	12	90
1257	S[550]	-1956.5	381	12	90
1258	S[551]	-1969.5	500	12	90
1259	S[552]	-1982.5	381	12	90
1260	S[553]	-1995.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1261	S[554]	-2008.5	381	12	90
1262	S[555]	-2021.5	500	12	90
1263	S[556]	-2034.5	381	12	90
1264	S[557]	-2047.5	500	12	90
1265	S[558]	-2060.5	381	12	90
1266	S[559]	-2073.5	500	12	90
1267	S[560]	-2086.5	381	12	90
1268	S[561]	-2099.5	500	12	90
1269	S[562]	-2112.5	381	12	90
1270	S[563]	-2125.5	500	12	90
1271	S[564]	-2138.5	381	12	90
1272	S[565]	-2151.5	500	12	90
1273	S[566]	-2164.5	381	12	90
1274	S[567]	-2177.5	500	12	90
1275	S[568]	-2190.5	381	12	90
1276	S[569]	-2203.5	500	12	90
1277	S[570]	-2216.5	381	12	90
1278	S[571]	-2229.5	500	12	90
1279	S[572]	-2242.5	381	12	90
1280	S[573]	-2255.5	500	12	90
1281	S[574]	-2268.5	381	12	90
1282	S[575]	-2281.5	500	12	90
1283	S[576]	-2294.5	381	12	90
1284	S[577]	-2307.5	500	12	90
1285	S[578]	-2320.5	381	12	90
1286	S[579]	-2333.5	500	12	90
1287	S[580]	-2346.5	381	12	90
1288	S[581]	-2359.5	500	12	90
1289	S[582]	-2372.5	381	12	90
1290	S[583]	-2385.5	500	12	90
1291	S[584]	-2398.5	381	12	90
1292	S[585]	-2411.5	500	12	90
1293	S[586]	-2424.5	381	12	90
1294	S[587]	-2437.5	500	12	90
1295	S[588]	-2450.5	381	12	90
1296	S[589]	-2463.5	500	12	90
1297	S[590]	-2476.5	381	12	90
1298	S[591]	-2489.5	500	12	90
1299	S[592]	-2502.5	381	12	90
1300	S[593]	-2515.5	500	12	90
1301	S[594]	-2528.5	381	12	90
1302	S[595]	-2541.5	500	12	90
1303	S[596]	-2554.5	381	12	90
1304	S[597]	-2567.5	500	12	90
1305	S[598]	-2580.5	381	12	90
1306	S[599]	-2593.5	500	12	90
1307	S[600]	-2606.5	381	12	90
1308	S[601]	-2619.5	500	12	90
1309	S[602]	-2632.5	381	12	90
1310	S[603]	-2645.5	500	12	90
1311	S[604]	-2658.5	381	12	90
1312	S[605]	-2671.5	500	12	90
1313	S[606]	-2684.5	381	12	90
1314	S[607]	-2697.5	500	12	90
1315	S[608]	-2710.5	381	12	90
1316	S[609]	-2723.5	500	12	90
1317	S[610]	-2736.5	381	12	90
1318	S[611]	-2749.5	500	12	90
1319	S[612]	-2762.5	381	12	90
1320	S[613]	-2775.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1321	S[614]	-2788.5	381	12	90
1322	S[615]	-2801.5	500	12	90
1323	S[616]	-2814.5	381	12	90
1324	S[617]	-2827.5	500	12	90
1325	S[618]	-2840.5	381	12	90
1326	S[619]	-2853.5	500	12	90
1327	S[620]	-2866.5	381	12	90
1328	S[621]	-2879.5	500	12	90
1329	S[622]	-2892.5	381	12	90
1330	S[623]	-2905.5	500	12	90
1331	S[624]	-2918.5	381	12	90
1332	S[625]	-2931.5	500	12	90
1333	S[626]	-2944.5	381	12	90
1334	S[627]	-2957.5	500	12	90
1335	S[628]	-2970.5	381	12	90
1336	S[629]	-2983.5	500	12	90
1337	S[630]	-2996.5	381	12	90
1338	S[631]	-3009.5	500	12	90
1339	S[632]	-3022.5	381	12	90
1340	S[633]	-3035.5	500	12	90
1341	S[634]	-3048.5	381	12	90
1342	S[635]	-3061.5	500	12	90
1343	S[636]	-3074.5	381	12	90
1344	S[637]	-3087.5	500	12	90
1345	S[638]	-3100.5	381	12	90
1346	S[639]	-3113.5	500	12	90
1347	S[640]	-3126.5	381	12	90
1348	S[641]	-3139.5	500	12	90
1349	S[642]	-3152.5	381	12	90
1350	S[643]	-3165.5	500	12	90
1351	S[644]	-3178.5	381	12	90
1352	S[645]	-3191.5	500	12	90
1353	S[646]	-3204.5	381	12	90
1354	S[647]	-3217.5	500	12	90
1355	S[648]	-3230.5	381	12	90
1356	S[649]	-3243.5	500	12	90
1357	S[650]	-3256.5	381	12	90
1358	S[651]	-3269.5	500	12	90
1359	S[652]	-3282.5	381	12	90
1360	S[653]	-3295.5	500	12	90
1361	S[654]	-3308.5	381	12	90
1362	S[655]	-3321.5	500	12	90
1363	S[656]	-3334.5	381	12	90
1364	S[657]	-3347.5	500	12	90
1365	S[658]	-3360.5	381	12	90
1366	S[659]	-3373.5	500	12	90
1367	S[660]	-3386.5	381	12	90
1368	S[661]	-3399.5	500	12	90
1369	S[662]	-3412.5	381	12	90
1370	S[663]	-3425.5	500	12	90
1371	S[664]	-3438.5	381	12	90
1372	S[665]	-3451.5	500	12	90
1373	S[666]	-3464.5	381	12	90
1374	S[667]	-3477.5	500	12	90
1375	S[668]	-3490.5	381	12	90
1376	S[669]	-3503.5	500	12	90
1377	S[670]	-3516.5	381	12	90
1378	S[671]	-3529.5	500	12	90
1379	S[672]	-3542.5	381	12	90
1380	S[673]	-3555.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1381	S[674]	-3568.5	381	12	90
1382	S[675]	-3581.5	500	12	90
1383	S[676]	-3594.5	381	12	90
1384	S[677]	-3607.5	500	12	90
1385	S[678]	-3620.5	381	12	90
1386	S[679]	-3633.5	500	12	90
1387	S[680]	-3646.5	381	12	90
1388	S[681]	-3659.5	500	12	90
1389	S[682]	-3672.5	381	12	90
1390	S[683]	-3685.5	500	12	90
1391	S[684]	-3698.5	381	12	90
1392	S[685]	-3711.5	500	12	90
1393	S[686]	-3724.5	381	12	90
1394	S[687]	-3737.5	500	12	90
1395	S[688]	-3750.5	381	12	90
1396	S[689]	-3763.5	500	12	90
1397	S[690]	-3776.5	381	12	90
1398	S[691]	-3789.5	500	12	90
1399	S[692]	-3802.5	381	12	90
1400	S[693]	-3815.5	500	12	90
1401	S[694]	-3828.5	381	12	90
1402	S[695]	-3841.5	500	12	90
1403	S[696]	-3854.5	381	12	90
1404	S[697]	-3867.5	500	12	90
1405	S[698]	-3880.5	381	12	90
1406	S[699]	-3893.5	500	12	90
1407	S[700]	-3906.5	381	12	90
1408	S[701]	-3919.5	500	12	90
1409	S[702]	-3932.5	381	12	90
1410	S[703]	-3945.5	500	12	90
1411	S[704]	-3958.5	381	12	90
1412	S[705]	-3971.5	500	12	90
1413	S[706]	-3984.5	381	12	90
1414	S[707]	-3997.5	500	12	90
1415	S[708]	-4010.5	381	12	90
1416	S[709]	-4023.5	500	12	90
1417	S[710]	-4036.5	381	12	90
1418	S[711]	-4049.5	500	12	90
1419	S[712]	-4062.5	381	12	90
1420	S[713]	-4075.5	500	12	90
1421	S[714]	-4088.5	381	12	90
1422	S[715]	-4101.5	500	12	90
1423	S[716]	-4114.5	381	12	90
1424	S[717]	-4127.5	500	12	90
1425	S[718]	-4140.5	381	12	90
1426	S[719]	-4153.5	500	12	90
1427	S[720]	-4166.5	381	12	90
1428	S[721]	-4179.5	500	12	90
1429	S[722]	-4192.5	381	12	90
1430	S[723]	-4205.5	500	12	90
1431	S[724]	-4218.5	381	12	90
1432	S[725]	-4231.5	500	12	90
1433	S[726]	-4244.5	381	12	90
1434	S[727]	-4257.5	500	12	90
1435	S[728]	-4270.5	381	12	90
1436	S[729]	-4283.5	500	12	90
1437	S[730]	-4296.5	381	12	90
1438	S[731]	-4309.5	500	12	90
1439	S[732]	-4322.5	381	12	90
1440	S[733]	-4335.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1441	S[734]	-4348.5	381	12	90
1442	S[735]	-4361.5	500	12	90
1443	S[736]	-4374.5	381	12	90
1444	S[737]	-4387.5	500	12	90
1445	S[738]	-4400.5	381	12	90
1446	S[739]	-4413.5	500	12	90
1447	S[740]	-4426.5	381	12	90
1448	S[741]	-4439.5	500	12	90
1449	S[742]	-4452.5	381	12	90
1450	S[743]	-4465.5	500	12	90
1451	S[744]	-4478.5	381	12	90
1452	S[745]	-4491.5	500	12	90
1453	S[746]	-4504.5	381	12	90
1454	S[747]	-4517.5	500	12	90
1455	S[748]	-4530.5	381	12	90
1456	S[749]	-4543.5	500	12	90
1457	S[750]	-4556.5	381	12	90
1458	S[751]	-4569.5	500	12	90
1459	S[752]	-4582.5	381	12	90
1460	S[753]	-4595.5	500	12	90
1461	S[754]	-4608.5	381	12	90
1462	S[755]	-4621.5	500	12	90
1463	S[756]	-4634.5	381	12	90
1464	S[757]	-4647.5	500	12	90
1465	S[758]	-4660.5	381	12	90
1466	S[759]	-4673.5	500	12	90
1467	S[760]	-4686.5	381	12	90
1468	S[761]	-4699.5	500	12	90
1469	S[762]	-4712.5	381	12	90
1470	S[763]	-4725.5	500	12	90
1471	S[764]	-4738.5	381	12	90
1472	S[765]	-4751.5	500	12	90
1473	S[766]	-4764.5	381	12	90
1474	S[767]	-4777.5	500	12	90
1475	S[768]	-4790.5	381	12	90
1476	S[769]	-4803.5	500	12	90
1477	S[770]	-4816.5	381	12	90
1478	S[771]	-4829.5	500	12	90
1479	S[772]	-4842.5	381	12	90
1480	S[773]	-4855.5	500	12	90
1481	S[774]	-4868.5	381	12	90
1482	S[775]	-4881.5	500	12	90
1483	S[776]	-4894.5	381	12	90
1484	S[777]	-4907.5	500	12	90
1485	S[778]	-4920.5	381	12	90
1486	S[779]	-4933.5	500	12	90
1487	S[780]	-4946.5	381	12	90
1488	S[781]	-4959.5	500	12	90
1489	S[782]	-4972.5	381	12	90
1490	S[783]	-4985.5	500	12	90
1491	S[784]	-4998.5	381	12	90
1492	S[785]	-5011.5	500	12	90
1493	S[786]	-5024.5	381	12	90
1494	S[787]	-5037.5	500	12	90
1495	S[788]	-5050.5	381	12	90
1496	S[789]	-5063.5	500	12	90
1497	S[790]	-5076.5	381	12	90
1498	S[791]	-5089.5	500	12	90
1499	S[792]	-5102.5	381	12	90
1500	S[793]	-5115.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1501	S[794]	-5128.5	381	12	90
1502	S[795]	-5141.5	500	12	90
1503	S[796]	-5154.5	381	12	90
1504	S[797]	-5167.5	500	12	90
1505	S[798]	-5180.5	381	12	90
1506	S[799]	-5193.5	500	12	90
1507	VBD[2]	-5206.5	381	12	90
1508	DUMMY[58]	-5219.5	500	12	90
1509	DUMMY[59]	-5232.5	381	12	90
1510	DUMMY[60]	-5331.5	500	12	90
1511	DUMMY[61]	-5344.5	381	12	90
1512	DUMMY[62]	-5356.5	500	12	90
1513	DUMMY[63]	-5369.5	381	12	90
1514	G[599]	-5381.5	500	12	90
1515	G[597]	-5394.5	381	12	90
1516	G[595]	-5406.5	500	12	90
1517	G[593]	-5419.5	381	12	90
1518	G[591]	-5431.5	500	12	90
1519	G[589]	-5444.5	381	12	90
1520	G[587]	-5456.5	500	12	90
1521	G[585]	-5469.5	381	12	90
1522	G[583]	-5481.5	500	12	90
1523	G[581]	-5494.5	381	12	90
1524	G[579]	-5506.5	500	12	90
1525	G[577]	-5519.5	381	12	90
1526	G[575]	-5531.5	500	12	90
1527	G[573]	-5544.5	381	12	90
1528	G[571]	-5556.5	500	12	90
1529	G[569]	-5569.5	381	12	90
1530	G[567]	-5581.5	500	12	90
1531	G[565]	-5594.5	381	12	90
1532	G[563]	-5606.5	500	12	90
1533	G[561]	-5619.5	381	12	90
1534	G[559]	-5631.5	500	12	90
1535	G[557]	-5644.5	381	12	90
1536	G[555]	-5656.5	500	12	90
1537	G[553]	-5669.5	381	12	90
1538	G[551]	-5681.5	500	12	90
1539	G[549]	-5694.5	381	12	90
1540	G[547]	-5706.5	500	12	90
1541	G[545]	-5719.5	381	12	90
1542	G[543]	-5731.5	500	12	90
1543	G[541]	-5744.5	381	12	90
1544	G[539]	-5756.5	500	12	90
1545	G[537]	-5769.5	381	12	90
1546	G[535]	-5781.5	500	12	90
1547	G[533]	-5794.5	381	12	90
1548	G[531]	-5806.5	500	12	90
1549	G[529]	-5819.5	381	12	90
1550	G[527]	-5831.5	500	12	90
1551	G[525]	-5844.5	381	12	90
1552	G[523]	-5856.5	500	12	90
1553	G[521]	-5869.5	381	12	90
1554	G[519]	-5881.5	500	12	90
1555	G[517]	-5894.5	381	12	90
1556	G[515]	-5906.5	500	12	90
1557	G[513]	-5919.5	381	12	90
1558	G[511]	-5931.5	500	12	90
1559	G[509]	-5944.5	381	12	90
1560	G[507]	-5956.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1561	G[505]	-5969.5	381	12	90
1562	G[503]	-5981.5	500	12	90
1563	G[501]	-5994.5	381	12	90
1564	G[499]	-6006.5	500	12	90
1565	G[497]	-6019.5	381	12	90
1566	G[495]	-6031.5	500	12	90
1567	G[493]	-6044.5	381	12	90
1568	G[491]	-6056.5	500	12	90
1569	G[489]	-6069.5	381	12	90
1570	G[487]	-6081.5	500	12	90
1571	G[485]	-6094.5	381	12	90
1572	G[483]	-6106.5	500	12	90
1573	G[481]	-6119.5	381	12	90
1574	G[479]	-6131.5	500	12	90
1575	G[477]	-6144.5	381	12	90
1576	G[475]	-6156.5	500	12	90
1577	G[473]	-6169.5	381	12	90
1578	G[471]	-6181.5	500	12	90
1579	G[469]	-6194.5	381	12	90
1580	G[467]	-6206.5	500	12	90
1581	G[465]	-6219.5	381	12	90
1582	G[463]	-6231.5	500	12	90
1583	G[461]	-6244.5	381	12	90
1584	G[459]	-6256.5	500	12	90
1585	G[457]	-6269.5	381	12	90
1586	G[455]	-6281.5	500	12	90
1587	G[453]	-6294.5	381	12	90
1588	G[451]	-6306.5	500	12	90
1589	G[449]	-6319.5	381	12	90
1590	G[447]	-6331.5	500	12	90
1591	G[445]	-6344.5	381	12	90
1592	G[443]	-6356.5	500	12	90
1593	G[441]	-6369.5	381	12	90
1594	G[439]	-6381.5	500	12	90
1595	G[437]	-6394.5	381	12	90
1596	G[435]	-6406.5	500	12	90
1597	G[433]	-6419.5	381	12	90
1598	G[431]	-6431.5	500	12	90
1599	G[429]	-6444.5	381	12	90
1600	G[427]	-6456.5	500	12	90
1601	G[425]	-6469.5	381	12	90
1602	G[423]	-6481.5	500	12	90
1603	G[421]	-6494.5	381	12	90
1604	G[419]	-6506.5	500	12	90
1605	G[417]	-6519.5	381	12	90
1606	G[415]	-6531.5	500	12	90
1607	G[413]	-6544.5	381	12	90
1608	G[411]	-6556.5	500	12	90
1609	G[409]	-6569.5	381	12	90
1610	G[407]	-6581.5	500	12	90
1611	G[405]	-6594.5	381	12	90
1612	G[403]	-6606.5	500	12	90
1613	G[401]	-6619.5	381	12	90
1614	G[399]	-6631.5	500	12	90
1615	G[397]	-6644.5	381	12	90
1616	G[395]	-6656.5	500	12	90
1617	G[393]	-6669.5	381	12	90
1618	G[391]	-6681.5	500	12	90
1619	G[389]	-6694.5	381	12	90
1620	G[387]	-6706.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1621	G[385]	-6719.5	381	12	90
1622	G[383]	-6731.5	500	12	90
1623	G[381]	-6744.5	381	12	90
1624	G[379]	-6756.5	500	12	90
1625	G[377]	-6769.5	381	12	90
1626	G[375]	-6781.5	500	12	90
1627	G[373]	-6794.5	381	12	90
1628	G[371]	-6806.5	500	12	90
1629	G[369]	-6819.5	381	12	90
1630	G[367]	-6831.5	500	12	90
1631	G[365]	-6844.5	381	12	90
1632	G[363]	-6856.5	500	12	90
1633	G[361]	-6869.5	381	12	90
1634	G[359]	-6881.5	500	12	90
1635	G[357]	-6894.5	381	12	90
1636	G[355]	-6906.5	500	12	90
1637	G[353]	-6919.5	381	12	90
1638	G[351]	-6931.5	500	12	90
1639	G[349]	-6944.5	381	12	90
1640	G[347]	-6956.5	500	12	90
1641	G[345]	-6969.5	381	12	90
1642	G[343]	-6981.5	500	12	90
1643	G[341]	-6994.5	381	12	90
1644	G[339]	-7006.5	500	12	90
1645	G[337]	-7019.5	381	12	90
1646	G[335]	-7031.5	500	12	90
1647	G[333]	-7044.5	381	12	90
1648	G[331]	-7056.5	500	12	90
1649	G[329]	-7069.5	381	12	90
1650	G[327]	-7081.5	500	12	90
1651	G[325]	-7094.5	381	12	90
1652	G[323]	-7106.5	500	12	90
1653	G[321]	-7119.5	381	12	90
1654	G[319]	-7131.5	500	12	90
1655	G[317]	-7144.5	381	12	90
1656	G[315]	-7156.5	500	12	90
1657	G[313]	-7169.5	381	12	90
1658	G[311]	-7181.5	500	12	90
1659	G[309]	-7194.5	381	12	90
1660	G[307]	-7206.5	500	12	90
1661	G[305]	-7219.5	381	12	90
1662	G[303]	-7231.5	500	12	90
1663	G[301]	-7244.5	381	12	90
1664	G[299]	-7256.5	500	12	90
1665	G[297]	-7269.5	381	12	90
1666	G[295]	-7281.5	500	12	90
1667	G[293]	-7294.5	381	12	90
1668	G[291]	-7306.5	500	12	90
1669	G[289]	-7319.5	381	12	90
1670	G[287]	-7331.5	500	12	90
1671	G[285]	-7344.5	381	12	90
1672	G[283]	-7356.5	500	12	90
1673	G[281]	-7369.5	381	12	90
1674	G[279]	-7381.5	500	12	90
1675	G[277]	-7394.5	381	12	90
1676	G[275]	-7406.5	500	12	90
1677	G[273]	-7419.5	381	12	90
1678	G[271]	-7431.5	500	12	90
1679	G[269]	-7444.5	381	12	90
1680	G[267]	-7456.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1681	G[265]	-7469.5	381	12	90
1682	G[263]	-7481.5	500	12	90
1683	G[261]	-7494.5	381	12	90
1684	G[259]	-7506.5	500	12	90
1685	G[257]	-7519.5	381	12	90
1686	G[255]	-7531.5	500	12	90
1687	G[253]	-7544.5	381	12	90
1688	G[251]	-7556.5	500	12	90
1689	G[249]	-7569.5	381	12	90
1690	G[247]	-7581.5	500	12	90
1691	G[245]	-7594.5	381	12	90
1692	G[243]	-7606.5	500	12	90
1693	G[241]	-7619.5	381	12	90
1694	G[239]	-7631.5	500	12	90
1695	G[237]	-7644.5	381	12	90
1696	G[235]	-7656.5	500	12	90
1697	G[233]	-7669.5	381	12	90
1698	G[231]	-7681.5	500	12	90
1699	G[229]	-7694.5	381	12	90
1700	G[227]	-7706.5	500	12	90
1701	G[225]	-7719.5	381	12	90
1702	G[223]	-7731.5	500	12	90
1703	G[221]	-7744.5	381	12	90
1704	G[219]	-7756.5	500	12	90
1705	G[217]	-7769.5	381	12	90
1706	G[215]	-7781.5	500	12	90
1707	G[213]	-7794.5	381	12	90
1708	G[211]	-7806.5	500	12	90
1709	G[209]	-7819.5	381	12	90
1710	G[207]	-7831.5	500	12	90
1711	G[205]	-7844.5	381	12	90
1712	G[203]	-7856.5	500	12	90
1713	G[201]	-7869.5	381	12	90
1714	G[199]	-7881.5	500	12	90
1715	G[197]	-7894.5	381	12	90
1716	G[195]	-7906.5	500	12	90
1717	G[193]	-7919.5	381	12	90
1718	G[191]	-7931.5	500	12	90
1719	G[189]	-7944.5	381	12	90
1720	G[187]	-7956.5	500	12	90
1721	G[185]	-7969.5	381	12	90
1722	G[183]	-7981.5	500	12	90
1723	G[181]	-7994.5	381	12	90
1724	G[179]	-8006.5	500	12	90
1725	G[177]	-8019.5	381	12	90
1726	G[175]	-8031.5	500	12	90
1727	G[173]	-8044.5	381	12	90
1728	G[171]	-8056.5	500	12	90
1729	G[169]	-8069.5	381	12	90
1730	G[167]	-8081.5	500	12	90
1731	G[165]	-8094.5	381	12	90
1732	G[163]	-8106.5	500	12	90
1733	G[161]	-8119.5	381	12	90
1734	G[159]	-8131.5	500	12	90
1735	G[157]	-8144.5	381	12	90
1736	G[155]	-8156.5	500	12	90
1737	G[153]	-8169.5	381	12	90
1738	G[151]	-8181.5	500	12	90
1739	G[149]	-8194.5	381	12	90
1740	G[147]	-8206.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1741	G[145]	-8219.5	381	12	90
1742	G[143]	-8231.5	500	12	90
1743	G[141]	-8244.5	381	12	90
1744	G[139]	-8256.5	500	12	90
1745	G[137]	-8269.5	381	12	90
1746	G[135]	-8281.5	500	12	90
1747	G[133]	-8294.5	381	12	90
1748	G[131]	-8306.5	500	12	90
1749	G[129]	-8319.5	381	12	90
1750	G[127]	-8331.5	500	12	90
1751	G[125]	-8344.5	381	12	90
1752	G[123]	-8356.5	500	12	90
1753	G[121]	-8369.5	381	12	90
1754	G[119]	-8381.5	500	12	90
1755	G[117]	-8394.5	381	12	90
1756	G[115]	-8406.5	500	12	90
1757	G[113]	-8419.5	381	12	90
1758	G[111]	-8431.5	500	12	90
1759	G[109]	-8444.5	381	12	90
1760	G[107]	-8456.5	500	12	90
1761	G[105]	-8469.5	381	12	90
1762	G[103]	-8481.5	500	12	90
1763	G[101]	-8494.5	381	12	90
1764	G[99]	-8506.5	500	12	90
1765	G[97]	-8519.5	381	12	90
1766	G[95]	-8531.5	500	12	90
1767	G[93]	-8544.5	381	12	90
1768	G[91]	-8556.5	500	12	90
1769	G[89]	-8569.5	381	12	90
1770	G[87]	-8581.5	500	12	90
1771	G[85]	-8594.5	381	12	90
1772	G[83]	-8606.5	500	12	90
1773	G[81]	-8619.5	381	12	90
1774	G[79]	-8631.5	500	12	90
1775	G[77]	-8644.5	381	12	90
1776	G[75]	-8656.5	500	12	90
1777	G[73]	-8669.5	381	12	90
1778	G[71]	-8681.5	500	12	90
1779	G[69]	-8694.5	381	12	90
1780	G[67]	-8706.5	500	12	90
1781	G[65]	-8719.5	381	12	90
1782	G[63]	-8731.5	500	12	90
1783	G[61]	-8744.5	381	12	90
1784	G[59]	-8756.5	500	12	90
1785	G[57]	-8769.5	381	12	90
1786	G[55]	-8781.5	500	12	90
1787	G[53]	-8794.5	381	12	90
1788	G[51]	-8806.5	500	12	90
1789	G[49]	-8819.5	381	12	90
1790	G[47]	-8831.5	500	12	90
1791	G[45]	-8844.5	381	12	90
1792	G[43]	-8856.5	500	12	90
1793	G[41]	-8869.5	381	12	90
1794	G[39]	-8881.5	500	12	90
1795	G[37]	-8894.5	381	12	90
1796	G[35]	-8906.5	500	12	90
1797	G[33]	-8919.5	381	12	90
1798	G[31]	-8931.5	500	12	90
1799	G[29]	-8944.5	381	12	90
1800	G[27]	-8956.5	500	12	90

No.	Name	X-axis	Y-axis	W	H
1801	G[25]	-8969.5	381	12	90
1802	G[23]	-8981.5	500	12	90
1803	G[21]	-8994.5	381	12	90
1804	G[19]	-9006.5	500	12	90
1805	G[17]	-9019.5	381	12	90
1806	G[15]	-9031.5	500	12	90
1807	G[13]	-9044.5	381	12	90
1808	G[11]	-9056.5	500	12	90
1809	G[9]	-9069.5	381	12	90
1810	G[7]	-9081.5	500	12	90
1811	G[5]	-9094.5	381	12	90
1812	G[3]	-9106.5	500	12	90
1813	G[1]	-9119.5	381	12	90
1814	DUMMY[64]	-9131.5	500	12	90
1815	DUMMY[65]	-9144.5	381	12	90
1816	DUMMY[66]	-9156.5	500	12	90
1817	DUMMY[67]	-9169.5	381	12	90

13. REVISION HISTORY

Revision	Content	Page	Date
1.0.0	1.new issue		2019/07/02
1.0.1	1.Add gate on times definition in R60H 2. Modified B/W mode statement in R50H	51 49	2019/08/30
1.0.2	1. Modify cascade circuit, Salve IC GDR, RESE keep open 2. value of wiring resistance to each pin	9 13	2019/09/19
1.0.3	1. Circuit/Bump View information	91	2019/12/26
1.0.4	1. Update bump height 12um to 9um	91	2020/05/29
1.0.5	Pin define modify	11, 12	2022/01/17