JADARD

JD9165BA

Rev. 0.0.2

PRELIMINARY DATA SHEET

1538CH TFT LCD Single Chip Driver with TCON

1. General Description

JD9165 is a one-chip solution for Amorphous Si TFT LCD panel. The source driver integrates 1538 source channels, a timing controller, and supports GOA control circuits for the middle size panel application. In addition, the chip also provides Gamma reference voltage and VCOM voltage.

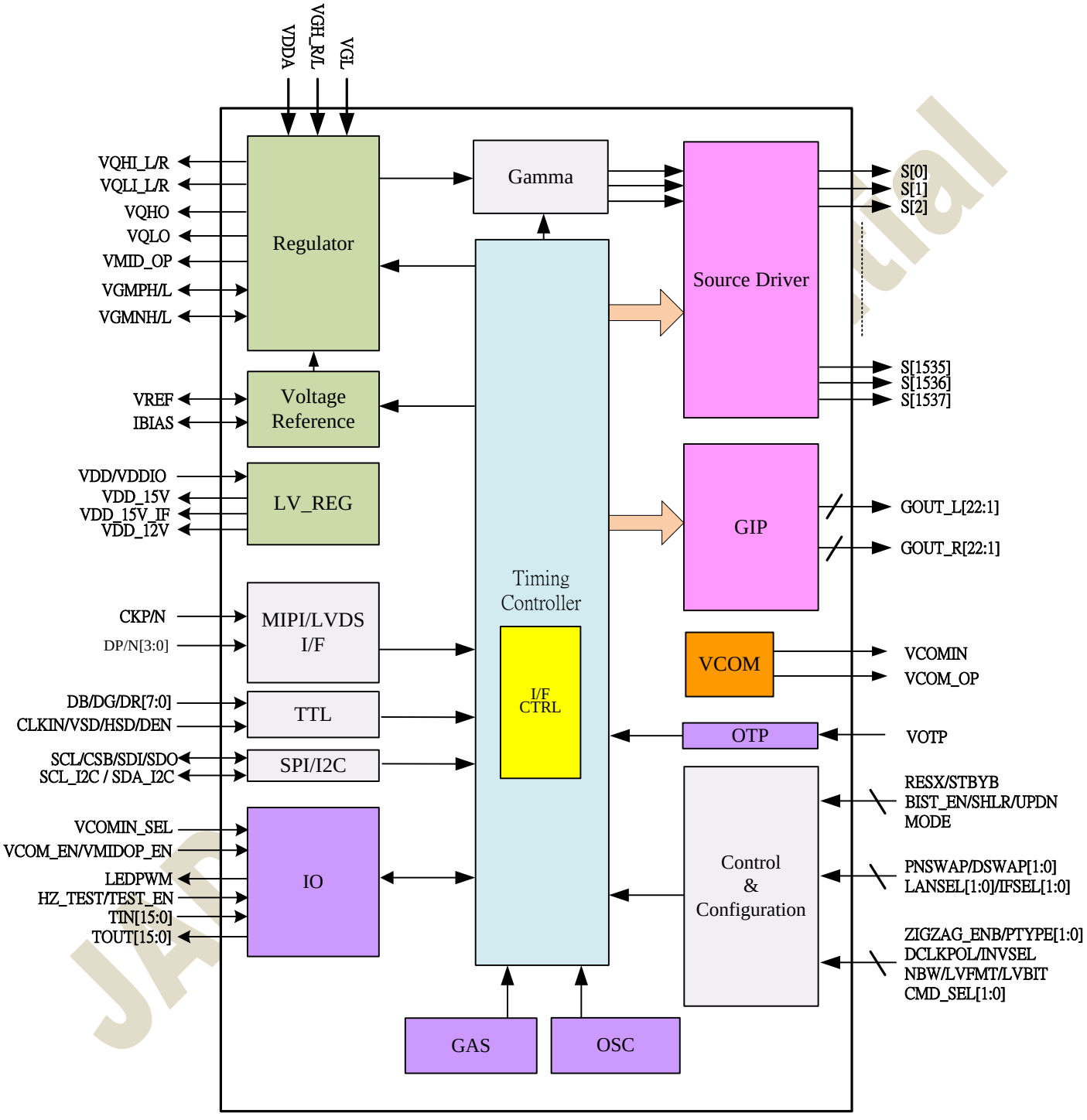
JD9165 also supports various types of peripheral interface such as MIPI interface without frame memory, LVDS interface, 24 parallel RGB interface, and provide 60Hz frame rate. The serial communication interface is also embedded for function setting.

2. Features

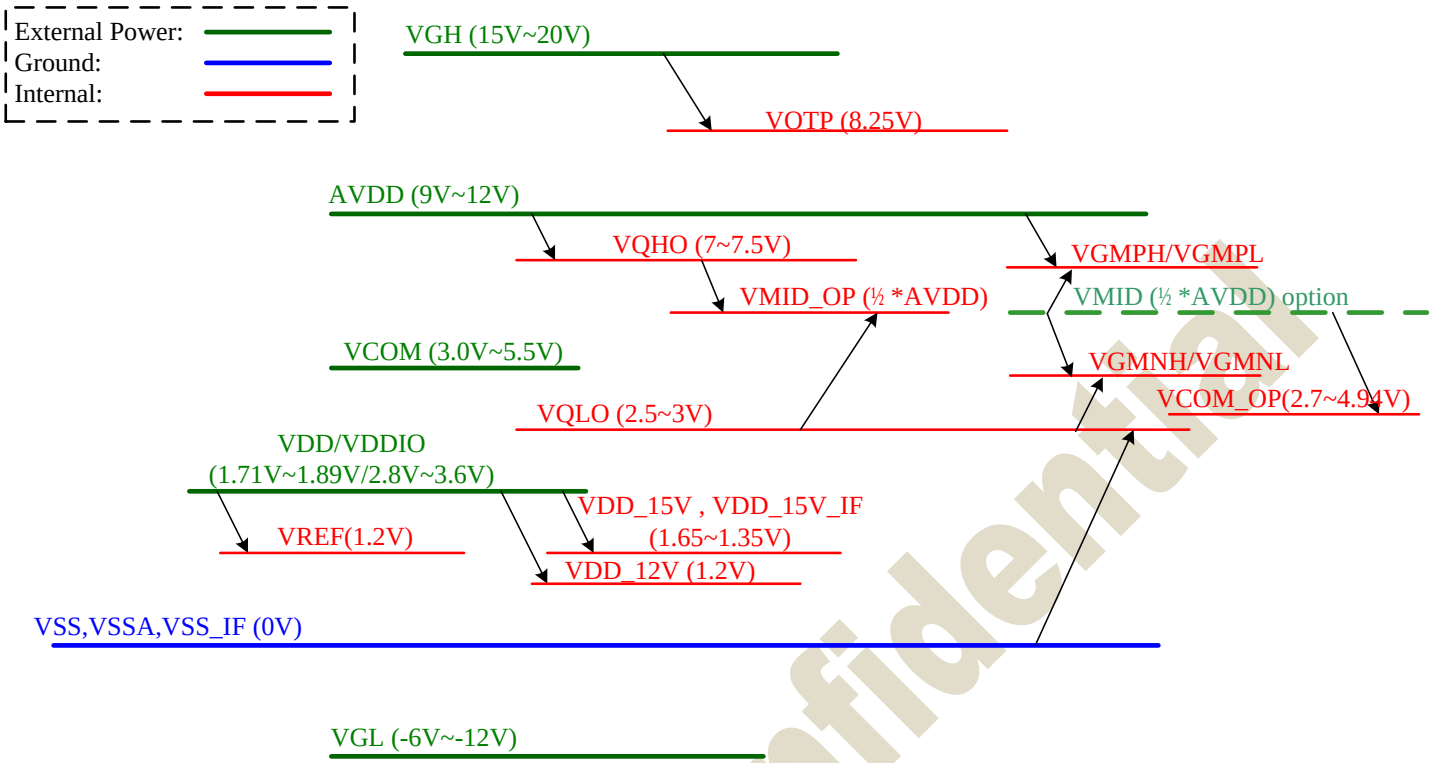
- Single chip solution for Amorphous Si TFT LCD display
- Integrated 1538 channel source driver
- Support panel resolution (HxV):
  - 1024RGBx768, (256RGB+4*n)xV
- Embedded GOA circuit, support 22 GOUT pins each on R-side/L-side
- Panel type:
  - Single chip: Dual gate panel/Dual gate+Zig-zag panel/Single gate panel
- Inversion architecture:
  - Column inversion
  - 1+2 dot inversion
  - 2 dot inversion
  - Dot inversion
- Support Normally black and white panel
- Provide total 28 register value for gamma correction adjustment
- Support BIST mode
- Support GAS function for abnormal power off
- Support SPI/I2C interface
- Source driver output with 8-bit DAC
- Embedded VCOM = 2.7V to 4.94V
- OTP memory to store initialization register settings
  - 1 times OTP for GOA setting
  - 2 times OTP for Gamma setting
  - 6 times OTP for VCOM setting
  - 1 times OTP for Other Register setting
- Input power supply:
  - VDD=1.71V to 1.89V / 2.8V to 3.6V **(power supply for digital circuit)**
  - AVDD=9V to 12V **(power supply for analog circuit)**
  - VCOM=3.0V to 5.5V **(power supply for analog circuit)**
  - VGH=15V to 20V **(power supply for GOA circuit)**
  - VGL= -6V to -12V **(power supply for GOA circuit)**
- Support MIPI DSI version 1.02
- Support MIPI D-PHY version 1.00
- Support MIPI 1port interface
- Support LVDS 1 port interface
- Support TTL 24-bit parallel RGB interface
- COG package
- Chip size = 28500um x 800um
- Chip thickness = 230um
- Operating temperature **(T_A)**: -30℃ to +85℃
- Storage temperature **(T_{STG})**: -55℃ to +125℃

3. BLOCK DIAGRAM

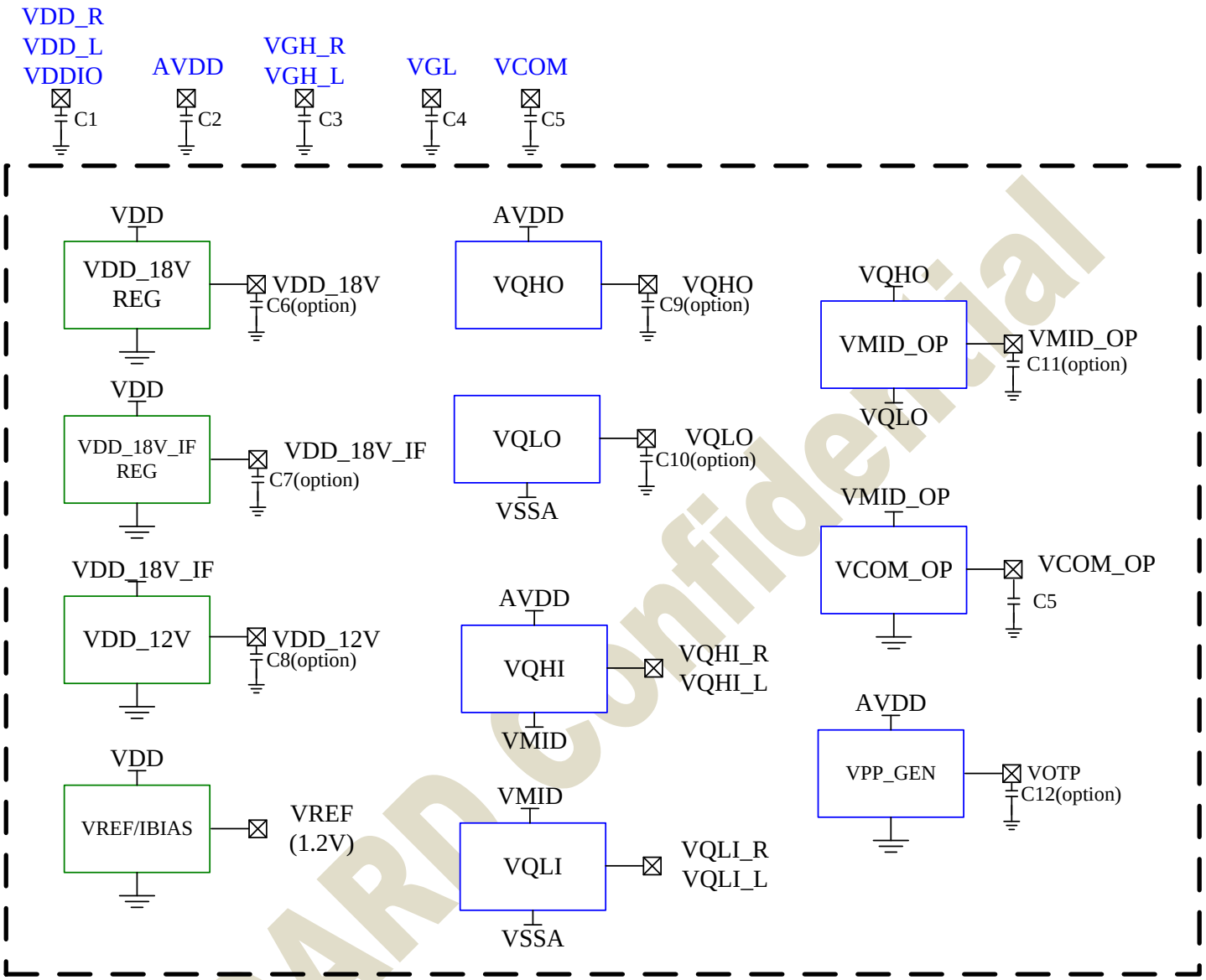
3.1 Function block diagram



3.2 Power structure



3.3 DC/DC circuit reference design



Ref. no	Typical
C1	4.7~10uF/6.3V
C2	4.7~10uF/25V
C3	2.2~4.7uF/25V
C4	2.2~4.7uF/25V
C5	2.2~4.7uF/16V
C6	2.2uF/6.3V
C7	2.2uF/6.3V
C8	1uF/6.3V
C9	4.7uF/10V
C10	4.7uF/10V
C11	4.7uF/10V
C12	1uF/25V

4. PIN DESCRIPTION

4.1 Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Interface pins</td></tr>
<tr><td>DP[0]/DN[0]
DP[1]/DN[1]
DP[2]/DN[2]
DP[3]/DN[3]</td><td>In</td><td>MIPI and LVDS data input pin.
If not used, let it open.</td></tr>
<tr><td>CKP/CKN</td><td>In</td><td>MIPI and LVDS clock input pin.
If not used, let it open.</td></tr>
<tr><td>DR[7:0]
DG[7:0]
DB[7:0]
(VDD)</td><td>In</td><td>TTL data input. Select by “IFSEL” pin.
If not used, please fix this pin at VSS level.</td></tr>
<tr><td>CLKIN
(VDD)</td><td>In</td><td>TTL clock input pin. Select by “IFSEL” pin.
If not used, please fix this pin at VSS level.</td></tr>
<tr><td>HSD
(VDD)</td><td>In</td><td>Horizontal sync input. Internally pulled high.
If not used, please fix this pin at VSS level.</td></tr>
<tr><td>VSD
(VDD)</td><td>In</td><td>Vertical sync input. Internally pulled high.
If not used, please fix this pin at VSS level.</td></tr>
<tr><td>DEN
(VDD)</td><td>In</td><td>DE signal when DE mode. Internally pulled low.
If not used, please fix this pin at VSS level.</td></tr>
<tr><td colspan="3">Global pins</td></tr>
<tr><td>RESX
(VDD)</td><td>In</td><td>Global reset pin, active low. (Default pull High)</td></tr>
<tr><td>STBYB
(VDD)</td><td>In</td><td>Standby mode selection.(Default pull High)
(only for TTL and LVDS, MIPI mode = dummy function)
STBYB=H, Normal mode.
STBYB=L, Standby mode.
If not used, please fix this pin at VDD level.</td></tr>
<tr><td>DSWAP[1:0]
(VDD)</td><td></td><td>These pins must be connected to VDD or VSSD. DSWAP[1:0] are used for the combination of data lane swap. (Default DSWAP[1:0]=11b)
<table>
<tr><th rowspan="2">DSWAP[1:0]</th><th>DP0</th><th>DN0</th><th>DP1</th><th>DN1</th><th>CKP</th><th>CKN</th><th>DP2</th><th>DN2</th><th>DP3</th><th>DN3</th></tr>
<tr><th colspan="10">MIPI lanes mapping table</th></tr>
<tr><td>00</td><td>DP3</td><td>DN3</td><td>DP2</td><td>DN2</td><td>CKP</td><td>CKN</td><td>DP1</td><td>DN1</td><td>DP0</td><td>DN0</td></tr>
<tr><td>01</td><td>DP0</td><td>DN0</td><td>DP1</td><td>DN1</td><td>CKP</td><td>CKN</td><td>DP2</td><td>DN2</td><td>DP3</td><td>DN3</td></tr>
<tr><td>10</td><td>DP3</td><td>DN3</td><td>DP2</td><td>DN2</td><td>CKP</td><td>CKN</td><td>DP1</td><td>DN1</td><td>DP0</td><td>DN0</td></tr>
<tr><td>11</td><td>DP0</td><td>DN0</td><td>DP1</td><td>DN1</td><td>CKP</td><td>CKN</td><td>DP2</td><td>DN2</td><td>DP3</td><td>DN3</td></tr>
</table>
<table>
<tr><th rowspan="2">DSWAP[1:0]</th><th>DP0</th><th>DN0</th><th>DP1</th><th>DN1</th><th>CKP</th><th>CKN</th><th>DP2</th><th>DN2</th><th>DP3</th><th>DN3</th></tr>
<tr><th colspan="10">LVDS lanes mapping table</th></tr>
<tr><td>00</td><td>DP3</td><td>DN3</td><td>DP2</td><td>DN2</td><td>DP1</td><td>DN1</td><td>DP0</td><td>DN0</td><td>CKP</td><td>CKN</td></tr>
<tr><td>01</td><td>CKP</td><td>CKN</td><td>DP0</td><td>DN0</td><td>DP1</td><td>DN1</td><td>DP2</td><td>DN2</td><td>DP3</td><td>DN3</td></tr>
<tr><td>10</td><td>DP3</td><td>DN3</td><td>DP2</td><td>DN2</td><td>CKP</td><td>CKN</td><td>DP1</td><td>DN1</td><td>DP0</td><td>DN0</td></tr>
<tr><td>11</td><td>DP0</td><td>DN0</td><td>DP1</td><td>DN1</td><td>CKP</td><td>CKN</td><td>DP2</td><td>DN2</td><td>DP3</td><td>DN3</td></tr>
</table>
If not used, please fix this pin at VDD level.</td></tr>
</table>

<table>
<tr><td>PNSWAP
(VDD)</td><td>In</td><td>MIPI and LVDS polarity selection. (Default pull Low)
<table>
<tr><td rowspan="2">PNSWAP</td><td>D0P/N</td><td>D1P/N</td><td>CKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td colspan="5">MIPI/LVDS lanes mapping table</td></tr>
<tr><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
</table>
If not used, please fix this pin at VSS level.</td></tr>
<tr><td>LANSEL[1:0]
(VDD)</td><td>In</td><td>MIPI lane number configuration. (Default LANSEL[1:0]=11b)
<table>
<tr><th>LANSEL[1:0]</th><th>MIPI lane number</th></tr>
<tr><td>00</td><td>1 lane</td></tr>
<tr><td>01</td><td>2 lanes</td></tr>
<tr><td>10</td><td>3 lanes</td></tr>
<tr><td>11</td><td>4 lanes</td></tr>
</table>
If not used, please fix this pin at VDD level.</td></tr>
<tr><td>IFSEL[1:0]
(VDD)</td><td>In</td><td>Interface selection. (Default IFSEL[1:0]=00b)
<table>
<tr><th>IFSEL[1:0]</th><th>Interface</th></tr>
<tr><td>00</td><td>LVDS</td></tr>
<tr><td>01</td><td>MIPI</td></tr>
<tr><td>10</td><td>TTL</td></tr>
<tr><td>11</td><td>T.B.D.</td></tr>
</table></td></tr>
<tr><td>BIST_EN
(VDD)</td><td>In</td><td>BIST mode enable, high active. (Default pull Low)
If not used, please fix this pin at VSS level.</td></tr>
<tr><td>SHLR
(VDD)</td><td>In</td><td>Horizontal scan direction. (Default pull Low)
<table>
<tr><th>SHLR</th><th>Function</th></tr>
<tr><td>1</td><td>S1537→S1536→.....S1→S0</td></tr>
<tr><td>0</td><td>S0→S1→.....S1536→S1537</td></tr>
</table></td></tr>
<tr><td>UPDN
(VDD)</td><td>In</td><td>Vertical scan direction. (Default pull Low)
<table>
<tr><th>UPDN</th><th>Function</th></tr>
<tr><td>1</td><td>Bottom → Top</td></tr>
<tr><td>0</td><td>Top → Bottom</td></tr>
</table></td></tr>
<tr><td>MODE
(VDD)</td><td>In</td><td>DE mode and Sync mode selection. (Default pull High)
<table>
<tr><th>MODE</th><th>Function</th></tr>
<tr><td>1</td><td>DE mode</td></tr>
<tr><td>0</td><td>Sync mode</td></tr>
</table>
If MIPI mode, please fix this pin at VDD level.</td></tr>
<tr><td>ZIGZAG_ENB
(VDD)</td><td>In</td><td>Dual gata or Zig-zag panel setting. (Default pull High)
<table>
<tr><th>ZIGZAG_ENB</th><th>Function</th></tr>
<tr><td>1</td><td>Dual gate panel</td></tr>
<tr><td>0</td><td>Dual gate+Zig-zag panel</td></tr>
</table></td></tr>
<tr><td>PTYPE[1:0]
(VDD)</td><td>In</td><td>Panel layout type selection. (Default PTYPE[1:0]=00b)
<table>
<tr><th>PTYPE[1:0]</th><th>Dual gate panel</th><th>Zig-zag panel</th></tr>
<tr><td>00</td><td rowspan="2">Dual gate layout type1</td><td>Zig-zag layout type1</td></tr>
<tr><td>01</td><td>Zig-zag layout type2</td></tr>
<tr><td>10</td><td rowspan="2">Dual gate layout type2</td><td>Zig-zag layout type3</td></tr>
<tr><td>11</td><td>Zig-zag layout type4</td></tr>
</table></td></tr>
<tr><td>DCLKPOL
(VDD)</td><td>In</td><td>TTL input clock edge selection. (Default pull Low)
<table>
<tr><th>DCLKPOL</th><th>Function</th></tr>
<tr><td>1</td><td>Latch data at DCLK rising edge</td></tr>
<tr><td>0</td><td>Latch data at DCLK falling edge</td></tr>
</table>
If MIPI/LVDS mode, please fix this pin at VSS level.</td></tr>
<tr><td>INVSEL
(VDD)</td><td>In</td><td>Inversion type selection. (Default pull High)
(only for dual gate panel, single gate and dual gate+zig-zag panel please fix this pin at VDD level.).
<table>
<tr><th>INVSEL</th><th>Function</th></tr>
<tr><td>1</td><td>1+2dot</td></tr>
<tr><td>0</td><td>2 dot</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>NBW
(VDD)</td><td>In</td><td>Normally black or normally white setting. (Default pull Low)
<table><tr><th>NBW</th><th>Function</th></tr><tr><td>1</td><td>Normally white panel</td></tr><tr><td>0</td><td>Normally black panel</td></tr></table></td></tr>
<tr><td>LVFMT
(VDD)</td><td>In</td><td>8-bit input format select for LVDS mode. (Default pull High)
(only for LVDS, TTL/MIPI mode please fix the pin at VDD level)
<table><tr><th>LVFMT</th><th>Function</th></tr><tr><td>1</td><td>VESA format</td></tr><tr><td>0</td><td>JEIDA format</td></tr></table></td></tr>
<tr><td>LVBIT
(VDD)</td><td>In</td><td>6-bit / 8-bit input select for LVDS mode. (Default pull High)
(only for LVDS, TTL/MIPI mode please fix the pin at VDD level)
<table><tr><th>LVBIT</th><th>Function</th></tr><tr><td>1</td><td>8-bit</td></tr><tr><td>0</td><td>6-bit</td></tr></table></td></tr>
<tr><td>CMD_SEL[1:0]
(VDD)</td><td>In</td><td>Command interface selection. (Default CMD_SEL[1:0]=00b).
<table><tr><th>CMD_SEL1</th><th>CMD_SEL0</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>3-wire SPI Ⅰ</td></tr><tr><td>0</td><td>1</td><td>3-wire SPI Ⅱ</td></tr><tr><td>1</td><td>X</td><td>I2C</td></tr></table>MIPI and SPI/I2C command can’t receive at the same time.</td></tr>
<tr><td>VCOMIN_SEL
(VDD)</td><td>In</td><td>Internal/External VCOM selection.(Default pull Low)
<table><tr><th>VCOMIN_SEL</th><th>Function</th></tr><tr><td>1</td><td>External VCOM</td></tr><tr><td>0</td><td>Internal VCOM</td></tr></table></td></tr>
<tr><td>VCOM_EN
(VDD)</td><td>In</td><td>VCOM buffer selection. (Default pull High)
<table><tr><th>VCOM_EN</th><th>Function</th></tr><tr><td>1</td><td>VCOM buffer enable</td></tr><tr><td>0</td><td>VCOM buffer disable</td></tr></table></td></tr>
<tr><td>VMIDOP_EN
(VDD)</td><td>In</td><td>Internal/external VMIDOP selection.(Default pull Low)
<table><tr><th>VMIDOP_EN</th><th>Function</th></tr><tr><td>1</td><td>VMIDOP Enable</td></tr><tr><td>0</td><td>VMIDOP Disable</td></tr></table></td></tr>
<tr><td>VDD18V_BPS</td><td>In</td><td>Dummy pin.
Please fix the pin at VSS or VDD level.</td></tr>
<tr><td>LEDPWM</td><td>Out</td><td>This pin is connected to the external LED driver.
PWM type control signal for brightness of the LED backlight.
If not used, let it open.</td></tr>
<tr><td>TP_SYNC</td><td>Out</td><td>Internal test pin.
Please keep test point in FPC.</td></tr>
<tr><td colspan="3">Panel control pins</td></tr>
<tr><td>S[1537:0]</td><td>Out</td><td>Source Driver output signals.
If not used, let it open.</td></tr>
<tr><td>GOUT_L[22:1]</td><td>Out</td><td>GOA control signal at left side.
If not used, let it open.</td></tr>
</table>

GOUT_R[22:1]	Out	GOA control signal at right side. If not used, let it open.
Power pins		
VDD_R/VDD_L	In	Power supply for digital circuits. VDD=1.71V to 1.89V / 2.8V to 3.6V
VDDIO	In	Power supply for I/O circuits. VDDIO=1.71V to 1.89V / 2.8V to 3.6V Connect to VDD_R/VDD_L in FPC.
AVDD	In	Power supply for analog circuits. AVDD=9V to 12V.
VGH_R/VGH_L	In	Power supply for GOA circuits. VGH=15V to 20V. Connect these pins to VGH in FPC.
VGL	In	Power supply for GOA circuits. VGL= -6V to -12V.
VDD_15V	Out	Internal power supply for logic circuits. Connect to a stabilizing capacitor.
VDD_15V_IF	Out	Internal power supply for interface circuits. Connect to a stabilizing capacitor.
VDD_12V_IF	Out	(Only for MIPI, TTL/LVDS mode please let it open). VDDLP LDO output for MIPI LP mode TX use. VDDLP LDO enable on MIPI interface. (IFSEL[1:0]=01b) Connect to a stabilizing capacitor.
VMID_R[1:0] VMID_L[1:0]	I/O	Power supply for analog circuits. Connect these pins to VMID_OP in FPC.
VMID_OP	Out	VMID OP output (VMID_OP=1/2*AVDD). Connect to a stabilizing capacitor.
VQHI_R/VQHI_L	Out	Internal source reference voltage (7V to 7.5V). Please let it open.
VQLI_R/VQLI_L	Out	Internal source reference voltage (2.8V to 3V). Please let it open.
VQHO	Out	Internal source reference voltage (0.75AVDD). Connect to a stabilizing capacitor.
VQLO	Out	Internal source reference voltage (0.25AVDD). Connect to a stabilizing capacitor.
VCOMIN	In	VCOM buffer in. If not used, let it open.
VCOM_OP	Out	VCOM buffer out (2.7V to 4.94V). Connect to a stabilizing capacitor. If not used, let it open.
VOTP	Out	Internal OTP voltage and operates at 8.25V. Connect to a stabilizing capacitor.
VPP_REN	Out	Internal test pin. Please let it open.
VSS	In	GND for the internal logic. VSS=0V. When using the COG method, connect to VSSA in FPC to prevent noise.
VSSA	In	Analog ground. VSS=0V. When using the COG method, connect to VSS in FPC to prevent noise.

VSS_IF	In	Ground for interface, connect to VSS.
Shielding_VSSA	In	Internal shielding ground pin. Please let it open.
Serial interface pins		
CSB (VDD)	In	Serial Interface chip enable signal for SPI interface. SPI_CSB=0: Selected (Accessible). SPI_CSB=1: Not selected (Inaccessible).
SCL (VDD)	In	Serial interface clock input for SPI interface.
SDI (VDD)	I/O	Serial interface address and data input/output for SPI interface.
SDO (VDD)	I/O	Serial interface data output for SPI interface.
SDA_I2C (VDD)	I/O	Serial interface address and data input/output for I2C interface. (I2C interface need external pull high resistance.)
SCL_I2C (VDD)	In	Serial interface clock input for I2C interface. (I2C interface need external pull high resistance.)
Pass line pins		
PASS2_R	In	VCOM pass line.
PASS1_R	In	VCOM pass line.
PASS2_L	In	VCOM pass line.
PASS1_L	In	VCOM pass line.
Test pins		
TEST_I[25:0]	In	Internal test pins. Please let it open.
TEST_O[19:0]	Out	Internal test pins. Please let it open.
TEST_VDD_I[0]	In	Internal test pins. Please let it open.
TEST_VDD_O[3:1]	Out	Internal test pins. Please let it open.
TEST_HV_I[1:0]	In	Internal test pins. Please let it open.
TEST_MV_I[1:0]	In	Internal test pins. Please let it open.
TEST_HV_O[1:0]	Out	Internal test pins. Please let it open.
TEST_MV_O[1:0]	Out	Internal test pins. Please let it open.
T_IRX	Out	Internal test pins. Please let it open.
Dummy pins		
DUMMY	In	Dummy pins. Please let it open.
DUMMY[1]/DUMMY36]	In	Dummy pins. Please let it open.

5. FUNCTION DESCRIPTION

5.1 Power On Sequence

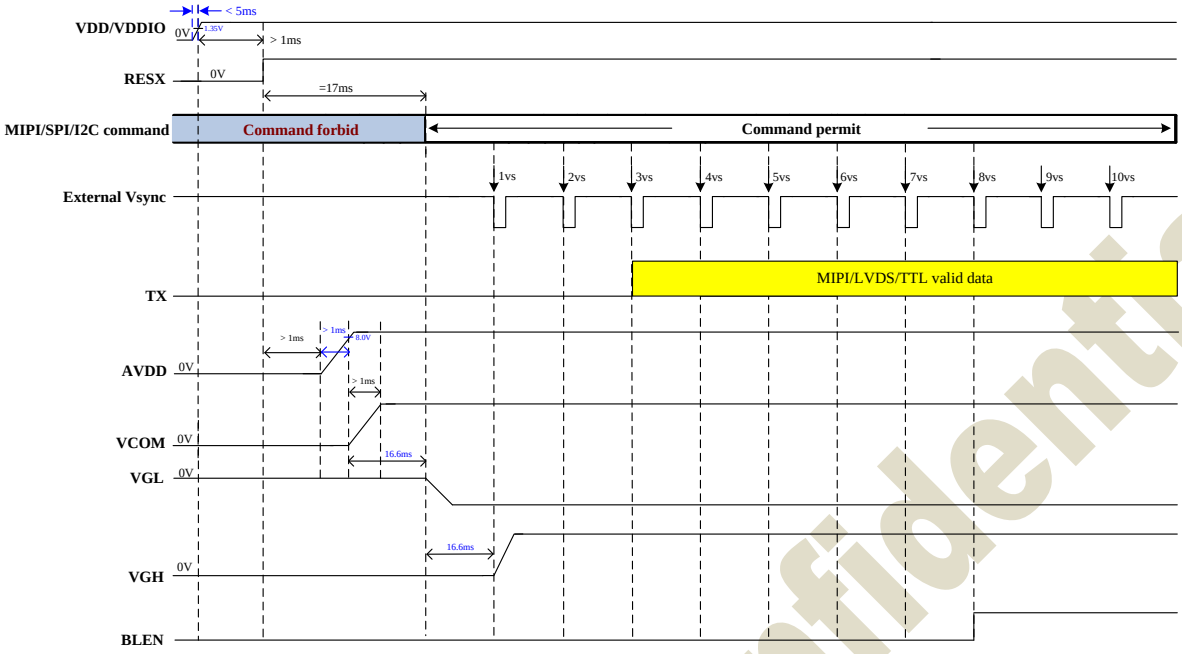


Figure 5.1: Power On timing chart

5.2 Power Off Sequence

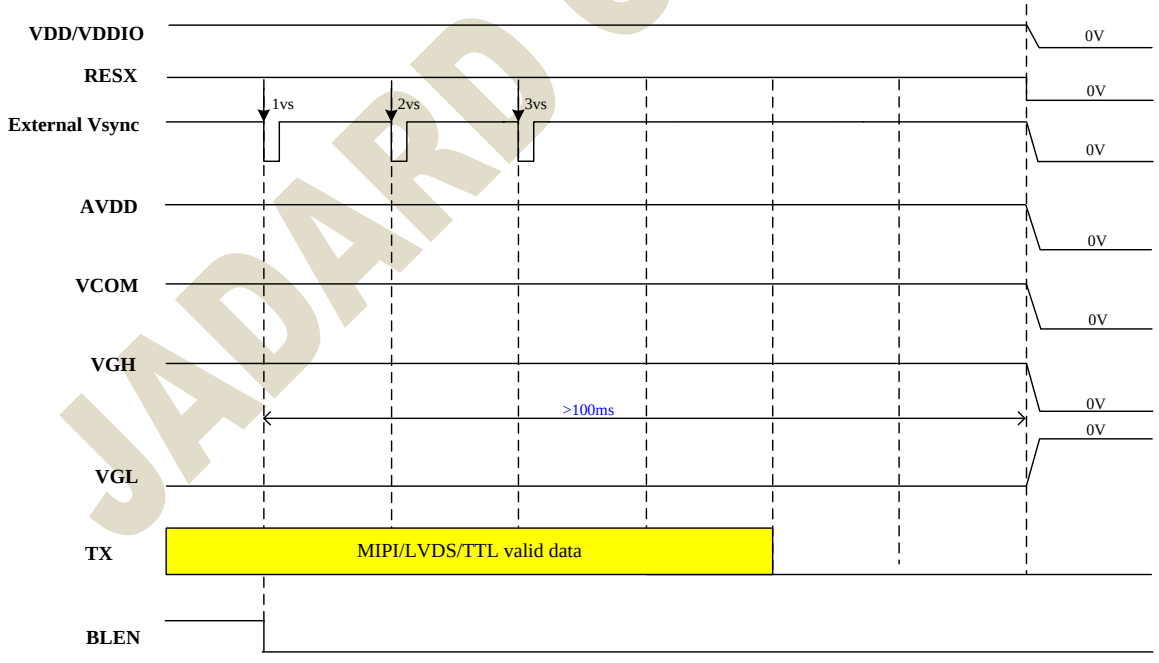


Figure 5.2: Power Off timing chart

5.3 Panel structure

JD9165 can support 3 types of driving method – Dual gate panel, Dual gate+Zig-Zag, and Single gate driving.

5.3.1 Dual Gate Panel Configuration

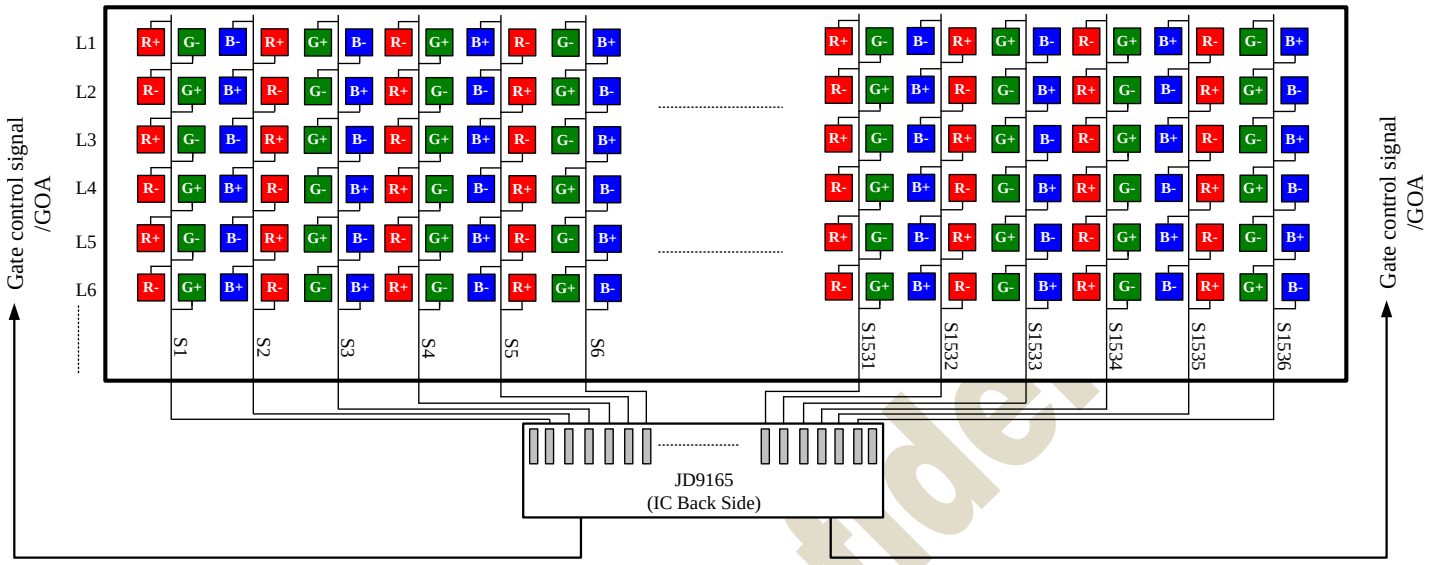


Figure 5.3: Dual gate type1 panel structure

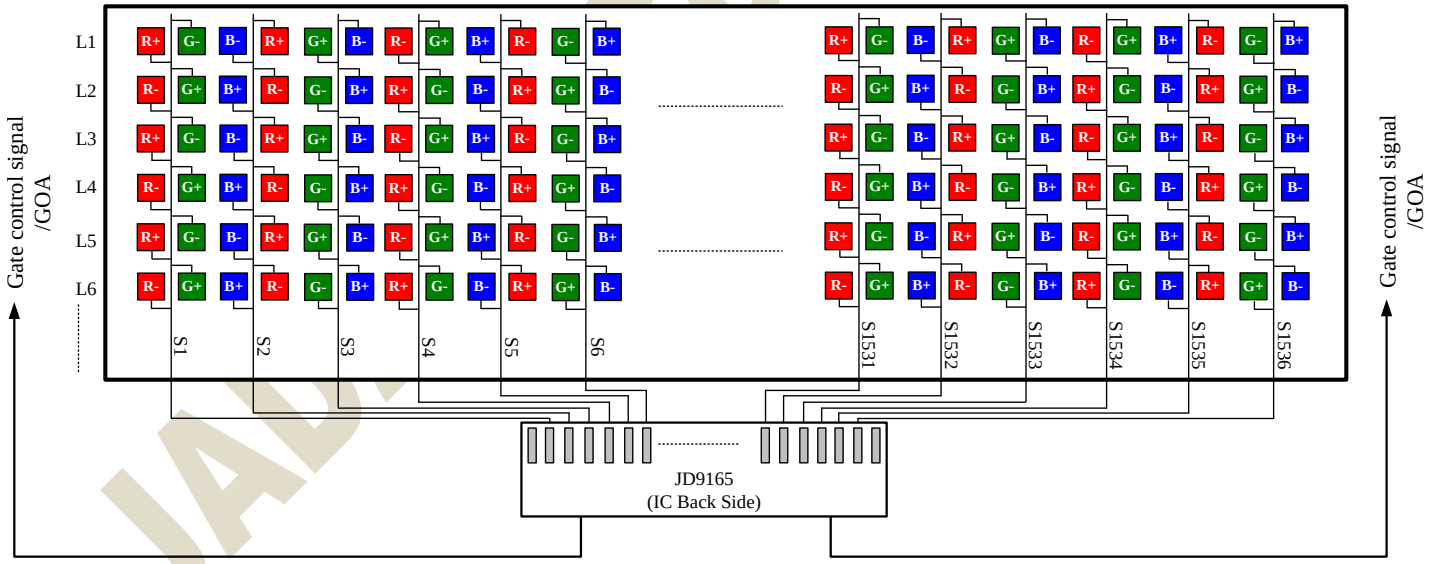


Figure 5.4: Dual gate type2 panel structure

5.3.2 Dual Gate + Zig-zag Panel Configuration

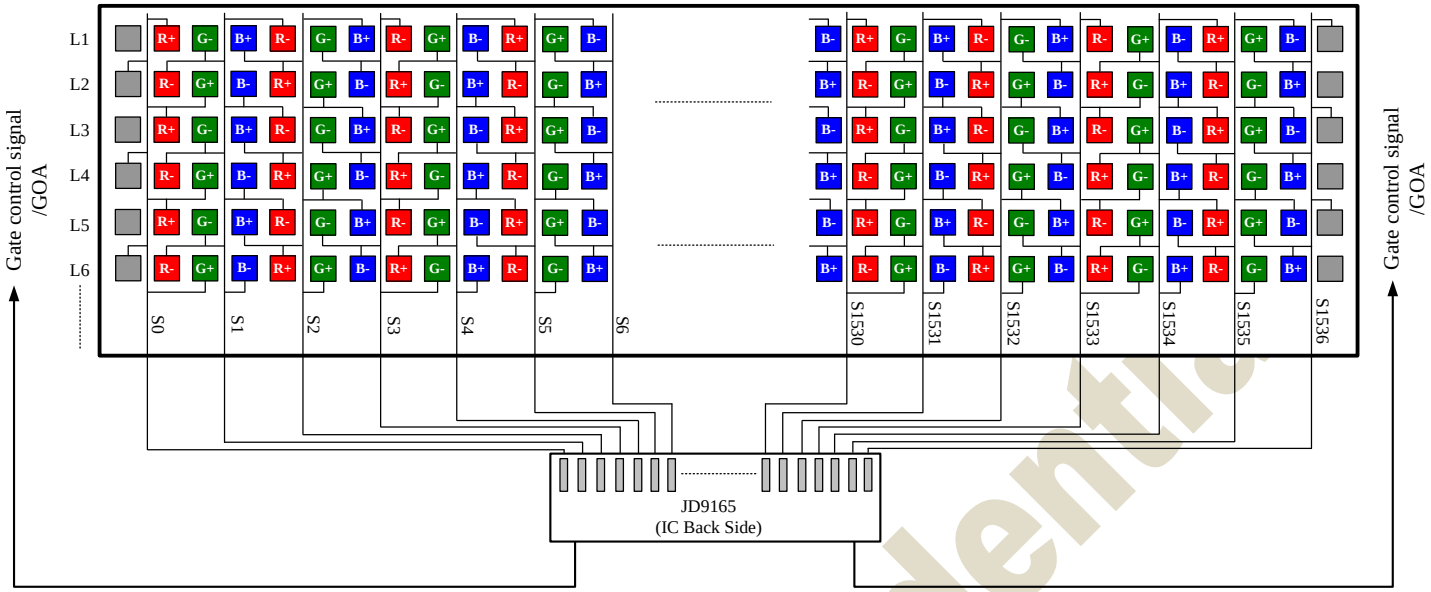


Figure 5.5: Dual gate+Zig-zag type1 panel structure

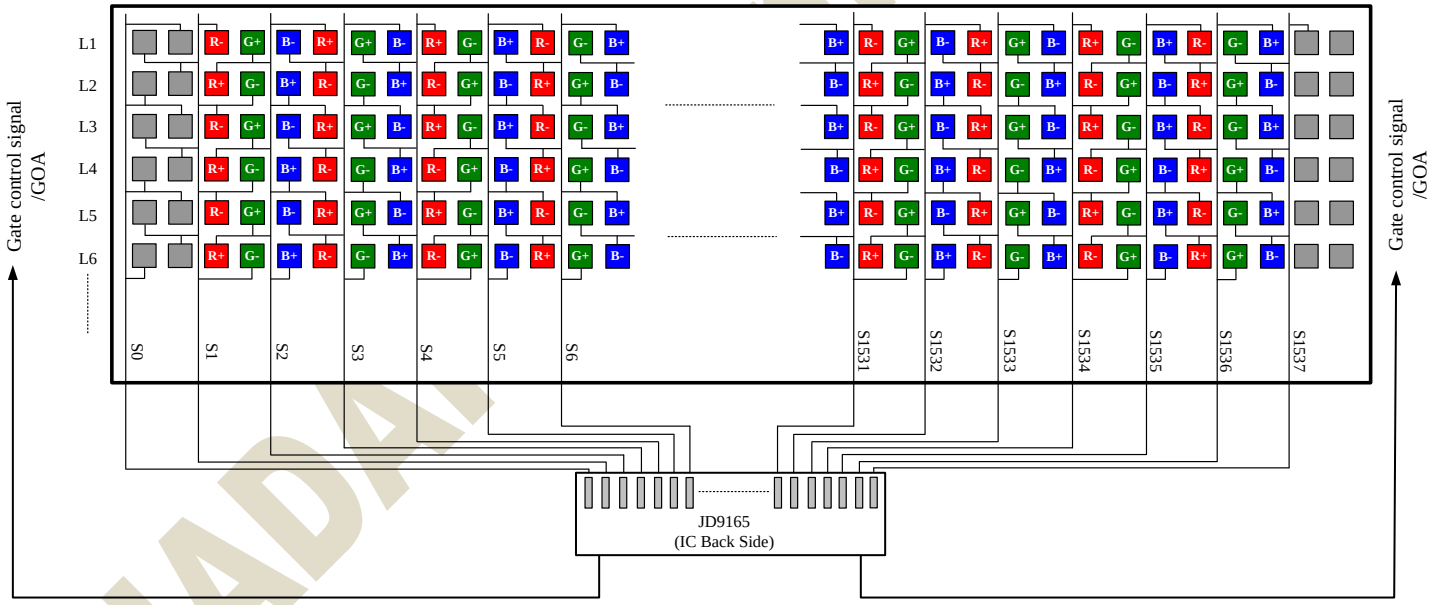


Figure 5.6: Dual gate+Zig-zag type2 panel structure

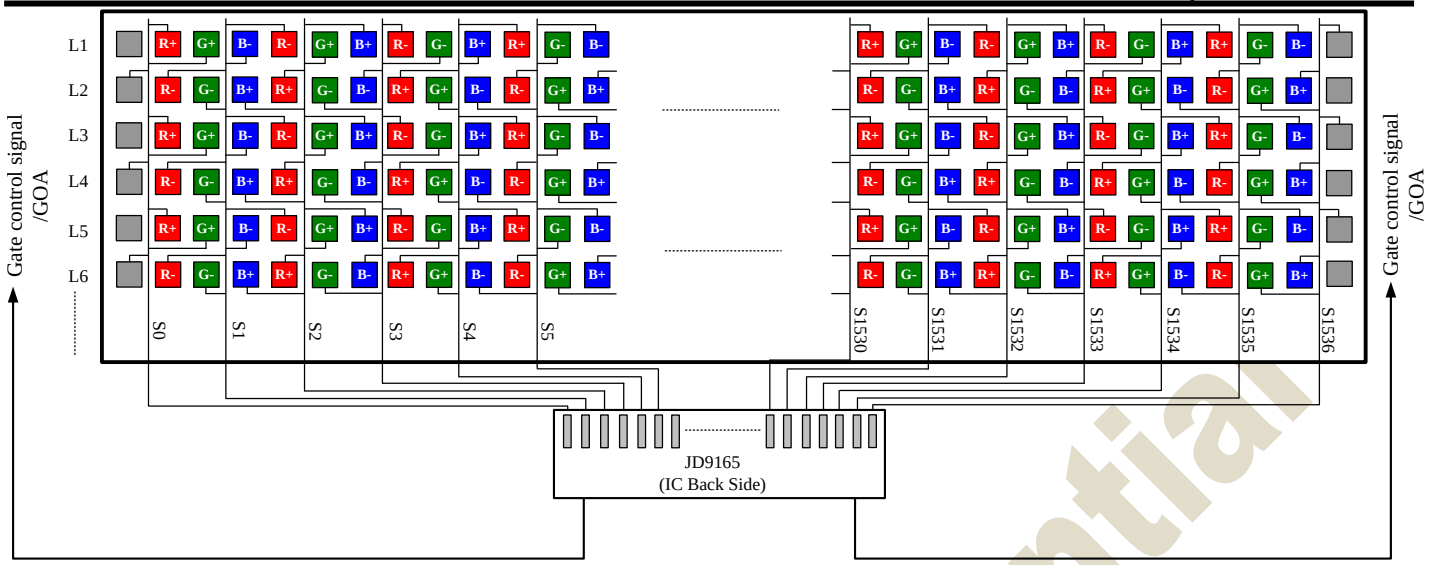


Figure 5.7: Dual gate+Zig-zag type3 panel structure

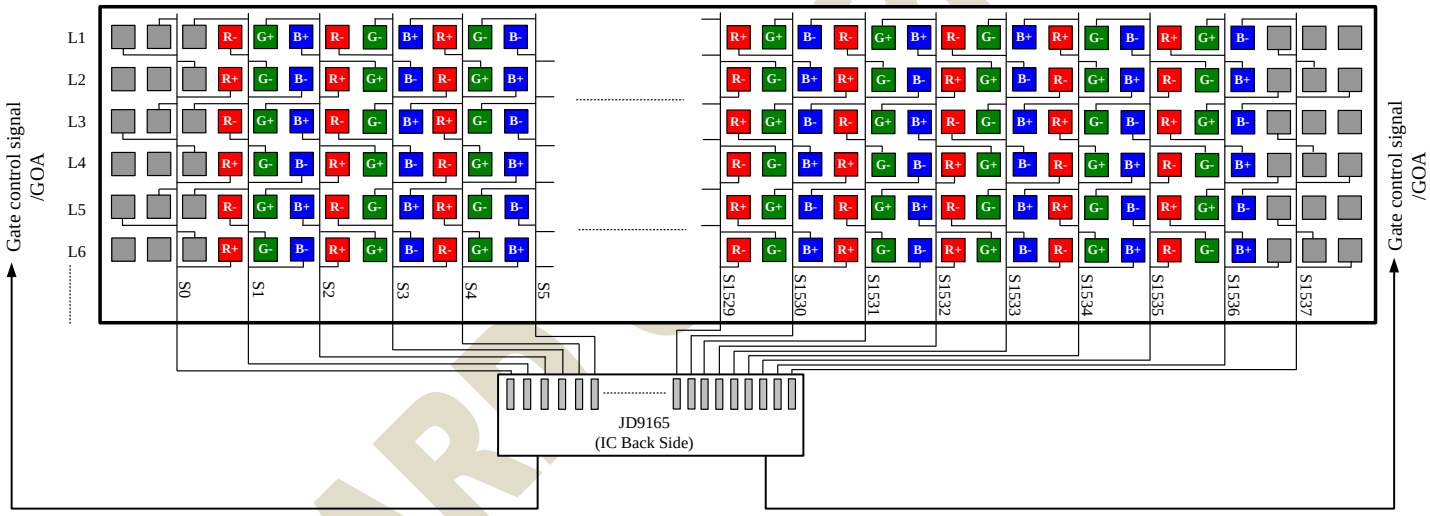


Figure 5.8: Dual gate+Zig-zag type4 panel structure

5.3.3 Single Gate Panel Configuration

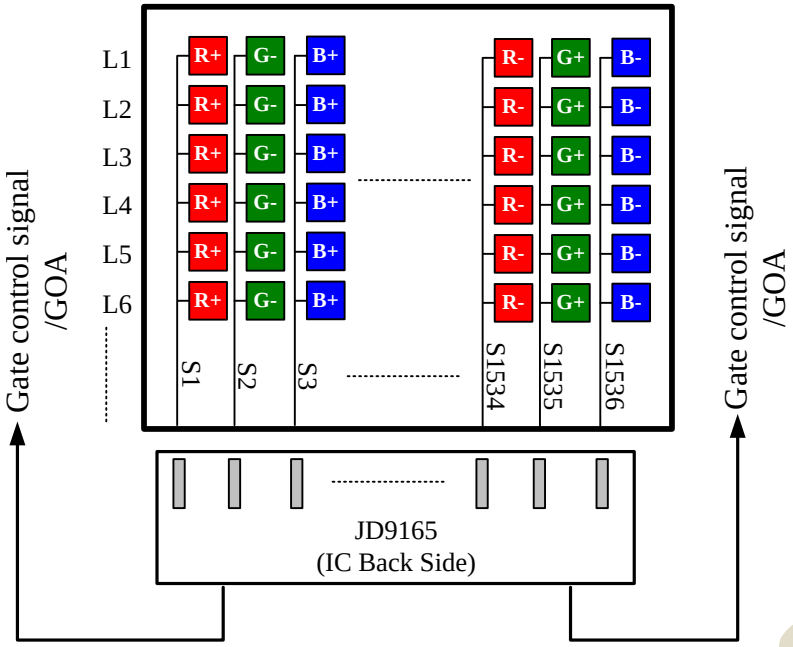


Figure 5.9: Single gate panel structure

5.4 Gamma correction

JD9165 gamma correction are done by 13-segment piecewise linear interpolation. The 13 segments are defined with 14 register values for level 0, 8, 16, 32, 60, 88, 116, 144, 172, 200, 220, 236, 248, 255.These gamma register stream has 64-1 selector to adjust voltage.

5.4.1 Gamma structure

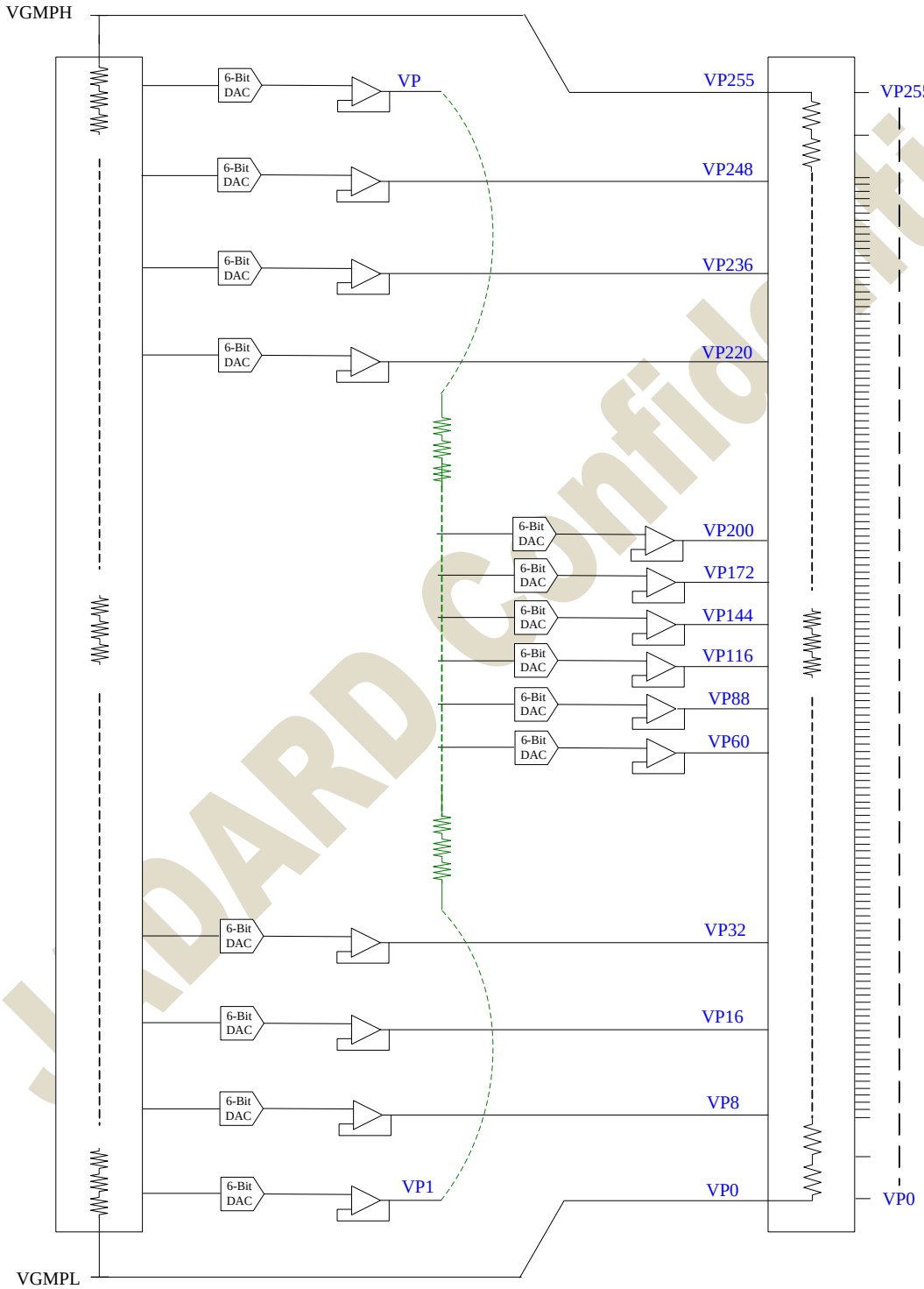


Figure 5.10: Positive analog gamma structure

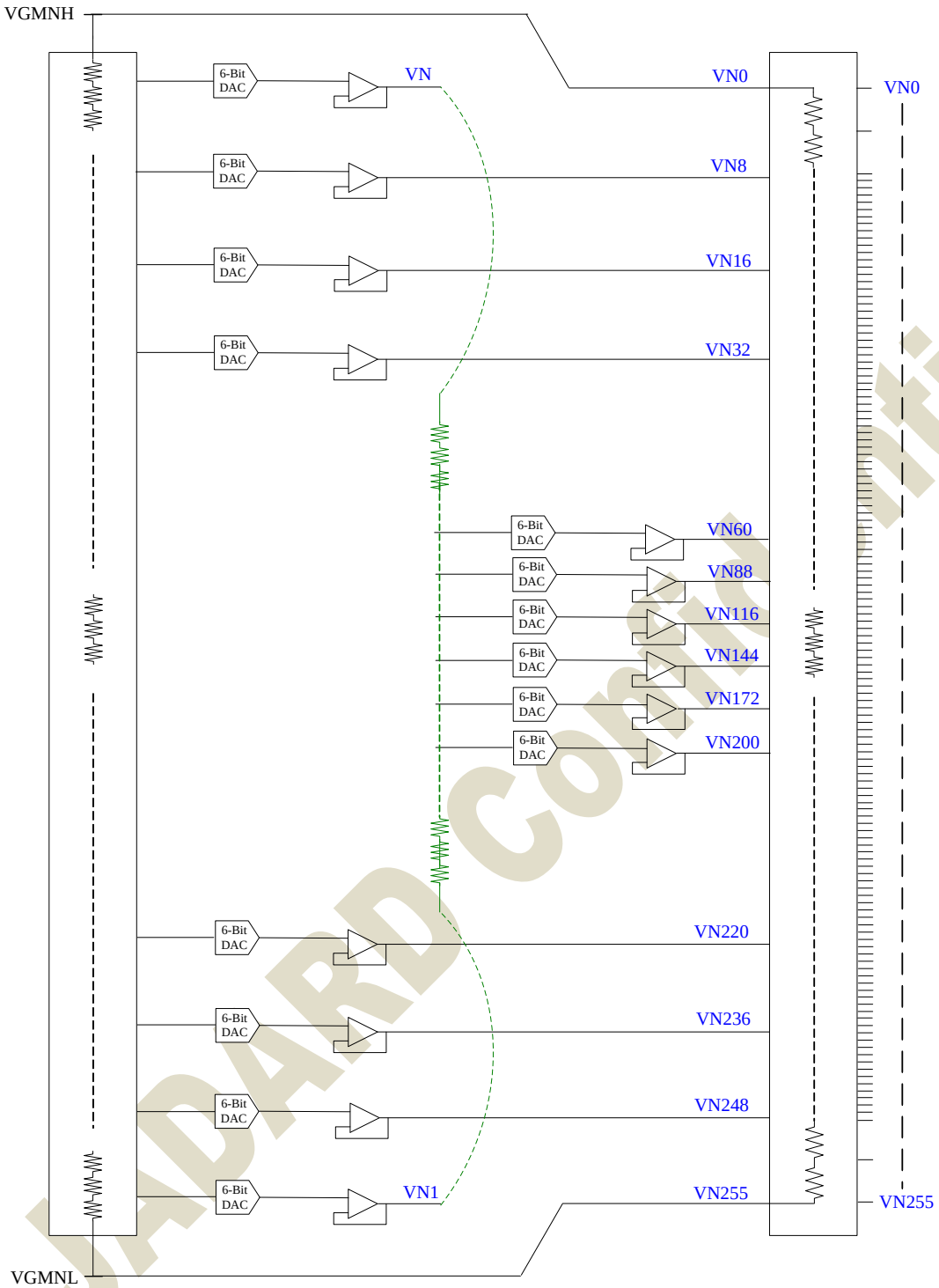


Figure 5.11: Negative analog gamma structure

5.4.2 Gamma voltage reference table

The reference voltages can be set by registers, as described in the following table.

Setting for positive gamma voltage

Gamma code	Reference voltage
VP1	VGMPL+(VGMPH-VGMPL)/200*(12+REG_VP0_S[5:0])
VP8	VGMPL+(VGMPH-VGMPL)/200*(1+REG_VP8_S[5:0])
VP16	VGMPL+(VGMPH-VGMPL)/200*(6+REG_VP16_S[5:0])
VP32	VGMPL+(VGMPH-VGMPL)/200*(12+REG_VP32_S[5:0])
VP60	VP32+(VP220-VP32)/150*(6+REG_VP60_S[5:0])
VP88	VP32+(VP220-VP32)/150*(10+REG_VP88_S[5:0])
VP116	VP32+(VP220-VP32)/150*(24+REG_VP116_S[5:0])
VP144	VP32+(VP220-VP32)/150*(39+REG_VP144_S[5:0])
VP172	VP32+(VP220-VP32)/150*(58+REG_VP172_S[5:0])
VP200	VP32+(VP220-VP32)/150*(80+REG_VP200_S[5:0])
VP220	VGMPL+(VGMPH-VGMPL)/200*(86+REG_VP220_S[5:0])
VP236	VGMPL+(VGMPH-VGMPL)/200*(116+REG_VP236_S[5:0])
VP248	VGMPL+(VGMPH-VGMPL)/200*(137+REG_VP248_S[5:0])
VP	VGMPL+(VGMPH-VGMPL)/200*(86+REG_VP255_S[5:0])

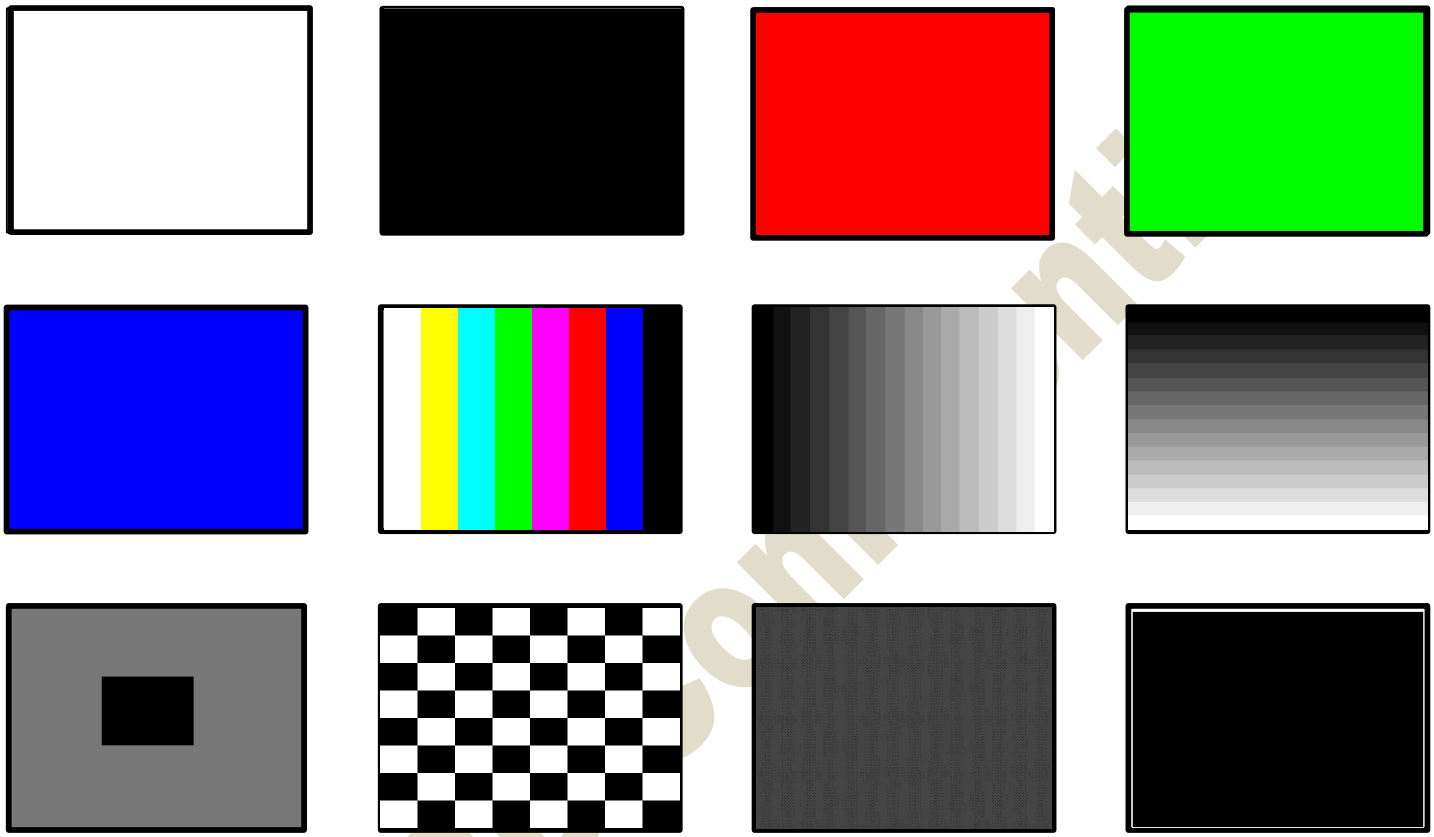
Setting for negative voltage

Gamma code	Reference voltage
VN	VGMNL+(VGMNH-VGMNL)/200*(12+REG_VN0_S[5:0])
VN8	VGMNL+(VGMNH-VGMNL)/200*(1+REG_VN8_S[5:0])
VN16	VGMNL+(VGMNH-VGMNL)/200*(6+REG_VN16_S[5:0])
VN32	VGMNL+(VGMNH-VGMNL)/200*(12+REG_VN32_S[5:0])
VN60	VN32+(VN220-VN32)/150*(6+REG_VN60_S[5:0])
VN88	VN32+(VN220-VN32)/150*(10+REG_VN88_S[5:0])
VN116	VN32+(VN220-VN32)/150*(24+REG_VN116_S[5:0])
VN144	VN32+(VN220-VN32)/150*(39+REG_VN144_S[5:0])
VN172	VN32+(VN220-VN32)/150*(58+REG_VN172_S[5:0])
VN200	VN32+(VN220-VN32)/150*(80+REG_VN200_S[5:0])
VN220	VGMNL+(VGMNH-VGMNL)/200*(86+REG_VN220_S[5:0])
VN236	VGMNL+(VGMNH-VGMNL)/200*(116+REG_VN236_S[5:0])
VN248	VGMNL+(VGMNH-VGMNL)/200*(137+REG_VN248_S[5:0])
VN1	VGMNL+(VGMNH-VGMNL)/200*(86+REG_VN255_S[5:0])

5.5 BIST function

When BIST is trigger to high, then JD9165 will leave normal operation mode and starts to generate the BIST pattern to LCD panel without TX input signals.

5.5.1 BIST pattern



White→Black→R→G→B→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern→Chess board (L255/L0)→Gray128→Black background with white out frame

5.6 GAS function

When battery is removed from an electronic device, the image still keeps on the LCD panel for a long time. GAS function can speed the process that image disappears.

The GAS function is a voltage detector. By GAS circuit, JD9165 can detect voltage of VDD/AVDD/VGH and sent ideal GAS signal to discharge residual potential in LCD panel and removes image. The detect voltage could be selected by register setting.

When VDD recovers, power on procedure must be done to return normal mode.

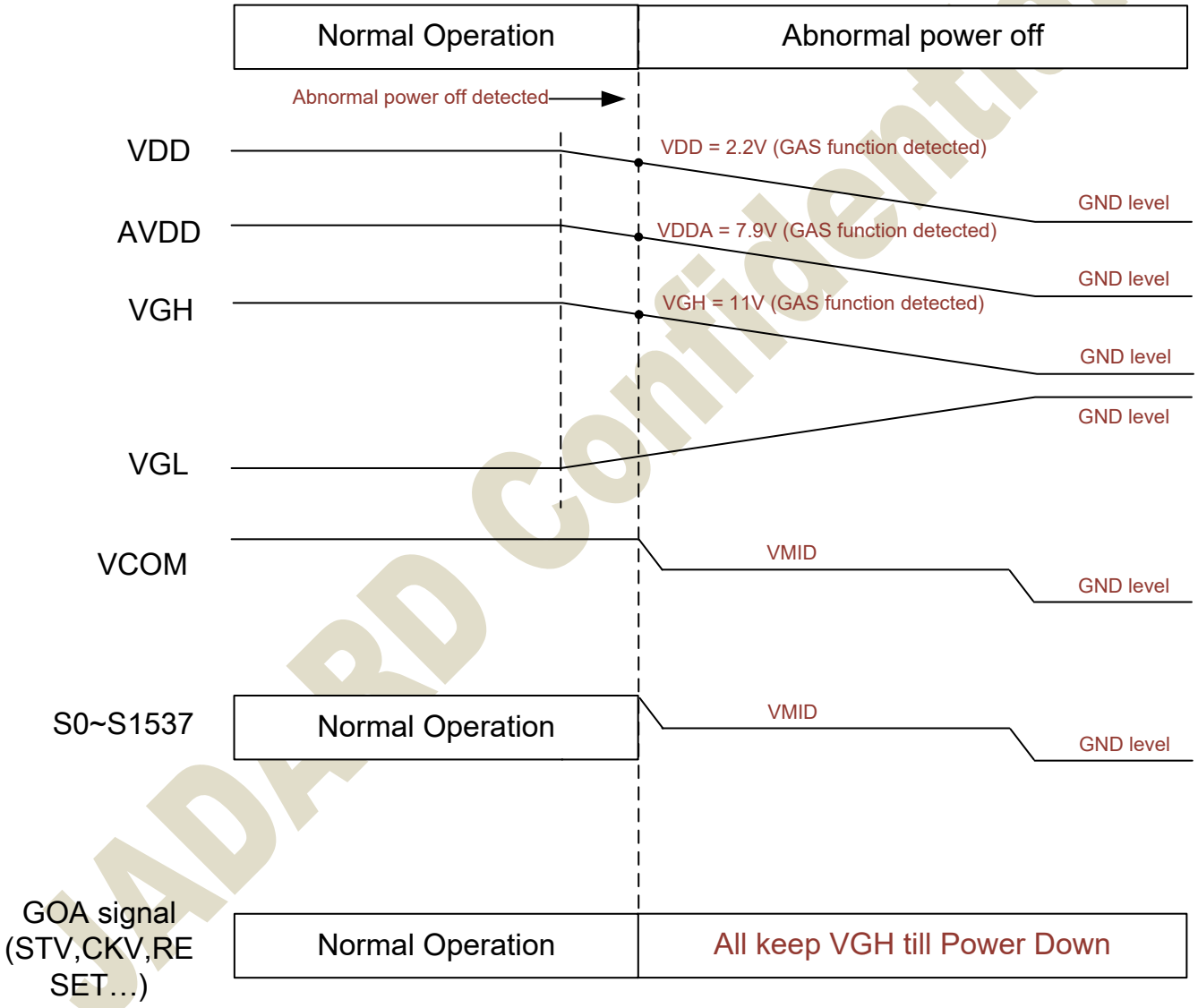


Figure 5.12: GAS discharge timing

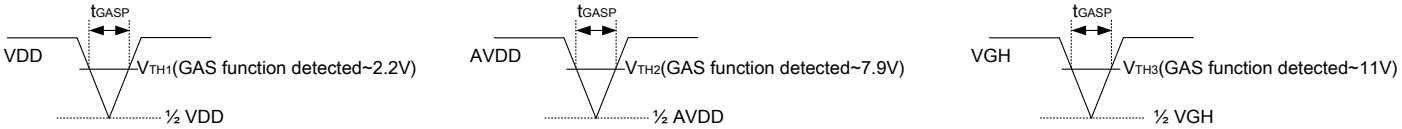


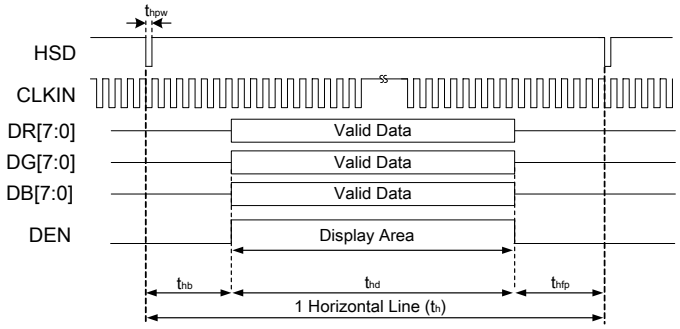
Figure 5.13: GAS V.S. VDD/AVDD/VGH

Parameter	Symbol	Step	Spec			Unit
			Min	Typ	Max	
VDD/AVDD power drop noise filter period.	T_{GASP}	-	100	-	-	ns
GAS function detection threshold voltage. VDD lower than V_{TH1}, IC will execute GAS function	V_{TH1}	0.1	1.5	2.2	3.0	V
GAS function detection threshold voltage. AVDD lower than V_{TH2}, IC will execute GAS function	V_{TH2}	0.5	7.11	7.9	8.3	V
GAS function detection threshold voltage. VGH lower than V_{TH3}, IC will execute GAS function	V_{TH3}	0.5	11	11	15	V

6. TTL INPUT TIMING

6.1 24-bit parallel RGB data input format

●Horizontal timing



● Vertical timing

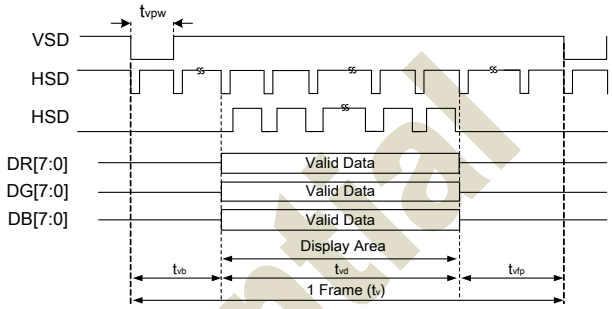


Figure 6.1: 24-bit parallel RGB mode horizontal/vertical input timing

6.2 TTL timing characteristic

24-bit parallel RGB Input Timing	Symbol	1024RGBx768			1024RGBx600			800RGBx600			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DCLK Frequency	-	52.7	65	71	41.4	51.2	67.2	33.1	39.6	62.4	MHZ
Horizontal Total	tht	1114	1344	1400	1114	1344	1400	890	1000	1300	DCLK
Hsync Pulse width	ths	1	24	HBP-1	1	24	HBP-1	1	24	HBP-1	DCLK
Horizontal Back Porch	thb	60	160	160	60	160	160	60	160	250	DCLK
Horizontal Valid Data	thd		1024			1024			800		DCLK
Horizontal Front Porch	thfp	30	160	216	30	160	216	30	40	250	DCLK
Vertical Total	tvt	788	806	845	620	635	800	620	660	800	THT
Vsync Pulse Width	tvs	1	2	VBP-1	1	2	VBP-1	1	2	VBP-1	THT
Vertical Back Porch	tvb	8	23	33	8	23	100	8	23	100	THT
Vertical Valid Data	tvd		768			600			600		THT
Vertical Front Porch	tvfp	12	15	44	12	12	100	12	37	100	THT

24-bit parallel RGB Input Timing	Symbol	800RGBx480			640RGBx480			480RGBx272			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DCLK Frequency	-	29	32.4	62	32.6	39.6	53.4	24.8	32.6	37.6	MHZ
Horizontal Total	tht	900	1000	1300	890	1000	1114	830	890	950	DCLK
Hsync Pulse width	ths	4	24	HBP-1	1	24	HBP-1	1	24	HBP-1	DCLK
Horizontal Back Porch	thb	62	160	250	140	88	220	180	210	240	DCLK
Horizontal Valid Data	thd		800			640			480		DCLK
Horizontal Front Porch	thfp	38	40	250	110	272	254	170	200	230	DCLK
Vertical Total	tvt	500	540	680	610	660	800	498	610	660	THT
Vsync Pulse Width	tvs	1	2	VBP-1	1	2	VBP-1	1	2	VBP-1	THT
Vertical Back Porch	tvb	8	23	100	28	39	160	126	180	210	THT
Vertical Valid Data	tvd		480			480			272		THT
Vertical Front Porch	tvfp	12	37	100	102	141	160	100	158	178	THT

6.3 TTL AC electrical characteristic

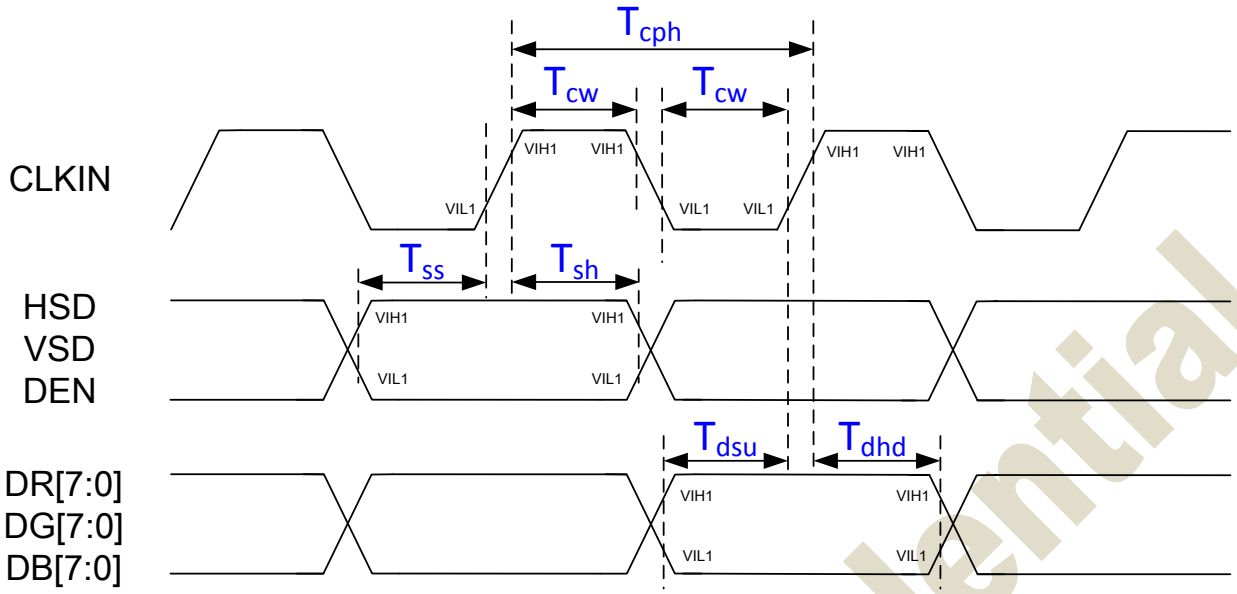


Figure 6.2: Input signal timing

Input data /sync parameters

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLKIN period	T_{cph}	14	-	-	ns
CLKIN duty ratio	T_{cw}	40	50	60	%
Data setup time	T_{dsu}	5	-	-	ns
Data hold time	T_{dhd}	5	-	-	ns
VSD setup time	T_{ss}	5	-	-	ns
VSD hold time	T_{sh}	5	-	-	ns
HSD setup time	T_{ss}	5	-	-	ns
HSD hold time	T_{sh}	5	-	-	ns
DEN setup time	T_{ss}	5	-	-	ns
DEN hold time	Ts_h	5	-	-	ns

Table 6.1: TTL mode AC electrical characteristics

7. LVDS INPUT TIMING

7.1 LVDS data input format

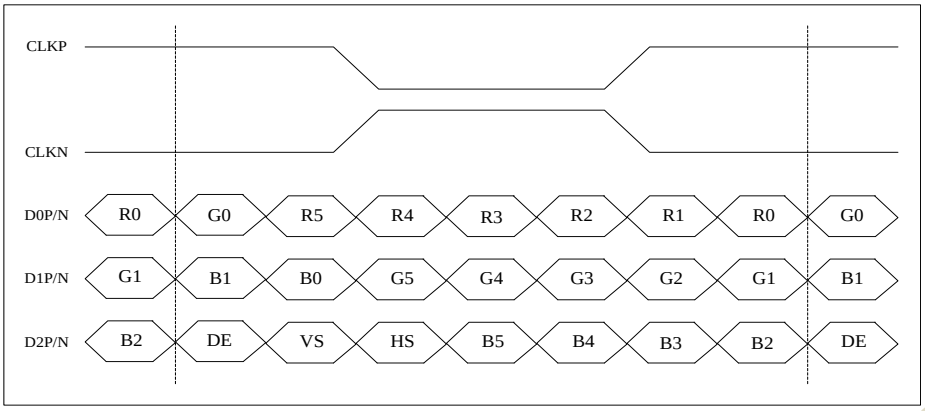


Figure 7.1: 6-bit RGB LVDS input timing

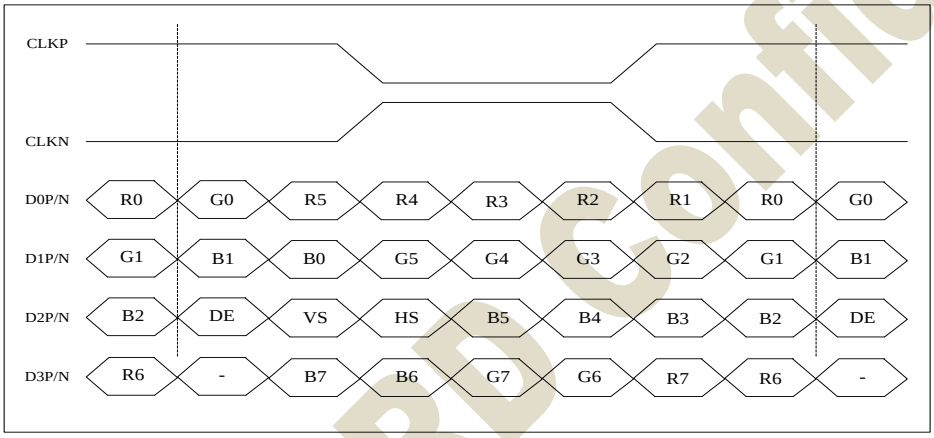


Figure 7.2: 8-bit RGB LVDS VESA input timing

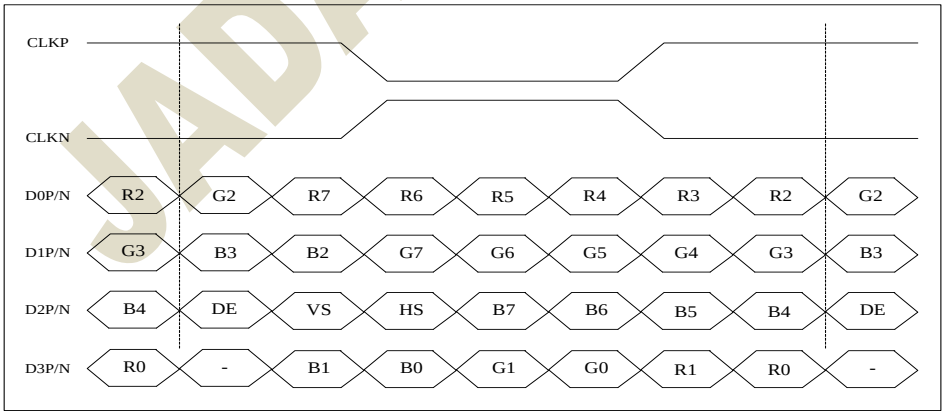


Figure 7.3: 8-bit RGB LVDS JEIDA input timing

7.2 LVDS timing characteristic

LVDS Input Timing	Symbol	1024RGBx768			1024RGBx600			800RGBx600			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DCLK Frequency	-	52.7	65	71	41.4	51.2	67.2	33.1	39.6	62.4	MHZ
Horizontal Total	tht	1114	1344	1400	1114	1344	1400	890	1000	1300	DCLK
Hsync Pulse width	ths	1	24	HBP-1	1	24	HBP-1	1	24	HBP-1	DCLK
Horizontal Back Porch	thb	60	160	160	60	160	160	60	160	250	DCLK
Horizontal Valid Data	thd		1024			1024			800		DCLK
Horizontal Front Porch	thfp	30	160	216	30	160	216	30	40	250	DCLK
Vertical Total	tvt	788	806	845	620	635	800	620	660	800	THT
Vsync Pulse Width	tvs	1	2	VBP-1	1	2	VBP-1	1	2	VBP-1	THT
Vertical Back Porch	tvb	8	23	33	8	23	100	8	23	100	THT
Vertical Valid Data	tvd		768			600			600		THT
Vertical Front Porch	tvfp	12	15	44	12	12	100	12	37	100	THT

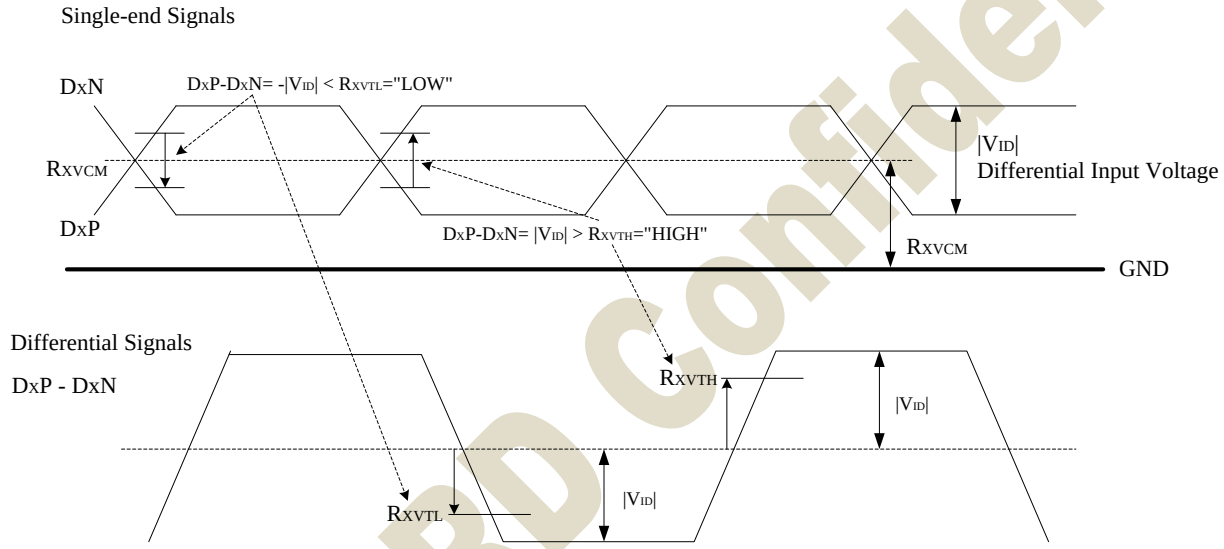
LVDS Input Timing	Symbol	800RGBx480			640RGBx480			480RGBx272			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DCLK Frequency	-	29	32.4	62	32.6	39.6	53.4	24.8	32.6	37.6	MHZ
Horizontal Total	tht	900	1000	1300	890	1000	1114	830	890	950	DCLK
Hsync Pulse width	ths	4	24	HBP-1	1	24	HBP-1	1	24	HBP-1	DCLK
Horizontal Back Porch	thb	62	160	250	140	88	220	180	210	240	DCLK
Horizontal Valid Data	thd		800			640			480		DCLK
Horizontal Front Porch	thfp	38	40	250	110	272	254	170	200	230	DCLK
Vertical Total	tvt	500	540	680	610	660	800	498	610	660	THT
Vsync Pulse Width	tvs	1	2	VBP-1	1	2	VBP-1	1	2	VBP-1	THT
Vertical Back Porch	tvb	8	23	100	28	39	160	126	180	210	THT
Vertical Valid Data	tvd		480			480			272		THT
Vertical Front Porch	tvfp	12	37	100	102	141	160	100	158	178	THT

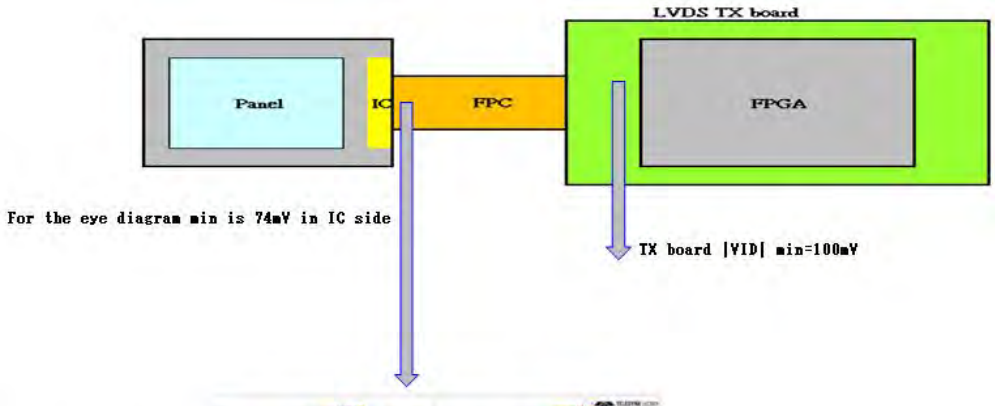
7.3 LVDS DC electrical characteristic

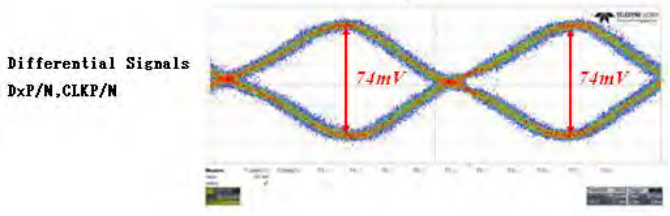
(Test condition: VDD=2.8V~3.6V, VSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input high threshold voltage	R_{XVTH}			+37	mV	
Differential input low threshold voltage	R_{XVTL}	-37			mV	
Input voltage range (singled-end)	R_{XVIN}	400	-	1650	mV	1. R_{XVCM}+1/2|V_{ID}|<=1650mV. 2. R_{XVCM}-1/2|V_{ID}|>=400mV.
Differential input common mode voltage	R_{XVCM}	600	1200	1375	mV	
Differential input voltage	|V_{ID}|	100	-	400	mV	
Differential input impedance	Z_{ID}	80	100	120	ohm	
Differential input leakage current	I_{LCLVDS}	-10	-	+10	uA	

Table 7.1: LVDS mode DC electrical characteristics







7.4 LVDS AC electrical characteristic

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	R_{xFCLK}	20	-	71	MHz	Refer to input timing table for each display resolution
Input data skew margin	T_{RSKM}	-0.2	-	0.2	UI	|VID| = 200mV RxVCM = 1.2V 1UI=1/(RxFCLKx7)
Clock high time	T_{LVCH}	-	3.5/(7* R_{xFCLK})	-	ns	
Clock low time	T_{LVCL}	-	3.5/(7* R_{xFCLK})	-	ns	
PLL wake-up time	T_{enPLL}	-	-	150	us	

Table 7.2: LVDS mode AC electrical characteristics

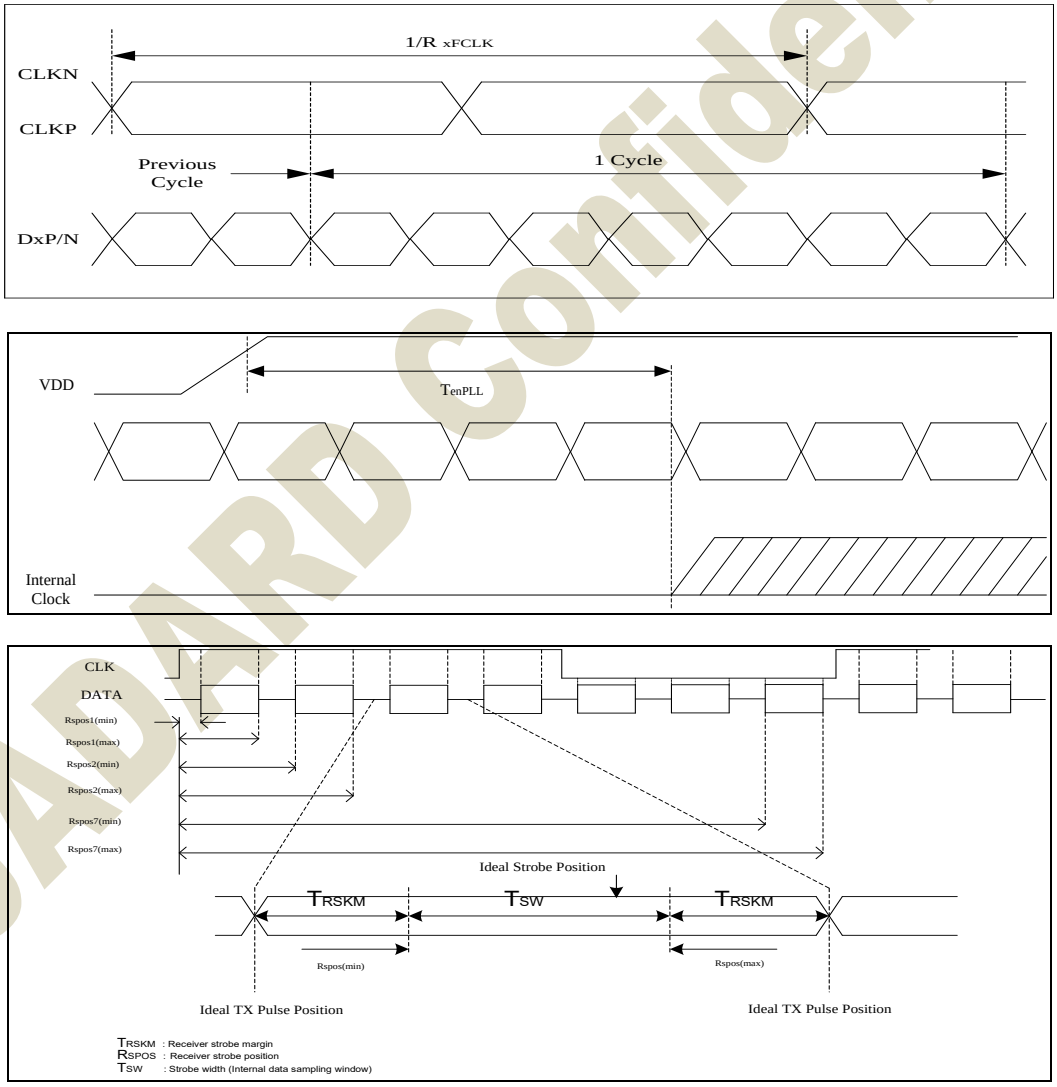


Figure 7.4: LVDS figure

8. MIPI INTERFACE

8.1 DSI system interface

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specification by adopting pixel formats and command set specified in DP1-2, DBI-2 and DCS standards.

Figure 8.1 shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.

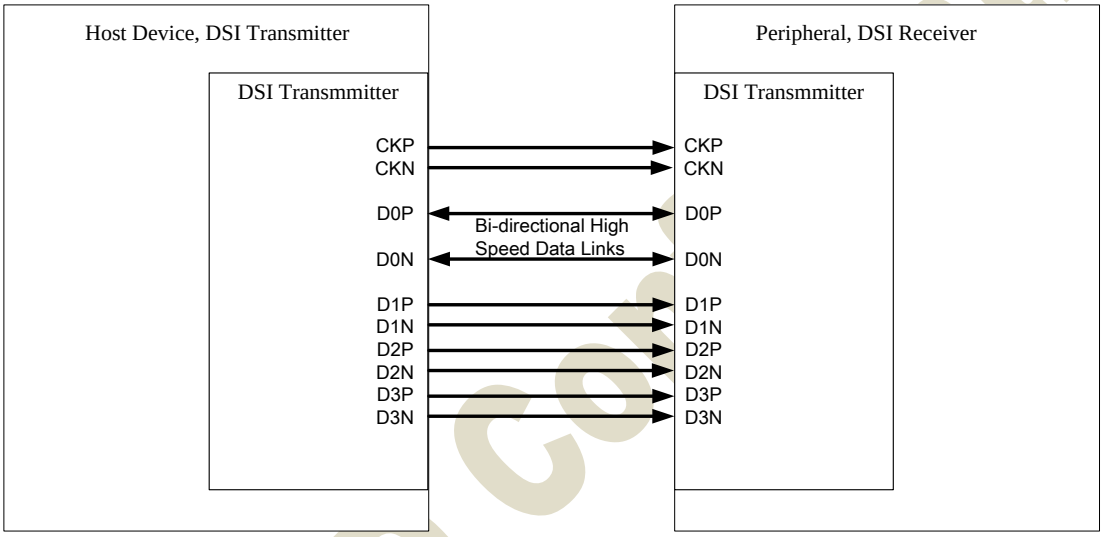


Figure 8.1: DSI transmitter and receiver interface

A conceptual vide of DSI organizes the interface into several functional layers. A description of the layers follows and is also shown in Figure 8.2

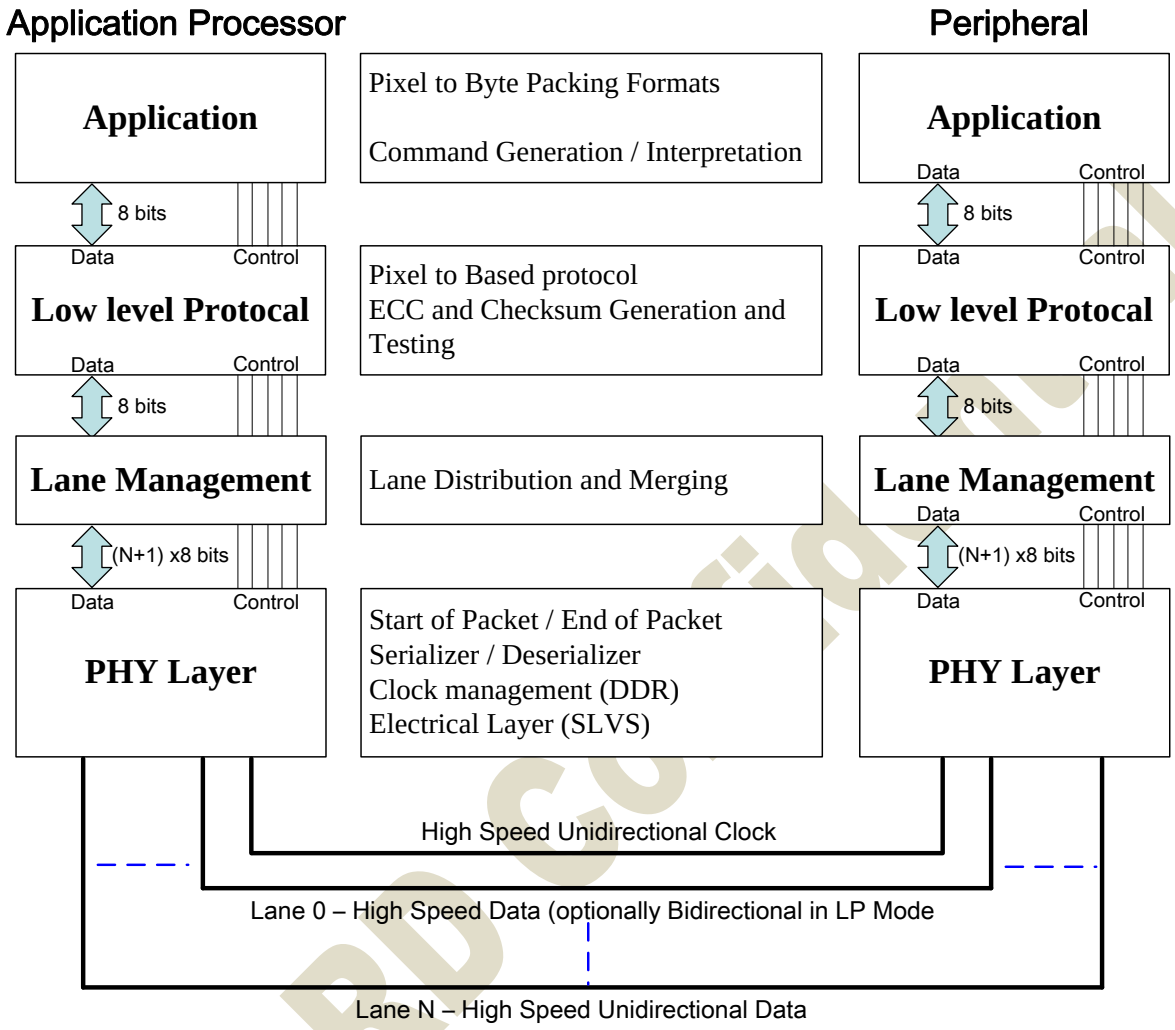


Figure 8.2: DSI Layer

PHY Layer: The PHY Layer specifies transmission medium (electrical conductors), the input/output circuitry and the clocking mechanism that captures “ones” and “zeroes” from the serial bit stream. Bit-level and byte-level synchronization mechanisms are included as part of the PHY.

Lane Management Layer: DSI is Lane-scalable for increased performance. The number of data signals may be 1,2,3, or 4 depending on the bandwidth requirements of the application. The transmitter side of the interface distributes the outgoing data stream to one or more Lanes (“distributor” function). On the receiving end, the interface collects bytes from the Lanes and merges them together into recombined data stream that restores the original stream sequence (“merger” function).

Protocol Layer: At the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets. The protocol defines required headers for each packet, and how header information is generated and interpreted. The transmitting side of the interface appends header and error-checking information to data being transmitted. On the receiving side, the header is stripped off and interpreted by corresponding logic in the receiver. Error-checking information may be used to test the integrity of incoming data. DSI protocol also documents how packets may be tagged for interleaving multiple command or data stream to

separate destinations using a single DSI.

Application Layer: This layer describes higher-level encoding and interpretation of data contained in the data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed format, or of commands that are interpreted by the display controller inside a display module. The DSI specification describes the mapping of pixel values, commands and command parameters to bytes in the packet assembly.

8.2 Video mode and Virtual Channel

Video Mode

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the display image. Video information should only be transmitted using High Speed Mode.

Some Video Mode architectures may include a simple timing controller and partial line buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Virtual Channel Capability

While this specification only addresses the connection of a host processor to a single peripheral, DSI incorporates a virtual channel capability for communication between a host processor and multiple, physical display modules. Since interface bandwidth is shared between peripherals, there are constraints that limit the physical extent and performance of multiple-peripheral systems. The DSI protocol permits up to four virtual channels, enabling traffic for multiple peripherals to share a common DSI Link. The DSI specification makes no requirements on the specific value assigned to each virtual channel used to designate interlaced fields, For clarity, the first interlaced video field may be assigned as DI[7:6]=2’b00 and the second interlaced video field may be assigned DI[7:6]=2’b01.

8.3 DSI Format

Information is transferred between host processor and peripheral using one or more serial data signals and accompanying serial clock. The action of sending high-speed serial data across the bus is called a HS transmission or burst. Between transmissions, the differential data signal or Lane goes to a low-power state (LPS). Interfaces should be in LPS when they are not actively transmitting or receiving high-speed data. Figure 8.3 shows the basic structure of a HS transmission. N is the total number of bytes sent in the transmission.

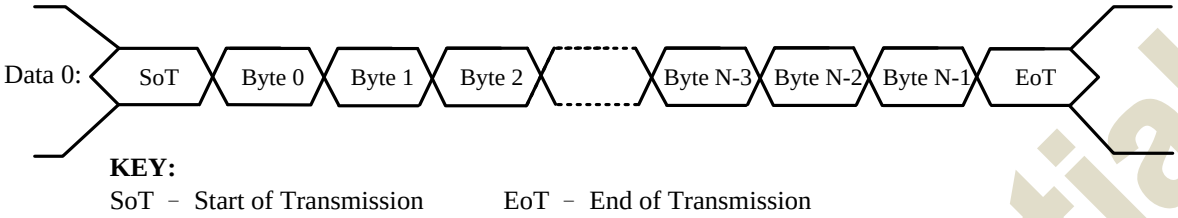


Figure 8.3: Basic HS Transmission Structure

Multi Lane Distribution and Merging

DSI is a Lane-scalable interface. Applications requiring more bandwidth than that provided by one Data Lane may expand the data path to two, three, or four Lanes wide and obtain approximately linear increases in peak bus bandwidth.

Multi-Lane implementations shall use a single common clock signal, shared by all Data Lanes. Conceptually, between the PHY and higher functional blocks is a layer that enables multi-Lane operation.

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel Sots, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission. Figure 8.4 & 8.5 illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

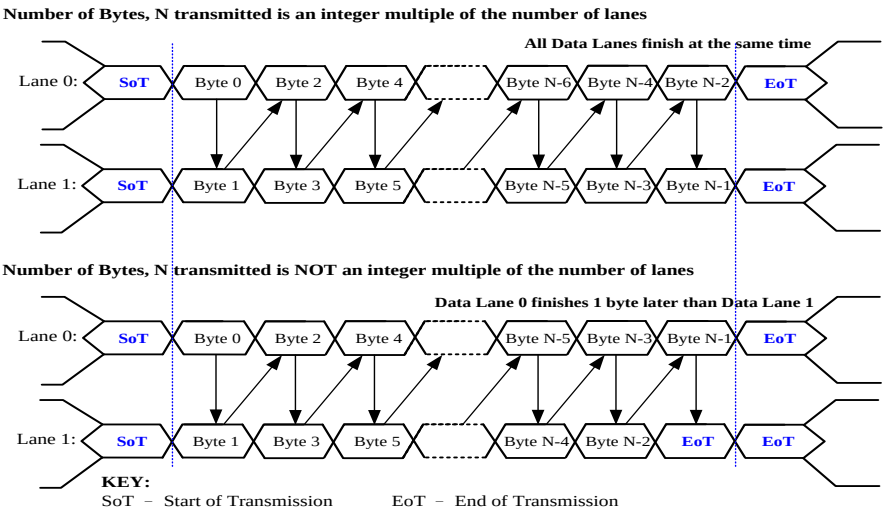


Figure 8.4: Two Lane HS Transmission Example

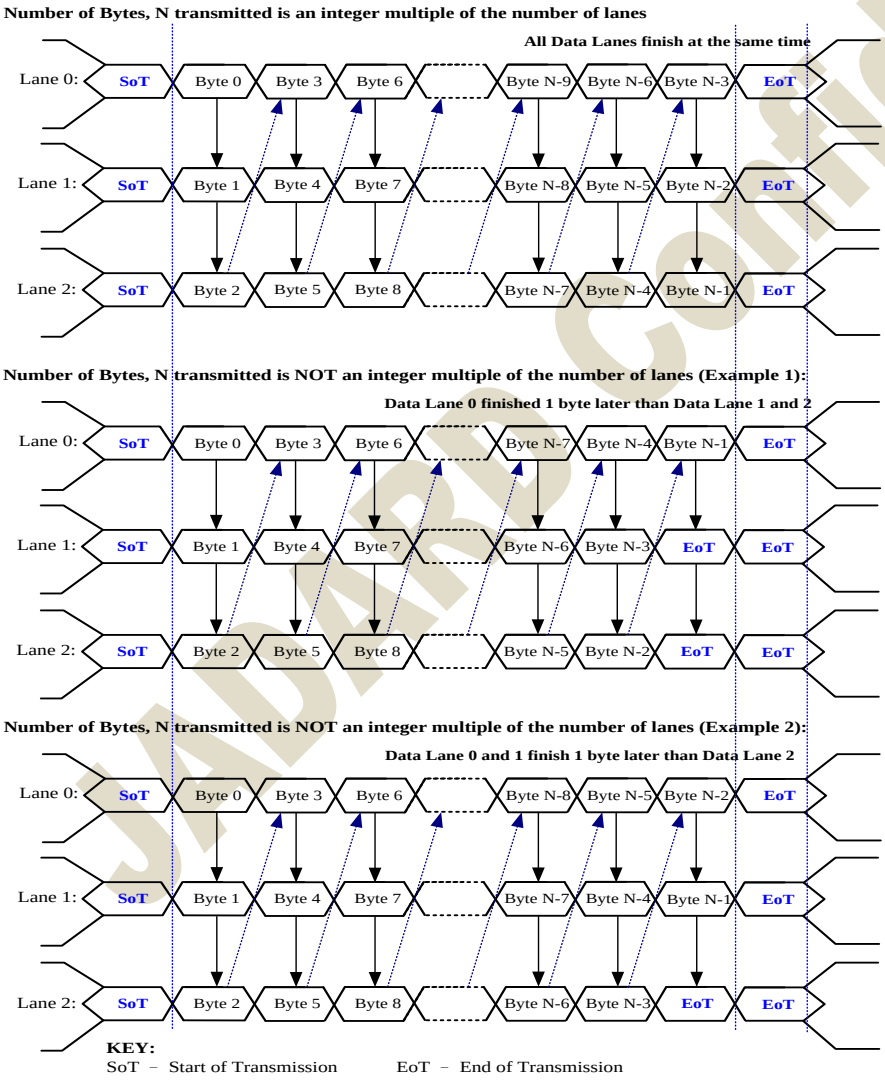


Figure 8.5: Three Lane HS Transmission Example

8.4 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets, following the packet organization documented in this section. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY.

8.5 Multiple Packets per Transmission

In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the overhead of frequent switching between LPS and High-Speed-Mode will severely limit bandwidth if packets are sent separately, e.g. one packet per transmission.

The DSI protocol permits multiple packets to be concatenated, which substantially boots effective bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup.

There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled. The method of enabling or disabling this capability is out of scope for this document.

The top diagram in Figure 8.6 illustrates a case where multiple packets are being sent separately with EoTp support disabled. In HS mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT issued by the PHY layer between packets. This constraint does not apply to LP transmissions. The bottom diagram in Figure 8.6 demonstrates a case where multiple packets are concatenated within a single HS transmission.

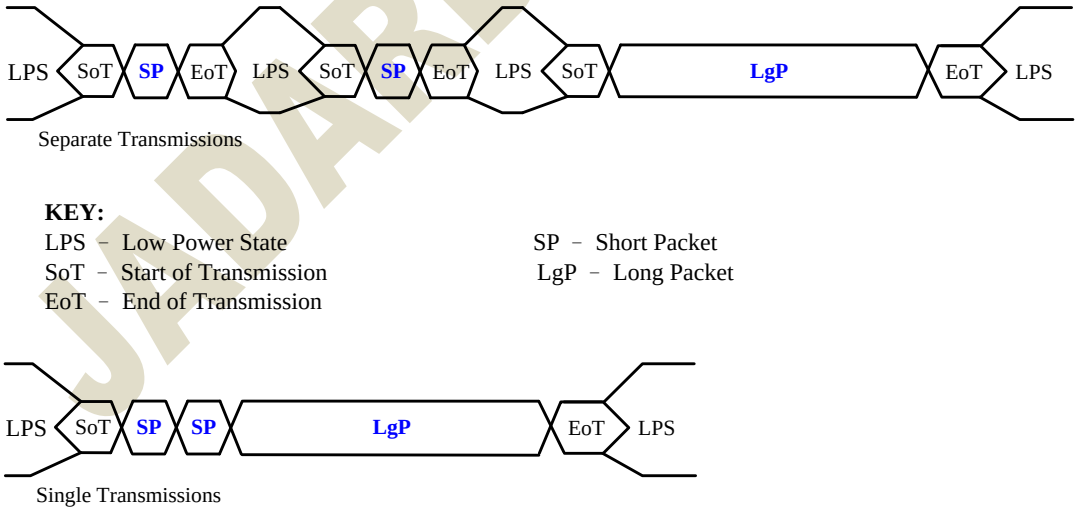


Figure 8.6: HS Transmission Examples with EoTp disabled

Figure 8.7 depicts HS transmission cases where EoTp generation is enabled. In the figure, EoT short packets are highlighted in red. The top diagram illustrates a case where a host is intending to send a short packet followed by a long packet using two separate transmissions. In this case, an additional EoT short packet is generated before each transmission ends. This mechanism provides a more robust environment, at the expense of increased overhead (four extra bytes per transmission) compared to cases where EoTp generation is disabled, i.e. the system only relies on the PHY layer EoT sequence for signaling the end of HS transmission. The overhead imposed by enabling EoTp can be minimized by sending multiple long and short packets within a single transmission as illustrated by the bottom diagram in Figure 8.7.

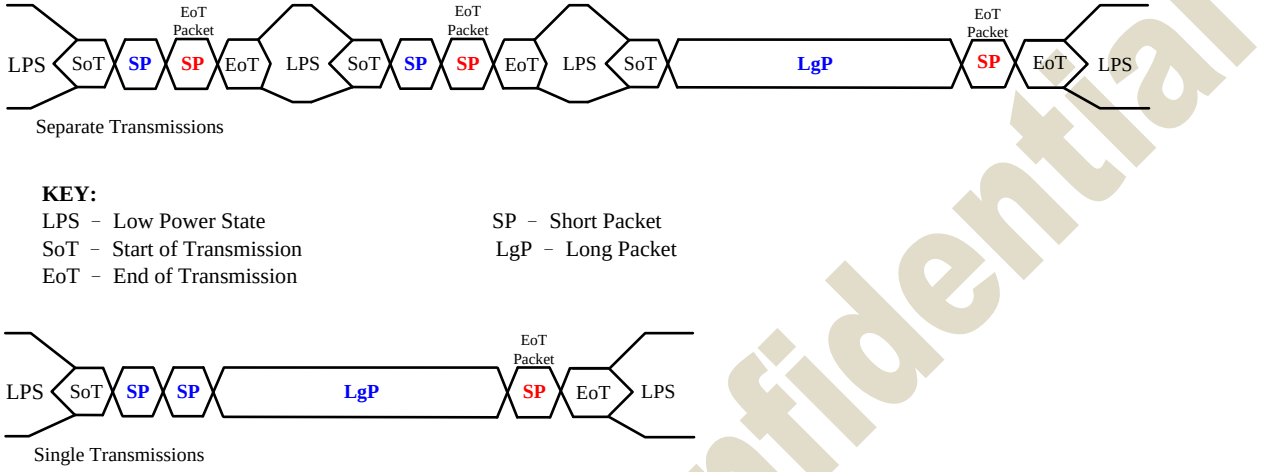


Figure 8.7: HS Transmission Examples with EoTp enabled

8.6 Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure 8.8 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

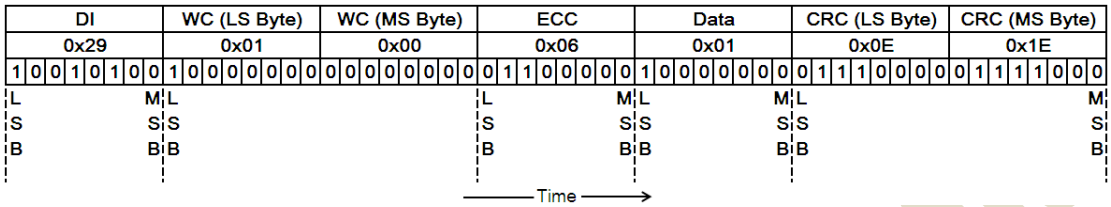


Figure 8.8: Endian Example (Long Packet)

8.7 Packet Structure

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. Packet sizes fall into two categories:

• **Long packets** specify the payload length using a two-byte Word Count field. Payloads may be from 0 to 216- 1 bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.

• **Short packets** are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.

The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

8.8 Long Packet

Figure 8.9 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

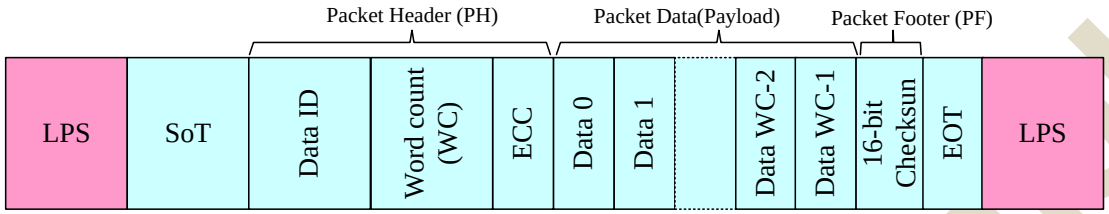


Figure 8.9: Long Packet Structure

The Data Identifier defines the Virtual Channel for the data and the Data Type for application specific payload data.

The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count.

The Error Correction Code (ECC) bytes allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count field.

After the end of the Packet Header, the receiver reads the next Word Count * bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used.

Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (0xFFFF). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0x0000). In the generic case, the length of the Data Payload shall be a multiple of bytes.

Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall transmitted least significant byte first.

8.9 Short Packet

Figure 8.10 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

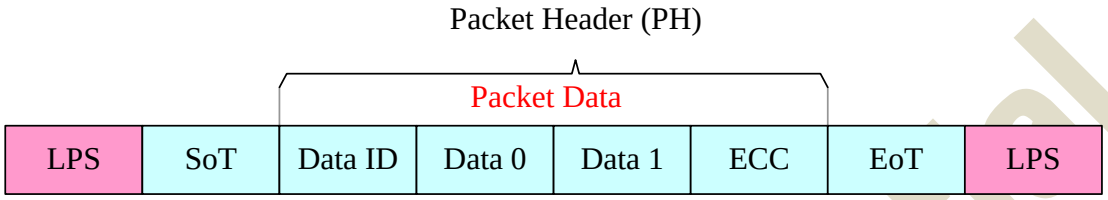


Figure 8.10: Short Packet Structure

8.10 Command Packet Elements

Long and Short packets have several common elements that are described in this section.

8.10.1 Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 8.11 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels. DI[5:4]: These two bits specify the Data Type.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		DT (Data Type)					

Figure 8.11: Data Identifier Byte

8.10.2 Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel.

8.10.3 Data Type Field DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

8.10.4 ECC

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communication.

8.11 DSI packet

8.11.1 Processor-sourced Packets

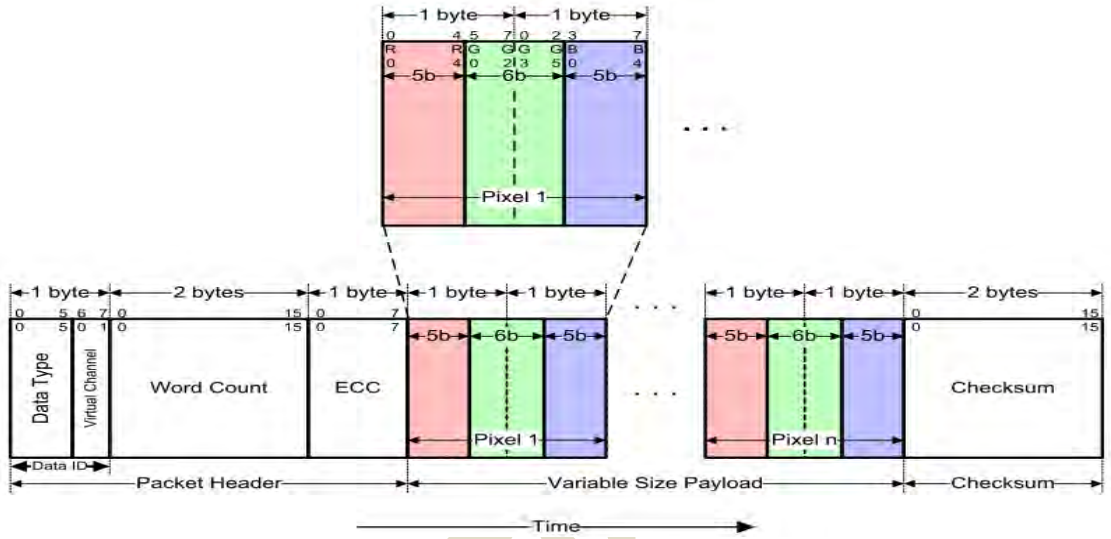
The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 8.1.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x08	00 1000	End of Transmission Packet (EoTP) Note1	Short
0x02	00 0010	Color Mode (CM) Off Command	Short
0x12	01 0010	Color Mode (CM) On Command	Short
0x22	10 0010	Shut Down Peripheral Command	Short
0x32	11 0010	Turn On Peripheral Command	Short
0x03	00 0011	Generic Short WRITE, no parameters	Short
0x13	01 0011	Generic Short WRITE, 1 parameters	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic Short READ, no parameters	Short
0x14	01 0100	Generic Short READ, 1 parameters	Short
0x24	10 0100	Generic Short READ, 2 parameters	Short
0x05	00 0101	DCS Write, No Parameter	Short
0x15	01 0101	DCS Write, 1 Parameter	Short
0x06	00 0110	DCS Read, No Parameter	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, No Data, Note2	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Write Long	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
0xX0 0xXF	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	--

Table 8.1: Data Types for supported Processor-sourced Packets

8.11.2 Packed Pixel Stream, 16-bit Format, Long Packet

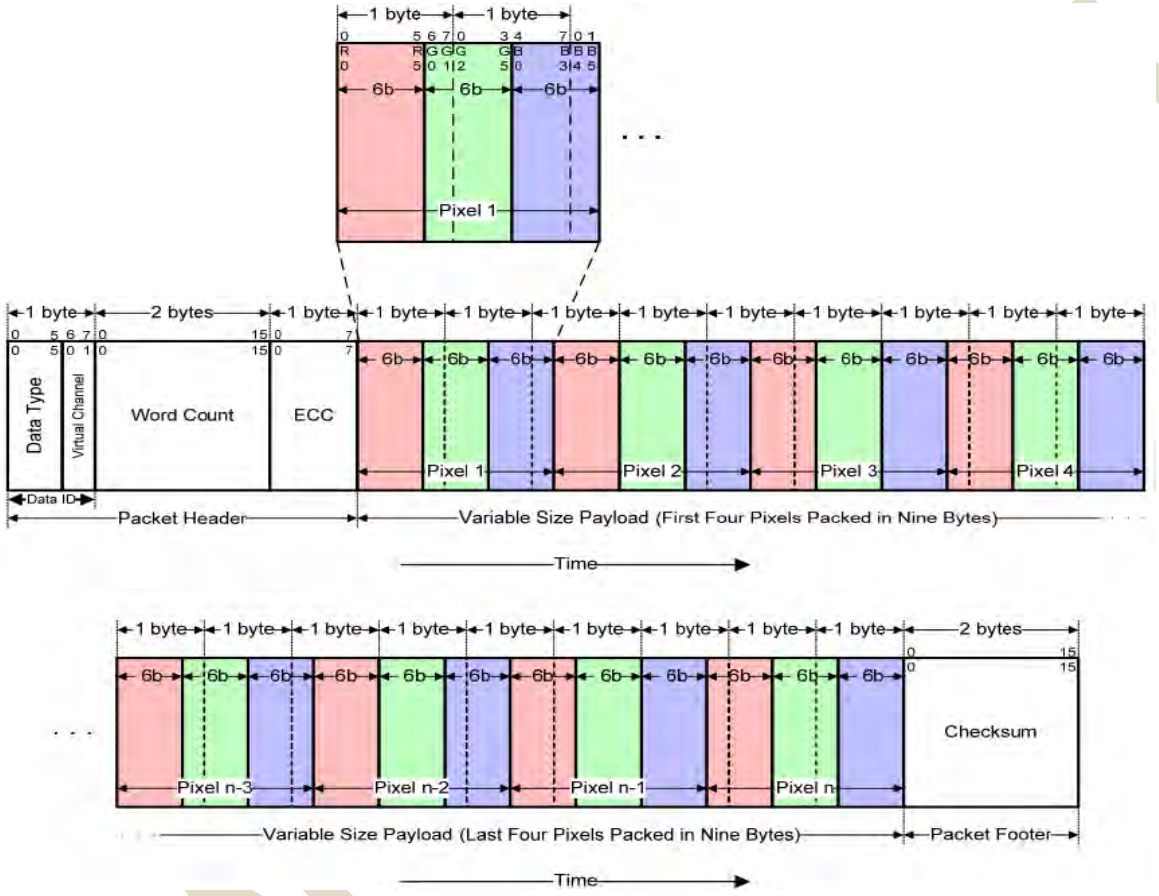
Data stream format – 16bit Format		
Data type (Hex)	**Function description**	**Number of byte**
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "**(5-bit)** red, **(6-bit)** green and **(5-bit)** blue".	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA+ PF)**



Note: (1) Within a color component, the "LSB is sent first, the MSB last ".

8.11.3 Packed Pixel Stream, 18-bit Format, Long Packet

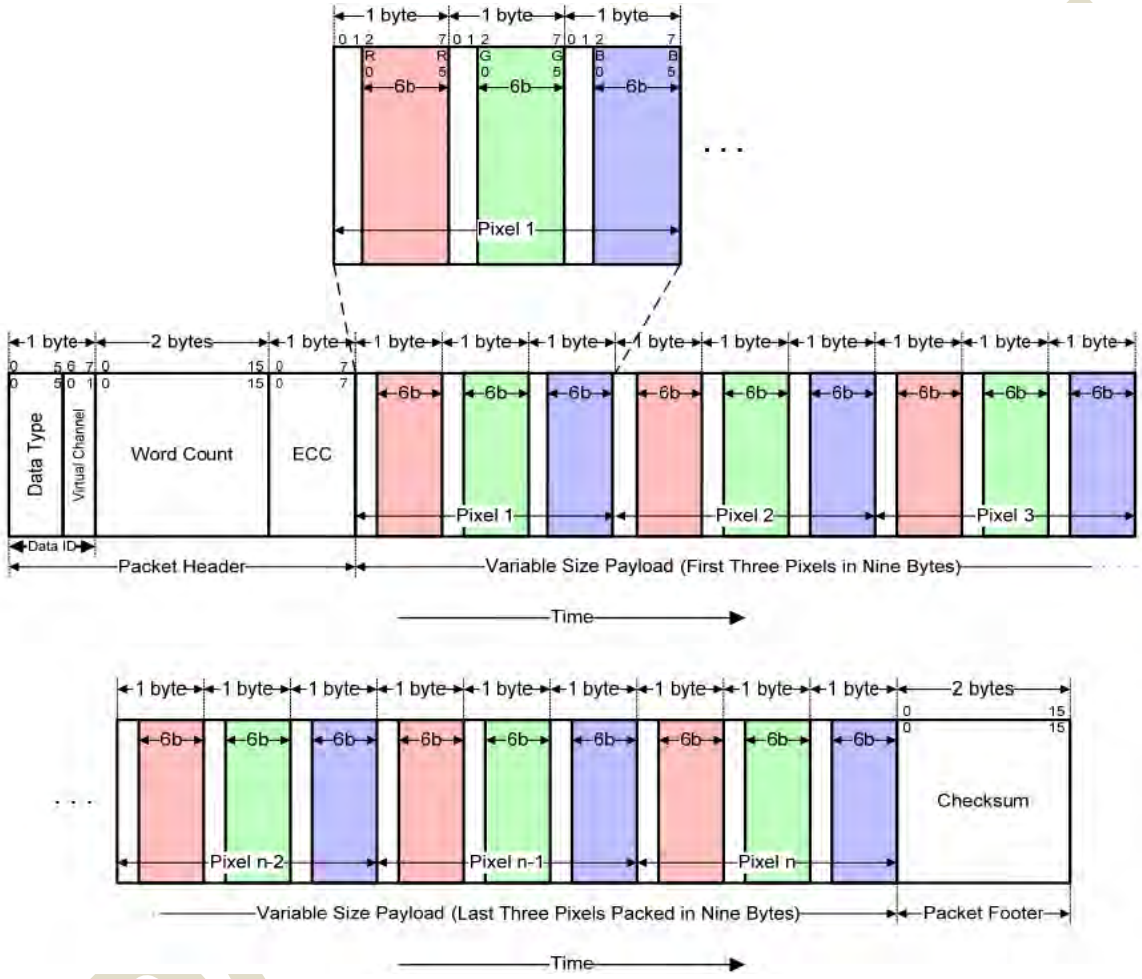
Data stream format – 18bit Format		
Data type (Hex)	**Function description**	**Number of byte**
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is "**(6-bit)** red, **(6-bit)** green and **(6-bit)** blue".	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA+PF)**



Note: (1) Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels **(nine bytes)**. Preferably, display modules employing this format have a horizontal extent **(width in pixels)** evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.

8.11.4 Packed Pixel Stream, 18-bit Loosely Format, Long Packet

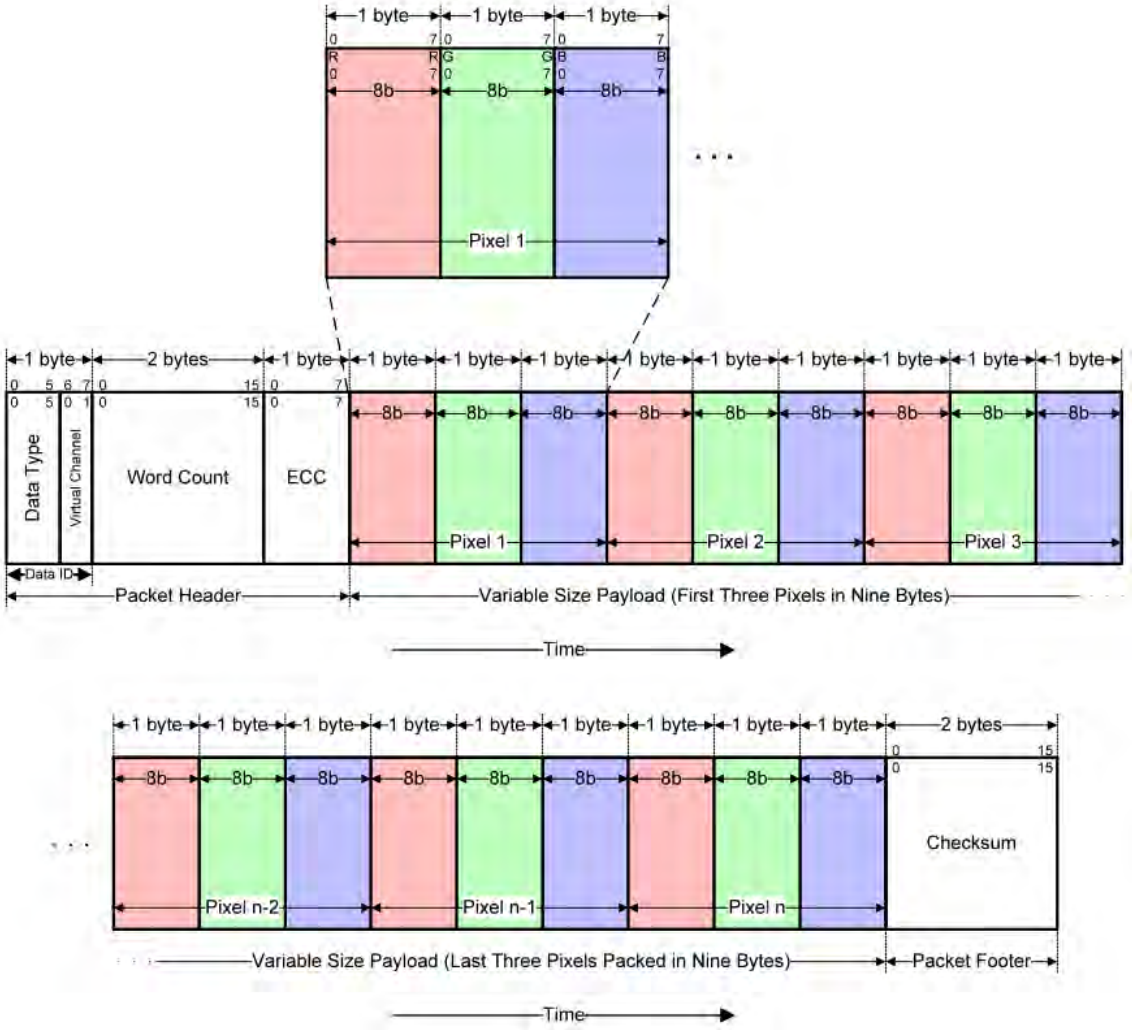
Data stream format – 18bit Format		
Data type (Hex)	**Function description**	**Number of byte**
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is "**(6-bit)** red, **(6-bit)** green and **(6-bit)** blue".	Up to 65541 bytes **(DI+WC+ECC+DCS CMD+Payload DATA+PF)**



Note: (1) Within a color component, the LSB is sent first, the MSB last and with this format, pixel boundaries line up with byte boundaries every three bytes.

8.11.5 Packed Pixel Stream, 24-bit Format, Long Packet

Data stream forma – 24bit Format		
Data type (Hex)	**Function description**	**Number of byte**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is **(8-bit)** red, **(8-bit)** green and **(8-bit)** blue.	Up to 65541 bytes **(DI+WC+ECC+DCS CMD +Payload DATA+PF)**



Note: (1) Within a color component, the LSB is sent first, the MSB last and with this format, pixel boundaries line up with byte boundaries every three bytes.

8.12 Peripheral to Processor Transmission

JD9165A-A3 has bidirectional capability for returning READ data, acknowledge, or error information to the host processor. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.
Peripheral-to-processor transactions are of four basic types:

- **Acknowledge** is a Trigger message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication, i.e. either trigger or packets, is received by the peripheral with no errors.

- **Acknowledge and Error Report** is a Short packet sent if any errors were detected in preceding transmissions from the host processor. Once reported, accumulated errors in the error register are cleared.

- **Response to Read Request** may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

8.12.1 Appropriate Responses to Commands and ACK Requests

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected response, are as follows:

- Following a non-Read command, the peripheral shall respond with Acknowledge if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

- Following a Read request, the peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

- Following a Read request if only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte Acknowledge and Error Report packet in the same LP transmission. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

- Following a non-Read command if only a single-bit ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

- Following a non-Read request, if multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

- Following a non-Read command, if multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

• Following any command, if SoT Error, SoT Sync Error or DSI VC ID Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response, with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication, in the two-byte error field. Only the Acknowledge and Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

• Following any command, if EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet with the appropriate error flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication. For a read command, only the Acknowledge and Error Report packet shall be transmitted; no read data shall be sent by the peripheral in response.

Once reported to the host processor, all errors documented in this section are cleared form the Error Register.

8.12.2 Peripheral-to-Processor Packet Description

Table 8.2 presents the complete set of peripheral-to-processor Data Types.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x02	00 0010	Acknowledge and Error Report	Short
0x11	01 0001	Generic Short READ Response, 1 byte returned	Short
0x12	01 0010	Generic Short READ Response, 2 byte returned	Short
0x1A	01 1010	Generic Long READ Response	Long
0x1C	01 1100	DCS Long READ Response	Long
0x21	10 0001	DCS Short READ Response, 1 byte returned	Short
0x22	10 0010	DCS Short READ Response, 2 byte returned	Short

Table 8.2: Data Types for Peripheral-sourced Packets

8.13 Video Mode Interface Timing

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

8.13.1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- **Non-Burst Mode with Sync Pulse –** enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

- **Non-Burst Mode with Sync Events –** similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

- **Burst Mode –** RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral.

To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. The host processor should return to LP state once per scanline during the horizontal blanking time.

During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX

- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode

- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode

- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode

- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with VSE or HSS. Note that the position of synchronization packets, such as VSS and HSS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. Transmission packet components used in the figures in this section are defined in Figure 8.12 unless otherwise specified.

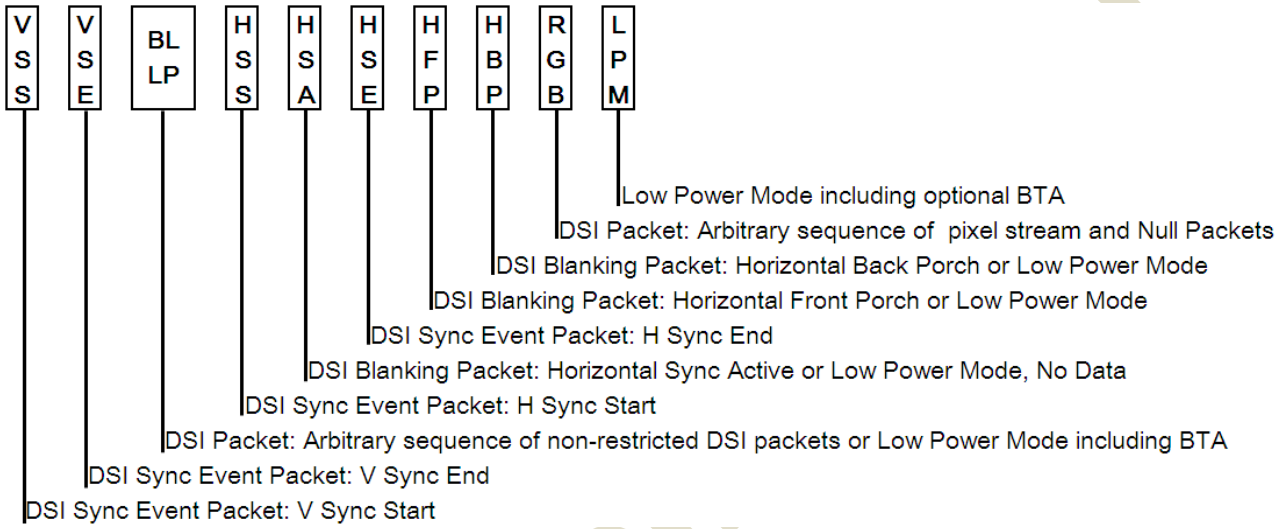


Figure 8.12: Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

8.13.2 Non-Burst sync pulse mode

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and width of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure 8.13

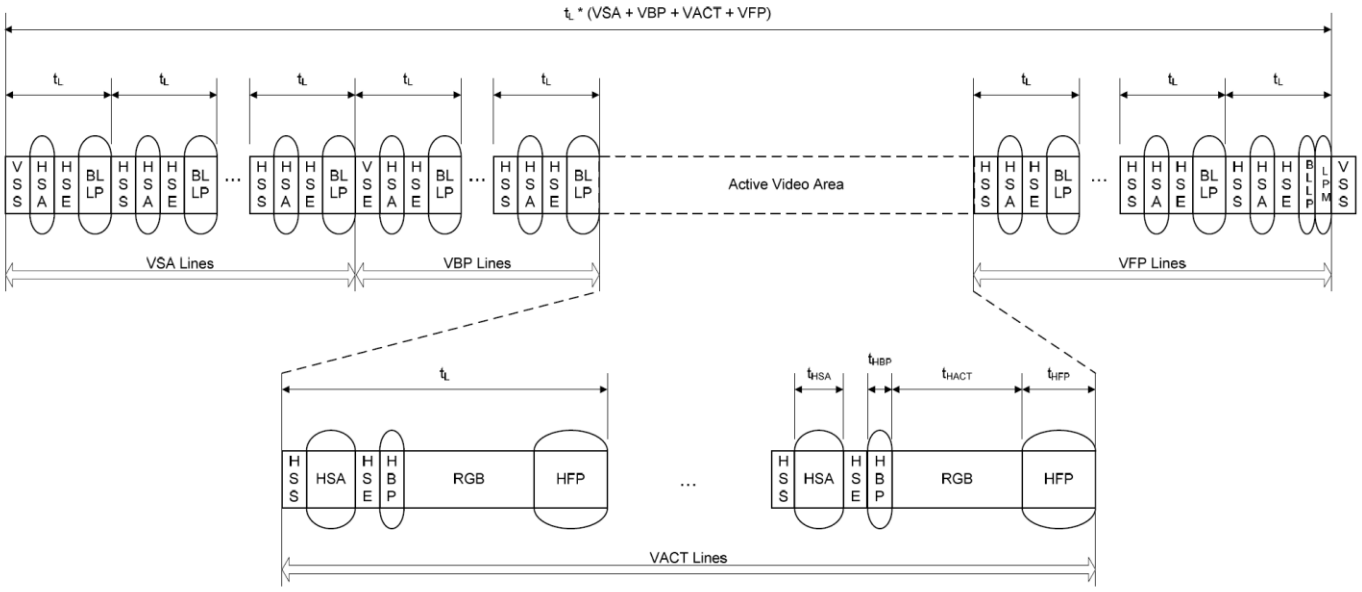


Figure 8.13: Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HAS (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power. During HAS, HBP and HFP periods, the bus should stay in the LP-11 state.

8.13.3 Non-Burst sync event mode

This mode is a simplification of the “Non-Burst Mode with Sync Pulses” format. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. An example of this mode is shown in Figure 8.14.

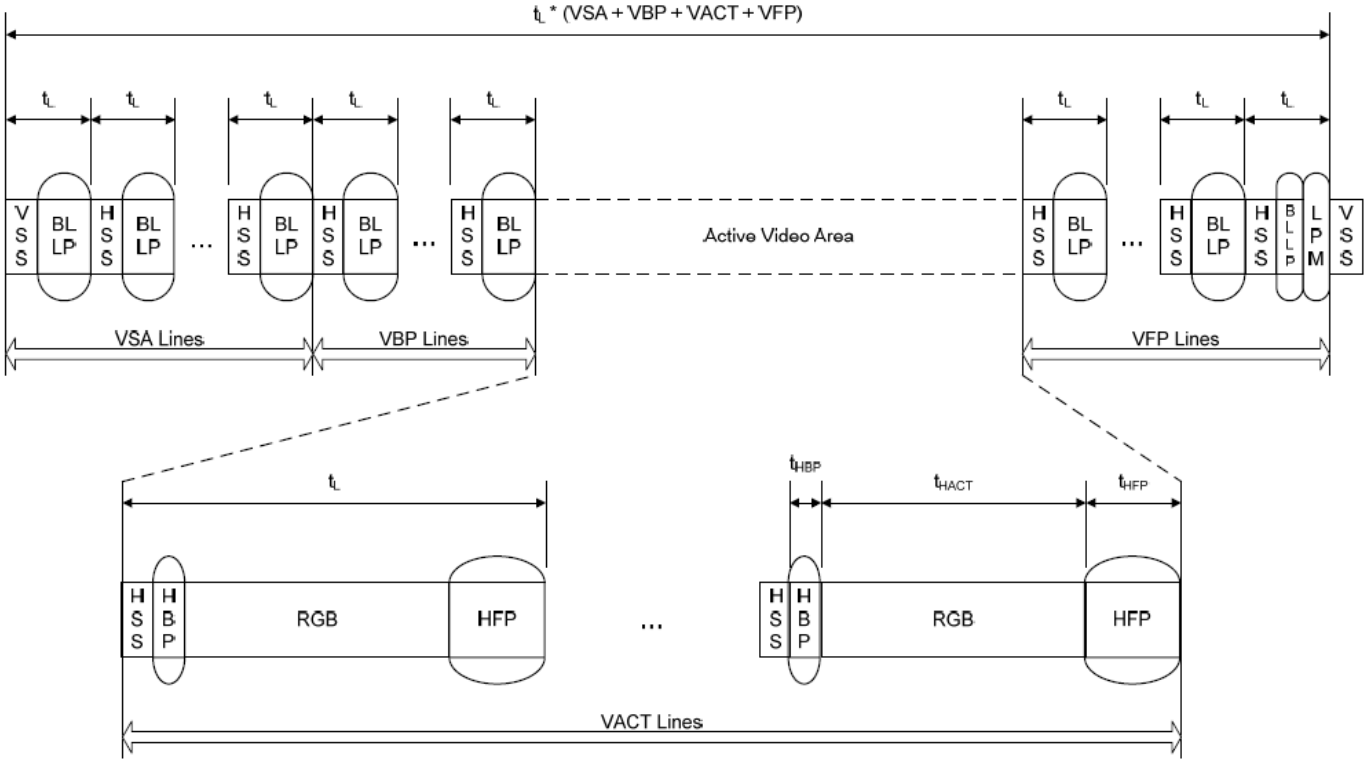


Figure 8.14: Video Mode Interface Timing: Non-Burst Transmission with Sync Events

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.13.4 Burst mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction.

Following HS pixel data transmission, the bus may stay in HS Mode for sending blanking packets or go to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its interval buffer memory to the display device. An example of this mode is shown in Figure 8.15

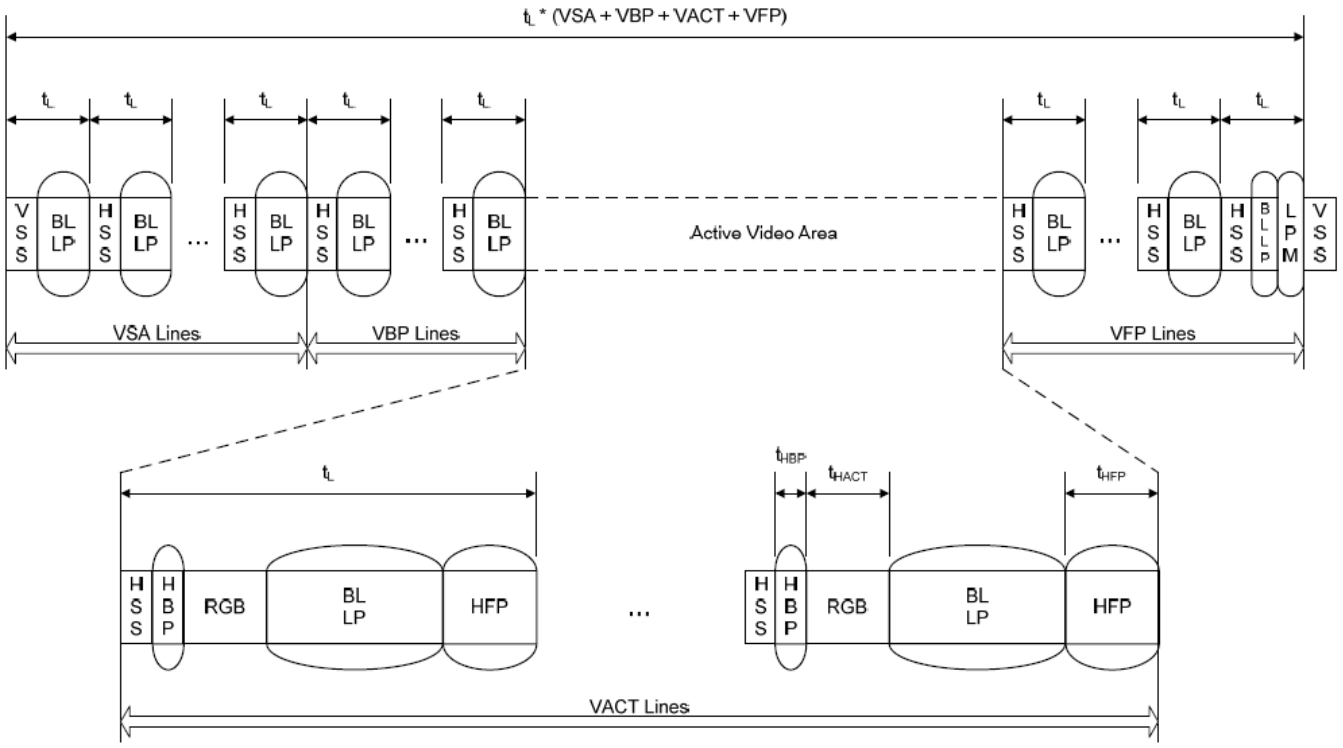


Figure 8.15: Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.14 Error-Correcting Code and Checksum

8.14.1 Error-Correcting Code(ECC)

MIPI DSI uses Hamming Code Theory as ECC generate rule. The parity of each bits in ECC are showed as below.

P7=0

P6=0

P5=D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D20^D21^D22^D23

P4=D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D21^D22^D23

P3=D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2=D0^D2^D3^D5^D6^D9^D11^12^D15^D18^D20^D21^D22

P1=D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0=D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

ECC is generated from the twenty-four bits with in the Packet Header as illustrated in Figure 8.16 which also serves as an ECC calculation example.

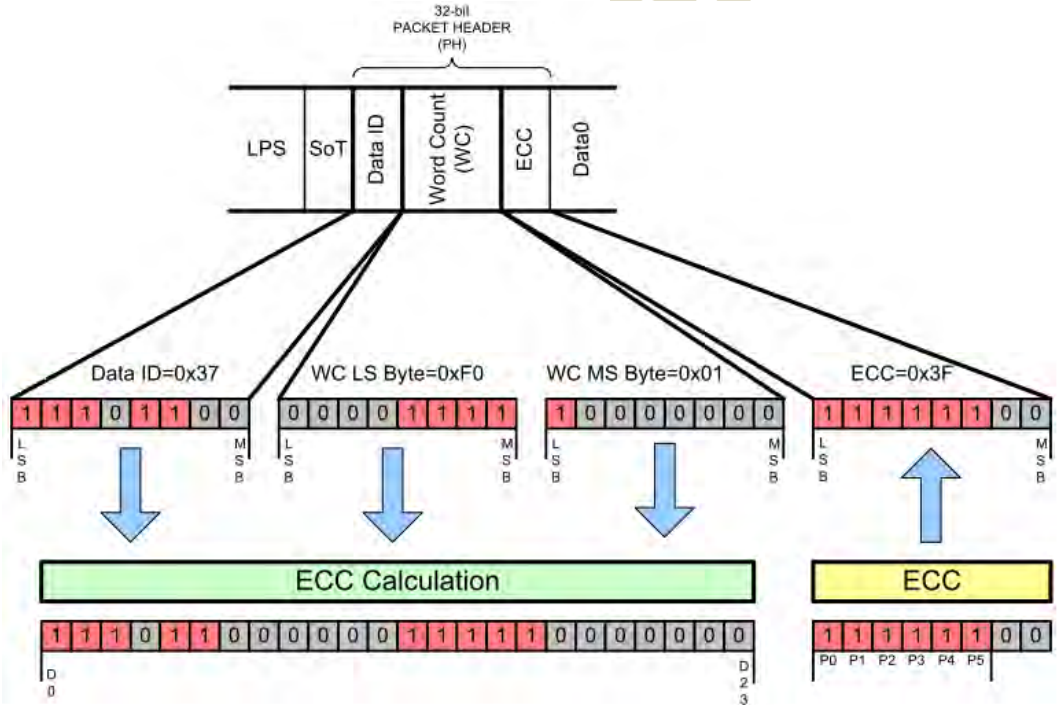


Figure 8.16: 24-bit ECC generation Example

8.14.2 Checksum Generation for Long Packet Payloads

To detect errors in transmission of Long packets, a checksum is calculated over the payload portion of the data packet. Note that, for the special case of a zero-length payload, the2-byte checksum is set to 0Xffff. The checksum shall be realized as a 16-bit CRC with a generator polynomial of x^16+x^12+x^5+x^0.

The transmission of the checksum is illustrated in Figure 8.17. The LS byte is sent first, followed by the MS byte. Note that within the byte, the LS bit is sent first.

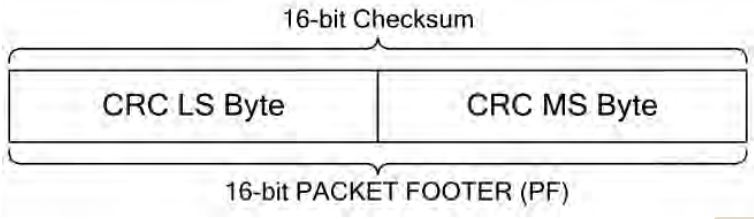


Figure 8.17: Checksum Transmission

The CRC implementation is presented in Figure 8.18. The CRC shift register shall be initialized to 0Xffff before packet data enters. Packet data not including the Packet Header then enters as a bitwise data stream from the left, LS bit first. Each bit is fed through the CRC shift register before it is passed to the output for transmission to the peripheral. After all bytes in the packet payload have passed through the CRC shift register, the shift register contains the checksum. C15 contains the checksum's MSB and C0 the LSB of the 16-bit checksum. The checksum is then appended to the data stream and sent to the register. The receiver uses its own generated CRC to verify that no errors have occurred in transmission.

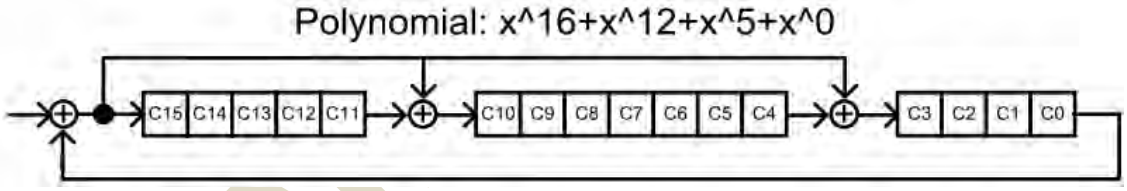


Figure 8.18: 16-bit CRC Generation Using a Shift Register

8.15 DPHY

8.15.1 Lane Module

A PHY configuration contains a Check Lane Module and one or more Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Each Lane Module consists of one or more differential High-Speed functions utilizing both interconnect wires simultaneously, one or more single-ended Low-Power functions operating on each of the interconnect wires individually, and control & interface logic. For proper operation, the set of functions in the Lane Modules on both sides of the Lane Interconnect has to be matched.

8.15.2 Lane Module Type of Clock Lane, Data0, Data1 and Data2

The required functions in a Lane Module depend on the Lane type and which side (master or slave) of the Lane Interconnect the Lane Module is located. There are three main Lane types: Clock Lane, Unidirectional Data Lane and Bi-directional Data Lane. Several PHY configurations can be constructed with these Lane types. Below show the lane module architecture of each lane.

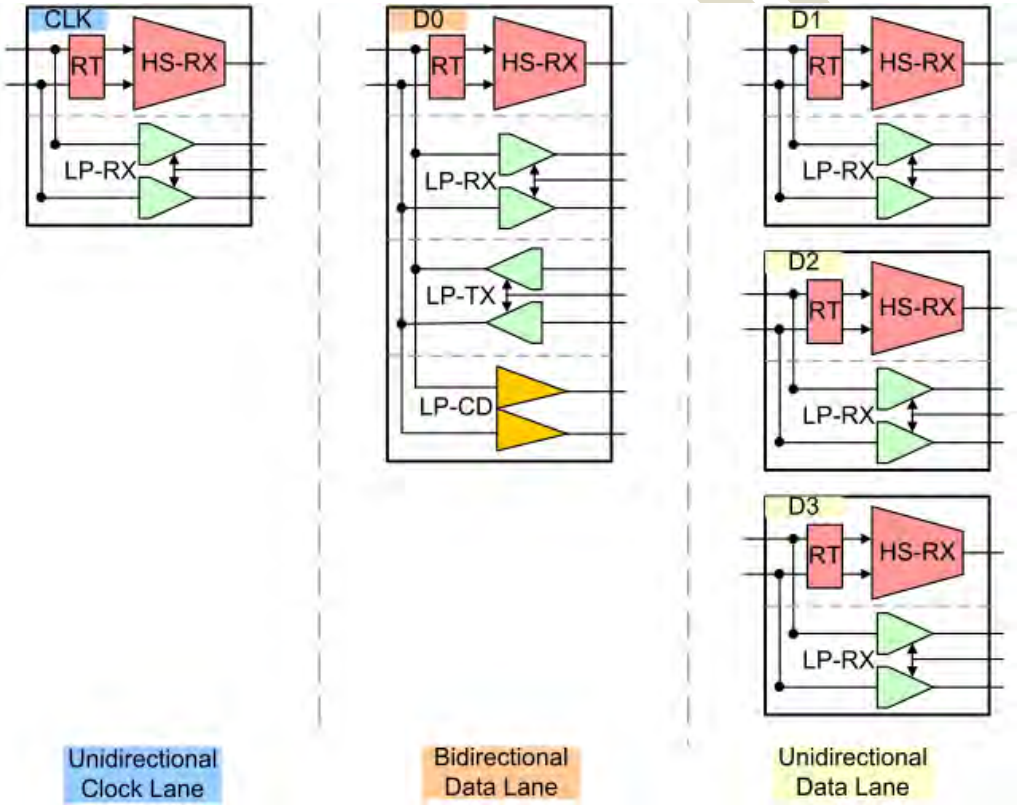


Figure 8.19: Lane Module Type

8.15.3 Master and Slave

Each Link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to the Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and the main data sink. The main direction of data communication, from source to sink, is denoted as the Forward direction. Data communication in the opposite direction is called Reverse transmission. Only bi-directional Data Lanes can transmit in the Reverse direction. In all cases, the Clock Lane remains in the Forward direction, but bi-directional Data Lane(s) can be turned around, sourcing data from the Slave side.

JD9165A-A3 serves as Slave side.

8.15.4 Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line levels. During normal operation either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High-Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential- 0 and Differential-1. The interpretation of Low-Power Lane states depends on the mode of operation. The LP-Receivers shall always interpret both High-Speed differential states as LP-00.

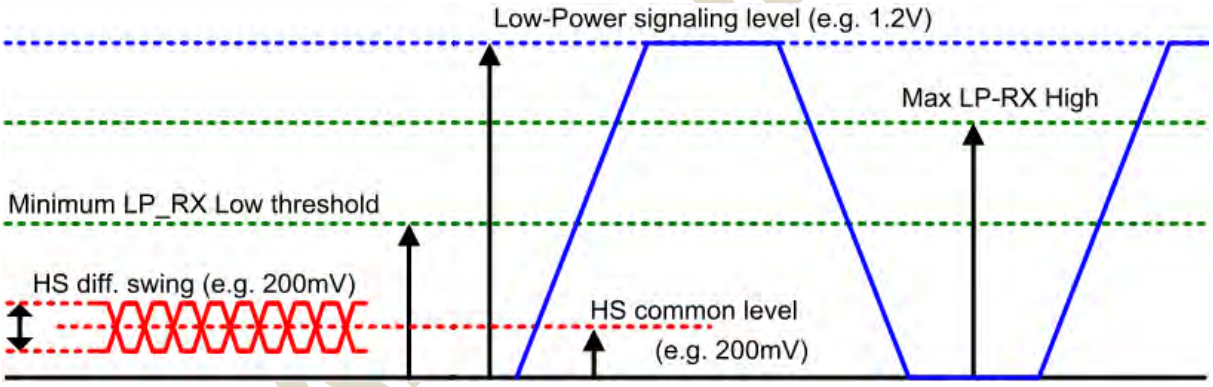


Figure 8.20: Line Levels

The Stop state has a very exclusive and central function. If the Line levels show a Stop state for the minimum required time, the PHY state machine shall return to the Stop state regardless of the previous state. This can be in RX or TX mode depending on the most recent operating direction. Table 8.3 lists all the states that can appear on a Lane during normal operation. All LP state periods shall be at least TLPX in duration. State transitions shall be smooth and exclude glitch effects. A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines. Ideally, the reconstructed clock has a duration of at least 2*TLPX, but may have a duty cycle other than 50% due to signal slope and trip levels effects.

Start Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

Table 8.3: Lane State Description

8.15.5 Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Notice that Master and Slave side shall not be changed by Turnaround.

Figure 8.21 shows the Turnaround procedure graphically.

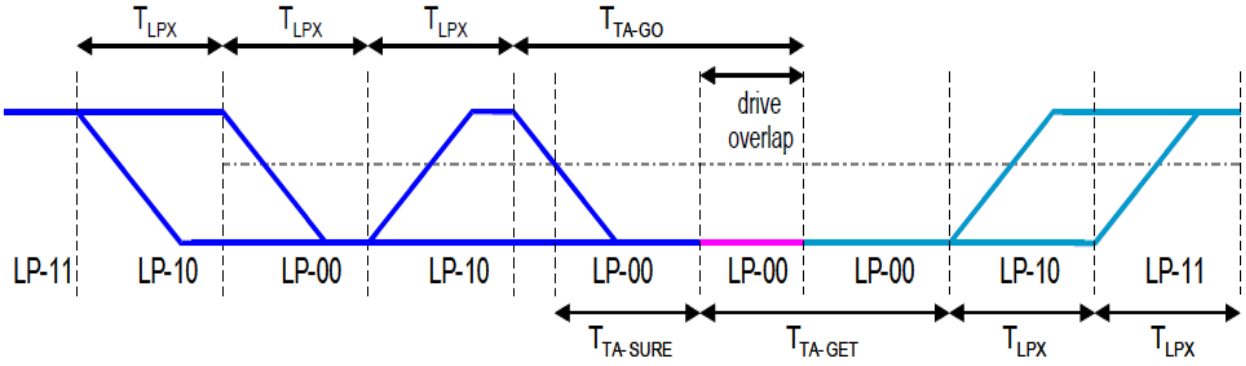


Figure 8.21: Turnaround Procedure

8.15.6 Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command, bye Spaced-One-Hot coding, to indicate the requested action. Table 8.4 lists all supported Escape mode commands and actions.

Spaced-One-Hot coding means that each Mark state is interleaved with a Space state. Each symbol consists therefore of two parts: a One-Hot phase (Mark-0 or Mark-1) and a Space phase. The TX shall send Mark-0 followed by a Space to transmit a ‘zero-bit’ and it shall send a Mark-1 followed by a Space to transmit a ‘one-bit’. A Mark that is not followed by a Space does not represent a bit. The last phase before exiting Escape mode with a Stop state shall be a Mark-1 state that is not part of the communicated bits, as it is not followed by a Space state.

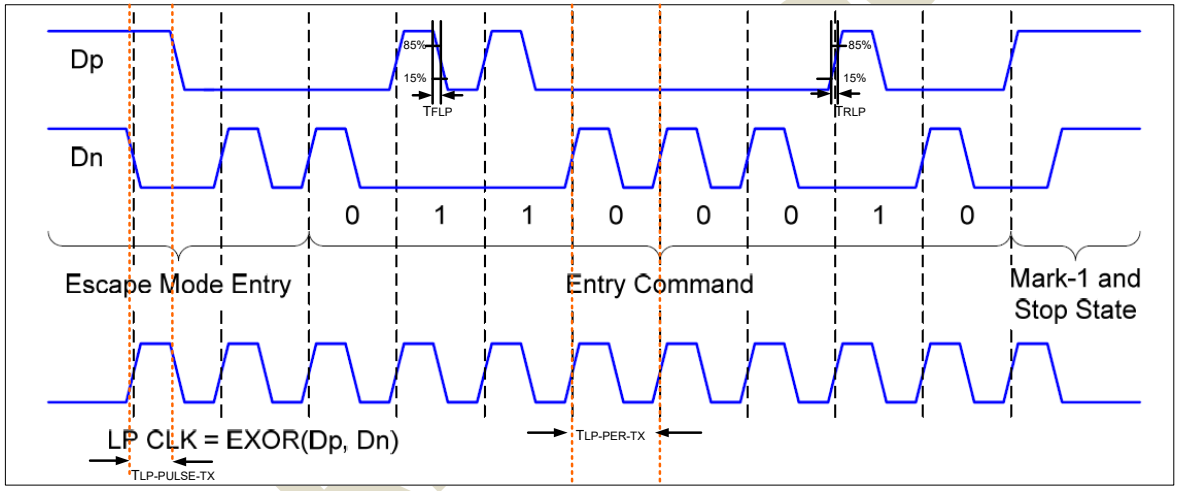


Figure 8.22: Trigger-Reset Command in Escape Mode

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Reset-Trigger	Trigger	01100010
Acknowledge	Trigger	00100001

Table 8.4: Escape Entry Codes

8.15.7 Low-Power Data Transmission(LPDT)

If the Escape mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in Low-Power mode. Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands. The data is self-clocked by the applied bit encoding and does not rely on the Clock Lane. The Lane can pause while using LPDT by maintaining a Space state on the Lines. A Stop state on the Lines stops LPDT, exits Escape mode, and switches the Lane to Control mode. The last phase before Stop state shall be a Mark-1 state, which does not represent a data-bit. At the end of LPDT the Lane shall return to the Stop state.

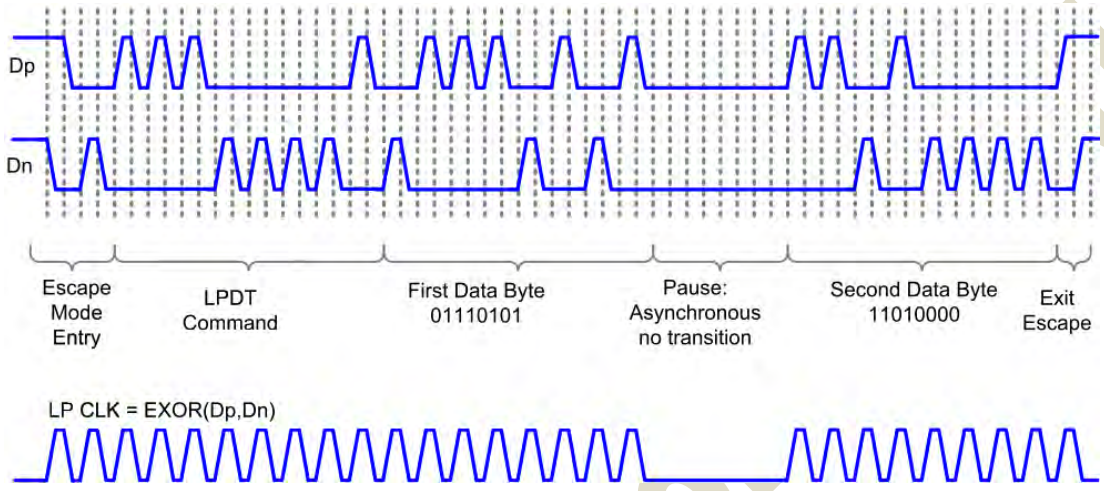


Figure 8.23: Two Data Byte Low-Power Data Transmission Example

8.16 High Speed Transmission

8.16.1 Burst Payload Data

The payload data of a burst shall always represent an integer number of payload data bytes with a minimum length of one byte. Note that for short bursts the Start and End overhead consumes much more time than the actual transfer of the payload data. There is no maximum number of bytes implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and the practical BER will not be zero. Therefore, it is important to consider for every individual protocol what the best choice is for maximum burst length.

8.16.2 Start-of-Transmission

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure. Table 8.5 describes the sequence of events on TX and RX side.

TX side	RX side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Rqst state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Line
Drives Bridge state (LP-00) for time $T_{HS-PREPARE}$	Observes transition from LP-01 to LP-00 on the Line, enables Line Termination after time $T_{D-TERM-EN}$
Enables High-Speed driver and disables Low-Powerdrivers simultaneously	
Drives HS-0 for a time $T_{HS-ZERO}$	Enables HS-RX and waits for timer $T_{HS-SETTLE}$ to expire in order to neglect transition effects
	Starts looking for Leader-Sequence
Insert the HS Sync-Sequence ‘00011101’ beginning on a rising Clock edge	
	Synchronizes upon recognition of Leader Sequence ‘011101’
Continues to Transmit High-Speed payload data	
	Receives payload data

Table 8.5: Start-of-Transmission Sequence

8.16.3 End-of-Transmission

At the end of a Data Burst, a Data Lane Levels High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 8.6 shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY.

TX side	RX side
Completes Transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time $T_{HS-EXIT}$	Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
	Neglect bits of last period $T_{HS-SKIP}$ to hide transition effects
	Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

Table 8.6: End-of-Transmission Sequence

8.16.4 High Speed Data Transmission

Figure 8.24 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most application the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane.

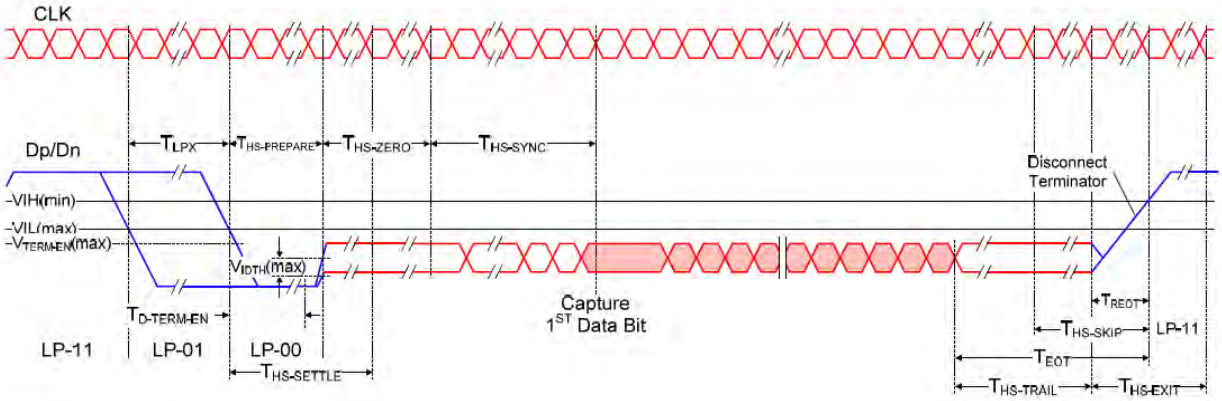


Figure 8.24: High-Speed Data Transmission in Bursts

8.16.5 High Speed Clock Transmission

In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock signal shall have quadrature-phase with respect to a toggling bit sequence on a Data Lane in the Forward direction and a rising edge in the center of the first transmitted bit of a burst. The detail Clock Start and Stop procedures are shown in Figure 8.25.

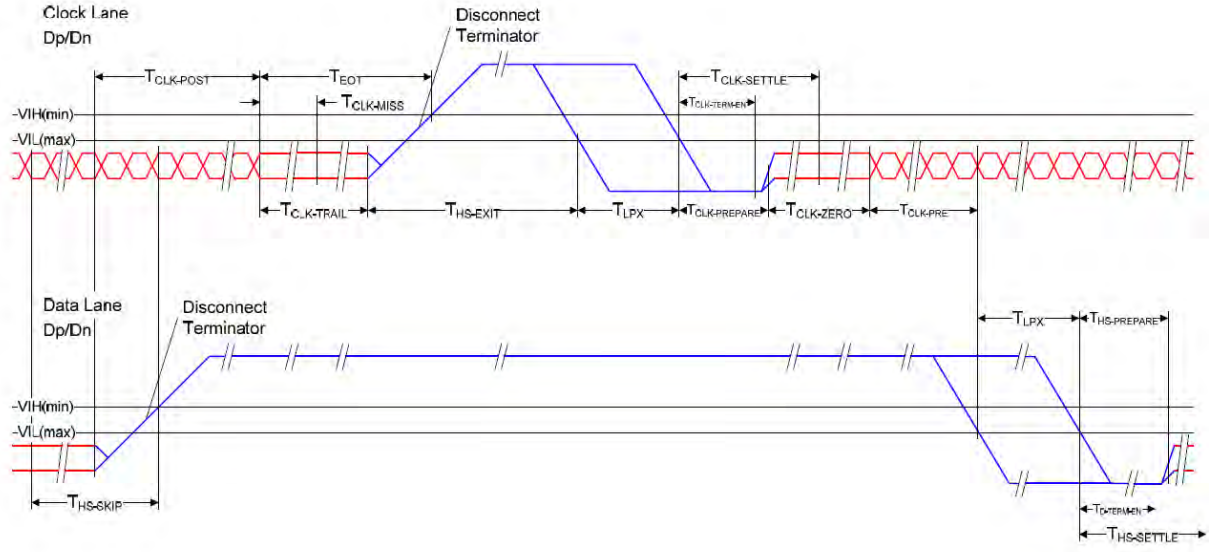


Figure 8.25: Switching the Clock Lane between Clock Transmission and Low-Power Mode

8.17 System Power state

Each Lane within a PHY configuration, that is powered and enabled, has potentially three different power consumption levels: High-Speed Transmission mode, Low-Power mode and Ultra-Low-Power State.

8.17.1 Initialization

After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11) for a period longer than TINIT. The first Stop state longer than the specified TINIT is called the Initialization period. The Master side shall ensure that a Stop State longer than TINIT does not occur on the Lines before the Master is initialized.

8.17.2 Global Operation Flow Diagram

Figure 8.26 shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround, and Initialization.

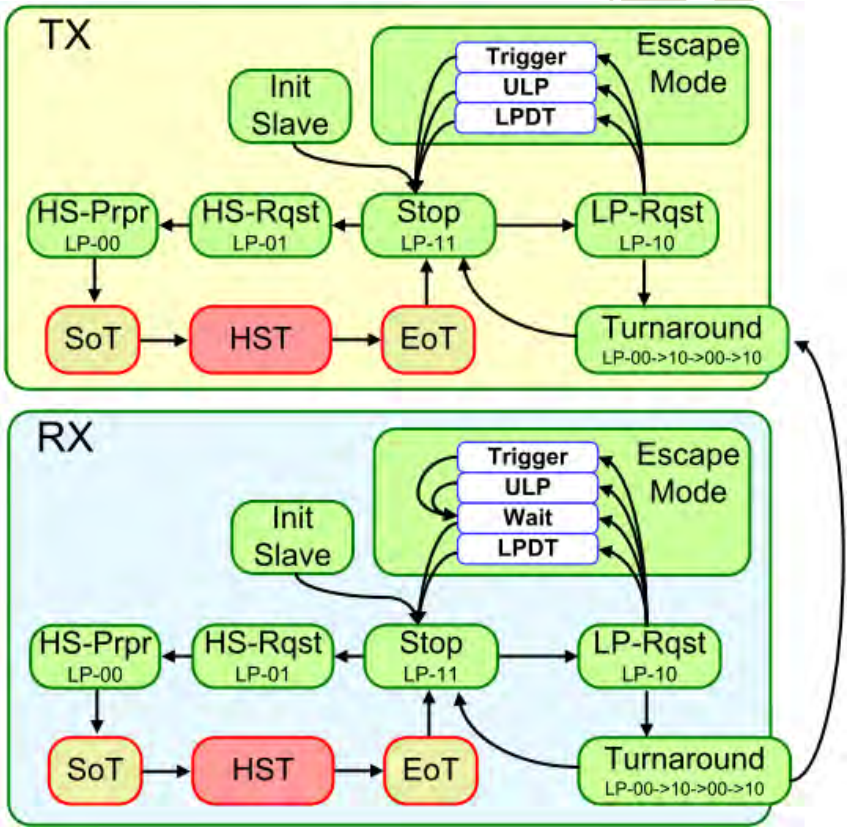


Figure 8.26: Data Lane Module State Diagram

Figure 8.27 shows the state diagram for a Clock Lane Module. The Clock Lane Module has four major operational states: Init (of unspecified duration), Low-Power Stop state, Ultra-Low Power state, and High-Speed clock transmission.

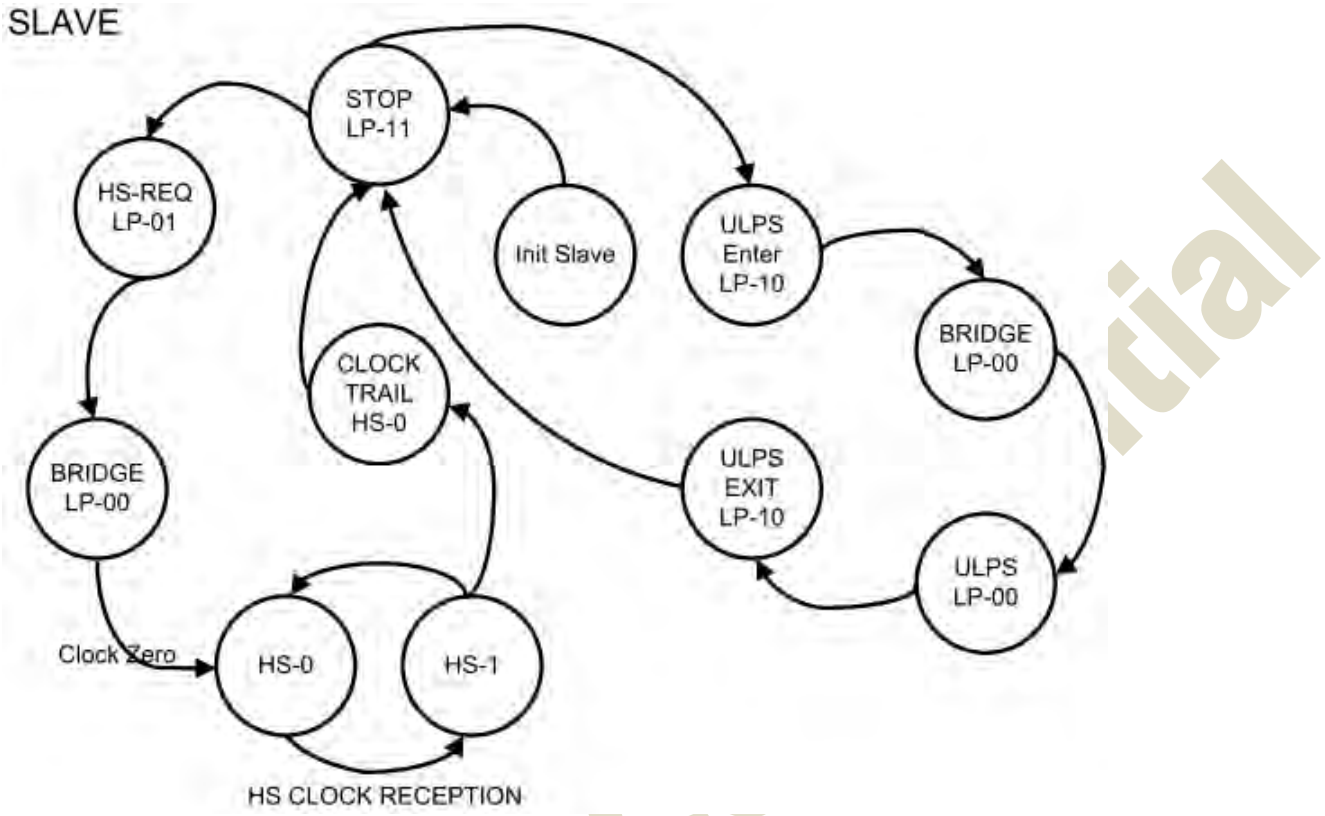


Figure 8.27: Clock Lane Module State Diagram

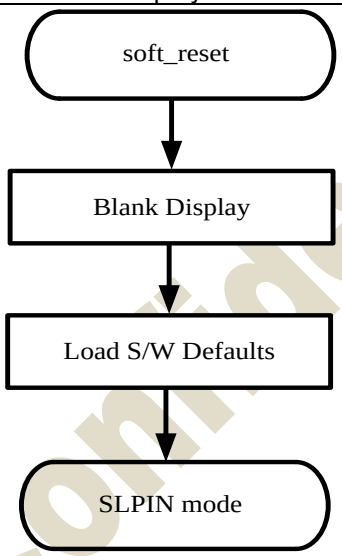
8.18 Command Description

Command	R/W	Hex	Description	Number of Parameters
NOP	W	00h	No operation.	0
SWRESET	W	01h	Software reset.	0
RDNUMPE	R	05h	Read number of the parity errors.	1
REDRD	R	06h	Read red color.	1
REDGREEN	R	07h	Read green color.	1
REDBLUE	R	08h	Read blue color.	1
RDDST	R	09h	Read display status.	1
RDDPM	R	0Ah	Read display power mode.	1
RDDMATCDL	R	0Bh	Read display MADCTL.	1
RDDIM	R	0Dh	Read display image mode.	1
SLPIN	W	10h	Sleep In.	0
SLPOUT	W	11h	Sleep out.	0
INVOFF	W	20h	Display inversion off.	0
INVON	W	21h	Display inversion on.	0
DISPOFF	W	28h	Display off.	0
DISPON	W	29h	Display on.	0
MADCTL	W	36h	Memory access control.	1
IDMOFF	W	38h	Idle mode off.	0
IDMON	W	39h	Idle mode on.	0
WRIMC	W	80h	Color selection.	1
RDRIMC	R	81h	Read color selection.	1

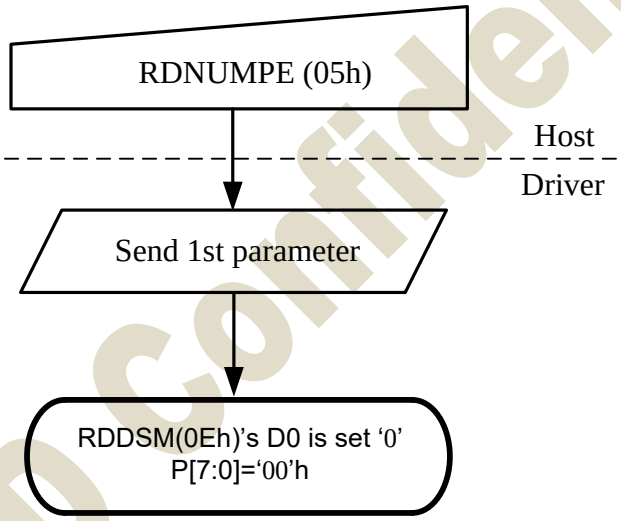
8.18.1 NOP (00h)

00H	NOP (No Operation)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	0	0	0	0	00
Parameter	No Parameter									
Description	- This command is empty command. It does have effect on the display module									
Restriction	-									
Flow Chart	-									

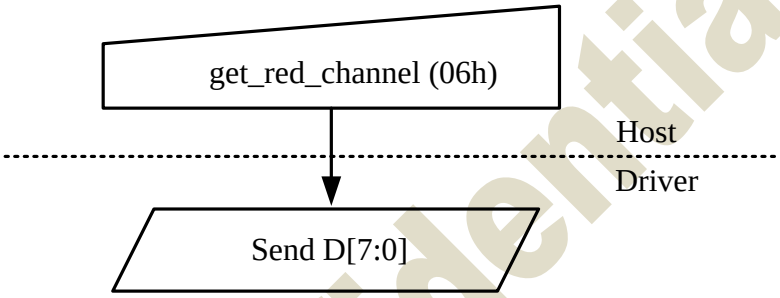
8.18.2 SWRESET (01h)

01H	SWRESET									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	0	0	0	1	01
Parameter	No Parameter									
Description	- When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values.									
Restriction	- It will be necessary to wait 5msec before sending new command following software reset. - The display module loads all display supplier's factory default values to the registers during 5msec. - If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. - Software Reset should not be sent when the display module is not in Sleep In mode.									
Flow Chart										

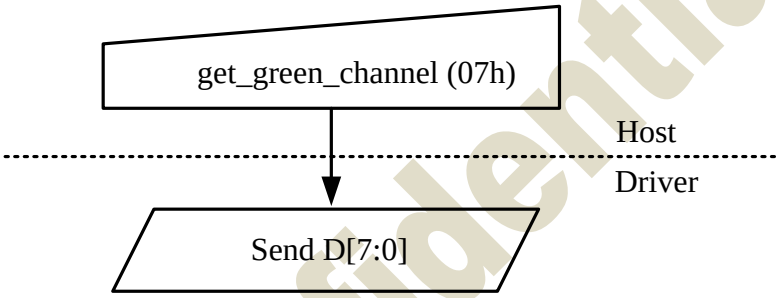
8.18.3 RDNUMPE (05h)

05H	RDNUMPE									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	0	1	0	1	05
Parameter 1	R	P7	P6	P5	P4	P3	P2	P1	P0	
Description	- The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. - P[6:0] bits are telling a number of the errors. - P[7] is set to '1' if there is overflow with P[6..0] bits. - P[7:0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (=The read function is completed).									
Restriction	-									
Flow Chart	DSI I/F Mode  									

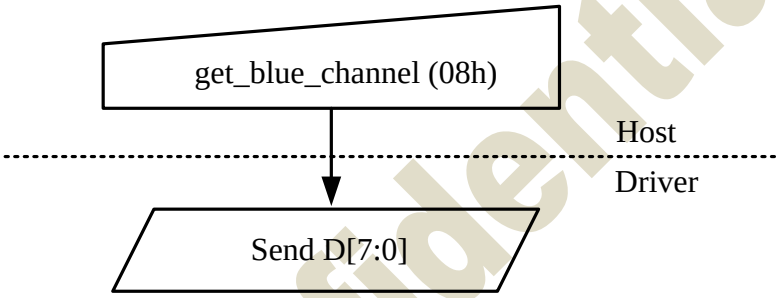
8.18.4 REDRD (06h)

06H	REDRD										
	R/W	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	-	0	0	0	0	0	1	1	0	06
Parameter 1	R	-	R7	R6	R5	R4	R3	R2	R1	R0	
Description	- The first parameter is telling red color value of the first pixel of the frame when there is used DPI I/F. - 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. - 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'. - 24 bit format: R7 is MSB and R0 is LSB. All bits are used.										
Restriction	-										
Flow Chart											

8.18.5 REDGREEN (07h)

07H	REDGREEN									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	0	1	1	1	07
Parameter 1	R	G7	G6	G5	G4	G3	G2	G1	G0	
Description	- The first parameter is telling green color value of the first pixel of the frame when there is used DPI I/F. - 16 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'. - 18 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'. - 24 bit format: G7 is MSB and G0 is LSB. All bits are used.									
Restriction	-									
Flow Chart										

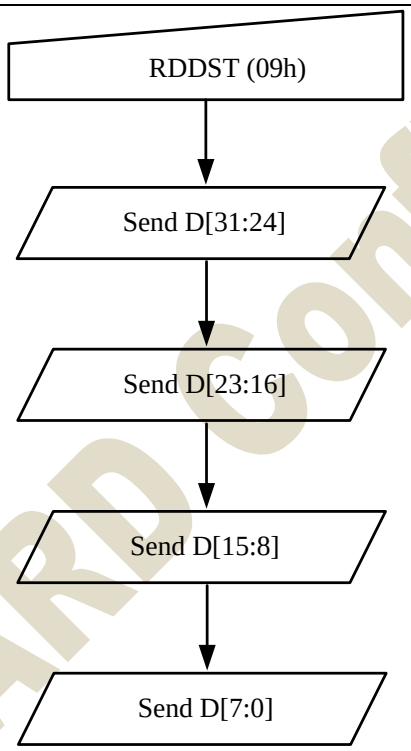
8.18.6 REDBLUE (08h)

08H	REDBLUE									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	1	0	0	0	08
Parameter 1	R	B7	B6	B5	B4	B3	B2	B1	B0	
Description	- The first parameter is telling blue color value of the first pixel of the frame when there is used DPI I/F. - 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and BR0 are set to '0'. - 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'. - 24 bit format: B7 is MSB and B0 is LSB. All bits are used.									
Restriction	-									
Flow Chart										

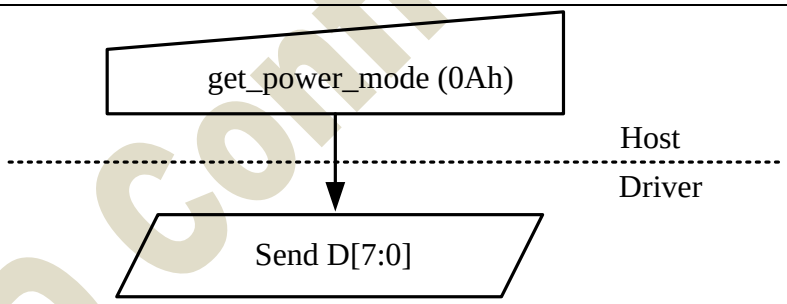
8.18.7 RDDST (09h)

<table>
<tr><th rowspan="2">09H</th><th colspan="10">RDDST</th></tr>
<tr><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>09</td></tr>
<tr><td>Parameter 1</td><td>R</td><td colspan="9">D[31:24]</td><td></td></tr>
<tr><td>Parameter 2</td><td>R</td><td colspan="9">D[23:16]</td><td></td></tr>
<tr><td>Parameter 3</td><td>R</td><td colspan="9">D[15:8]</td><td></td></tr>
<tr><td>Parameter 4</td><td>R</td><td colspan="9">D[7:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="11">-This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D31</td><td>Booster voltage status</td><td>‘0’ = booster off
‘1’ = booster on</td></tr>
<tr><td>D30</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D29</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D28</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D27</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D26</td><td>RGB/BGR order</td><td>‘0’ = RGB (MADCTL B4=‘0’)
‘1’ = BGR (MADCTL B4=‘1’)</td></tr>
<tr><td>D25</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D24</td><td>Source scan sequence</td><td>‘0’ = Source output Left to Right (MADCTL B1=‘0’)
‘1’ = Source output Right to Left (MADCTL B1=‘1’)</td></tr>
<tr><td>D23</td><td>Gate scan sequence</td><td>‘0’ = Gate output Top to Bottom (MADCTL B0=‘0’)
‘1’ = Gate output Bottom to Top (MADCTL B0=‘1’)</td></tr>
<tr><td>D22</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D21</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D20</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D19</td><td>Idle mode on/off</td><td>‘0’ = Idle mode off.
‘1’ = Idle mode on.</td></tr>
<tr><td>D18</td><td>Partial mode on/off</td><td>‘0’ = Partial mode off.
‘1’ = Partial mode on.</td></tr>
<tr><td>D17</td><td>Sleep in/out</td><td>‘0’ = Sleep in mode.
‘1’ = Sleep out mode.</td></tr>
<tr><td>D16</td><td>Not defined</td><td>Set to ‘1’</td></tr>
<tr><td>D13</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D12</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D11</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D10</td><td>Display on/off</td><td>‘0’ = Display is off.
‘1’ = Display is on.</td></tr>
<tr><td>D9</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D8</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D7</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D6</td><td>Not defined</td><td>Set to ‘0’</td></tr>
</table></td></tr>
</table>

	D5	Not defined	Set to ‘0’
	D4	Not defined	Set to ‘0’
	D3	Not defined	Set to ‘0’
	D2	Not defined	Set to ‘0’
	D1	Not defined	Set to ‘0’
	D0	Not defined	Set to ‘0’

Restriction	-
Flow Chart	

8.18.8 RDDPM (0Ah)

<table>
<tr><th rowspan="2">0AH</th><th colspan="10">RDDPM</th></tr>
<tr><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">-This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Not Defined</td><td>Set to ‘0’ or ‘1’</td></tr>
<tr><td>D6</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D5</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D4</td><td>Sleep in/out</td><td>‘0’ = sleep in mode
‘1’ = sleep out mode</td></tr>
<tr><td>D3</td><td>Not Defined</td><td>Set to ‘1’</td></tr>
<tr><td>D2</td><td>Display on/off</td><td>‘0’ = display is off
‘1’ = display is on</td></tr>
<tr><td>D1</td><td>Not defined</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>ESD detect</td><td>‘0’ = ESD detect off
‘1’ = ESD detect on</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

8.18.9 RDDMATCDL (0Bh)

0BH	RDDMATCDL									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	1	0	1	1	0B
Parameter 1	R	0	0	0	0	0	0	D1	D0	

Description

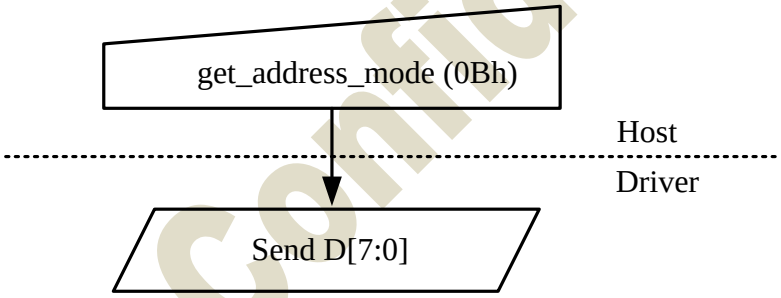
-This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D1	Source scan sequence	'0' = left to right (when MADCTL B1='0') '1' = right to left (when MADCTL B1='1')
D0	Gate scan sequence	'0' = top to bottom (when MADCTL B0='0') '1' = bottom to top (when MADCTL B0='1')

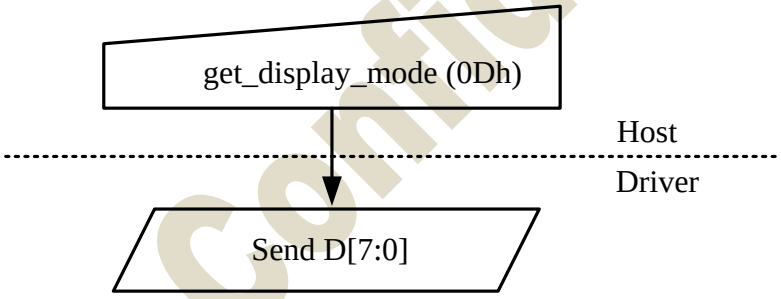
Restriction

-

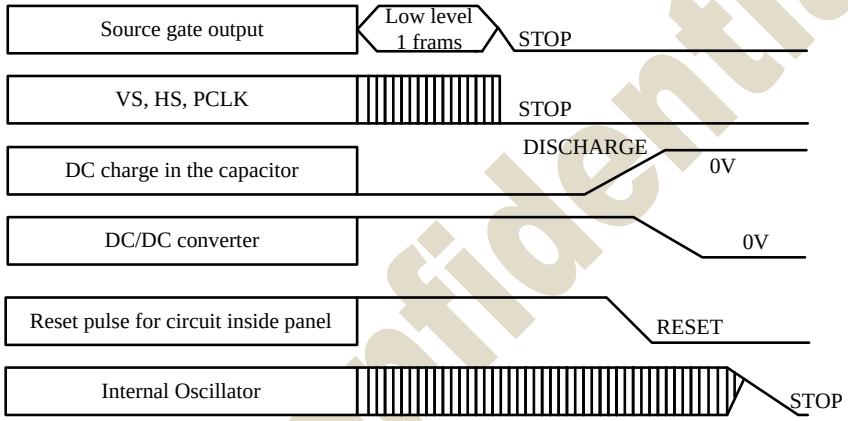
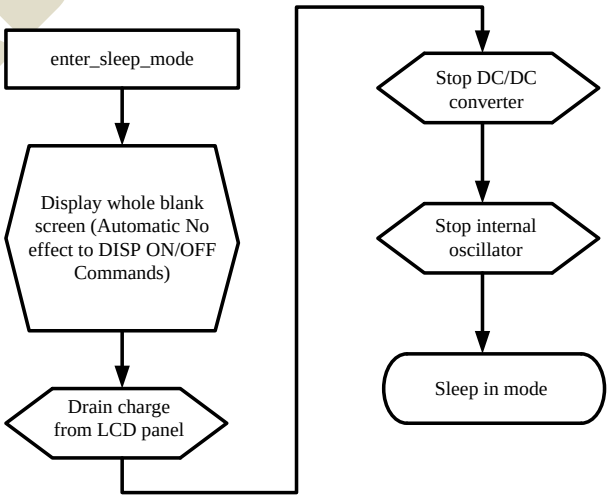
Flow Chart



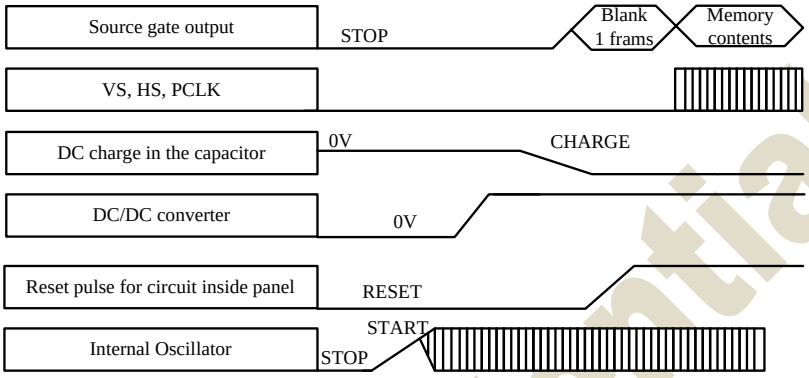
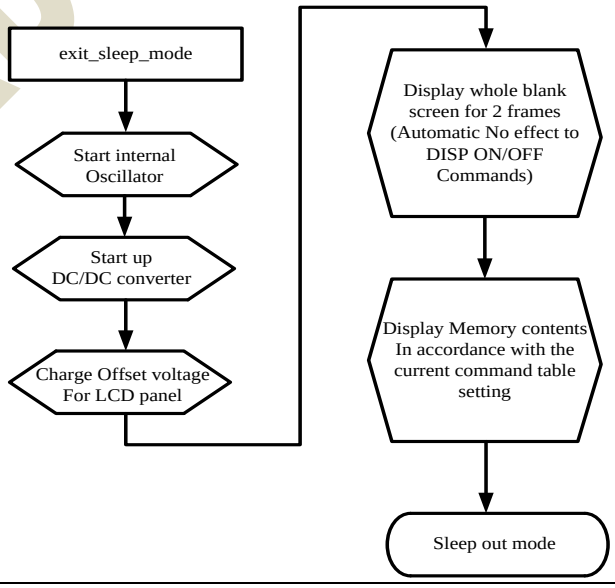
8.18.10 RDDIM (0Dh)

<table>
<tr><th rowspan="2">0DH</th><th colspan="10">RDDIM</th></tr>
<tr><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0D</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>0</td><td>D6</td><td>D5</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">-This is command indicates the current status of the display as described in the table below.
<table><tr><td>Bit</td><td>Description</td><td>Value</td></tr><tr><td>D6</td><td>Horizontal Scrolling Status</td><td>This bit is not applicable for this project, set it to ‘0’</td></tr><tr><td>D5</td><td>Inversion On/Off</td><td>‘0’ = Inversion is Off.
‘1’ = Inversion is On.</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

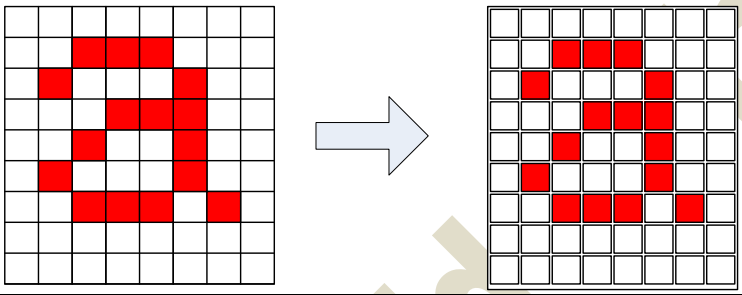
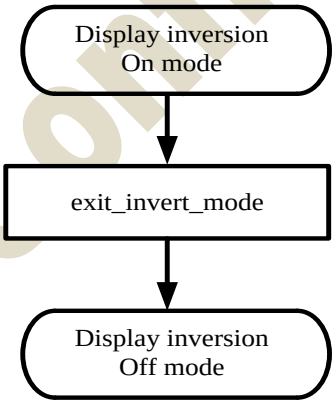
8.18.11 SLPIN (10h)

10H	SLPIN									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	1	0	0	0	0	10
Description	- This command causes the LCD module to enter the minimum power consumption mode. In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest power mode the display module supports. DBI or DSI Command Mode remains operational and the line buffer maintains its contents. The host processor continues to send PCLK, HS and VS information to DPI IF for two frames after this command is sent when the display module is in Normal mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  									
Restriction	- This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.									
Flow Chart	It takes 120msec to get into Sleep In mode after SLPIN command issued.  									

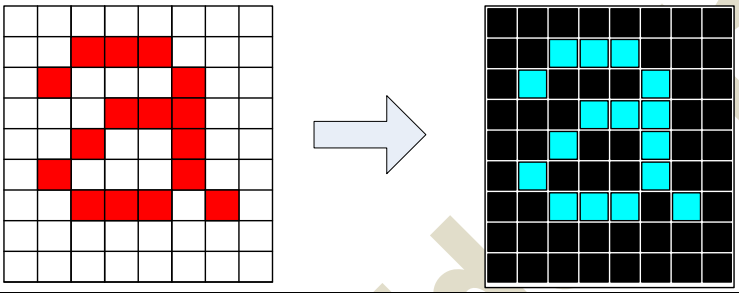
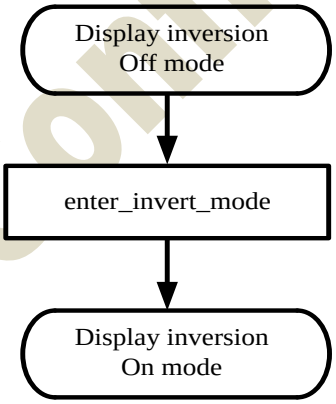
8.18.12 SLPOUT (11h)

11H	SLPOUT									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	1	0	0	0	1	11
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started  User can start to send PCLK, HS and VS information on DPI IF before Sleep Out command and this information is valid at least 1 frames before Sleep Out command, if there is left Sleep In -mode to Sleep Out-mode in Normal Mode On. There is used an internal oscillator for blank display.									
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.									
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued.  									

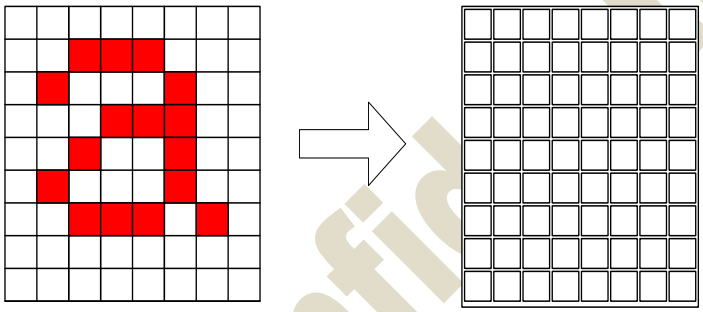
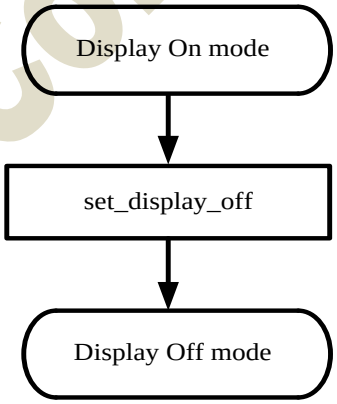
8.18.13 INVOFF (20h)

20H	INVOFF									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	0	0	20
Description	This command is used to recover from display inversion mode. This command makes no change of contents of image. This command does not change any other status. (Example) Image → Display Panel 									
Restriction	This command has no effect when module is already in inversion off mode.									
Flow Chart										

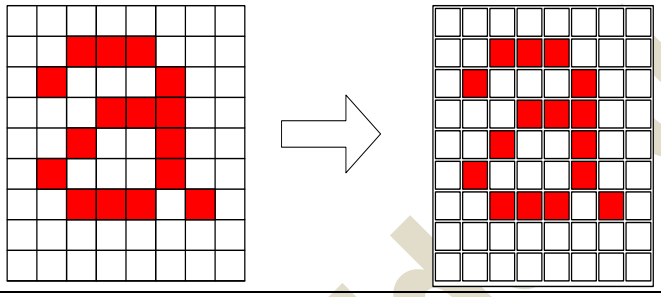
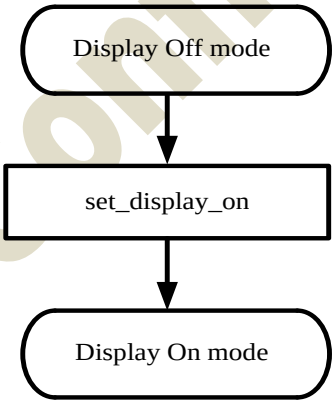
8.18.14 INVON (21h)

21H	INVON									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	0	1	21
Description	This command is used to enter into display inversion mode. This command makes change of contents of image. Every bit is inverted from the image to the display. This command does not change any other status. (Example) Image → Display Panel 									
Restriction	This command has no effect when module is already in inversion on mode.									
Flow Chart										

8.18.15 DISPOFF (28h)

28H	DISPOFF									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	1	0	0	0	28
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Line Buffer is disabled and blank page inserted. This command makes no change of contents of line buffer. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Memory Display Panel 									
Restriction	It will be necessary to wait 40msec and send Sleep In command for power off sequence.									
Flow Chart										

8.18.16 DISPON (29h)

29H	DISPON									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	1	0	0	1	29
Description	This command is used to recover from DISPLAY OFF mode. Output from the Line Buffer is enabled. This command makes no change of contents of line buffer. This command does not change any other status. (Example) Memory Display Panel 									
Restriction	This command has no effect when module is already in display on mode.									
Flow Chart										

8.18.17 MADCTL (36h)

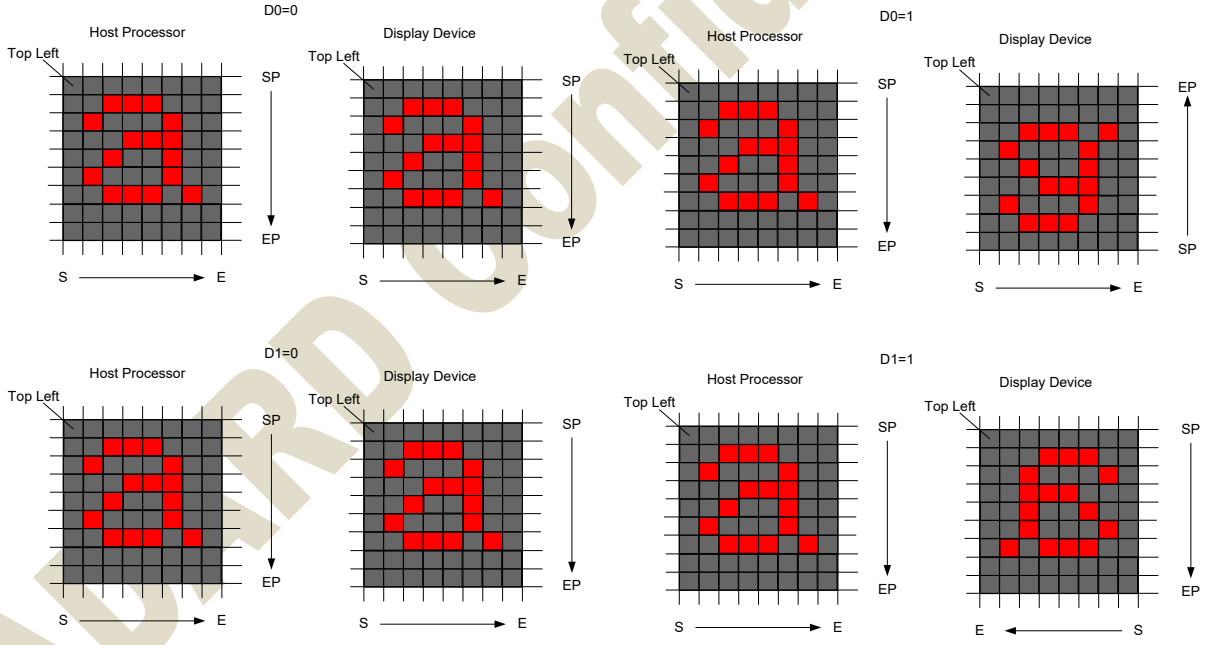
36H	MADCTL									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	0	1	1	0	36
Parameter 1	W	0	0	0	0	D3	0	D1	D0	

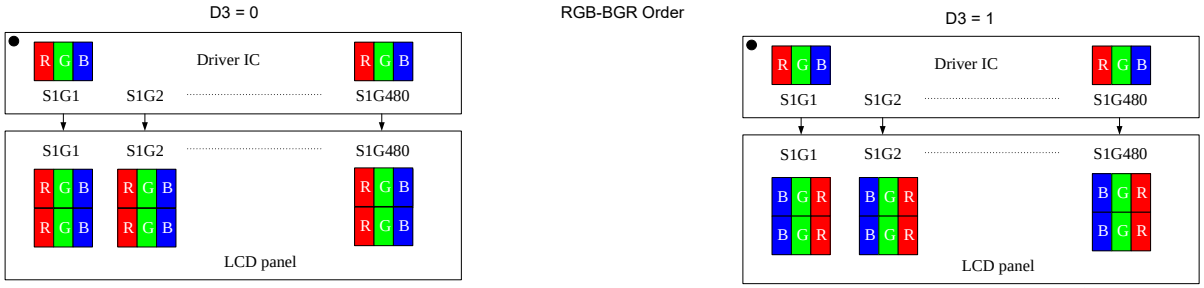
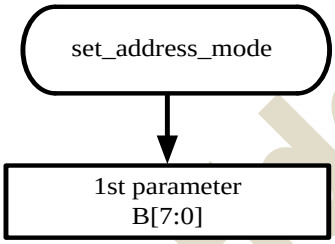
Description

This command defines read/write scanning direction of line buffer.

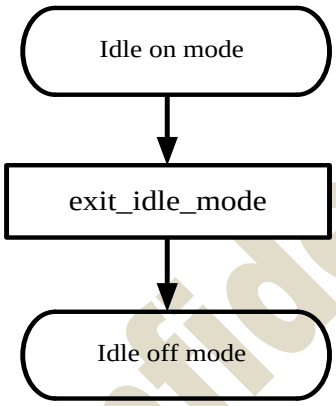
This command makes no change on the other driver status.

Bit	Description	Value
D3	RGB-BGR ORDER	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
D1	Source scan sequence	Horizontal scan 0=Left to right 1=Right to left
D0	Gate scan sequence	Vertical scan 0=Top to bottom 1=Bottom to top



	
Restriction	
Flow Chart	

8.18.18 IDMOFF (38h)

38H	IDMOFF									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	1	0	0	0	38
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colors.									
Restriction	This command has no effect when module is already in idle off mode.									
Flow Chart										

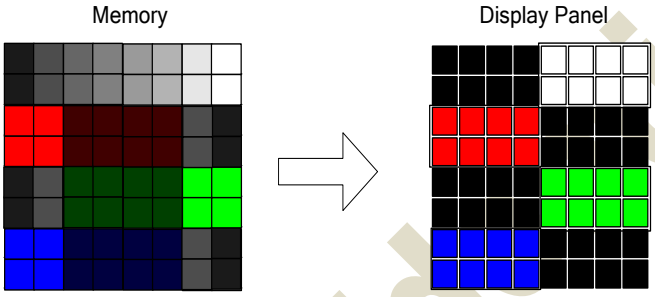
8.18.19 IDMON (39h)

39H	IDMON									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	1	0	0	1	39

Description

This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the line buffer, 8 color depth data is displayed.

(Example)



Memory contents vs. Display Color

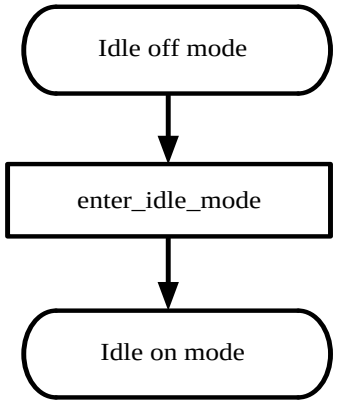
	R7 – R0	G7 – G0	B7 – B0
Black	0XXXXX	0 XXXXX	0 XXXXX
Blue	0 XXXXX	0 XXXXX	1 XXXXX
Red	1 XXXXX	0 XXXXX	0 XXXXX
Magent	1 XXXXX	0 XXXXX	1 XXXXX
Green	0 XXXXX	1 XXXXX	0 XXXXX
Cyan	0 XXXXX	1 XXXXX	1 XXXXX
Yellow	1 XXXXX	1 XXXXX	0 XXXXX
White	1 XXXXX	1 XXXXX	1 XXXXX

X=don't care

Restriction

This command has no effect when module is already in idle on mode.

Flow Chart



8.18.20 WRIMC (80h)

<table>
<tr><th rowspan="2">80H</th><th colspan="10">WRIMC</th></tr>
<tr><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>80</td></tr>
<tr><td>Parameter 1</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>R</td><td>G</td><td>B</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command is used to select color for 1bpp Idle Mode. Color selection is configured with bits [D2:D0].
D2: R Component
D1: G Component
D0: B Component
Color selection is defined in following table:
<table>
<tr><th>1bpp Idle Mode Color Selection</th><th>R</th><th>G</th><th>B</th></tr>
<tr><td>Black</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Blue</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Green</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Cyan</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Red</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Magenta</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Yellow</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>White</td><td>1</td><td>1</td><td>1</td></tr>
</table>
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-This command is only applicable to 1bpp Compression in Idle Mode.</td></tr>
<tr><td>Flow Chart</td><td colspan="10">-</td></tr>
</table>

8.18.21 RDRIMC (81h)

<table>
<tr><th rowspan="2">81H</th><th colspan="10">RDRIMC</th></tr>
<tr><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>81</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>R</td><td>G</td><td>B</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command returns the current color selection of 1bpp Idle Mode which color selection is configured with bits [D2:D0].
D2: R Component
D1: G Component
D0: B Component
Color selection is defined in following table:
<table>
<tr><th>1bpp Idle Mode Color Selection</th><th>R</th><th>G</th><th>B</th></tr>
<tr><td>Black</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Blue</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Green</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Cyan</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Red</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Magenta</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Yellow</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>White</td><td>1</td><td>1</td><td>1</td></tr>
</table>
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-This command is only applicable to 1bpp Compression in Idle Mode.</td></tr>
<tr><td>Flow Chart</td><td colspan="10">-</td></tr>
</table>

8.19 MIPI DC characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	120	ohm
HS transmit differential voltage($V_{OD}=V_{DP}-V_{DN}$)	$\|V_{OD}\|$	100	200	250	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Ground shift	V_{GNDSH}	-50	-	50	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	1000	-	1350	mV
Input hysteresis	V_{HYST}	25	-	-	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	ZOLP	110			ohm
Logic 0 contention threshold	$V_{ILCD,MAX}$	-	-	200	mV
Logic 1 contention threshold	$V_{IHCD,MIN}$	450	-	-	mV
MIPI Digital Operating Current	$I_{VDDMIPI}$	-	15	20	mA
MIPI Digital Stand-by Current	I_{STMIPI}	-	-	250	uA

Note: MIPI Digital Operating and Stand-by Current is at RT 25℃ condition.

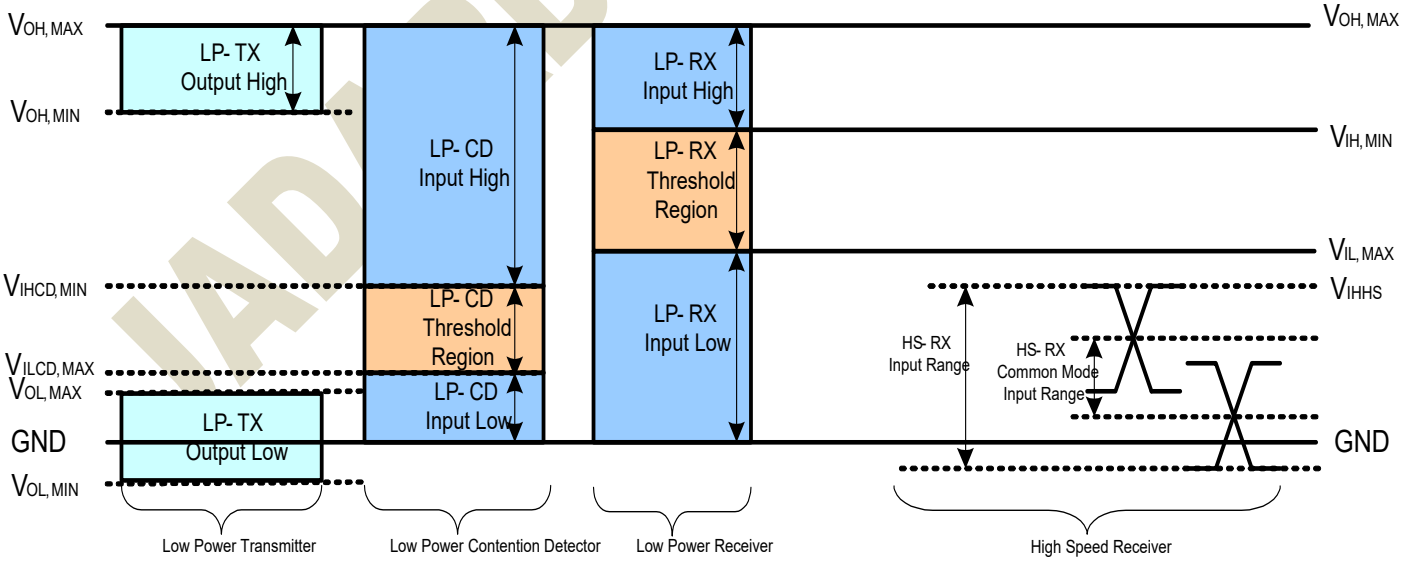


Figure 8.28: MIPI signaling and contention voltage levels

8.20 MIPI AC characteristic

8.20.1 MIPI Low Power Transmitter AC Specification

Parameter		Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time		T_{RLP} /T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time		T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$T_{LP-PULSE-TX}$	100	-	-	ns	-
	All other pulses		100	-	-	ns	-
Period of the LP EXOR clock(LP Speed)		$T_{LP-PER-TX}$	200	-	-	ns	-
Slew Rate @CLOAD =0pF		δ V/δ t_{SR}	20	-	500	mV/ns	-
Slew Rate @CLOAD =5pF			20	-	200	mV/ns	-
Slew Rate @CLOAD =20pF			20	-	150	mV/ns	-
Slew Rate @CLOAD =70pF			20	-	100	mV/ns	-
Load Capacitance		T_{RLP}	-	-	70	pF	-

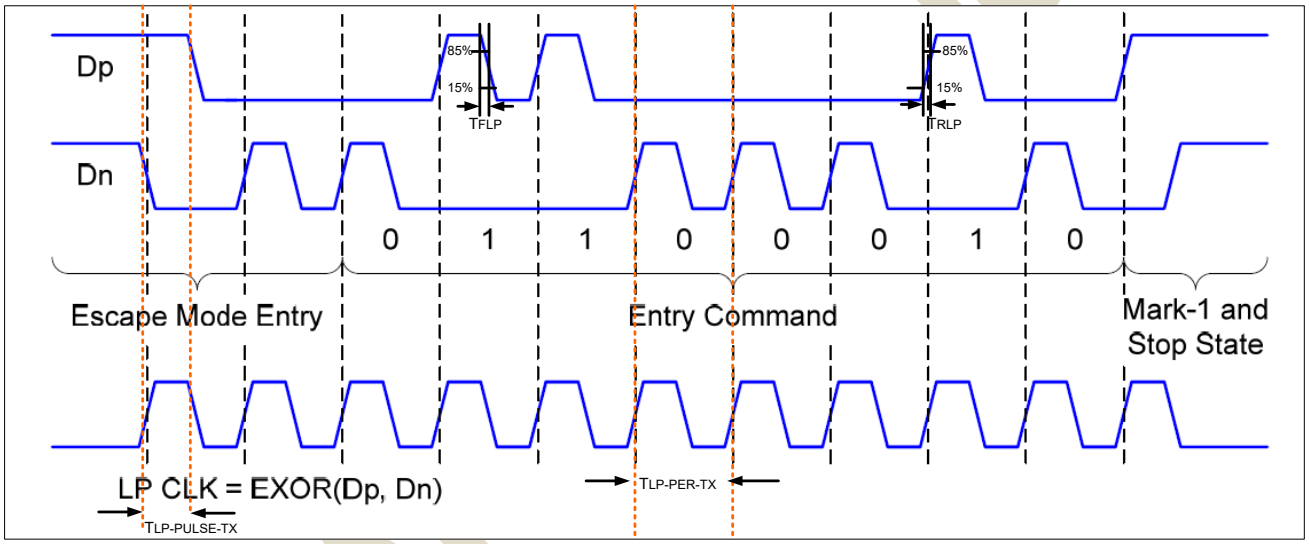


Figure 8.29: MIPI LP AC timing

8.20.2 MIPI Low Power Turnaround Procedure

Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period	T_{LPX}	100	-	-	ns
Time-out before new TX side start driving	$T_{TA\text{-}Sure}$	T_{LPX}	-	$2T_{LPX}$	ns
Time to drive LP-00 by new TX	$T_{TA\text{-}GET}$	-	$5T_{LPX}$	-	ns
Time to drive LP-00 after Turnaround Request	$T_{TA\text{-}GO}$	-	$4T_{LPX}$	-	ns

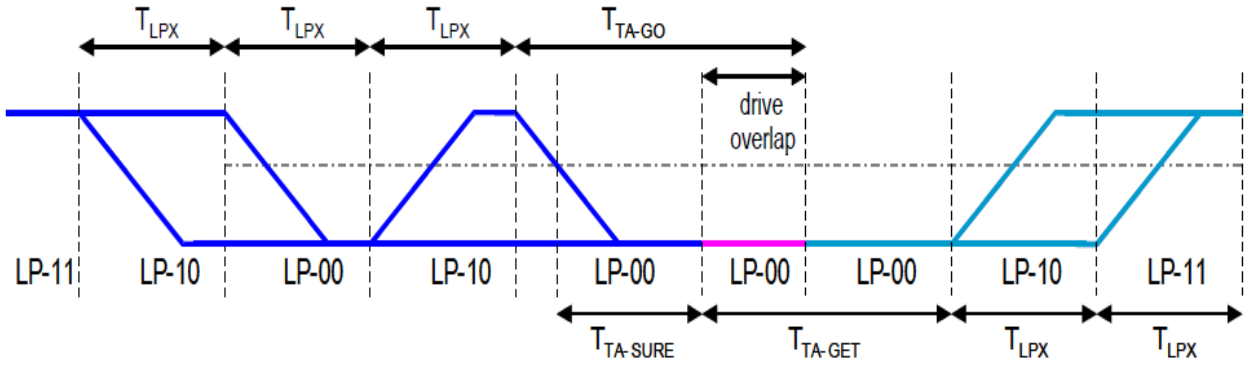


Figure 8.30: Turnaround Procedure

8.20.3 MIPI High Speed AC characteristics

Parameter	Descript	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI	-		ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-		UI
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI	-	145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+n*12*UI	-
$T_{HS-EXIT}$(1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	100	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For $T_{CLK-POST}$ example:
$T_{CLK-POST}$ min value =164UI when MIPI max frequency per lane = 0.5Gbps.
$T_{CLK-POST}$ min value =112UI when MIPI max frequency per lane = 1Gbps
(2) For T_{EOT}:
When n = 1 for Forward-direction HS mode and n=4 for Reverse-direction HS mode.

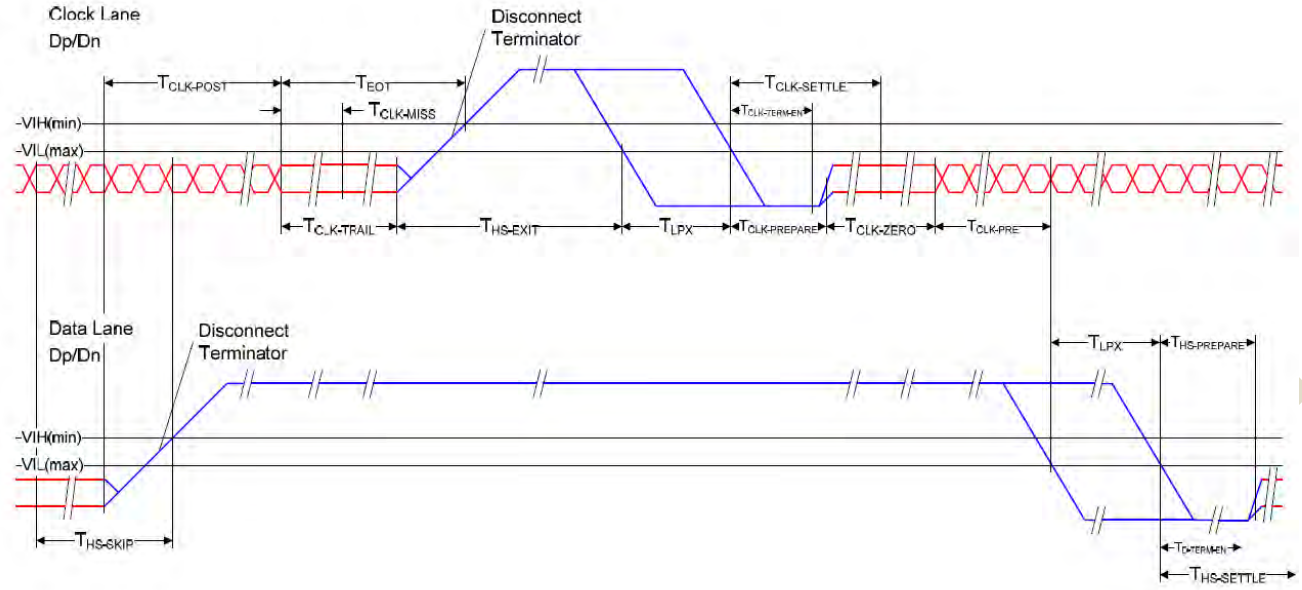


Figure 8.31: Switching the clock lane between clock transmission and low-power mode

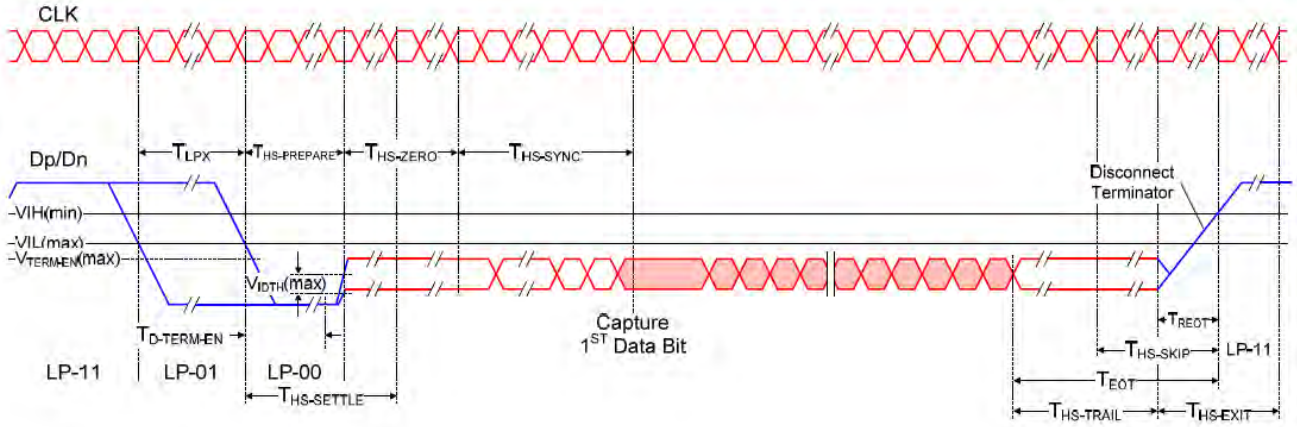


Figure 8.32: Timing of high-speed data transmission in bursts

8.20.4 MIPI data-clock timing specification

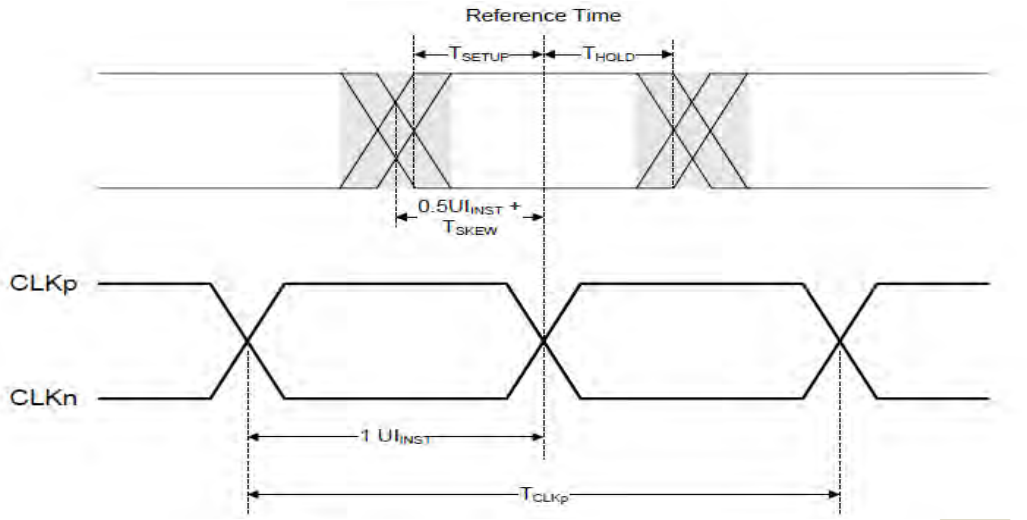


Figure 8.33: Data to clock timing

Parameter	Symbol	Min	Typ	Max	Units
Data to clock setup time	$T_{SETUP[RX]}$	0.15(1)	-	-	UI_{INST}
Data to clock hold time	$T_{HOLD[RX]}$	0.15(1)	-	-	UI_{INST}

Note: (1) Total setup and hold window for receiver of 0.3* UI_{INST}.

Table 8.8: Data to Clock Timing Specifications

8.21 MIPI video input timing

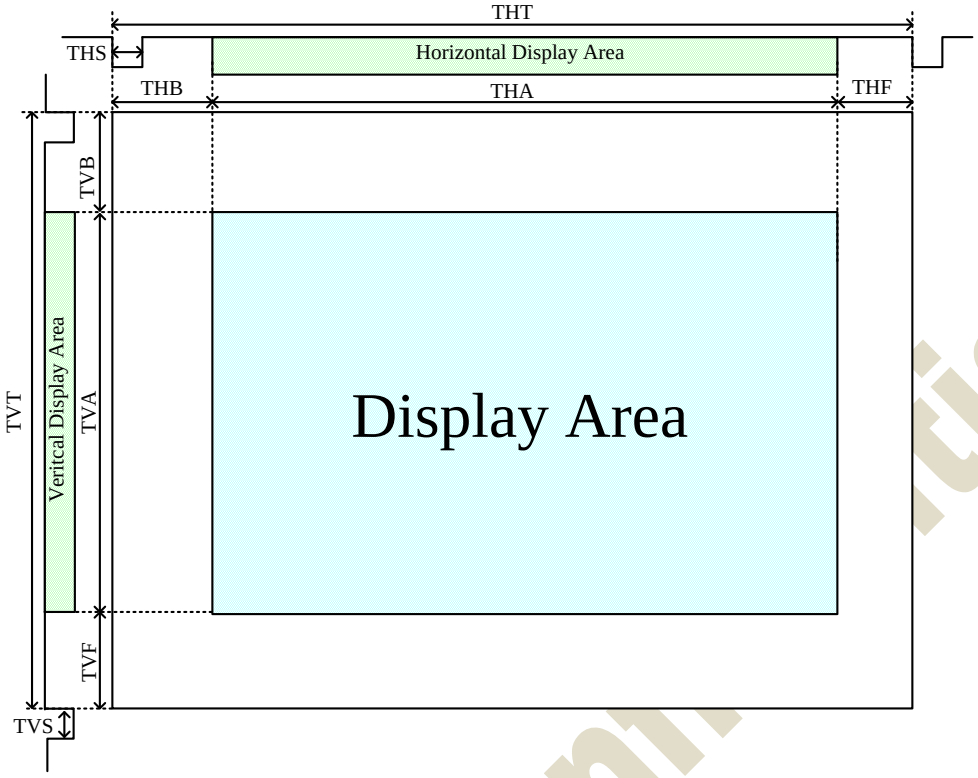


Figure 8.34: MIPI video input timing

8.21.1 MIPI timing characteristic

MIPI Input Timing	Symbol	1024RGBx768			1024RGBx600			800RGBx600			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MIPI 24-bit RGB@ 2 lane Operating Frequency	-	500	-	750	400	616	750	330	476	750	Mbps
MIPI 24-bit RGB@ 4 lane Operating Frequency	-	250	390	500	200	308	500	165	238	500	Mbps
Frame Rate@ 2 lane	-	47	-	-	48	60	-	49	60	-	Hz
Frame Rate@ 4 lane	-	47	60	-	48	60	-	49	60	-	Hz
Horizontal Total	tht	1114	1344	1400	1114	1344	1400	890	1000	1300	DCLK
Hsync Pulse width	ths	1	24	HBP-1	1	24	HBP-1	1	24	HBP-1	DCLK
Horizontal Back Porch	thb	60	160	160	60	160	160	60	160	250	DCLK
Horizontal Valid Data	thd		1024			1024			800		DCLK
Horizontal Front Porch	thfp	30	160	216	30	160	216	30	40	250	DCLK
Vertical Total	tvt	788	806	845	620	635	800	620	660	800	THT
Vsync Pulse Width	tvs	1	2	VBP-1	1	2	VBP-1	1	2	VBP-1	THT
Vertical Back Porch	tvb	8	23	33	8	23	100	8	39	100	THT
Vertical Valid Data	tvd		768			600			600		THT
Vertical Front Porch	tvfp	12	15	44	12	12	100	12	21	100	THT

MIPI Input Timing	Symbol	800RGBx480			640RGBx480			480RGBx272			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MIPI 24-bit RGB@ 2 lane Operating Frequency	-	270	390	650	330	476	650	260	392	500	Mbps
MIPI 24-bit RGB@ 4 lane Operating Frequency	-	135	195	400	165	238	400	130	196	300	Mbps
Frame Rate@ 2 lane	-	50	60	-	50	60	-	52	60	-	Hz
Frame Rate@ 4 lane	-	50	60	-	50	60	-	52	60	-	Hz
Horizontal Total	tht	900	1000	1300	890	1000	1114	830	890	950	DCLK
Hsync Pulse width	ths	4	24	HBP-1	1	24	HBP-1	1	24	HBP-1	DCLK
Horizontal Back Porch	thb	62	160	250	140	88	220	180	210	240	DCLK
Horizontal Valid Data	thd		800			640			480		DCLK
Horizontal Front Porch	thfp	38	40	250	110	272	254	170	200	230	DCLK
Vertical Total	tvt	500	540	680	610	660	800	498	610	660	THT
Vsync Pulse Width	tvs	1	2	VBP-1	1	2	VBP-1	1	2	VBP-1	THT
Vertical Back Porch	tvb	8	23	100	28	39	160	126	180	210	THT
Vertical Valid Data	tvd		480			480			272		THT
Vertical Front Porch	tvfp	12	37	100	102	141	160	100	158	178	THT

9. SPI FORMAT

9.1 3-wire SPI format

The JD9165 supports the 3-wire serial peripheral interface **(SPI)** to set internal register. The basic operation of SPI interface is shown below. The Host asserts the CSB when it wants to initiate a read or write transaction. This is followed by the Host sending 9 pulses on the SPI clock **(SCL)**. The 1th bit of SCL pulses is defined to write command or parameter. **(0=command , 1=parameter)**. The Host de-asserts the CSB to indicate end of transfer.

9.1.1 3-wire SPI interface Ⅰ

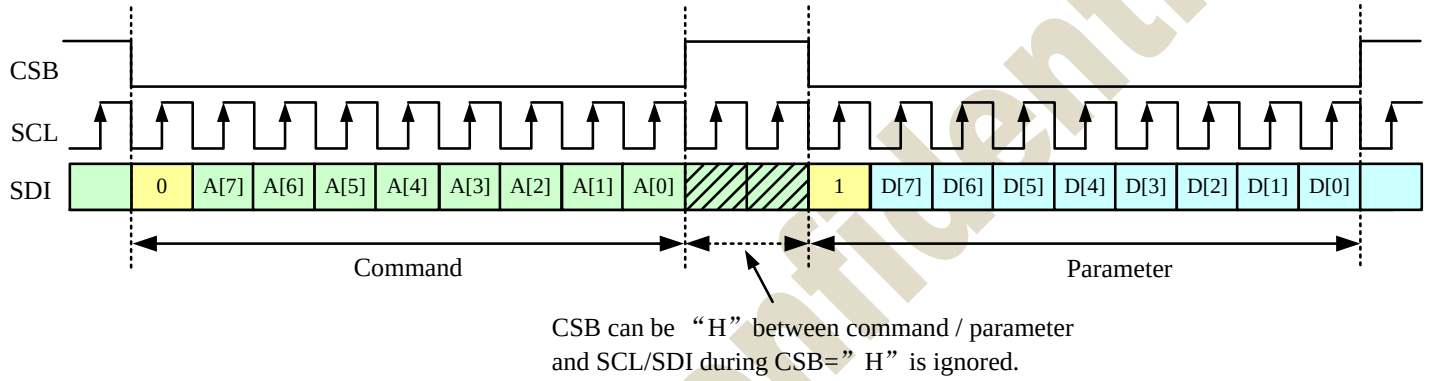


Figure 9.1: 3-wire SPI Ⅰ single write operation

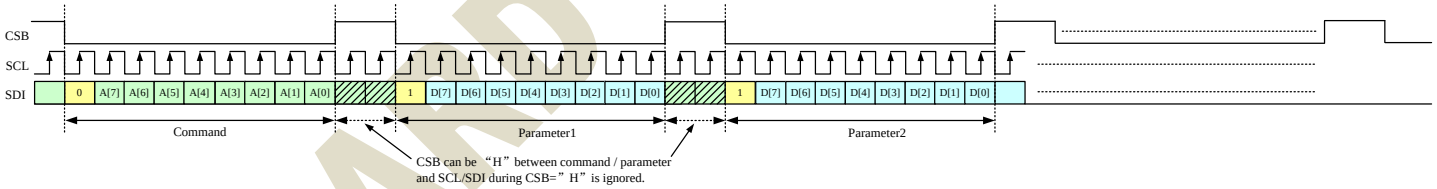


Figure 9.2: 3-wire SPI Ⅰ multi write operation

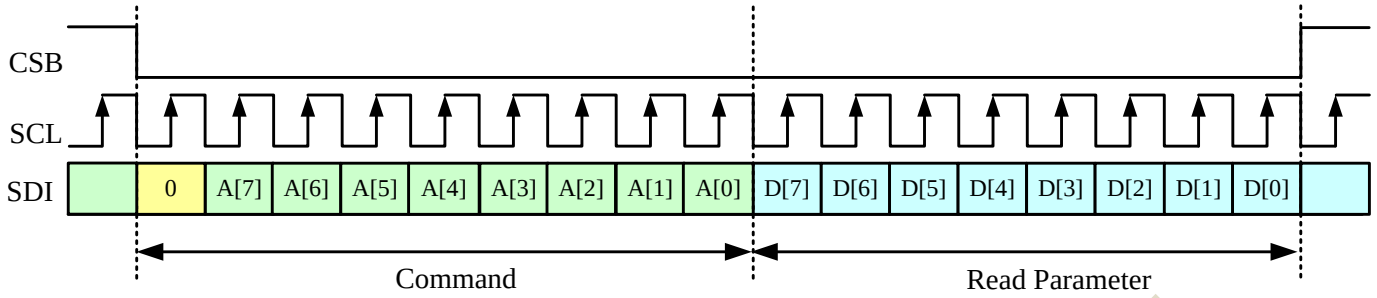


Figure 9.3: 3-wire SPI I single read operation

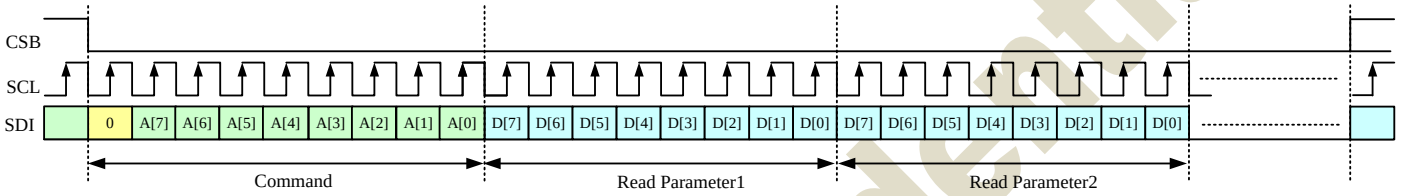


Figure 9.4: 3-wire SPI I multi read operation

9.1.2 3-wire SPI interface Ⅱ

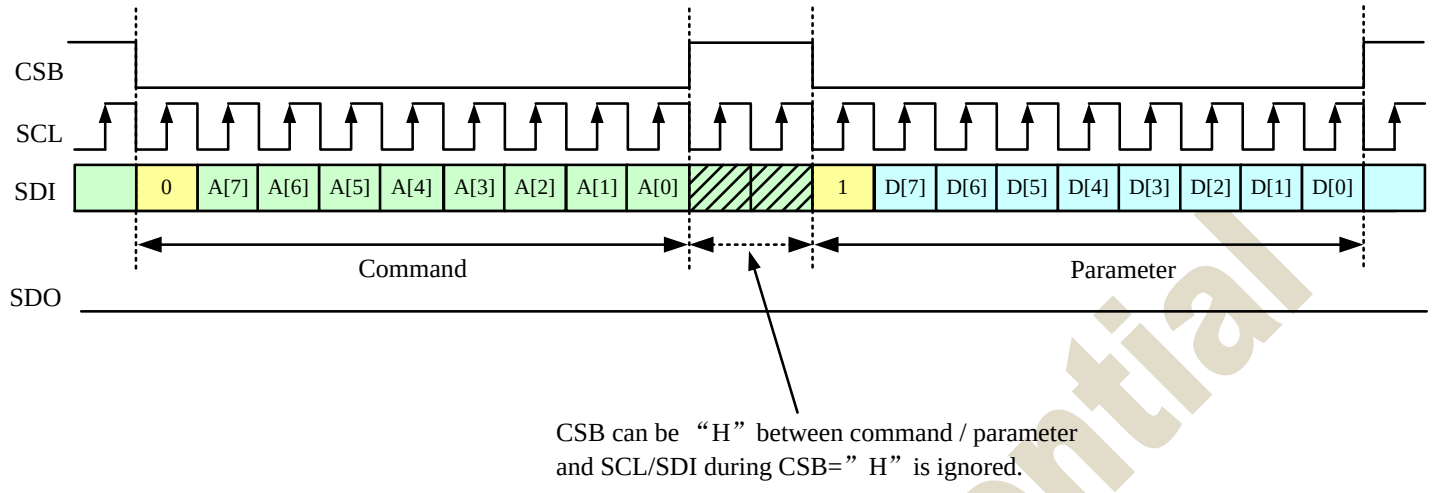


Figure 9.5: 3-wire SPI Ⅱ single write operation

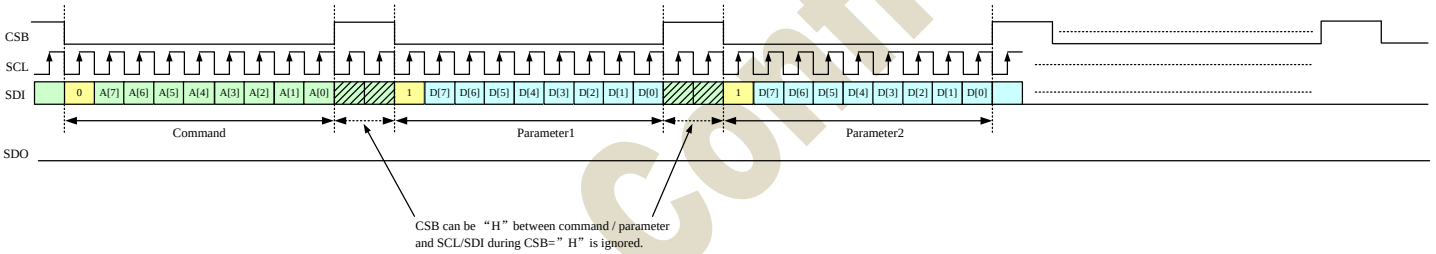


Figure 9.6: 3-wire SPI Ⅱ multi write operation

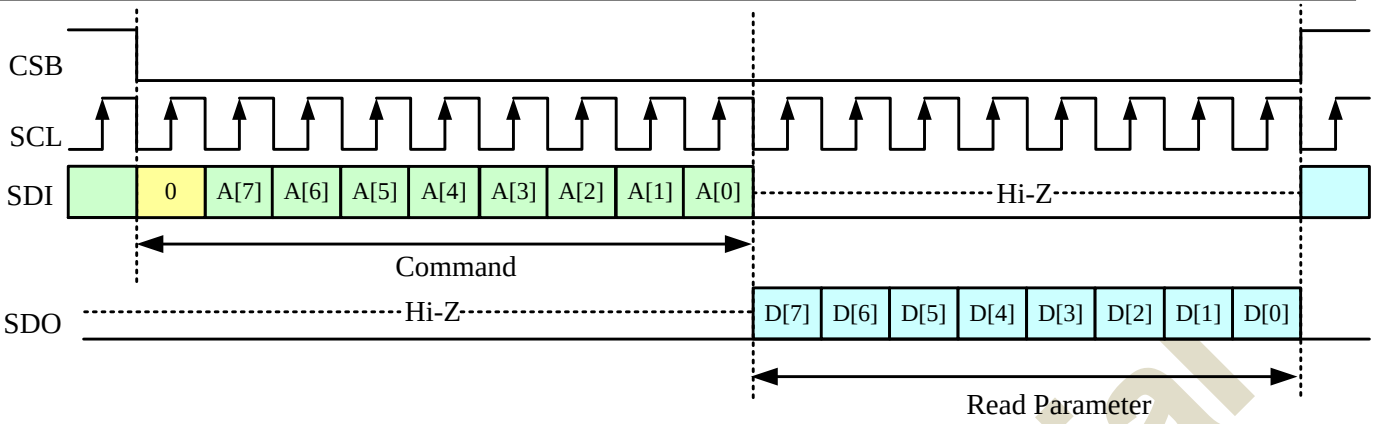


Figure 9.7: 3-wire SPI Ⅱ single read operation

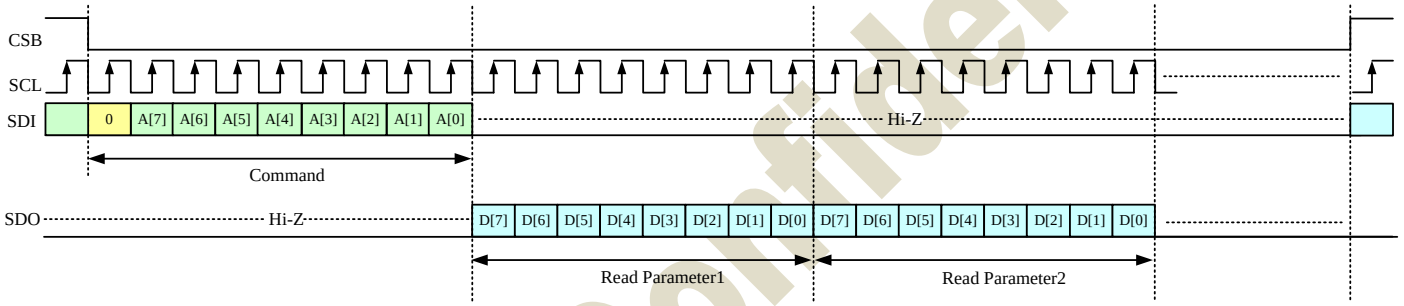


Figure 9.8: 3-wire SPI Ⅱ multi read operation

9.2 3-wire interface characteristics

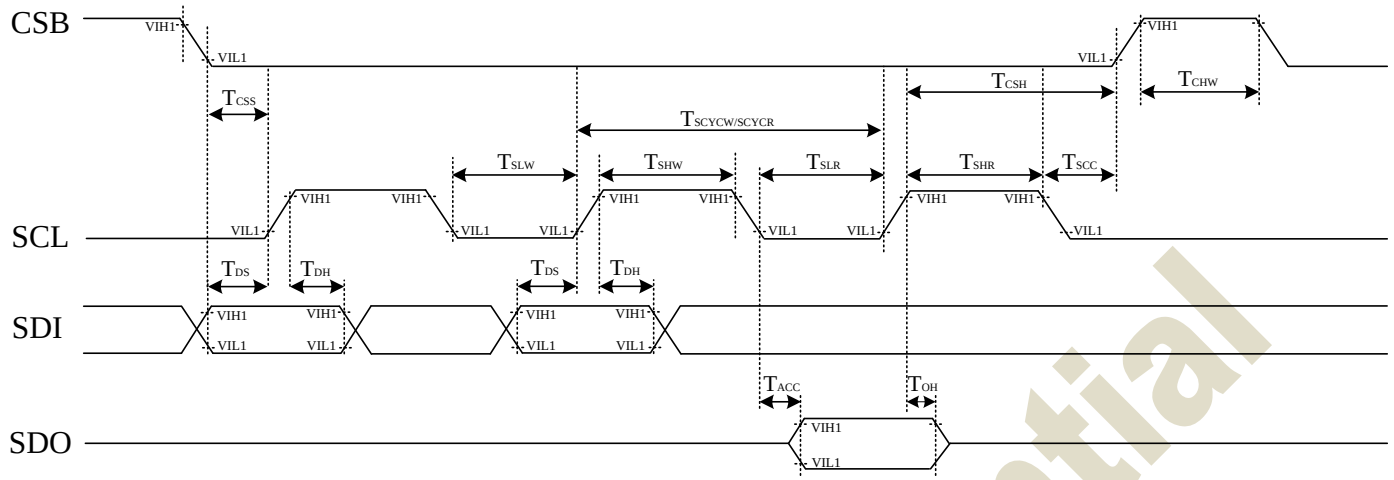


Figure 9.9: 3-wire SPI interface characteristics

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max	
Chip select setup time	T_{CSS}	120	-	-	ns
Chip select hold time	T_{CSH}	220	-	-	ns
Chip select setup time	T_{SCC}	120	-	-	ns
Chip select high width	T_{CHW}	100	-	-	ns
Serial clock cycle (Write)	T_{SCYCW}	74	-	-	ns
SCL “H” pulse width (Write)	T_{SHW}	37	-	-	ns
SCL “L” pulse width (Write)	T_{SLW}	37	-	-	ns
Serial clock cycle (Read)	T_{SCYCR}	200	-	-	ns
SCL “H” pulse width (Read)	T_{SHR}	100	-	-	ns
SCL “L” pulse width (Read)	T_{SHL}	100	-	-	ns
Data setup time	T_{SDS}	18	-	-	ns
Data hold time	T_{SDH}	18	-	-	ns
Access time	T_{ACC}	10	-	75	ns
Output disable time	T_{OH}	10	-	75	ns

10. I2C FORMAT

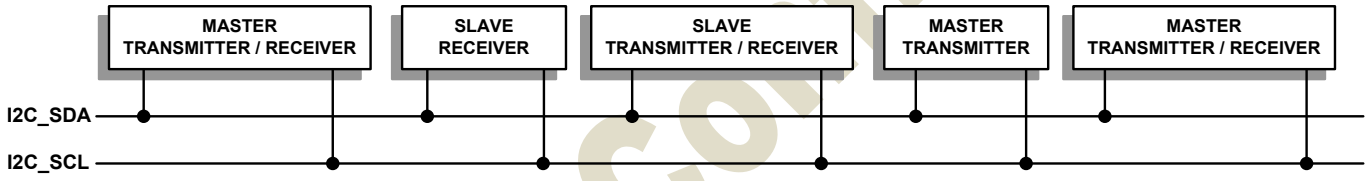
The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I²C_SDA) and the Serial Clock Line (I²C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I²C-Bus Protocol:

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

(b) Definitions:

- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



10.1 Register write sequence of I²C interface

JD9165 supports register write sequence via I²C-bus transfer. The register writing support single register write mode and multi-register write mode. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in below.
(2) After the START condition (S), a slave address is sent. R/W bit is setting to "0" for WRITE.
(3) The slave issues an ACK to master.
(4) 8 bits register address transfer first then transfer the register data parameter.
(5) A data transfer is always terminated by a STOP condition.
(6) JD9165 DA[6:0]=110_1000

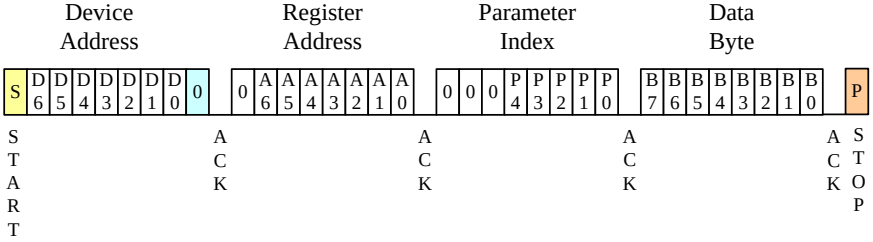


Figure 10.1: Single Register Writing Timing

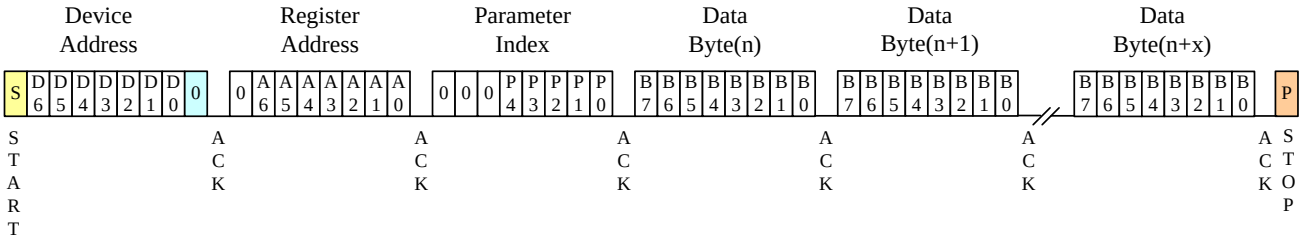


Figure 10.2: Multi Register Writing Timing

10.2 Register read sequence of I²C interface

JD9165 supports register read sequence via I²C-bus transfer. The register reading only support single register read mode.

Register data reading transfers follow the format and is shown in below.

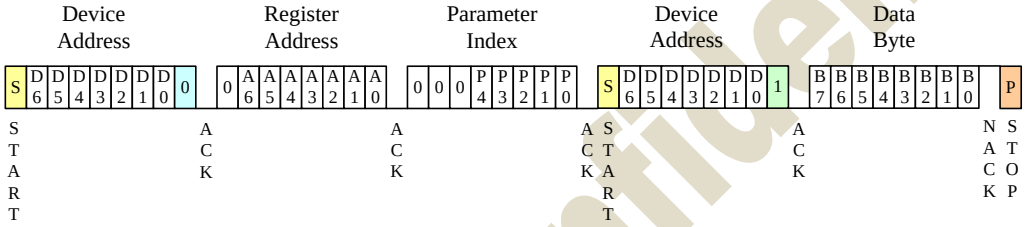


Figure 10.3: Single Register Reading Timing

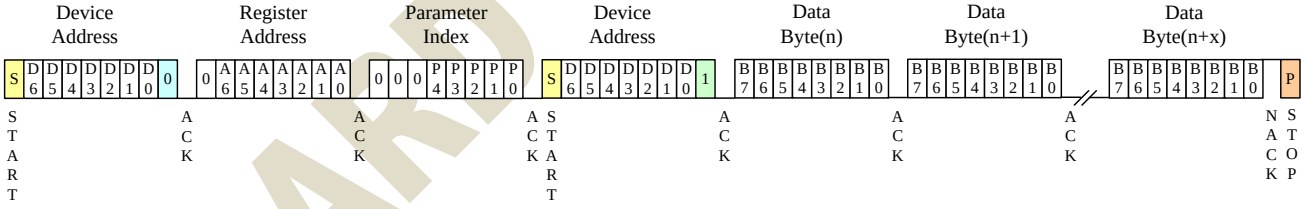


Figure 10.4: Multi Register Reading Timing

11. REGISTER FUNCTION

11.1 Register page selection

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
30	00	W/R	register page selection								**00**

R30h_00

Address	Bit							
R30h	D7	D6	D5	D4	D3	D2	D1	D0
Name	register page selection							
Default	0	0	0	0	0	0	0	0

R30h[7:0]: Register page selection.

R30h[7:0]	Function	Note
00h	Register page 0	Default
01h	Register page 1	-
02h	Register page 2	-
06h	Register page 6	-
07h	Register page 7	-
08h	Register page 8	-
09h	Register page 9	-
0Ah	Register page A	-
0Dh	Register page D	-

11.2 Page 0 command

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00	00	W	NOP								--
01	00	W	SWRESET								--
10	00	W	SLPIN								--
11	00	W	SLPOUT								--
20	00	W	INVOFF								--
21	00	W	INVON								--
28	00	W	DISPOFF								--
29	00	W	DISPON								--
34	00	W	tp_off								--
35	00	W	-	-	-	-	-	-	-	tp_on	**00**
36	00	W	-	-	-	-	bgr	-	ss	gs	**00**
7E	00	W/R	-	-	-	-	-	-	-	stbyb	**01**
F7	00	W/R	key1								**00**
F7	01	W/R	key2								**00**
F7	02	W/R	key3								**00**
F7	03	W/R	key4								**00**

R00h: MIPI empty command (refer to 8.18.1 NOP section)

Address	Bit							
R00h	D7	D6	D5	D4	D3	D2	D1	D0
Name	NOP							

R01h: MIPI software reset command (refer to 8.18.2 SWRESET section)

Address	Bit							
R01h	D7	D6	D5	D4	D3	D2	D1	D0
Name	SWRESET							

R10h: MIPI sleep in command (refer to 8.18.11 SLPIN section)

Address	Bit							
R10h	D7	D6	D5	D4	D3	D2	D1	D0
Name	SLPIN							

R11h: MIPI sleep out command (refer to 8.18.12 SLPOUT section)

Address	Bit							
R11h	D7	D6	D5	D4	D3	D2	D1	D0
Name	SLPOUT-							

R20h: This command makes no change of contents of image (refer to 8.18.13 INVOFF section)

Address	Bit							
R20h	D7	D6	D5	D4	D3	D2	D1	D0
Name	INVOFF							

R21h: Every bit is inverted from the image to the display (refer to 8.18.14 INVON section)

Address	Bit							
R21h	D7	D6	D5	D4	D3	D2	D1	D0
Name	INVON							

R28h: MIPI display off command (refer to 8.18.15 DISPOFF section)

Address	Bit							
R28h	D7	D6	D5	D4	D3	D2	D1	D0
Name	DISPOFF							

R29h: MIPI display on command (refer to 8.18.16 DISPON section)

Address	Bit							
R29h	D7	D6	D5	D4	D3	D2	D1	D0
Name	DISPON							

R34h: TP_SYNC off command

Address	Bit							
R34h	D7	D6	D5	D4	D3	D2	D1	D0
Name	tp_off							

R35h: TP_SYNC on command

Address	Bit							
R35h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	tp_on
Default	0	0	0	0	0	0	0	0

R35h[0]: Vertical scan direction.

R35h[0]	Function	Note
0	TP_SYNC = no signal	Default
1	TP_SYNC = Internal Vsync	-

R36h_00

Address	Bit							
R36h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	bgr	-	ss	gs
Default	0	0	0	0	0	0	0	0

R36h[0]: Vertical scan direction.

R36h[0]	Function	Note
0	Top -> Bottom	Default
1	Bottom -> Top	-

Note: R36h[0] is only support for MIPI.

R36h[1]: Horizontal scan direction.

R36h[1]	Function	Note
0	S0 -> S1-> …….. -> S1536 -> S1537	Default
1	S1537 -> S1536 -> ……. -> S1 ->S0	-

Note: R36h[1] is only support for MIPI.

R36h[3]: RGB-BGR order.

R36h[3]	Function	Note
0	RGB color filter	Default
1	BGR color filter	-

Note: R36h[3] is only support for MIPI.

R7Eh_00

Address	Bit							
R7Eh	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	stbyb
Default	0	0	0	0	0	0	0	1

R7Eh[0]: IC Standby mode selection.

R7Eh[0]	Function	Note
0	Standby mode	Default
1	Normal display	-

Note: R7Eh[0] is only support for TTL and LVDS.

RF7h_00/01/02/03

Address	Bit							
RF7h	D7	D6	D5	D4	D3	D2	D1	D0
Name	key1							
Name	key2							
Name	key3							
Name	key4							
Default	0	0	0	0	0	0	0	0

RF7h_00/01/02/03: IC inhouse command entry.

RF7h	Function	Note
00	49h	-
01	61h	-
02	02h	-
03	00h	-

11.3 Page 1 command

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
04	00	W/R	r_nbw_sel_reg	-	-	-	r_updn_sel_reg	r_shlr_sel_reg	-	-	**00**
05	00	W/R	r_lvbit_sel_reg	r_lvfmt_sel reg	-	-	-	-	-	r_bist_sel_reg	**00**
06	00	W/R		r_bist	r_nbw	-	-	-	r_updn	r_shlr	**00**
07	00	W/R	r_prog_hres[7:0]								**00**
08	00	W/R	r_lvbit	r_lvfmt	-	-	-	r_prog_hres[10:8]			**00**
09	00	W/R	r_prog_vres[7:0]								**00**
0A	00	W/R	r_force_single_gate	r_prog_vres_en	r_prog_hres_en	-	-	r_prog_vres[10:8]			**00**
0B	00	W/R	-	r_res[2:0]			-	-	r_lansel[1:0]		**00**
18	00	W/R	IC_Version_ID[7:0]								**02**
18	01	W/R	Panel_Version_ID1[7:0]								**00**
18	02	W/R	Panel_Version_ID2[7:0]								**00**
1B	00	W/R	-	-	-	-	-	-	-	otp_cmd_program	**00**
1F	00	W/R	-	-	-	r_hs_settle[4:0]					**00**
20	00	W/R	-	-	-	-	-	lansel_sel_reg	-	-	**00**
23	00	W/R	-	-	-	GAS_VDD_EN	GAS_EN	PSD_GAS_VDDA_EN	-	-	**3C**
25	00	W/R	-	-	VCOM_LPC[2:0]			-	VCOM_MILLER_EN	-	**01**
27	00	W/R							VCOM_DA[1:0]		**AB**
28	00	W/R	-	-	-	-	-	-	VCOM_GND_HIZ_ON_STB[1:0]		**1A**
29	00	W/R	VCOMR_SEL[7:0]								**04**
2A	00	W/R	-	-	-	-	-	-	-	VCOMR_SEL[8]	**01**
2B	00	W/R	VCOM_SEL[7:0]								**04**
2C	00	W/R	-	-	-	-	-	-	-	VCOM_SEL[8]	**01**
39	00	W/R	-	r_ledpwm_en	r_ledpwm_duty[2:0]			r_ledpwm_freq[2:0]			**1C**

R04h_00

Address	Bit							
R04h	D7	D6	D5	D4	D3	D2	D1	D0
Name	r_nbw_sel_reg	-	-	-	r_updn_sel_reg	r_shlr_sel_reg	-	-
Default	0	0	0	0	0	0	0	0

R04h[2]: Horizontal scan direction selection.

R04h[2]	Function	Note
0	SHLR setting by H/W pin	Default
1	SHLR setting by register	-

R04h[3]: Vertical scan direction selection.

R04h[3]	Function	Note
0	UPDN setting by H/W pin	Default
1	UPDN setting by register	-

R04h[7]: Panel type selection.

R04h[7]	Function	Note
0	NBW setting by H/W pin	Default
1	NBW by register	-

R05h_00

Address	Bit							
R05h	D7	D6	D5	D4	D3	D2	D1	D0
Name	r_lvbit_sel_reg	r_lvfmt_sel_reg	-	-	-	-	-	r_bist_sel_reg
Default	0	0	0	0	0	0	0	0

R05h[0]: BIST mode selection.

R05h[0]	Function	Note
0	BIST_EN setting by H/W pin	Default
1	BIST_EN setting by register	-

R05h[6]: LVDS 8-bit input format selection.

R05h[6]	Function	Note
0	LVFMT setting by H/W pin	Default
1	LVFMT setting by register	-

R05h[7]: LVDS 6-bit/8-bit input selection.

R05h[7]	Function	Note
0	LVBIT setting by H/W pin	Default
1	LVBIT setting by register	-

R06h_00

Address	Bit							
R06h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	r_bist	r_nbw	-	-	-	r_updn	r_shlr
Default	0	0	0	0	0	0	0	0

R06h[0]: Horizontal scan direction.

R06h[0]	Function	Note
0	S0 -> S1-> …….. -> S1536 -> S1537	Default
1	S1537 -> S1536 -> ……. -> S1 ->S0	-

Note: R06h[0] is only support for TTL and LVDS.

R06h[1]: Vertical scan direction.

R06h[1]	Function	Note
0	Top -> Bottom	Default
1	Bottom -> Top	-

Note: R06h[1] is only support for TTL and LVDS.

R06h[5]: Panel type selection.

R06h[5]	Function	Note
0	Normally black panel	Default
1	Normally white panel	-

R06h[6]: BIST mode selection.

R06h[6]	Function	Note
0	Normal mode	Default
1	BIST mode	-

R07h_00

Address	Bit							
R07h	D7	D6	D5	D4	D3	D2	D1	D0
Name	r_prog_hres[7:0]							
Default	0	0	0	0	0	0	0	0

R07h[7:0]/R08h[2:0]: Free horizontal resolution selection.
Ex: 600RGB => R07h=58h/R08h=02h.

R08h_00

Address	Bit							
R08h	D7	D6	D5	D4	D3	D2	D1	D0
Name	r_lvbit	r_lvfmt	-	-	-	r_prog_hres[10:8]		
Default	0	0	0	0	0	0	0	0

R08h[6]: LVDS 8-bit input format selection.

R08h[6]	Function	Note
0	JEIDA format	Default
1	VESA format	-

R08h[7]: LVDS 6-bit/8-bit input selection.

R08h[7]	Function	Note
0	6-bit	Default
1	8-bit	-

R09h_00

Address	Bit							
R09h	D7	D6	D5	D4	D3	D2	D1	D0
Name	r_prog_vres[7:0]							
Default	0	0	0	0	0	0	0	0

R09h[7:0]/R0Ah[2:0]: Free vertical resolution selection.
Ex: 480line => R09h=E0h/R0Ah=01h

R0Ah_00

Address	Bit							
R0Ah	D7	D6	D5	D4	D3	D2	D1	D0
Name	r_force_single_gate	r_prog_vres_en	r_prog_hres_en	-	-	r_prog_vres[10:8]		
Default	0	0	0	0	0	0	0	0

R0Ah[5]: Free horizontal resolution enable.

R0Ah[5]	Function	Note
0	disable	Default
1	enable	-

R0Ah[6]: Free vertical resolution enable.

R0Ah[6]	Function	Note
0	disable	Default
1	enable	-

R0Ah[7]: Dual gate / Single gate selection.

R0Ah[7]	Function	Note
0	Dual gate	Default
1	Single gate	-

R0Bh_00

Address	Bit							
R0Bh	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	r_res[2:0]			-	-	r_lansel[1:0]	
Default	0	0	0	0	0	0	0	0

R0Bh[1:0]: MIPI lane number selection.

R0Bh[1:0]	Function	Note
00	1 lane	Default
01	2 lane	-
10	3 lane	
11	4 lane	

Note: R20h[2]=1 set MIPI lane number function by register setting.

R0Bh[6:4]: Panel resolution selection.

R0Bh[6:4]	Function	Note
000	1024RGB x 768	Default
001	1024RGB x 600	-
010	800RGB x 600	-
011	640RGB x 480	-
100	480RGB x 272	-
101	T.B.D	-
110	T.B.D	-
111	T.B.D	-

R18h_00: IC_Version_ID

Address	Bit							
R18h	D7	D6	D5	D4	D3	D2	D1	D0
Name	IC_Version_ID[7:0]							
Default	0	0	0	0	0	0	1	0

R18h_01: Panel_Version_ID1

Address	Bit							
R18h	D7	D6	D5	D4	D3	D2	D1	D0
Name	Panel_Version_ID1[7:0]							
Default	0	0	0	0	0	0	0	0

R18h_02: IC_Version_ID2

Address	Bit							
R18h	D7	D6	D5	D4	D3	D2	D1	D0
Name	Panel_Version_ID2[7:0]							
Default	0	0	0	0	0	0	0	0

Note: R18h_00/01/02 is already OTP.

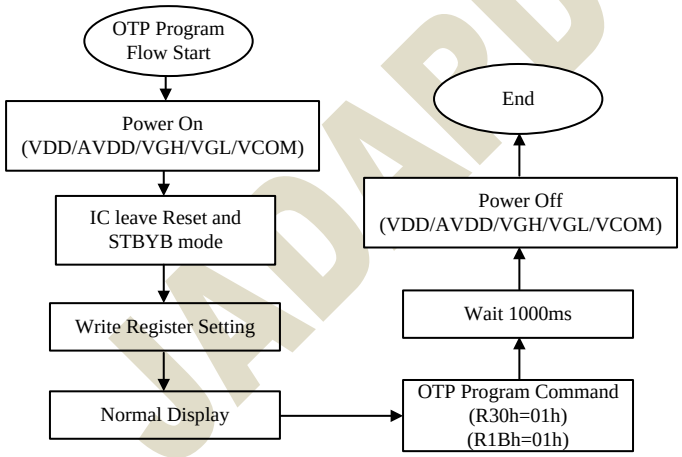
R1Bh_00

Address	Bit							
R1Bh	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	otp_cmd_program
Default	0	0	0	0	0	0	0	0

R1Bh[0]: OTP program command.

R1Bh[0]	Function	Note
0	disable	Default
1	enable	-

OTP Flow:



R1Fh_00

Address	Bit							
R1Fh	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	r_hs_settle[4:0]				
Default	0	0	0	0	0	0	0	0

R1Fh[4:0]: MIPI high speed settle time.

R1Fh[4:0]	Function	Note
00h	100+8*UI(ns)	Default
01h	100+12*UI(ns)	-
02h	100+16*UI(ns)	-
03h	100+20*UI(ns)	-
04h	100+24*UI(ns)	-
05h	100+28*UI(ns)	-
:	:	-
10h	100+72*UI(ns)	-
11h	100+76*UI(ns)	-
:	:	-
1Eh	100+128*UI(ns)	-
1Fh	100+132*UI(ns)	-

Ex: MIPI Speed=500Mbps, 1UI=2ns.

R20h_00: MIPI lane number function.

Address	Bit							
R20h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	lansel_sel_reg	-	-
Default	0	0	0	0	0	0	0	0

R20h[2]: MIPI lane number function.

R20h[2]	Function	Note
0	MIPI lane number setting by H/W pin	Default
1	MIPI lane number setting by register	-

R23h_00

Address	Bit							
R23h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	GAS_VDD_EN	GAS_EN	PSD_GAS_VDDA_EN	-	-
Default	0	0	1	1	1	1	0	0

R23h[2]: GAS detect by AVDD voltage

R23h[2]	Function	Note
0	disable	-
1	enable	Default

R23h[3]: GAS function

R23h[3]	Function	Note
0	disable	-
1	enable	Default

R23h[4]: GAS detect by VDD voltage

R23h[4]	Function	Note
0	disable	-
1	enable	Default

R25h_00

Address	Bit							
R25h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	VCOM_LPC[2:0]			-	VCOM_MILLER_EN	-
Default	0	0	0	0	0	0	0	1

R25h[1]: VCOM compensation method.

R25h[1]	Function	Note
0	miller off	Default
1	miller on	-

R25h[5:3]: VCOM slew rate selection.

R25h[5:3]	Function	Note
000	2us	Default
001	4us	-
010	6us	-
011	8us	-
100	10us	-
101	12us	-
110	14us	-
111	16us	-

R27h_00

Address	Bit							
R27h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	VCOM_DA[1:0]	
Default	1	0	1	0	1	0	1	1

R27h[1:0]: VCOM output driving ability

R27h[1:0]	Function	Note
00	Only Soft Start	-
01	x1	-
10	x2	-
11	x3	Default

R28h_00

Address	Bit							
R28h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	VCOM_GND_HIZ_ON_STB[1:0]	
Default	0	0	0	1	1	0	1	0

R28h[1:0]: VCOM voltage behavior in the Standby mode.

R28h[1:0]	Function	Note
00	Discharge to VMID	-
01	reserved	-
10	Hi-Z	Default
11	reserved	-

R29h_00

Address	Bit							
R29h	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOMR_SEL[7:0]							
Default	0	0	0	0	0	1	0	0

R2Ah_00

Address	Bit							
R2Ah	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	VCOMR_SEL[8]
Default	0	0	0	0	0	0	0	1

R29h[7:0]/R2Ah[0]: VCOM voltage. (Panel bottom to top scan)

000000000	reserved	000110010	4.85	001100100	4.6	010010110	4.35	011001000	4.1	011111010	3.85	100101100	3.6	101011110	3.35	110010000	3.1	111000010	2.85	111110100	reserved
000000001	reserved	000110011	4.845	001100101	4.595	010010111	4.345	011001001	4.095	011111011	3.845	100101101	3.595	101011111	3.345	110010001	3.095	111000011	2.845	111110101	reserved
000000010	reserved	000110100	4.84	001100110	4.59	010011000	4.34	011001010	4.09	011111100	3.84	100101110	3.59	101100000	3.34	110010010	3.09	111000100	2.84	111110110	reserved
000000011	reserved	000110101	4.835	001100111	4.585	010011001	4.335	011001011	4.085	011111101	3.835	100101111	3.585	101100001	3.335	110010011	3.085	111000101	2.835	111110111	reserved
000000100	reserved	000110110	4.83	001101000	4.58	010011010	4.33	011001100	4.08	011111110	3.83	100110000	3.58	101100010	3.33	110010100	3.08	111000110	2.83	111111000	reserved
000000101	reserved	000110111	4.825	001101001	4.575	010011011	4.325	011001101	4.075	011111111	3.825	100110001	3.575	101100011	3.325	110010101	3.075	111000111	2.825	111111001	reserved
000000110	reserved	000111000	4.82	001101010	4.57	010011100	4.32	011001110	4.07	100000000	3.82	100110010	3.57	101100100	3.32	110010110	3.07	111001000	2.82	111111010	reserved
000000111	reserved	000111001	4.815	001101011	4.565	010011101	4.315	011001111	4.065	100000001	3.815	100110011	3.565	101100101	3.315	110010111	3.065	111001001	2.815	111111011	reserved
000001000	reserved	000111010	4.81	001101100	4.56	010011110	4.31	011010000	4.06	100000010	3.81	100110100	3.56	101100110	3.31	110011000	3.06	111001010	2.81	111111100	reserved
000001001	reserved	000111011	4.805	001101101	4.555	010011111	4.305	011010001	4.055	100000011	3.805	100110101	3.555	101100111	3.305	110011001	3.055	111001011	2.805	111111101	reserved
000001010	reserved	000111100	4.8	001101110	4.55	010100000	4.3	011010010	4.05	100000100	3.8	100110110	3.55	101101000	3.3	110011010	3.05	111001100	2.8	111111110	reserved
000001011	reserved	000111101	4.795	001101111	4.545	010100001	4.295	011010011	4.045	100000101	3.795	100110111	3.545	101101001	3.295	110011011	3.045	111001101	2.795	111111111	reserved
000001100	reserved	000111110	4.79	001110000	4.54	010100010	4.29	011010100	4.04	100000110	3.79	100111000	3.54	101101010	3.29	110011100	3.04	111001110	2.79		
000001101	reserved	000111111	4.785	001110001	4.535	010100011	4.285	011010101	4.035	100000111	3.785	100111001	3.535	101101011	3.285	110011101	3.035	111001111	2.785		
000001110	reserved	001000000	4.78	001110010	4.53	010100100	4.28	011010110	4.03	100001000	3.78	100111010	3.53	101101100	3.28	110011110	3.03	111010000	2.78		
000001111	reserved	001000001	4.775	001110011	4.525	010100101	4.275	011010111	4.025	100001001	3.775	100111011	3.525	101101101	3.275	110011111	3.025	111010001	2.775		
000010000	reserved	001000010	4.77	001110100	4.52	010100110	4.27	011011000	4.02	100001010	3.77	100111100	3.52	101101110	3.27	110100000	3.02	111010010	2.77		
000010001	reserved	001000011	4.765	001110101	4.515	010100111	4.265	011011001	4.015	100001011	3.765	100111101	3.515	101101111	3.265	110100001	3.015	111010011	2.765		
000010010	reserved	001000100	4.76	001110110	4.51	010101000	4.26	011011010	4.01	100001100	3.76	100111110	3.51	101110000	3.26	110100010	3.01	111010100	2.76		
000010011	reserved	001000101	4.755	001110111	4.505	010101001	4.255	011011011	4.005	100001101	3.755	100111111	3.505	101110001	3.255	110100011	3.005	111010101	2.755		
000010100	reserved	001000110	4.75	001111000	4.5	010101010	4.25	011011100	4	100001110	3.75	101000000	3.5	101110010	3.25	110100100	3	111010110	2.75		
000010101	reserved	001000111	4.745	001111001	4.495	010101011	4.245	011011101	3.995	100001111	3.745	101000001	3.495	101110011	3.245	110100101	2.995	111010111	2.745		
000010110	reserved	001001000	4.74	001111010	4.49	010101100	4.24	011011110	3.99	100010000	3.74	101000010	3.49	101110100	3.24	110100110	2.99	111011000	2.74		
000010111	reserved	001001001	4.735	001111011	4.485	010101101	4.235	011011111	3.985	100010001	3.735	101000011	3.485	101110101	3.235	110100111	2.985	111011001	2.735		
000011000	reserved	001001010	4.73	001111100	4.48	010101110	4.23	011100000	3.98	100010010	3.73	101000100	3.48	101110110	3.23	110101000	2.98	111011010	2.73		
000011001	reserved	001001011	4.725	001111101	4.475	010101111	4.225	011100001	3.975	100010011	3.725	101000101	3.475	101110111	3.225	110101001	2.975	111011011	2.725		
000011010	reserved	001001100	4.72	001111110	4.47	010110000	4.22	011100010	3.97	100010100	3.72	101000110	3.47	101111000	3.22	110101010	2.97	111011100	2.72		
000011011	reserved	001001101	4.715	001111111	4.465	010110001	4.215	011100011	3.965	100010101	3.715	101000111	3.465	101111001	3.215	110101011	2.965	111011101	2.715		
000011100	reserved	001001110	4.71	010000000	4.46	010110010	4.21	011100100	3.96	100010110	3.71	101001000	3.46	101111010	3.21	110101100	2.96	111011110	2.71		
000011101	reserved	001001111	4.705	010000001	4.455	010110011	4.205	011100101	3.955	100010111	3.705	101001001	3.455	101111011	3.205	110101101	2.955	111011111	2.705		
000011110	reserved	001010000	4.7	010000010	4.45	010110100	4.2	011100110	3.95	100011000	3.7	101001010	3.45	101111100	3.2	110101110	2.95	111100000	2.7		
000011111	reserved	001010001	4.695	010000011	4.445	010110101	4.195	011100111	3.945	100011001	3.695	101001011	3.445	101111101	3.195	110101111	2.945	111100001	reserved		
000100000	4.94	001010010	4.69	010000100	4.44	010110110	4.19	011101000	3.94	100011010	3.69	101001100	3.44	101111110	3.19	110110000	2.94	111100010	reserved		
000100001	4.935	001010011	4.685	010000101	4.435	010110111	4.185	011101001	3.935	100011011	3.685	101001101	3.435	101111111	3.185	110110001	2.935	111100011	reserved		
000100010	4.93	001010100	4.68	010000110	4.43	010111000	4.18	011101010	3.93	100011100	3.68	101001110	3.43	110000000	3.18	110110010	2.93	111100100	reserved		
000100011	4.925	001010101	4.675	010000111	4.425	010111001	4.175	011101011	3.925	100011101	3.675	101001111	3.425	110000001	3.175	110110011	2.925	111100101	reserved		
000100100	4.92	001010110	4.67	010001000	4.42	010111010	4.17	011101100	3.92	100011110	3.67	101010000	3.42	110000010	3.17	110110100	2.92	111100110	reserved		
000100101	4.915	001010111	4.665	010001001	4.415	010111011	4.165	011101101	3.915	100011111	3.665	101010001	3.415	110000011	3.165	110110101	2.915	111100111	reserved		
000100110	4.91	001011000	4.66	010001010	4.41	010111100	4.16	011101110	3.91	100100000	3.66	101010010	3.41	110000100	3.16	110110110	2.91	111101000	reserved		
000100111	4.905	001011001	4.655	010001011	4.405	010111101	4.155	011101111	3.905	100100001	3.655	101010011	3.405	110000101	3.155	110110111	2.905	111101001	reserved		
000101000	4.9	001011010	4.65	010001100	4.4	010111110	4.15	011110000	3.9	100100010	3.65	101010100	3.4	110000110	3.15	110111000	2.9	111101010	reserved		
000101001	4.895	001011011	4.645	010001101	4.395	010111111	4.145	011110001	3.895	100100011	3.645	101010101	3.395	110000111	3.145	110111001	2.895	111101011	reserved		
000101010	4.89	001011100	4.64	010001110	4.39	011000000	4.14	011110010	3.89	100100100	3.64	101010110	3.39	110001000	3.14	110111010	2.89	111101100	reserved		
000101011	4.885	001011101	4.635	010001111	4.385	011000001	4.135	011110011	3.885	100100101	3.635	101010111	3.385	110001001	3.135	110111011	2.885	111101101	reserved		
000101100	4.88	001011110	4.63	010010000	4.38	011000010	4.13	011110100	3.88	100100110	3.63	101011000	3.38	110001010	3.13	110111100	2.88	111101110	reserved		
000101101	4.875	001011111	4.625	010010001	4.375	011000011	4.125	011110101	3.875	100100111	3.625	101011001	3.375	110001011	3.125	110111101	2.875	111101111	reserved		
000101110	4.87	001100000	4.62	010010010	4.37	011000100	4.12	011110110	3.87	100101000	3.62	101011010	3.37	110001100	3.12	110111110	2.87	111110000	reserved		
000101111	4.865	001100001	4.615	010010011	4.365	011000101	4.115	011110111	3.865	100101001	3.615	101011011	3.365	110001101	3.115	110111111	2.865	111110001	reserved		
000110000	4.86	001100010	4.61	010010100	4.36	011000110	4.11	011111000	3.86	100101010	3.61	101011100	3.36	110001110	3.11	111000000	2.86	111110010	reserved		
000110001	4.855	001100011	4.605	010010101	4.355	011000111	4.105	011111001	3.855	100101011	3.605	101011101	3.355	110001111	3.105	111000001	2.855	111110011	reserved		

Note: VCOM max= VMID - 0.2V.

R2Bh_00

Address	Bit							
R2Bh	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCOM_SEL[7:0]							
Default	0	0	0	0	0	1	0	0

R2Ch_00

Address	Bit							
R2Ch	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	VCOM_SEL[8]
Default	0	0	0	0	0	0	0	1

R2Bh[7:0]/R2Ch[0]: VCOM voltage. (Panel top to bottom scan)

000000000	reserved	000110010	4.85	001100100	4.6	010010110	4.35	011001000	4.1	011111010	3.85	100101100	3.6	101011110	3.35	110010000	3.1	111000010	2.85	111110100	reserved
000000001	reserved	000110011	4.845	001100101	4.595	010010111	4.345	011001001	4.095	011111011	3.845	100101101	3.595	101011111	3.345	110010001	3.095	111000011	2.845	111110101	reserved
000000010	reserved	000110100	4.84	001100110	4.59	010011000	4.34	011001010	4.09	011111100	3.84	100101110	3.59	101100000	3.34	110010010	3.09	111000100	2.84	111110110	reserved
000000011	reserved	000110101	4.835	001100111	4.585	010011001	4.335	011001011	4.085	011111101	3.835	100101111	3.585	101100001	3.335	110010011	3.085	111000101	2.835	111110111	reserved
000000100	reserved	000110110	4.83	001101000	4.58	010011010	4.33	011001100	4.08	011111110	3.83	100110000	3.58	101100010	3.33	110010100	3.08	111000110	2.83	111111000	reserved
000000101	reserved	000110111	4.825	001101001	4.575	010011011	4.325	011001101	4.075	011111111	3.825	100110001	3.575	101100011	3.325	110010101	3.075	111000111	2.825	111111001	reserved
000000110	reserved	000111000	4.82	001101010	4.57	010011100	4.32	011001110	4.07	100000000	3.82	100110010	3.57	101100100	3.32	110010110	3.07	111001000	2.82	111111010	reserved
000000111	reserved	000111001	4.815	001101011	4.565	010011101	4.315	011001111	4.065	100000001	3.815	100110011	3.565	101100101	3.315	110010111	3.065	111001001	2.815	111111011	reserved
000001000	reserved	000111010	4.81	001101100	4.56	010011110	4.31	011010000	4.06	100000010	3.81	100110100	3.56	101100110	3.31	110011000	3.06	111001010	2.81	111111100	reserved
000001001	reserved	000111011	4.805	001101101	4.555	010011111	4.305	011010001	4.055	100000011	3.805	100110101	3.555	101100111	3.305	110011001	3.055	111001011	2.805	111111101	reserved
000001010	reserved	000111100	4.8	001101110	4.55	010100000	4.3	011010010	4.05	100000100	3.8	100110110	3.55	101101000	3.3	110011010	3.05	111001100	2.8	111111110	reserved
000001011	reserved	000111101	4.795	001101111	4.545	010100001	4.295	011010011	4.045	100000101	3.795	100110111	3.545	101101001	3.295	110011011	3.045	111001101	2.795	111111111	reserved
000001100	reserved	000111110	4.79	001110000	4.54	010100010	4.29	011010100	4.04	100000110	3.79	100111000	3.54	101101010	3.29	110011100	3.04	111001110	2.79		
000001101	reserved	000111111	4.785	001110001	4.535	010100011	4.285	011010101	4.035	100000111	3.785	100111001	3.535	101101011	3.285	110011101	3.035	111001111	2.785		
000001110	reserved	001000000	4.78	001110010	4.53	010100100	4.28	011010110	4.03	100001000	3.78	100111010	3.53	101101100	3.28	110011110	3.03	111010000	2.78		
000001111	reserved	001000001	4.775	001110011	4.525	010100101	4.275	011010111	4.025	100001001	3.775	100111011	3.525	101101101	3.275	110011111	3.025	111010001	2.775		
000010000	reserved	001000010	4.77	001110100	4.52	010100110	4.27	011011000	4.02	100001010	3.77	100111100	3.52	101101110	3.27	110100000	3.02	111010010	2.77		
000010001	reserved	001000011	4.765	001110101	4.515	010100111	4.265	011011001	4.015	100001011	3.765	100111101	3.515	101101111	3.265	110100001	3.015	111010011	2.765		
000010010	reserved	001000100	4.76	001110110	4.51	010101000	4.26	011011010	4.01	100001100	3.76	100111110	3.51	101110000	3.26	110100010	3.01	111010100	2.76		
000010011	reserved	001000101	4.755	001110111	4.505	010101001	4.255	011011011	4.005	100001101	3.755	100111111	3.505	101110001	3.255	110100011	3.005	111010101	2.755		
000010100	reserved	001000110	4.75	001111000	4.5	010101010	4.25	011011100	4	100001110	3.75	101000000	3.5	101110010	3.25	110100100	3	111010110	2.75		
000010101	reserved	001000111	4.745	001111001	4.495	010101011	4.245	011011101	3.995	100001111	3.745	101000001	3.495	101110011	3.245	110100101	2.995	111010111	2.745		
000010110	reserved	001001000	4.74	001111010	4.49	010101100	4.24	011011110	3.99	100010000	3.74	101000010	3.49	101110100	3.24	110100110	2.99	111011000	2.74		
000010111	reserved	001001001	4.735	001111011	4.485	010101101	4.235	011011111	3.985	100010001	3.735	101000011	3.485	101110101	3.235	110100111	2.985	111011001	2.735		
000011000	reserved	001001010	4.73	001111100	4.48	010101110	4.23	011100000	3.98	100010010	3.73	101000100	3.48	101110110	3.23	110101000	2.98	111011010	2.73		
000011001	reserved	001001011	4.725	001111101	4.475	010101111	4.225	011100001	3.975	100010011	3.725	101000101	3.475	101110111	3.225	110101001	2.975	111011011	2.725		
000011010	reserved	001001100	4.72	001111110	4.47	010110000	4.22	011100010	3.97	100010100	3.72	101000110	3.47	101111000	3.22	110101010	2.97	111011100	2.72		
000011011	reserved	001001101	4.715	001111111	4.465	010110001	4.215	011100011	3.965	100010101	3.715	101000111	3.465	101111001	3.215	110101011	2.965	111011101	2.715		
000011100	reserved	001001110	4.71	010000000	4.46	010110010	4.21	011100100	3.96	100010110	3.71	101001000	3.46	101111010	3.21	110101100	2.96	111011110	2.71		
000011101	reserved	001001111	4.705	010000001	4.455	010110011	4.205	011100101	3.955	100010111	3.705	101001001	3.455	101111011	3.205	110101101	2.955	111011111	2.705		
000011110	reserved	001010000	4.7	010000010	4.45	010110100	4.2	011100110	3.95	100011000	3.7	101001010	3.45	101111100	3.2	110101110	2.95	111100000	2.7		
000011111	reserved	001010001	4.695	010000011	4.445	010110101	4.195	011100111	3.945	100011001	3.695	101001011	3.445	101111101	3.195	110101111	2.945	111100001	reserved		
000100000	4.94	001010010	4.69	010000100	4.44	010110110	4.19	011101000	3.94	100011010	3.69	101001100	3.44	101111110	3.19	110110000	2.94	111100010	reserved		
000100001	4.935	001010011	4.685	010000101	4.435	010110111	4.185	011101001	3.935	100011011	3.685	101001101	3.435	101111111	3.185	110110001	2.935	111100011	reserved		
000100010	4.93	001010100	4.68	010000110	4.43	010111000	4.18	011101010	3.93	100011100	3.68	101001110	3.43	110000000	3.18	110110010	2.93	111100100	reserved		
000100011	4.925	001010101	4.675	010000111	4.425	010111001	4.175	011101011	3.925	100011101	3.675	101001111	3.425	110000001	3.175	110110011	2.925	111100101	reserved		
000100100	4.92	001010110	4.67	010001000	4.42	010111010	4.17	011101100	3.92	100011110	3.67	101010000	3.42	110000010	3.17	110110100	2.92	111100110	reserved		
000100101	4.915	001010111	4.665	010001001	4.415	010111011	4.165	011101101	3.915	100011111	3.665	101010001	3.415	110000011	3.165	110110101	2.915	111100111	reserved		
000100110	4.91	001011000	4.66	010001010	4.41	010111100	4.16	011101110	3.91	100100000	3.66	101010010	3.41	110000100	3.16	110110110	2.91	111101000	reserved		
000100111	4.905	001011001	4.655	010001011	4.405	010111101	4.155	011101111	3.905	100100001	3.655	101010011	3.405	110000101	3.155	110110111	2.905	111101001	reserved		
000101000	4.9	001011010	4.65	010001100	4.4	010111110	4.15	011110000	3.9	100100010	3.65	101010100	3.4	110000110	3.15	110111000	2.9	111101010	reserved		
000101001	4.895	001011011	4.645	010001101	4.395	010111111	4.145	011110001	3.895	100100011	3.645	101010101	3.395	110000111	3.145	110111001	2.895	111101011	reserved		
000101010	4.89	001011100	4.64	010001110	4.39	011000000	4.14	011110010	3.89	100100100	3.64	101010110	3.39	110001000	3.14	110111010	2.89	111101100	reserved		
000101011	4.885	001011101	4.635	010001111	4.385	011000001	4.135	011110011	3.885	100100101	3.635	101010111	3.388	110001001	3.135	110111011	2.885	111101101	reserved		
000101100	4.88	001011110	4.63	010010000	4.38	011000010	4.13	011110100	3.88	100100110	3.63	101011000	3.38	110001010	3.13	110111100	2.88	111101110	reserved		
000101101	4.875	001011111	4.625	010010001	4.375	011000011	4.125	011110101	3.875	100100111	3.625	101011001	3.375	110001011	3.125	110111101	2.875	111101111	reserved		
000101110	4.87	001100000	4.62	010010010	4.37	011000100	4.12	011110110	3.87	100101000	3.62	101011010	3.37	110001100	3.12	110111110	2.87	111110000	reserved		
000101111	4.865	001100001	4.615	010010011	4.365	011000101	4.115	011110111	3.865	100101001	3.615	101011011	3.365	110001101	3.115	110111111	2.865	111110001	reserved		
000110000	4.86	001100010	4.61	010010100	4.36	011000110	4.11	011111000	3.86	100101010	3.61	101011100	3.36	110001110	3.11	111000000	2.86	111110010	reserved		
000110001	4.855	001100011	4.605	010010101	4.355	011000111	4.105	011111001	3.855	100101011	3.605	101011101	3.355	110001111	3.105	111000001	2.855	111110011	reserved		

Note: VCOM max= VMID - 0.2V.

R39h_00

Address	Bit							
R39h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	r_ledpwm_en	r_ledpwm_duty[2:0]			r_ledpwm_freq[2:0]		
Default	0	0	0	1	1	1	0	0

R39h[2:0]: LEDPWM frequency selection.

R39h[2:0]	Function	Note
000	2kHz	-
001	4kHz	-
010	6kHz	-
011	8kHz	-
100	10kHz	Default
101	12kHz	-
110	14kHz	-
111	16kHz	-

R39h[5:3]: LEDPWM duty selection.

R39h[5:3]	Function	Note
000	15%	-
001	25%	-
010	35%	-
011	50%	Default
100	65%	-
101	75%	-
110	85%	-
111	100%	-

R39h[6]: LEDPWM selection.

R39h[6]	Function	Note
0	disable	Default
1	enable	-

11.4 Page 2 command

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00	00	W/R	force_flc_clr_en	sub_flc_dis[1:0]		stv_ckv_dis[2:0]			stv_ckv_stagger	GIP_DR	05
0B	00	W/R	-	-	-	goutr1_sel_u2d[4:0]					00
0B	01	W/R	-	-	-	goutr2_sel_u2d[4:0]					00
0B	02	W/R	-	-	-	goutr3_sel_u2d[4:0]					00
0B	03	W/R	-	-	-	goutr4_sel_u2d[4:0]					00
0B	04	W/R	-	-	-	goutr5_sel_u2d[4:0]					00
0B	05	W/R	-	-	-	goutr6_sel_u2d[4:0]					00
0B	06	W/R	-	-	-	goutr7_sel_u2d[4:0]					00
0B	07	W/R	-	-	-	goutr8_sel_u2d[4:0]					00
0B	08	W/R	-	-	-	goutr9_sel_u2d[4:0]					00
0B	09	W/R	-	-	-	goutr10_sel_u2d[4:0]					00
0B	0A	W/R	-	-	-	goutr11_sel_u2d[4:0]					00
0C	00	W/R	-	-	-	goutr12_sel_u2d[4:0]					00
0C	01	W/R	-	-	-	goutr13_sel_u2d[4:0]					00
0C	02	W/R	-	-	-	goutr14_sel_u2d[4:0]					00
0C	03	W/R	-	-	-	goutr15_sel_u2d[4:0]					00
0C	04	W/R	-	-	-	goutr16_sel_u2d[4:0]					00
0C	05	W/R	-	-	-	goutr17_sel_u2d[4:0]					00
0C	06	W/R	-	-	-	goutr18_sel_u2d[4:0]					00
0C	07	W/R	-	-	-	goutr19_sel_u2d[4:0]					00
0C	08	W/R	-	-	-	goutr20_sel_u2d[4:0]					00
0C	09	W/R	-	-	-	goutr21_sel_u2d[4:0]					00
0C	0A	W/R	-	-	-	goutr22_sel_u2d[4:0]					00
0D	00	W/R	-	-	-	goutl1_sel_u2d[4:0]					00
0D	01	W/R	-	-	-	goutl2_sel_u2d[4:0]					00
0D	02	W/R	-	-	-	goutl3_sel_u2d[4:0]					00
0D	03	W/R	-	-	-	goutl4_sel_u2d[4:0]					00
0D	04	W/R	-	-	-	goutl5_sel_u2d[4:0]					00
0D	05	W/R	-	-	-	goutl6_sel_u2d[4:0]					00
0D	06	W/R	-	-	-	goutl7_sel_u2d[4:0]					00
0D	07	W/R	-	-	-	goutl8_sel_u2d[4:0]					00
0D	08	W/R	-	-	-	goutl9_sel_u2d[4:0]					00
0D	09	W/R	-	-	-	goutl10_sel_u2d[4:0]					00
0D	0A	W/R	-	-	-	goutl11_sel_u2d[4:0]					00
0E	00	W/R	-	-	-	goutl12_sel_u2d[4:0]					00
0E	01	W/R	-	-	-	goutl13_sel_u2d[4:0]					00
0E	02	W/R	-	-	-	goutl14_sel_u2d[4:0]					00
0E	03	W/R	-	-	-	goutl15_sel_u2d[4:0]					00
0E	04	W/R	-	-	-	goutl16_sel_u2d[4:0]					00

0E	05	W/R	-	-	-	goutl17_sel_u2d[4:0]	00
0E	06	W/R	-	-	-	goutl18_sel_u2d[4:0]	00
0E	07	W/R	-	-	-	goutl19_sel_u2d[4:0]	00
0E	08	W/R	-	-	-	goutl20_sel_u2d[4:0]	00
0E	09	W/R	-	-	-	goutl21_sel_u2d[4:0]	00
0E	0A	W/R	-	-	-	goutl22_sel_u2d[4:0]	00
0F	00	W/R	-	-	-	goutr1_sel_d2u[4:0]	00
0F	01	W/R	-	-	-	goutr2_sel_d2u[4:0]	00
0F	02	W/R	-	-	-	goutr3_sel_d2u[4:0]	00
0F	03	W/R	-	-	-	goutr4_sel_d2u[4:0]	00
0F	04	W/R	-	-	-	goutr5_sel_d2u[4:0]	00
0F	05	W/R	-	-	-	goutr6_sel_d2u[4:0]	00
0F	06	W/R	-	-	-	goutr7_sel_d2u[4:0]	00
0F	07	W/R	-	-	-	goutr8_sel_d2u[4:0]	00
0F	08	W/R	-	-	-	goutr9_sel_d2u[4:0]	00
0F	09	W/R	-	-	-	goutr10_sel_d2u[4:0]	00
0F	0A	W/R	-	-	-	goutr11_sel_d2u[4:0]	00
10	00	W/R	-	-	-	goutr12_sel_d2u[4:0]	00
10	01	W/R	-	-	-	goutr13_sel_d2u[4:0]	00
10	02	W/R	-	-	-	goutr14_sel_d2u[4:0]	00
10	03	W/R	-	-	-	goutr15_sel_d2u[4:0]	00
10	04	W/R	-	-	-	goutr16_sel_d2u[4:0]	00
10	05	W/R	-	-	-	goutr17_sel_d2u[4:0]	00
10	06	W/R	-	-	-	goutr18_sel_d2u[4:0]	00
10	07	W/R	-	-	-	goutr19_sel_d2u[4:0]	00
10	08	W/R	-	-	-	goutr20_sel_d2u[4:0]	00
10	09	W/R	-	-	-	goutr21_sel_d2u[4:0]	00
10	0A	W/R	-	-	-	goutr22_sel_d2u[4:0]	00
11	00	W/R	-	-	-	goutl1_sel_d2u[4:0]	00
11	01	W/R	-	-	-	goutl2_sel_d2u[4:0]	00
11	02	W/R	-	-	-	goutl3_sel_d2u[4:0]	00
11	03	W/R	-	-	-	goutl4_sel_d2u[4:0]	00
11	04	W/R	-	-	-	goutl5_sel_d2u[4:0]	00
11	05	W/R	-	-	-	goutl6_sel_d2u[4:0]	00
11	06	W/R	-	-	-	goutl7_sel_d2u[4:0]	00
11	07	W/R	-	-	-	goutl8_sel_d2u[4:0]	00
11	08	W/R	-	-	-	goutl9_sel_d2u[4:0]	00
11	09	W/R	-	-	-	goutl10_sel_d2u[4:0]	00
11	0A	W/R	-	-	-	goutl11_sel_d2u[4:0]	00
12	00	W/R	-	-	-	goutl12_sel_d2u[4:0]	00
12	01	W/R	-	-	-	goutl13_sel_d2u[4:0]	00

12	02	W/R	-	-	-	goutl14_sel_d2u[4:0]	00
12	03	W/R	-	-	-	goutl15_sel_d2u[4:0]	00
12	04	W/R	-	-	-	goutl16_sel_d2u[4:0]	00
12	05	W/R	-	-	-	goutl17_sel_d2u[4:0]	00
12	06	W/R	-	-	-	goutl18_sel_d2u[4:0]	00
12	07	W/R	-	-	-	goutl19_sel_d2u[4:0]	00
12	08	W/R	-	-	-	goutl20_sel_d2u[4:0]	00
12	09	W/R	-	-	-	goutl21_sel_d2u[4:0]	00
12	0A	W/R	-	-	-	goutl22_sel_d2u[4:0]	00
14	00	W/R	gckv_rise_o[7:0]				00
14	01	W/R	gckv_rise_e[7:0]				00
14	02	W/R	gckv_fall_o[7:0]				41
14	03	W/R	gckv_fall_e[7:0]				41

R00h_00

Address	Bit							
R00h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	stv_ckv_dis[2:0]			-	-
Default	0	0	0	0	0	1	0	1

R00h[4:2]: stv rising before ckv.

R00h[4:2]	Function	Note
000	stv rising before ckv 1 linne	-
001	stv rising before ckv 2 linne	Default
010	stv rising before ckv 3 linne	-
011	stv rising before ckv 4 linne	-
100	stv rising before ckv 5 linne	-
101	stv rising before ckv 6 linne	-
110	stv rising before ckv 7 linne	-
111	stv rising before ckv 8 linne	-

R0Bh_00~0A: right side goa flexible select at u2d.

Address	Bit							
R0Bh	D7	D6	D5	D4	D3	D2	D1	D0
00	-	-	-	goutr1_sel_u2d[4:0]				
01	-	-	-	goutr2_sel_u2d[4:0]				
02	-	-	-	goutr3_sel_u2d[4:0]				
03	-	-	-	goutr4_sel_u2d[4:0]				
04	-	-	-	goutr5_sel_u2d[4:0]				
05	-	-	-	goutr6_sel_u2d[4:0]				
06	-	-	-	goutr7_sel_u2d[4:0]				
07	-	-	-	goutr8_sel_u2d[4:0]				
08	-	-	-	goutr9_sel_u2d[4:0]				
09	-	-	-	goutr10_sel_u2d[4:0]				
0A	-	-	-	goutr11_sel_u2d[4:0]				
Default	0	0	0	0	0	0	0	0

R0Ch_00~0A: right side goa flexible select at u2d.

Address	Bit							
R0Ch	D7	D6	D5	D4	D3	D2	D1	D0
00	-	-	-	goutr12_sel_u2d[4:0]				
01	-	-	-	goutr13_sel_u2d[4:0]				
02	-	-	-	goutr14_sel_u2d[4:0]				
03	-	-	-	goutr15_sel_u2d[4:0]				
04	-	-	-	goutr16_sel_u2d[4:0]				
05	-	-	-	goutr17_sel_u2d[4:0]				
06	-	-	-	goutr18_sel_u2d[4:0]				
07	-	-	-	goutr19_sel_u2d[4:0]				
08	-	-	-	goutr20_sel_u2d[4:0]				
09	-	-	-	goutr21_sel_u2d[4:0]				
0A	-	-	-	goutr22_sel_u2d[4:0]				
Default	0	0	0	0	0	0	0	0

R0Dh_00~0A: left side goa flexible select at u2d.

Address	Bit							
R0Dh	D7	D6	D5	D4	D3	D2	D1	D0
00	-	-	-	goutl1_sel_u2d[4:0]				
01	-	-	-	goutl2_sel_u2d[4:0]				
02	-	-	-	goutl3_sel_u2d[4:0]				
03	-	-	-	goutl4_sel_u2d[4:0]				
04	-	-	-	goutl5_sel_u2d[4:0]				
05	-	-	-	goutl6_sel_u2d[4:0]				
06	-	-	-	goutl7_sel_u2d[4:0]				
07	-	-	-	goutl8_sel_u2d[4:0]				
08	-	-	-	goutl9_sel_u2d[4:0]				
09	-	-	-	goutl10_sel_u2d[4:0]				
0A	-	-	-	goutl11_sel_u2d[4:0]				
Default	0	0	0	0	0	0	0	0

R0Eh_00~0A: left side goa flexible select at u2d.

Address	Bit							
R0Eh	D7	D6	D5	D4	D3	D2	D1	D0
00	-	-	-	goutl12_sel_u2d[4:0]				
01	-	-	-	goutl13_sel_u2d[4:0]				
02	-	-	-	goutl14_sel_u2d[4:0]				
03	-	-	-	goutl15_sel_u2d[4:0]				
04	-	-	-	goutl16_sel_u2d[4:0]				
05	-	-	-	goutl17_sel_u2d[4:0]				
06	-	-	-	goutl18_sel_u2d[4:0]				
07	-	-	-	goutl19_sel_u2d[4:0]				
08	-	-	-	goutl20_sel_u2d[4:0]				
09	-	-	-	goutl21_sel_u2d[4:0]				
0A	-	-	-	goutl22_sel_u2d[4:0]				
Default	0	0	0	0	0	0	0	0

R0Fh_00~0A: right side goa flexible select at d2u.

Address	Bit							
R0Fh	D7	D6	D5	D4	D3	D2	D1	D0
00	-	-	-	goutr1_sel_du2[4:0]				
01	-	-	-	goutr2_sel_du2[4:0]				
02	-	-	-	goutr3_sel_du2[4:0]				
03	-	-	-	goutr4_sel_du2[4:0]				
04	-	-	-	goutr5_sel_d2u[4:0]				
05	-	-	-	goutr6_sel_d2u[4:0]				
06	-	-	-	goutr7_sel_d2u[4:0]				
07	-	-	-	goutr8_sel_d2u[4:0]				
08	-	-	-	goutr9_sel_d2u[4:0]				
09	-	-	-	goutr10_sel_d2u[4:0]				
0A	-	-	-	goutr11_sel_d2u[4:0]				
Default	0	0	0	0	0	0	0	0

R10h_00~0A: right side goa flexible select at d2u.

Address	Bit							
R10h	D7	D6	D5	D4	D3	D2	D1	D0
00	-	-	-	goutr12_sel_d2u[4:0]				
01	-	-	-	goutr13_sel_d2u[4:0]				
02	-	-	-	goutr14_sel_d2u[4:0]				
03	-	-	-	goutr15_sel_d2u[4:0]				
04	-	-	-	goutr16_sel_d2u[4:0]				
05	-	-	-	goutr17_sel_d2u[4:0]				
06	-	-	-	goutr18_sel_d2u[4:0]				
07	-	-	-	goutr19_sel_d2u[4:0]				
08	-	-	-	goutr20_sel_d2u[4:0]				
09	-	-	-	goutr21_sel_d2u[4:0]				
0A	-	-	-	goutr22_sel_d2u[4:0]				
Default	0	0	0	0	0	0	0	0

R11h_00~0A: left side goa flexible select at d2u.

Address	Bit							
R11h	D7	D6	D5	D4	D3	D2	D1	D0
00	-	-	-	goutl1_sel_du2[4:0]				
01	-	-	-	goutl2_sel_du2[4:0]				
02	-	-	-	goutl3_sel_du2[4:0]				
03	-	-	-	goutl4_sel_du2[4:0]				
04	-	-	-	goutl5_sel_d2u[4:0]				
05	-	-	-	goutl6_sel_d2u[4:0]				
06	-	-	-	goutl7_sel_d2u[4:0]				
07	-	-	-	goutl8_sel_d2u[4:0]				
08	-	-	-	goutl9_sel_d2u[4:0]				
09	-	-	-	goutl10_sel_d2u[4:0]				
0A	-	-	-	goutl11_sel_d2u[4:0]				
Default	0	0	0	0	0	0	0	0

R12h_00~0A: left side goa flexible select at d2u.

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
00	-	-	-	goutl12_sel_d2u[4:0]				
01	-	-	-	goutl13_sel_d2u[4:0]				
02	-	-	-	goutl14_sel_d2u[4:0]				
03	-	-	-	goutl15_sel_d2u[4:0]				
04	-	-	-	goutl16_sel_d2u[4:0]				
05	-	-	-	goutl17_sel_d2u[4:0]				
06	-	-	-	goutl18_sel_d2u[4:0]				
07	-	-	-	goutl19_sel_d2u[4:0]				
08	-	-	-	goutl20_sel_d2u[4:0]				
09	-	-	-	goutl21_sel_d2u[4:0]				
0A	-	-	-	goutl22_sel_d2u[4:0]				
Default	0	0	0	0	0	0	0	0

Flexible GIP output mapping table.

goutr/ln_sel_u2d[4:0] goutr/ln_sel_d2u[4:0] n=1~22	output	goutr/ln_sel_u2d[4:0] goutr/ln_sel_d2u[4:0] n=1~22	output
0	GND	10	FLCA
1	CSV	11	FLCB
2	CSV_N	12	Sub-FLCA
3	GAS	13	Sub-FLCB
4	GAS_N	14	GCH
5	RST1	15	GCL
6	CKV4	16	STV2
7	CKV3	17	RST2
8	CKV2	18	STV3
9	CKV1	19	STV4
A	STV1	1A	RST3
B	VGH	1B	RST4
C	VGL	1C	CKV5
D	VGL	1D	CKV6
E	VGL	1E	CKV7
F	VRSET	1F	CKV8

Note: GAS=VGL@Normal display ; GAS=VGH@GAS event.

14h_00~01[7:0]: ckv rising edge adjustment.

Address	Bit							
R14h	D7	D6	D5	D4	D3	D2	D1	D0
00	gckv_rise_o[7:0]							
01	gckv_rise_e[7:0]							
Default	0	0	0	0	0	0	0	0

R14h_00[7:0]: odd ckv rising edge fine tune.

R14h_00	Function	Note
00h	odd stv rising shift 0 clk	Default
01h	odd stv rising shift 1 clk	-
02h	odd stv rising shift 2 clk	-
:	:	-
41h	odd stv rising shift 65 clk	-
42h	odd stv rising shift 66 clk	-
:	:	-
FEh	odd stv rising shift 254 clk	-
FFh	odd stv rising shift 255 clk	-

R14h_01[7:0]: even ckv rising edge fine tune.

R14h_01	Function	Note
00h	odd stv rising shift 0 clk	Default
01h	odd stv rising shift 1 clk	-
02h	odd stv rising shift 2 clk	-
:	:	-
41h	odd stv rising shift 65 clk	-
42h	odd stv rising shift 66 clk	-
:	:	-
FEh	odd stv rising shift 254 clk	-
FFh	odd stv rising shift 255 clk	-

14h_02~03[7:0]: ckv falling edge adjustment.

Address	Bit							
R14h	D7	D6	D5	D4	D3	D2	D1	D0
02	gckv_fall_o[7:0]							
03	gckv_fall_e[7:0]							
Default	0	1	0	0	0	0	0	1

R14h_02[7:0]: odd ckv falling edge fine tune.

R14h_02	Function	Note
00h	odd stv rising shift 0 clk	-
01h	odd stv rising shift 1 clk	-
02h	odd stv rising shift 2 clk	-
:	:	-
41h	odd stv rising shift 65 clk	Default
42h	odd stv rising shift 66 clk	-
:	:	-
FEh	odd stv rising shift 254 clk	-
FFh	odd stv rising shift 255 clk	-

R14h_03[7:0]: even ckv falling edge fine tune.

R14h_03	Function	Note
00h	odd stv rising shift 0 clk	-
01h	odd stv rising shift 1 clk	-
02h	odd stv rising shift 2 clk	-
:	:	-
41h	odd stv rising shift 65 clk	Default
42h	odd stv rising shift 66 clk	-
:	:	-
FEh	odd stv rising shift 254 clk	-
FFh	odd stv rising shift 255 clk	-

11.5 Page 6 command

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
12	00	W/R	-	-	REG_GA_GSH255[5:0]						**3F**
12	01	W/R	-	-	REG_GA_GSH248[5:0]						**2E**
12	02	W/R	-	-	REG_GA_GSH236[5:0]						**28**
12	03	W/R	-	-	REG_GA_GSH220[5:0]						**20**
12	04	W/R	-	-	REG_GA_GSH200[5:0]						**12**
12	05	W/R	-	-	REG_GA_GSH172[5:0]						**02**
12	06	W/R	-	-	REG_GA_GSH144[5:0]						**1E**
12	07	W/R	-	-	REG_GA_GSH116[5:0]						**20**
12	08	W/R	-	-	REG_GA_GSH88[5:0]						**32**
12	09	W/R	-	-	REG_GA_GSH60[5:0]						**32**
12	0A	W/R	-	-	REG_GA_GSH32[5:0]						**28**
12	0B	W/R	-	-	REG_GA_GSH16[5:0]						**22**
12	0C	W/R	-	-	REG_GA_GSH8[5:0]						**1C**
12	0D	W/R	-	-	REG_GA_GSH0[5:0]						**00**
13	00	W/R	-	-	REG_GA_GSL255[5:0]						**3F**
13	01	W/R	-	-	REG_GA_GSL248[5:0]						**2E**
13	02	W/R	-	-	REG_GA_GSL236[5:0]						**28**
13	03	W/R	-	-	REG_GA_GSL220[5:0]						**20**
13	04	W/R	-	-	REG_GA_GSL200[5:0]						**12**
13	05	W/R	-	-	REG_GA_GSL172[5:0]						**02**
13	06	W/R	-	-	REG_GA_GSL144[5:0]						**1E**
13	07	W/R	-	-	REG_GA_GSL116[5:0]						**20**
13	08	W/R	-	-	REG_GA_GSL88[5:0]						**32**
13	09	W/R	-	-	REG_GA_GSL60[5:0]						**32**
13	0A	W/R	-	-	REG_GA_GSL32[5:0]						**28**
13	0B	W/R	-	-	REG_GA_GSL16[5:0]						**22**
13	0C	W/R	-	-	REG_GA_GSL8[5:0]						**1C**
13	0D	W/R	-	-	REG_GA_GSL0[5:0]						**00**

R12h_00

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH255[5:0]					
Default	0	0	1	1	1	1	1	1

R12h[5:0]: VP positive voltage(Normally black panel).

R12h[5:0]	Function	Note
3Eh	VP - 23mV	-
3Fh	VP	Default

R12h_01

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH248[5:0]					
Default	0	0	1	0	1	1	1	0

R12h[5:0]: Gray248 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
2Dh	Gray248 - 23mV	
2Eh	Gray248	Default
2Fh	Gray248 + 23mV	-

R12h_02

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH236[5:0]					
Default	0	0	1	0	1	0	0	0

R12h[5:0]: Gray236 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
27h	Gray236 - 23mV	
28h	Gray236	Default
29h	Gray236 + 23mV	-

R12h_03

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH220[5:0]					
Default	0	0	1	0	0	0	0	0

R12h[5:0]: Gray220 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
1Fh	Gray220 - 23mV	
20h	Gray220	Default
21h	Gray220 + 23mV	-

R12h_04

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH200[5:0]					
Default	0	0	0	1	0	0	1	0

R12h[5:0]: Gray200 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
11h	Gray200 - 23mV	
12h	Gray200	Default
13h	Gray200 + 23mV	-

R12h_05

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH172[5:0]					
Default	0	0	0	0	0	0	1	0

R12h[5:0]: Gray172 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
01h	Gray172 - 23mV	
02h	Gray172	Default
03h	Gray172 + 23mV	-

R12h_06

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH144[5:0]					
Default	0	0	0	1	1	1	1	0

R12h[5:0]: Gray144 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
1Dh	Gray144 - 23mV	
1Eh	Gray144	Default
1Fh	Gray144 + 23mV	-

R12h_07

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH116[5:0]					
Default	0	0	1	0	0	0	0	0

R12h[5:0]: Gray116 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
1Fh	Gray116 - 23mV	
20h	Gray116	Default
21h	Gray116 + 23mV	-

R12h_08

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH88[5:0]					
Default	0	0	1	1	0	0	1	0

R12h[5:0]: Gray88 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
31h	Gray88 - 23mV	
32h	Gray88	Default
33h	Gray88 + 23mV	-

R12h_09

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH60[5:0]					
Default	0	0	1	1	0	0	1	0

R12h[5:0]: Gray60 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
31h	Gray60 - 23mV	
32h	Gray60	Default
33h	Gray60 + 23mV	-

R12h_0A

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH32[5:0]					
Default	0	0	1	0	1	0	0	0

R12h[5:0]: Gray32 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
27h	Gray32 - 23mV	
28h	Gray32	Default
29h	Gray32 + 23mV	-

R12h_0B

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH16[5:0]					
Default	0	0	1	0	0	0	1	0

R12h[5:0]: Gray16 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
21h	Gray16 - 23mV	
22h	Gray16	Default
23h	Gray16 + 23mV	-

R12h_0C

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH8[5:0]					
Default	0	0	0	1	1	1	0	0

R12h[5:0]: Gray8 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
1Bh	Gray8 - 23mV	
1Ch	Gray8	Default
1Dh	Gray8 + 23mV	-

R12h_0D

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSH0[5:0]					
Default	0	0	0	0	0	0	0	0

R12h[5:0]: VP1 positive voltage(Normally black panel).

R12h[5:0]	Function	Note
00h	VP1	Default
01h	VP1 + 23mV	-

R13h_00

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL255[5:0]					
Default	0	0	1	1	1	1	1	1

R13h[5:0]: VN1 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
3Eh	VN1 + 23mV	-
3Fh	VN1	Default

R13h_01

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL248[5:0]					
Default	0	0	1	0	1	1	1	0

R13h[5:0]: Gray248 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
2Dh	Gray248 + 23mV	
2Eh	Gray248	Default
2Fh	Gray248 - 23mV	-

R13h_02

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL236[5:0]					
Default	0	0	1	0	1	0	0	0

R13h[5:0]: Gray236 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
27h	Gray236 + 23mV	
28h	Gray236	Default
29h	Gray236 - 23mV	-

R13h_03

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL220[5:0]					
Default	0	0	1	0	0	0	0	0

R13h[5:0]: Gray220 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
1Fh	Gray220 + 23mV	
20h	Gray220	Default
21h	Gray220 - 23mV	-

R13h_04

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL200[5:0]					
Default	0	0	0	1	0	0	1	0

R13h[5:0]: Gray200 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
11h	Gray200 + 23mV	
12h	Gray200	Default
13h	Gray200 - 23mV	-

R13h_05

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL172[5:0]					
Default	0	0	0	0	0	0	1	0

R13h[5:0]: Gray172 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
01h	Gray172 + 23mV	
02h	Gray172	Default
03h	Gray172 - 23mV	-

R13h_06

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL144[5:0]					
Default	0	0	0	1	1	1	1	0

R13h[5:0]: Gray144 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
1Dh	Gray144 + 23mV	
1Eh	Gray144	Default
1Fh	Gray144 - 23mV	-

R13h_07

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL116[5:0]					
Default	0	0	1	0	0	0	0	0

R13h[5:0]: Gray116 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
1Fh	Gray116 + 23mV	
20h	Gray116	Default
21h	Gray116 - 23mV	-

R13h_08

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL88[5:0]					
Default	0	0	1	1	0	0	1	0

R13h[5:0]: Gray88 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
31h	Gray88 + 23mV	
32h	Gray88	Default
33h	Gray88 - 23mV	-

R13h_09

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL60[5:0]					
Default	0	0	1	1	0	0	1	0

R13h[5:0]: Gray60 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
31h	Gray60 + 23mV	
32h	Gray60	Default
33h	Gray60 - 23mV	-

R13h_0A

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL32[5:0]					
Default	0	0	1	0	1	0	0	0

R13h[5:0]: Gray32 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
27h	Gray32 + 23mV	
28h	Gray32	Default
29h	Gray32 - 23mV	-

R13h_0B

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL16[5:0]					
Default	0	0	1	0	0	0	1	0

R13h[5:0]: Gray16 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
21h	Gray16 + 23mV	
22h	Gray16	Default
23h	Gray16 - 23mV	-

R13h_0C

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL8[5:0]					
Default	0	0	0	1	1	1	0	0

R13h[5:0]: Gray8 negative voltage(Normally black panel).

R13h[5:0]	Function	Note
1Bh	Gray8 + 23mV	
1Ch	Gray8	Default
1Dh	Gray8 - 23mV	-

R13h_0D

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	REG_GA_GSL0[5:0]					
Default	0	0	0	0	0	0	0	0

R13h[5:0]: VN negative voltage(Normally black panel).

R13h[5:0]	Function	Note
00h	VN	Default
01h	VN - 23mV	-

11.6 Page 7 command

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
0D	00	W/R	-	-	-	-	-	-	-	ulpslp11_check_enb	**00**

R0Dh_00

Address	Bit							
R0Dh	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	ulpslp11_check_enb
Default	0	0	0	0	0	0	0	0

R0Dh[0]: MIPI clk lane sequence check.

R00h[0]	Function	Note
0	enable	default
1	disable	-

11.7 Page 8 command

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
05	00	W/R		-	-	-	-	-	-	esd_rst_en	**00**
0C	00	W/R	-	-	-	-	-	-	esd_det_en	-	**18**
0D	00	W/R	-	-	-	-	-	-	analog_esd_det_en	-	**0C**

R05h_00

Address	Bit							
R05h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	esd_rst_en
Default	0	0	0	0	0	0	0	0

R05h[0]: ESD event trig IC reset function.

R05h[0]	Function	Note
0	disable	Default
1	enable	-

R0Ch_00

Address	Bit							
R0Ch	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	esd_det_en	-
Default	0	0	0	1	1	0	0	0

R0Ch[1]: ESD event detection

R0Ch[1]	Function	Note
0	disable	Default
1	enable	-

R0Dh_00

Address	Bit							
R0Dh	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	analog_esd_det_en	-
Default	0	0	0	0	1	1	0	0

R0Dh[1]: Analog ESD event detection

R0Dh[1]	Function	Note
0	disable	Default
1	enable	-

11.8 Page 9 command

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
17	00	R	-	-	index_reverse_vcom6	index_reverse_vcom5	index_reverse_vcom4	index_reverse_vcom3	index_reverse_vcom2	index_reverse_vcom1	**00**
1A	00	R	-	-	-	-	-	-	index_gamma2	index_gamma1	**00**
20	00	R	-	-	index_normal_vcom6	index_normal_vcom5	index_normal_vcom4	index_normal_vcom3	index_normal_vcom2	index_normal_vcom1	**00**

R17h_00

Address	Bit							
R17h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	index_reverse_vcom6	index_reverse_vcom5	index_reverse_vcom4	index_reverse_vcom3	index_reverse_vcom2	index_reverse_vcom1
Default	0	0	0	0	0	0	0	0

R17h[5:0]: Reverse Scan VCOM OTP number of times.

R17h[5:0]	Function	Note
00h	VCOM OTP 0 times	Default
01h	VCOM OTP 1 times	-
03h	VCOM OTP 2 times	-
07h	VCOM OTP 3 times	-
0Fh	VCOM OTP 4 times	-
1Fh	VCOM OTP 5 times	-
3Fh	VCOM OTP 6 times	-

R1Ah_00

Address	Bit							
R1Ah	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	index_gamma2	index_gamma1
Default	0	0	0	0	0	0	0	0

R1Ah[1:0]: Gamma OTP number of times.

R1Ah[1:0]	Function	Note
00h	Gamma OTP 0 times	Default
01h	Gamma OTP 1 times	-
03h	Gamma OTP 2 times	-

R20h_00

Address	Bit							
R20h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	index_normal_vcom6	index_normal_vcom5	index_normal_vcom4	index_normal_vcom3	index_normal_vcom2	index_normal_vcom1
Default	0	0	0	0	0	0	0	0

R20h[5:0]: Normal Scan VCOM OTP number of times.

R20h[5:0]	Function	Note
00h	VCOM OTP 0 times	Default
01h	VCOM OTP 1 times	-
03h	VCOM OTP 2 times	-
07h	VCOM OTP 3 times	-
0Fh	VCOM OTP 4 times	-
1Fh	VCOM OTP 5 times	-
3Fh	VCOM OTP 6 times	-

11.9 Page A command

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
01	00	W/R	sd_hz_col_t[3:0]				-	-	-	-	**27**
02	00	W/R	-	-	dummy	-		-	-	-	**6F**
03	00	W/R	-	-	-	-	-	sd_bias_sel_nd[2:0]			**12**
09	00	W/R	-	-	-	-	sd_lr_osw_nd[1:0]		-	-	**00**
0B	00	W/R	-	-	sd_slpin_opt[1:0]		-	-	-	-	**50**

R01h_00

Address	Bit							
R01h	D7	D6	D5	D4	D3	D2	D1	D0
Name	sd_hz_col_t				-	-	-	-
Default	0	0	1	0	0	1	1	1

R01h[7:4]: Source Hi-Z area.

R17h[5:0]	Function	Note
00h	200ns	-
01h	400ns	-
02h	600ns	Default
03h	800ns	-
04h	1000ns	-
05h	1200ns	-
06h	1400ns	-
07h	1600ns	-
08h	1800ns	-
09h	2000ns	-
0Ah-0Fh	reserved	-

R02h_00

Address	Bit							
R02h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	dummy	-	-	-	-	-
Default	0	1	1	0	1	1	1	1

R02h[5]: dummy function.

R02h[5]	Function	Note
0	dummy function	-
1	dummy function	Default

R03h_00

Address	Bit							
R03h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	sd_bias_sel_nd[2:0]		
Default	0	0	0	1	0	0	1	0

R03h[2:0]: Source bias current selection.

R03h[20]	Function	Note
00h	0.8uA	-
01h	1.6uA	-
02h	2.4uA	Default
03h	3.2uA	-
04h	4.0uA	-
05h	4.8uA	-
06h	5.6uA	-
07h	7.2uA	-

R09h_00

Address	Bit							
R09h	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	sd_lr_osw_nd[1:0]		-	-
Default	0	0		0	0		0	0

R09h[3:2]: Source output equivalent resistance.

R09h[3:2]	Function	Note
00h	5K ohm	Default
01h	1.3K ohm	-
10h	400 ohm	-
11h	300 0hm	-

R0Bh_00

Address	Bit							
R0Bh	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	sd_slpin_opt[1:0]		-	-	-	-
Default	0	1	0	1	0	0	0	0

R0Bh[5:4]: Source behavior in Standby mode.

R0Bh[5:4]	Function	Note
00h	VMID	-
01h	charge share	Default
10h	reserved	-
11h	reserved	-

11.10 Page D command

X Address	Y Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
0D	00	W/R	-	-	-	-	GAS_VDD	-	-	-	**04**
10	00	W/R	VGMPH[7:0]								**0C**
11	00	W/R	VGMPL[7:0]								**0C**
12	00	W/R	VGMNH[7:0]								**0C**
13	00	W/R	VGMNL[7:0]								**0C**

R0Dh_00

Address	Bit							
R0Dh	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-			GAS_VDD	-	-	-
Default	0	0	0	0	0	1	0	0

R0Dh[3]: GAS_VDD detection voltage

R0Dh[3]	Function	Note
0	1.5V	Default
1	2.2V	-

R10h_00

Address	Bit							
R10h	D7	D6	D5	D4	D3	D2	D1	D0
Name	VGMPH [7:0]							
Default	0	0	0	0	1	1	0	0

R10h[7:0]: Gamma positive high level reference voltage.

R10h[7:0]	Function	Note
0Bh	AVDD - (15AVDD/800)	-
0Ch	AVDD – (16AVDD/800)	Default
0Dh	AVDD – (17AVDD/800)	-
0Eh	AVDD – (18AVDD/800)	-
0Fh	AVDD – (19AVDD/800)	-
:	:	-
1Eh	AVDD – (34AVDD/800)	-
1Fh	AVDD – (35AVDD/800)	-

Operating voltage limits : AVDD – VGMPH ≥ 0.2V.

R11h_00

Address	Bit							
R11h	D7	D6	D5	D4	D3	D2	D1	D0
Name	VGMPL [7:0]							
Default	0	0	0	0	1	1	0	0

R11h[7:0]: Gamma positive low level reference voltage.

R11h[7:0]	Function	Note
0Bh	415AVDD/800	-
0Ch	416AVDD/800	Default
0Dh	417AVDD/800	-
0Eh	418AVDD/800	-
0Fh	419AVDD/800	-
:	:	-
1Eh	434AVDD/800	-
1Fh	435AVDD/800	-

Operating voltage limits : VGMPL – VMID ≥ 0.2V.

R12h_00

Address	Bit							
R12h	D7	D6	D5	D4	D3	D2	D1	D0
Name	VGMNH [7:0]							
Default	0	0	0	0	1	1	0	0

R12h[7:0]: Gamma negative high level reference voltage.

R12h[7:0]	Function	Note
0Bh	AVDD – (415AVDD/800)	-
0Ch	AVDD – (416AVDD/800)	Default
0Dh	AVDD – (417AVDD/800)	-
0Eh	AVDD – (418AVDD/800)	-
0Fh	AVDD – (419AVDD/800)	-
:	:	-
1Eh	AVDD – (434AVDD/800)	-
1Fh	AVDD – (435AVDD/800)	-

Operating voltage limits : VMID – VGMNH ≥ 0.2V.

R13h_00

Address	Bit							
R13h	D7	D6	D5	D4	D3	D2	D1	D0
Name	VGMNL[7:0]							
Default	0	0	0	0	1	1	0	0

R13h[7:0]: Gamma negative low level reference voltage.

R13h[7:0]	Function	Note
0Bh	15AVDD/800	-
0Ch	16AVDD/800	Default
0Dh	17AVDD/800	-
0Eh	18AVDD/800	-
0Fh	19AVDD/800	-
:	:	-
1Eh	34AVDD/800	-
1Fh	35AVDD/800	-

Operating voltage limits : VGMNL – GND ≥ 0.2V.

12. DC CHARACTERISTICS

12.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Supply power voltage	VDD	-0.30	-	3.96	V	
IO supply voltage	VDDIO	-0.30		3.96	V	
AVDD voltage	AVDD	-0.30	-	12	V	
VGH voltage	VGH	-0.30	-	VGL+32V	V	
VGL voltage	VGL	VGH-32V	-	0.30	V	
VMID voltage	VMID	-0.30	-	6.6	V	
VCOM voltage	VCOM_OP	-0.30	-	5.43	V	
VOTP **(OTP power)**	VOTP	-	-	9	V	
Operating Temperature	T_{OPR}	-30	-	+85	℃	
Storage temperature	T_{STG}	-55	-	125	℃	

12.2 Typical operating condition

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Supply power voltage	VDD	1.71	1.8	1.89	V	MIPI mode condition1
I/O power voltage	VDDIO	1.71	1.8	1.89	V	
Supply power voltage	VDD	2.8	3.3	3.6	V	TTL mode condition LVDS mode condition MIPI mode condition2
I/O power voltage	VDDIO	2.8	3.3	3.6	V	
AVDD voltage	AVDD	9	-	12	V	
VGH voltage	VGH	15	18	20	V	
VGL voltage	VGL	-12	-8	-6	V	
VMID voltage	VMID	4.5	5	6.0	V	
VMID_OP voltage	VMID_OP	4.5	5	6.0	V	
VQHO voltage	VQHO	-	0.75AVDD	-	V	
VQLO voltage	VQLO	-	0.25AVDD	-	V	
VCOM voltage	VCOM_OP	2.7	3.8	4.94	V	
VOTP	VOTP	8.0	8.25	8.5	V	
Low level input voltage	V_{IL}	VSS	-	0.2xVDD	V	
High level input voltage	V_{IH}	0.8xVDD	-	VDD	V	
Low level output voltage	V_{OL}	VSS	-	0.1xVDD	V	
High level output voltage	V_{OH}	0.9xVDD	-	VDD	V	

12.3 VDD power on slew time

Be sure that VDD input can't result automatically in power on sequence.

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
VDD power on skew time	T_{POR}	From 0V to 1.35V	0.1	-	5	ms

12.4 Timing requirements for RESX

When RESX of the reset pin equals to Low, it will be in the condition of reset.
When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

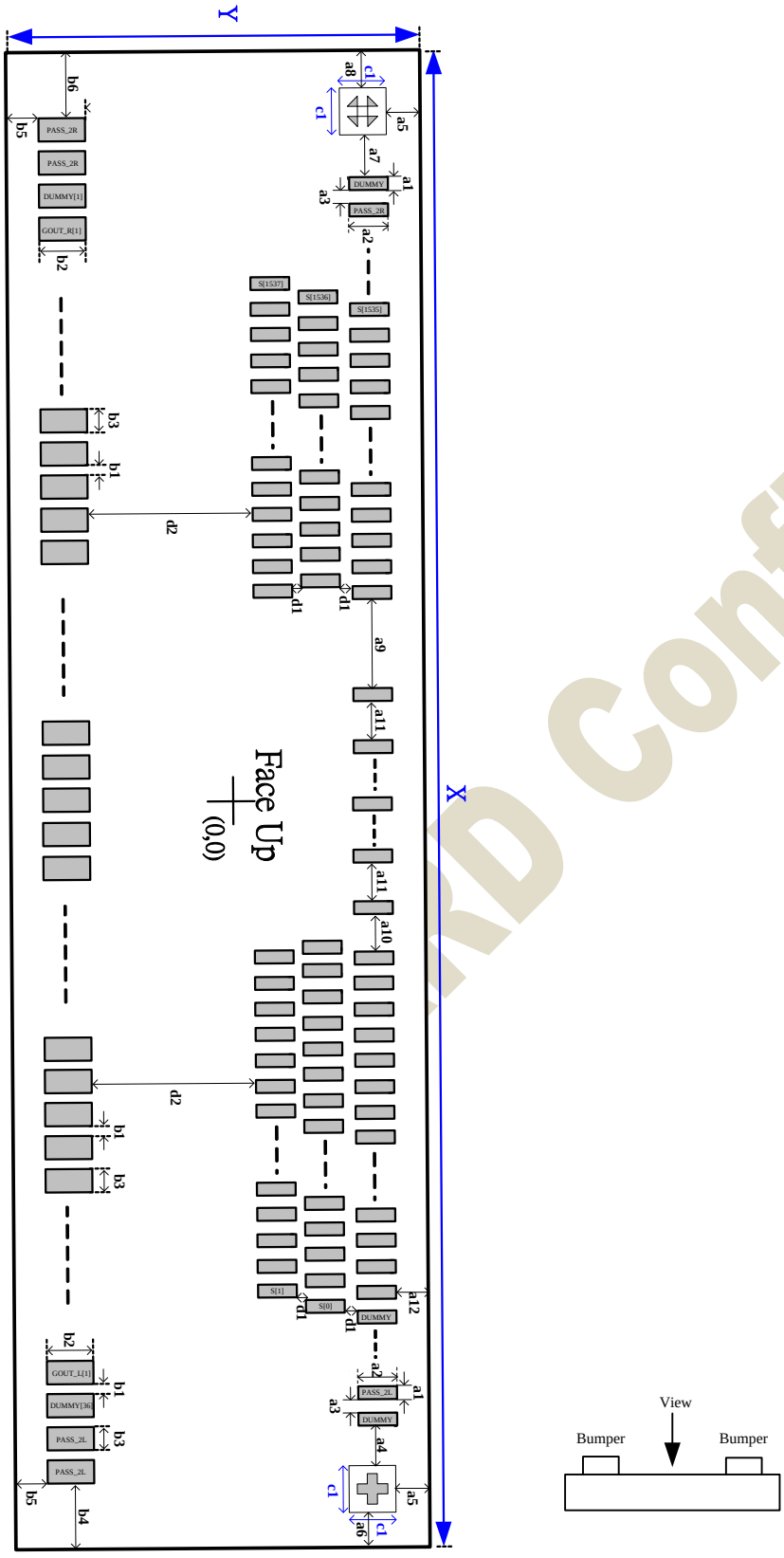
The closed interval of Low can be shown as the following.

(Test condition: VDD=1.71V to 1.89V / 2.8V to 3.6V , VSS=0V, T_A=-30 ~+85)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		6	-	-	µs

13. CHIP INFORMATION

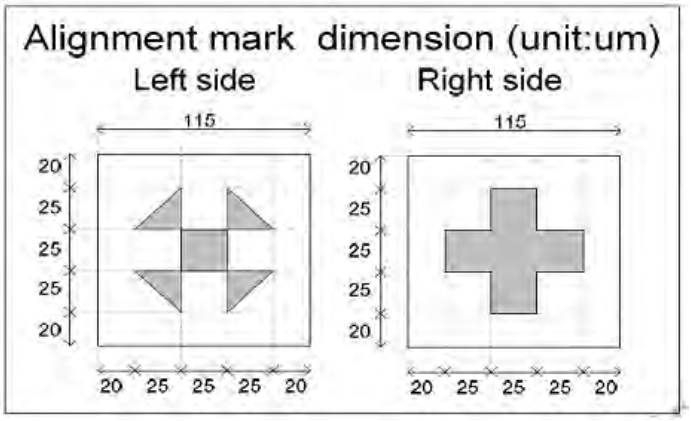
13.1 Chip outline dimensions



symbol	Dimension (um)	symbol	Dimension (um)
a1	18	b2	100
a2	65	b3	30
a3	18	b4	60
a4	240	b5	15
a5	22	b6	60
a6	22	c1	115
a7	163	d1	25
a8	22	d2	422.5
a9	135	X	28500
a10	58	Y	800
a11	54		
a12	17.5		
b1	15		

Table: Chip Outline Dimension (No Scribe Line)

13.2 Alignment mark



Alignment Mark

13.3 Pad Coordinate

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1	PASS2_R	-14175	-335	30x100	57	VGH_R	-11655	-335	30x100
2	PASS2_R	-14130	-335	30x100	58	VGH_R	-11610	-335	30x100
3	DUMMY[1]	-14085	-335	30x100	59	VGH_R	-11565	-335	30x100
4	GOUT_R[1]	-14040	-335	30x100	60	Shielding_VSSA	-11520	-335	30x100
5	GOUT_R[1]	-13995	-335	30x100	61	PASS1_R	-11475	-335	30x100
6	GOUT_R[2]	-13950	-335	30x100	62	PASS1_R	-11430	-335	30x100
7	GOUT_R[2]	-13905	-335	30x100	63	Shielding_VSSA	-11385	-335	30x100
8	GOUT_R[3]	-13860	-335	30x100	64	Shielding_VSSA	-11340	-335	30x100
9	GOUT_R[3]	-13815	-335	30x100	65	TEST_I[0]	-11295	-335	30x100
10	GOUT_R[4]	-13770	-335	30x100	66	TEST_I[1]	-11250	-335	30x100
11	GOUT_R[4]	-13725	-335	30x100	67	TEST_I[2]	-11205	-335	30x100
12	GOUT_R[5]	-13680	-335	30x100	68	TEST_I[3]	-11160	-335	30x100
13	GOUT_R[5]	-13635	-335	30x100	69	TEST_I[4]	-11115	-335	30x100
14	GOUT_R[6]	-13590	-335	30x100	70	TEST_I[5]	-11070	-335	30x100
15	GOUT_R[6]	-13545	-335	30x100	71	TEST_I[6]	-11025	-335	30x100
16	GOUT_R[7]	-13500	-335	30x100	72	TEST_I[7]	-10980	-335	30x100
17	GOUT_R[7]	-13455	-335	30x100	73	TEST_I[8]	-10935	-335	30x100
18	GOUT_R[8]	-13410	-335	30x100	74	TEST_I[9]	-10890	-335	30x100
19	GOUT_R[8]	-13365	-335	30x100	75	TEST_I[10]	-10845	-335	30x100
20	GOUT_R[9]	-13320	-335	30x100	76	TEST_I[11]	-10800	-335	30x100
21	GOUT_R[9]	-13275	-335	30x100	77	TEST_I[12]	-10755	-335	30x100
22	GOUT_R[10]	-13230	-335	30x100	78	TEST_I[13]	-10710	-335	30x100
23	GOUT_R[10]	-13185	-335	30x100	79	TEST_I[14]	-10665	-335	30x100
24	GOUT_R[11]	-13140	-335	30x100	80	TEST_I[15]	-10620	-335	30x100
25	GOUT_R[11]	-13095	-335	30x100	81	TEST_I[16]	-10575	-335	30x100
26	GOUT_R[12]	-13050	-335	30x100	82	TEST_I[17]	-10530	-335	30x100
27	GOUT_R[12]	-13005	-335	30x100	83	TEST_I[18]	-10485	-335	30x100
28	GOUT_R[13]	-12960	-335	30x100	84	TEST_I[19]	-10440	-335	30x100
29	GOUT_R[13]	-12915	-335	30x100	85	TEST_I[20]	-10395	-335	30x100
30	GOUT_R[14]	-12870	-335	30x100	86	TEST_I[21]	-10350	-335	30x100
31	GOUT_R[14]	-12825	-335	30x100	87	TEST_I[22]	-10305	-335	30x100
32	GOUT_R[15]	-12780	-335	30x100	88	VDD18V_BPS	-10260	-335	30x100
33	GOUT_R[15]	-12735	-335	30x100	89	Shielding_VSSA	-10215	-335	30x100
34	GOUT_R[16]	-12690	-335	30x100	90	Shielding_VSSA	-10170	-335	30x100
35	GOUT_R[16]	-12645	-335	30x100	91	Shielding_VSSA	-10125	-335	30x100
36	GOUT_R[17]	-12600	-335	30x100	92	Shielding_VSSA	-10080	-335	30x100
37	GOUT_R[17]	-12555	-335	30x100	93	Shielding_VSSA	-10035	-335	30x100
38	GOUT_R[18]	-12510	-335	30x100	94	Shielding_VSSA	-9990	-335	30x100
39	GOUT_R[18]	-12465	-335	30x100	95	Shielding_VSSA	-9945	-335	30x100
40	GOUT_R[19]	-12420	-335	30x100	96	Shielding_VSSA	-9900	-335	30x100
41	GOUT_R[19]	-12375	-335	30x100	97	Shielding_VSSA	-9855	-335	30x100
42	GOUT_R[20]	-12330	-335	30x100	98	VQLI_R	-9810	-335	30x100
43	GOUT_R[20]	-12285	-335	30x100	99	VQLI_R	-9765	-335	30x100
44	GOUT_R[21]	-12240	-335	30x100	100	VQHI_R	-9720	-335	30x100
45	GOUT_R[21]	-12195	-335	30x100	101	VQHI_R	-9675	-335	30x100
46	GOUT_R[22]	-12150	-335	30x100	102	Shielding_VSSA	-9630	-335	30x100
47	GOUT_R[22]	-12105	-335	30x100	103	Shielding_VSSA	-9585	-335	30x100
48	VGL	-12060	-335	30x100	104	Shielding_VSSA	-9540	-335	30x100
49	VGL	-12015	-335	30x100	105	Shielding_VSSA	-9495	-335	30x100
50	VGL	-11970	-335	30x100	106	Shielding_VSSA	-9450	-335	30x100
51	VGL	-11925	-335	30x100	107	Shielding_VSSA	-9405	-335	30x100
52	VGL	-11880	-335	30x100	108	Shielding_VSSA	-9360	-335	30x100
53	VGL	-11835	-335	30x100	109	Shielding_VSSA	-9315	-335	30x100
54	VGH_R	-11790	-335	30x100	110	Shielding_VSSA	-9270	-335	30x100
55	VGH_R	-11745	-335	30x100	111	VSSA	-9225	-335	30x100
56	VGH_R	-11700	-335	30x100	112	VSSA	-9180	-335	30X100

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
113	VSSA	-9135	-335	30x100	169	Shielding_VSSA	-6615	-335	30x100
114	VSSA	-9090	-335	30x100	170	Shielding_VSSA	-6570	-335	30x100
115	VSSA	-9045	-335	30x100	171	Shielding_VSSA	-6525	-335	30x100
116	VSSA	-9000	-335	30x100	172	Shielding_VSSA	-6480	-335	30x100
117	VMID_R[1]	-8955	-335	30x100	173	Shielding_VSSA	-6435	-335	30x100
118	VMID_R[1]	-8910	-335	30x100	174	Shielding_VSSA	-6390	-335	30x100
119	VMID_R[1]	-8865	-335	30x100	175	Shielding_VSSA	-6345	-335	30x100
120	VMID_R[1]	-8820	-335	30x100	176	Shielding_VSSA	-6300	-335	30x100
121	VMID_R[1]	-8775	-335	30x100	177	TEST_VDD_O[1]	-6255	-335	30x100
122	VMID_R[1]	-8730	-335	30x100	178	TEST_VDD_O[2]	-6210	-335	30x100
123	AVDD	-8685	-335	30x100	179	TEST_VDD_O[3]	-6165	-335	30x100
124	AVDD	-8640	-335	30x100	180	VPP_GEN	-6120	-335	30x100
125	AVDD	-8595	-335	30x100	181	VPP_GEN	-6075	-335	30x100
126	AVDD	-8550	-335	30x100	182	VOTP	-6030	-335	30x100
127	AVDD	-8505	-335	30x100	183	VOTP	-5985	-335	30x100
128	AVDD	-8460	-335	30x100	184	Shielding_VSSA	-5940	-335	30x100
129	VSS	-8415	-335	30x100	185	Shielding_VSSA	-5895	-335	30x100
130	VSS	-8370	-335	30x100	186	Shielding_VSSA	-5850	-335	30x100
131	VSS	-8325	-335	30x100	187	Shielding_VSSA	-5805	-335	30x100
132	VSS	-8280	-335	30x100	188	Shielding_VSSA	-5760	-335	30x100
133	VSS	-8235	-335	30x100	189	Shielding_VSSA	-5715	-335	30x100
134	VSS	-8190	-335	30x100	190	Shielding_VSSA	-5670	-335	30x100
135	TEST_O[0]	-8145	-335	30x100	191	Shielding_VSSA	-5625	-335	30x100
136	TEST_O[1]	-8100	-335	30x100	192	Shielding_VSSA	-5580	-335	30x100
137	TEST_O[2]	-8055	-335	30x100	193	Shielding_VSSA	-5535	-335	30x100
138	TEST_O[3]	-8010	-335	30x100	194	Shielding_VSSA	-5490	-335	30x100
139	TEST_O[4]	-7965	-335	30x100	195	Shielding_VSSA	-5445	-335	30x100
140	TEST_O[5]	-7920	-335	30x100	196	VSSA	-5400	-335	30x100
141	TEST_O[6]	-7875	-335	30x100	197	VSSA	-5355	-335	30x100
142	TEST_O[7]	-7830	-335	30x100	198	VSSA	-5310	-335	30x100
143	TEST_O[8]	-7785	-335	30x100	199	VSSA	-5265	-335	30x100
144	TEST_O[9]	-7740	-335	30x100	200	VSSA	-5220	-335	30x100
145	TEST_O[10]	-7695	-335	30x100	201	VSSA	-5175	-335	30x100
146	TEST_O[11]	-7650	-335	30x100	202	VMID_R[0]	-5130	-335	30x100
147	TEST_O[12]	-7605	-335	30x100	203	VMID_R[0]	-5085	-335	30x100
148	TEST_O[13]	-7560	-335	30x100	204	VMID_R[0]	-5040	-335	30x100
149	TEST_O[14]	-7515	-335	30x100	205	VMID_R[0]	-4995	-335	30x100
150	TEST_O[15]	-7470	-335	30x100	206	VMID_R[0]	-4950	-335	30x100
151	Shielding_VSSA	-7425	-335	30x100	207	VMID_R[0]	-4905	-335	30x100
152	TEST_HV_I[0]	-7380	-335	30x100	208	AVDD	-4860	-335	30x100
153	TEST_HV_I[1]	-7335	-335	30x100	209	AVDD	-4815	-335	30x100
154	TEST_MV_I[0]	-7290	-335	30x100	210	AVDD	-4770	-335	30x100
155	TEST_MV_I[1]	-7245	-335	30x100	211	AVDD	-4725	-335	30x100
156	Shielding_VSSA	-7200	-335	30x100	212	AVDD	-4680	-335	30x100
157	TEST_VDD_I[0]	-7155	-335	30x100	213	AVDD	-4635	-335	30x100
158	Shielding_VSSA	-7110	-335	30x100	214	VSS	-4590	-335	30x100
159	Shielding_VSSA	-7065	-335	30x100	215	VSS	-4545	-335	30x100
160	Shielding_VSSA	-7020	-335	30x100	216	VSS	-4500	-335	30x100
161	Shielding_VSSA	-6975	-335	30x100	217	VSS	-4455	-335	30x100
162	Shielding_VSSA	-6930	-335	30x100	218	VSS	-4410	-335	30x100
163	Shielding_VSSA	-6885	-335	30x100	219	VSS	-4365	-335	30x100
164	Shielding_VSSA	-6840	-335	30x100	220	VDD_15V	-4320	-335	30x100
165	Shielding_VSSA	-6795	-335	30x100	221	VDD_15V	-4275	-335	30x100
166	Shielding_VSSA	-6750	-335	30x100	222	VDD_15V	-4230	-335	30x100
167	Shielding_VSSA	-6705	-335	30x100	223	VDD_15V	-4185	-335	30x100
168	Shielding_VSSA	-6660	-335	30x100	224	VDD_15V	-4140	-335	30x100

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
225	VDD_15V	-4095	-335	30x100	281	CKN	-1575	-335	30x100
226	VDD_R	-4050	-335	30x100	282	CKN	-1530	-335	30x100
227	VDD_R	-4005	-335	30x100	283	CKN	-1485	-335	30x100
228	VDD_R	-3960	-335	30x100	284	CKN	-1440	-335	30x100
229	VDD_R	-3915	-335	30x100	285	CKN	-1395	-335	30x100
230	VDD_R	-3870	-335	30x100	286	VSS_IF	-1350	-335	30x100
231	VDD_R	-3825	-335	30x100	287	DP[2]	-1305	-335	30x100
232	VDD_15V_IF	-3780	-335	30x100	288	DP[2]	-1260	-335	30x100
233	VDD_15V_IF	-3735	-335	30x100	289	DP[2]	-1215	-335	30x100
234	VDD_15V_IF	-3690	-335	30x100	290	DP[2]	-1170	-335	30x100
235	VDD_15V_IF	-3645	-335	30x100	291	DP[2]	-1125	-335	30x100
236	VDD_15V_IF	-3600	-335	30x100	292	DP[2]	-1080	-335	30x100
237	VDD_15V_IF	-3555	-335	30x100	293	DN[2]	-1035	-335	30x100
238	VDD_12V_IF	-3510	-335	30x100	294	DN[2]	-990	-335	30x100
239	VDD_12V_IF	-3465	-335	30x100	295	DN[2]	-945	-335	30x100
240	VSS_IF	-3420	-335	30x100	296	DN[2]	-900	-335	30x100
241	VSS_IF	-3375	-335	30x100	297	DN[2]	-855	-335	30x100
242	VSS_IF	-3330	-335	30x100	298	DN[2]	-810	-335	30x100
243	VSS_IF	-3285	-335	30x100	299	VSS_IF	-765	-335	30x100
244	VSS_IF	-3240	-335	30x100	300	DP[3]	-720	-335	30x100
245	VSS_IF	-3195	-335	30x100	301	DP[3]	-675	-335	30x100
246	T_IRX	-3150	-335	30x100	302	DP[3]	-630	-335	30x100
247	VSS_IF	-3105	-335	30x100	303	DP[3]	-585	-335	30x100
248	DP[0]	-3060	-335	30x100	304	DP[3]	-540	-335	30x100
249	DP[0]	-3015	-335	30x100	305	DP[3]	-495	-335	30x100
250	DP[0]	-2970	-335	30x100	306	DN[3]	-450	-335	30x100
251	DP[0]	-2925	-335	30x100	307	DN[3]	-405	-335	30x100
252	DP[0]	-2880	-335	30x100	308	DN[3]	-360	-335	30x100
253	DP[0]	-2835	-335	30x100	309	DN[3]	-315	-335	30x100
254	DN[0]	-2790	-335	30x100	310	DN[3]	-270	-335	30x100
255	DN[0]	-2745	-335	30x100	311	DN[3]	-225	-335	30x100
256	DN[0]	-2700	-335	30x100	312	VSS_IF	-180	-335	30x100
257	DN[0]	-2655	-335	30x100	313	VSS_IF	-135	-335	30x100
258	DN[0]	-2610	-335	30x100	314	VDD_15V_IF	-90	-335	30x100
259	DN[0]	-2565	-335	30x100	315	VDD_15V_IF	-45	-335	30x100
260	VSS_IF	-2520	-335	30x100	316	VDDIO	0	-335	30x100
261	DP[1]	-2475	-335	30x100	317	VDDIO	45	-335	30x100
262	DP[1]	-2430	-335	30x100	318	VSS	90	-335	30x100
263	DP[1]	-2385	-335	30x100	319	VSS	135	-335	30x100
264	DP[1]	-2340	-335	30x100	320	VSD	180	-335	30x100
265	DP[1]	-2295	-335	30x100	321	VSD	225	-335	30x100
266	DP[1]	-2250	-335	30x100	322	VSS	270	-335	30x100
267	DN[1]	-2205	-335	30x100	323	HSD	315	-335	30x100
268	DN[1]	-2160	-335	30x100	324	HSD	360	-335	30x100
269	DN[1]	-2115	-335	30x100	325	VSS	405	-335	30x100
270	DN[1]	-2070	-335	30x100	326	DEN	450	-335	30x100
271	DN[1]	-2025	-335	30x100	327	DEN	495	-335	30x100
272	DN[1]	-1980	-335	30x100	328	VSS	540	-335	30x100
273	VSS_IF	-1935	-335	30x100	329	CLKIN	585	-335	30x100
274	CKP	-1890	-335	30x100	330	CLKIN	630	-335	30x100
275	CKP	-1845	-335	30x100	331	VSS	675	-335	30x100
276	CKP	-1800	-335	30x100	332	DB[7]	720	-335	30x100
277	CKP	-1755	-335	30x100	333	DB[7]	765	-335	30x100
278	CKP	-1710	-335	30x100	334	DB[6]	810	-335	30x100
279	CKP	-1665	-335	30x100	335	DB[6]	855	-335	30x100
280	CKN	-1620	-335	30x100	336	VSS	900	-335	30x100

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
337	DB[5]	945	-335	30x100	393	VDDIO	3465	-335	30x100
338	DB[5]	990	-335	30x100	394	VDDIO	3510	-335	30x100
339	DB[4]	1035	-335	30x100	395	VDDIO	3555	-335	30x100
340	DB[4]	1080	-335	30x100	396	VSS	3600	-335	30x100
341	VSS	1125	-335	30x100	397	VSS	3645	-335	30x100
342	DB[3]	1170	-335	30x100	398	VSS	3690	-335	30x100
343	DB[3]	1215	-335	30x100	399	VSS	3735	-335	30x100
344	DB[2]	1260	-335	30x100	400	VSS	3780	-335	30x100
345	DB[2]	1305	-335	30x100	401	VSS	3825	-335	30x100
346	VSS	1350	-335	30x100	402	VDD_15V	3870	-335	30x100
347	DB[1]	1395	-335	30x100	403	VDD_15V	3915	-335	30x100
348	DB[1]	1440	-335	30x100	404	VDD_15V	3960	-335	30x100
349	DB[0]	1485	-335	30x100	405	VDD_15V	4005	-335	30x100
350	DB[0]	1530	-335	30x100	406	VDD_L	4050	-335	30x100
351	VSS	1575	-335	30x100	407	VDD_L	4095	-335	30x100
352	DG[7]	1620	-335	30x100	408	VDD_L	4140	-335	30x100
353	DG[7]	1665	-335	30x100	409	VDD_L	4185	-335	30x100
354	DG[6]	1710	-335	30x100	410	AVDD	4230	-335	30x100
355	DG[6]	1755	-335	30x100	411	AVDD	4275	-335	30x100
356	VSS	1800	-335	30x100	412	AVDD	4320	-335	30x100
357	DG[5]	1845	-335	30x100	413	AVDD	4365	-335	30x100
358	DG[5]	1890	-335	30x100	414	AVDD	4410	-335	30x100
359	DG[4]	1935	-335	30x100	415	AVDD	4455	-335	30x100
360	DG[4]	1980	-335	30x100	416	VMID_L[0]	4500	-335	30x100
361	VSS	2025	-335	30x100	417	VMID_L[0]	4545	-335	30x100
362	DG[3]	2070	-335	30x100	418	VMID_L[0]	4590	-335	30x100
363	DG[3]	2115	-335	30x100	419	VMID_L[0]	4635	-335	30x100
364	DG[2]	2160	-335	30x100	420	VMID_L[0]	4680	-335	30x100
365	DG[2]	2205	-335	30x100	421	VMID_L[0]	4725	-335	30x100
366	VSS	2250	-335	30x100	422	VSSA	4770	-335	30x100
367	DG[1]	2295	-335	30x100	423	VSSA	4815	-335	30x100
368	DG[1]	2340	-335	30x100	424	VSSA	4860	-335	30x100
369	DG[0]	2385	-335	30x100	425	VSSA	4905	-335	30x100
370	DG[0]	2430	-335	30x100	426	VSSA	4950	-335	30x100
371	VSS	2475	-335	30x100	427	VSSA	4995	-335	30x100
372	DR[7]	2520	-335	30x100	428	Shielding_VSSA	5040	-335	30x100
373	DR[7]	2565	-335	30x100	429	Shielding_VSSA	5085	-335	30x100
374	DR[6]	2610	-335	30x100	430	TEST_MV_O[0]	5130	-335	30x100
375	DR[6]	2655	-335	30x100	431	TEST_MV_O[1]	5175	-335	30x100
376	VSS	2700	-335	30x100	432	Shielding_VSSA	5220	-335	30x100
377	DR[5]	2745	-335	30x100	433	Shielding_VSSA	5265	-335	30x100
378	DR[5]	2790	-335	30x100	434	Shielding_VSSA	5310	-335	30x100
379	DR[4]	2835	-335	30x100	435	Shielding_VSSA	5355	-335	30x100
380	DR[4]	2880	-335	30x100	436	Shielding_VSSA	5400	-335	30x100
381	VSS	2925	-335	30x100	437	Shielding_VSSA	5445	-335	30x100
382	DR[3]	2970	-335	30x100	438	Shielding_VSSA	5490	-335	30x100
383	DR[3]	3015	-335	30x100	439	Shielding_VSSA	5535	-335	30x100
384	DR[2]	3060	-335	30x100	440	Shielding_VSSA	5580	-335	30x100
385	DR[2]	3105	-335	30x100	441	Shielding_VSSA	5625	-335	30x100
386	VSS	3150	-335	30x100	442	Shielding_VSSA	5670	-335	30x100
387	DR[1]	3195	-335	30x100	443	Shielding_VSSA	5715	-335	30x100
388	DR[1]	3240	-335	30x100	444	Shielding_VSSA	5760	-335	30x100
389	DR[0]	3285	-335	30x100	445	Shielding_VSSA	5805	-335	30x100
390	DR[0]	3330	-335	30x100	446	TEST_HV_O[0]	5850	-335	30x100
391	VSS	3375	-335	30x100	447	TEST_HV_O[1]	5895	-335	30x100
392	VSS	3420	-335	30x100	448	Shielding_VSSA	5940	-335	30x100

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
449	Shielding_VSSA	5985	-335	30x100	505	VMIDOP_EN	8505	-335	30x100
450	Shielding_VSSA	6030	-335	30x100	506	Shielding_VSSA	8550	-335	30x100
451	Shielding_VSSA	6075	-335	30x100	507	VQLI_L	8595	-335	30x100
452	SCL_I2C	6120	-335	30x100	508	VQLI_L	8640	-335	30x100
453	SCL_I2C	6165	-335	30x100	509	VQHI_L	8685	-335	30x100
454	SDA_I2C	6210	-335	30x100	510	VQHI_L	8730	-335	30x100
455	SDA_I2C	6255	-335	30x100	511	Shielding_VSSA	8775	-335	30x100
456	Shielding_VSSA	6300	-335	30x100	512	VSS	8820	-335	30x100
457	Shielding_VSSA	6345	-335	30x100	513	VSS	8865	-335	30x100
458	Shielding_VSSA	6390	-335	30x100	514	VSS	8910	-335	30x100
459	CSB	6435	-335	30x100	515	VSS	8955	-335	30x100
460	CSB	6480	-335	30x100	516	VSS	9000	-335	30x100
461	SCL	6525	-335	30x100	517	VSS	9045	-335	30x100
462	SCL	6570	-335	30x100	518	AVDD	9090	-335	30x100
463	SDI	6615	-335	30x100	519	AVDD	9135	-335	30x100
464	SDI	6660	-335	30x100	520	AVDD	9180	-335	30x100
465	SDO	6705	-335	30x100	521	AVDD	9225	-335	30x100
466	SDO	6750	-335	30x100	522	AVDD	9270	-335	30x100
467	TP_SYNC	6795	-335	30x100	523	AVDD	9315	-335	30x100
468	LEDPWM	6840	-335	30x100	524	VMID_L[1]	9360	-335	30x100
469	LEDPWM	6885	-335	30x100	525	VMID_L[1]	9405	-335	30x100
470	TEST_I[24]	6930	-335	30x100	526	VMID_L[1]	9450	-335	30x100
471	TEST_I[25]	6975	-335	30x100	527	VMID_L[1]	9495	-335	30x100
472	RESX	7020	-335	30x100	528	VMID_L[1]	9540	-335	30x100
473	RESX	7065	-335	30x100	529	VMID_L[1]	9585	-335	30x100
474	STBYB	7110	-335	30x100	530	VSSA	9630	-335	30x100
475	STBYB	7155	-335	30x100	531	VSSA	9675	-335	30x100
476	BIST_EN	7200	-335	30x100	532	VSSA	9720	-335	30x100
477	BIST_EN	7245	-335	30x100	533	VSSA	9765	-335	30x100
478	SHLR	7290	-335	30x100	534	VSSA	9810	-335	30x100
479	SHLR	7335	-335	30x100	535	VSSA	9855	-335	30x100
480	UPDN	7380	-335	30x100	536	Shielding_VSSA	9900	-335	30x100
481	UPDN	7425	-335	30x100	537	VCOMIN	9945	-335	30x100
482	MODE	7470	-335	30x100	538	VCOMIN	9990	-335	30x100
483	PNSWAP	7515	-335	30x100	539	Shielding_VSSA	10035	-335	30x100
484	DSWAP[1]	7560	-335	30x100	540	VCOM_OP	10080	-335	30x100
485	DSWAP[0]	7605	-335	30x100	541	VCOM_OP	10125	-335	30x100
486	LANSEL[1]	7650	-335	30x100	542	VCOM_OP	10170	-335	30x100
487	LANSEL[0]	7695	-335	30x100	543	VCOM_OP	10215	-335	30x100
488	IFSEL[1]	7740	-335	30x100	544	VCOM_OP	10260	-335	30x100
489	IFSEL[0]	7785	-335	30x100	545	VCOM_OP	10305	-335	30x100
490	ZIGZAG_ENB	7830	-335	30x100	546	Shielding_VSSA	10350	-335	30x100
491	PTYPE[1]	7875	-335	30x100	547	Shielding_VSSA	10395	-335	30x100
492	PTYPE[0]	7920	-335	30x100	548	Shielding_VSSA	10440	-335	30x100
493	DCLKPOL	7965	-335	30x100	549	Shielding_VSSA	10485	-335	30x100
494	INVSEL	8010	-335	30x100	550	Shielding_VSSA	10530	-335	30x100
495	NBW	8055	-335	30x100	551	VQLO	10575	-335	30x100
496	LVFMT	8100	-335	30x100	552	VQLO	10620	-335	30x100
497	LVBIT	8145	-335	30x100	553	VQLO	10665	-335	30x100
498	CMD_SEL[1]	8190	-335	30x100	554	VQLO	10710	-335	30x100
499	CMD_SEL[0]	8235	-335	30x100	555	VMID_OP	10755	-335	30x100
500	VCOMIN_SEL	8280	-335	30x100	556	VMID_OP	10800	-335	30x100
501	VCOMIN_SEL	8325	-335	30x100	557	VMID_OP	10845	-335	30x100
502	VCOM_EN	8370	-335	30x100	558	VMID_OP	10890	-335	30x100
503	VCOM_EN	8415	-335	30x100	559	VMID_OP	10935	-335	30x100
504	VMIDOP_EN	8460	-335	30x100	560	VMID_OP	10980	-335	30x100

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
561	VQHO	11025	-335	30x100	617	GOUT_L[6]	13545	-335	30x100
562	VQHO	11070	-335	30x100	618	GOUT_L[6]	13590	-335	30x100
563	VQHO	11115	-335	30x100	619	GOUT_L[5]	13635	-335	30x100
564	VQHO	11160	-335	30x100	620	GOUT_L[5]	13680	-335	30x100
565	Shielding_VSSA	11205	-335	30x100	621	GOUT_L[4]	13725	-335	30x100
566	Shielding_VSSA	11250	-335	30x100	622	GOUT_L[4]	13770	-335	30x100
567	Shielding_VSSA	11295	-335	30x100	623	GOUT_L[3]	13815	-335	30x100
568	Shielding_VSSA	11340	-335	30x100	624	GOUT_L[3]	13860	-335	30x100
569	Shielding_VSSA	11385	-335	30x100	625	GOUT_L[2]	13905	-335	30x100
570	PASS1_L	11430	-335	30x100	626	GOUT_L[2]	13950	-335	30x100
571	PASS1_L	11475	-335	30x100	627	GOUT_L[1]	13995	-335	30x100
572	Shielding_VSSA	11520	-335	30x100	628	GOUT_L[1]	14040	-335	30x100
573	VGH_L	11565	-335	30x100	629	DUMMY[36]	14085	-335	30x100
574	VGH_L	11610	-335	30x100	630	PASS2_L	14130	-335	30x100
575	VGH_L	11655	-335	30x100	631	PASS2_L	14175	-335	30x100
576	VGH_L	11700	-335	30x100	632	DUMMY	13864	350	18x65
577	VGH_L	11745	-335	30x100	633	PASS2_L	13828	350	18x65
578	VGH_L	11790	-335	30x100	634	PASS2_L	13792	350	18x65
579	VGL	11835	-335	30x100	635	PASS2_L	13756	350	18x65
580	VGL	11880	-335	30x100	636	PASS2_L	13720	350	18x65
581	VGL	11925	-335	30x100	637	DUMMY	13684	350	18x65
582	VGL	11970	-335	30x100	638	PASS1_L	13648	350	18x65
583	VGL	12015	-335	30x100	639	PASS1_L	13612	350	18x65
584	VGL	12060	-335	30x100	640	PASS1_L	13576	350	18x65
585	GOUT_L[22]	12105	-335	30x100	641	PASS1_L	13540	350	18x65
586	GOUT_L[22]	12150	-335	30x100	642	DUMMY	13504	350	18x65
587	GOUT_L[21]	12195	-335	30x100	643	DUMMY	13468	350	18x65
588	GOUT_L[21]	12240	-335	30x100	644	DUMMY	13432	350	18x65
589	GOUT_L[20]	12285	-335	30x100	645	DUMMY	13396	350	18x65
590	GOUT_L[20]	12330	-335	30x100	646	DUMMY	13360	350	18x65
591	GOUT_L[19]	12375	-335	30x100	647	DUMMY	13324	350	18x65
592	GOUT_L[19]	12420	-335	30x100	648	DUMMY	13288	350	18x65
593	GOUT_L[18]	12465	-335	30x100	649	DUMMY	13252	350	18x65
594	GOUT_L[18]	12510	-335	30x100	650	DUMMY	13216	350	18x65
595	GOUT_L[17]	12555	-335	30x100	651	DUMMY	13180	350	18x65
596	GOUT_L[17]	12600	-335	30x100	652	S[0]	13168	260	18x65
597	GOUT_L[16]	12645	-335	30x100	653	S[1]	13156	170	18x65
598	GOUT_L[16]	12690	-335	30x100	654	S[2]	13144	350	18x65
599	GOUT_L[15]	12735	-335	30x100	655	S[3]	13132	260	18x65
600	GOUT_L[15]	12780	-335	30x100	656	S[4]	13120	170	18x65
601	GOUT_L[14]	12825	-335	30x100	657	S[5]	13108	350	18x65
602	GOUT_L[14]	12870	-335	30x100	658	S[6]	13096	260	18x65
603	GOUT_L[13]	12915	-335	30x100	659	S[7]	13084	170	18x65
604	GOUT_L[13]	12960	-335	30x100	660	S[8]	13072	350	18x65
605	GOUT_L[12]	13005	-335	30x100	661	S[9]	13060	260	18x65
606	GOUT_L[12]	13050	-335	30x100	662	S[10]	13048	170	18x65
607	GOUT_L[11]	13095	-335	30x100	663	S[11]	13036	350	18x65
608	GOUT_L[11]	13140	-335	30x100	664	S[12]	13024	260	18x65
609	GOUT_L[10]	13185	-335	30x100	665	S[13]	13012	170	18x65
610	GOUT_L[10]	13230	-335	30x100	666	S[14]	13000	350	18x65
611	GOUT_L[9]	13275	-335	30x100	667	S[15]	12988	260	18x65
612	GOUT_L[9]	13320	-335	30x100	668	S[16]	12976	170	18x65
613	GOUT_L[8]	13365	-335	30x100	669	S[17]	12964	350	18x65
614	GOUT_L[8]	13410	-335	30x100	670	S[18]	12952	260	18x65
615	GOUT_L[7]	13455	-335	30x100	671	S[19]	12940	170	18x65
616	GOUT_L[7]	13500	-335	30x100	672	S[20]	12928	350	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
673	S[21]	12916	260	18x65	729	S[77]	12244	350	18x65
674	S[22]	12904	170	18x65	730	S[78]	12232	260	18x65
675	S[23]	12892	350	18x65	731	S[79]	12220	170	18x65
676	S[24]	12880	260	18x65	732	S[80]	12208	350	18x65
677	S[25]	12868	170	18x65	733	S[81]	12196	260	18x65
678	S[26]	12856	350	18x65	734	S[82]	12184	170	18x65
679	S[27]	12844	260	18x65	735	S[83]	12172	350	18x65
680	S[28]	12832	170	18x65	736	S[84]	12160	260	18x65
681	S[29]	12820	350	18x65	737	S[85]	12148	170	18x65
682	S[30]	12808	260	18x65	738	S[86]	12136	350	18x65
683	S[31]	12796	170	18x65	739	S[87]	12124	260	18x65
684	S[32]	12784	350	18x65	740	S[88]	12112	170	18x65
685	S[33]	12772	260	18x65	741	S[89]	12100	350	18x65
686	S[34]	12760	170	18x65	742	S[90]	12088	260	18x65
687	S[35]	12748	350	18x65	743	S[91]	12076	170	18x65
688	S[36]	12736	260	18x65	744	S[92]	12064	350	18x65
689	S[37]	12724	170	18x65	745	S[93]	12052	260	18x65
690	S[38]	12712	350	18x65	746	S[94]	12040	170	18x65
691	S[39]	12700	260	18x65	747	S[95]	12028	350	18x65
692	S[40]	12688	170	18x65	748	S[96]	12016	260	18x65
693	S[41]	12676	350	18x65	749	S[97]	12004	170	18x65
694	S[42]	12664	260	18x65	750	S[98]	11992	350	18x65
695	S[43]	12652	170	18x65	751	S[99]	11980	260	18x65
696	S[44]	12640	350	18x65	752	S[100]	11968	170	18x65
697	S[45]	12628	260	18x65	753	S[101]	11956	350	18x65
698	S[46]	12616	170	18x65	754	S[102]	11944	260	18x65
699	S[47]	12604	350	18x65	755	S[103]	11932	170	18x65
700	S[48]	12592	260	18x65	756	S[104]	11920	350	18x65
701	S[49]	12580	170	18x65	757	S[105]	11908	260	18x65
702	S[50]	12568	350	18x65	758	S[106]	11896	170	18x65
703	S[51]	12556	260	18x65	759	S[107]	11884	350	18x65
704	S[52]	12544	170	18x65	760	S[108]	11872	260	18x65
705	S[53]	12532	350	18x65	761	S[109]	11860	170	18x65
706	S[54]	12520	260	18x65	762	S[110]	11848	350	18x65
707	S[55]	12508	170	18x65	763	S[111]	11836	260	18x65
708	S[56]	12496	350	18x65	764	S[112]	11824	170	18x65
709	S[57]	12484	260	18x65	765	S[113]	11812	350	18x65
710	S[58]	12472	170	18x65	766	S[114]	11800	260	18x65
711	S[59]	12460	350	18x65	767	S[115]	11788	170	18x65
712	S[60]	12448	260	18x65	768	S[116]	11776	350	18x65
713	S[61]	12436	170	18x65	769	S[117]	11764	260	18x65
714	S[62]	12424	350	18x65	770	S[118]	11752	170	18x65
715	S[63]	12412	260	18x65	771	S[119]	11740	350	18x65
716	S[64]	12400	170	18x65	772	S[120]	11728	260	18x65
717	S[65]	12388	350	18x65	773	S[121]	11716	170	18x65
718	S[66]	12376	260	18x65	774	S[122]	11704	350	18x65
719	S[67]	12364	170	18x65	775	S[123]	11692	260	18x65
720	S[68]	12352	350	18x65	776	S[124]	11680	170	18x65
721	S[69]	12340	260	18x65	777	S[125]	11668	350	18x65
722	S[70]	12328	170	18x65	778	S[126]	11656	260	18x65
723	S[71]	12316	350	18x65	779	S[127]	11644	170	18x65
724	S[72]	12304	260	18x65	780	S[128]	11632	350	18x65
725	S[73]	12292	170	18x65	781	S[129]	11620	260	18x65
726	S[74]	12280	350	18x65	782	S[130]	11608	170	18x65
727	S[75]	12268	260	18x65	783	S[131]	11596	350	18x65
728	S[76]	12256	170	18x65	784	S[132]	11584	260	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
785	S[133]	11572	170	18x65	841	S[189]	10900	260	18x65
786	S[134]	11560	350	18x65	842	S[190]	10888	170	18x65
787	S[135]	11548	260	18x65	843	S[191]	10876	350	18x65
788	S[136]	11536	170	18x65	844	S[192]	10864	260	18x65
789	S[137]	11524	350	18x65	845	S[193]	10852	170	18x65
790	S[138]	11512	260	18x65	846	S[194]	10840	350	18x65
791	S[139]	11500	170	18x65	847	S[195]	10828	260	18x65
792	S[140]	11488	350	18x65	848	S[196]	10816	170	18x65
793	S[141]	11476	260	18x65	849	S[197]	10804	350	18x65
794	S[142]	11464	170	18x65	850	S[198]	10792	260	18x65
795	S[143]	11452	350	18x65	851	S[199]	10780	170	18x65
796	S[144]	11440	260	18x65	852	S[200]	10768	350	18x65
797	S[145]	11428	170	18x65	853	S[201]	10756	260	18x65
798	S[146]	11416	350	18x65	854	S[202]	10744	170	18x65
799	S[147]	11404	260	18x65	855	S[203]	10732	350	18x65
800	S[148]	11392	170	18x65	856	S[204]	10720	260	18x65
801	S[149]	11380	350	18x65	857	S[205]	10708	170	18x65
802	S[150]	11368	260	18x65	858	S[206]	10696	350	18x65
803	S[151]	11356	170	18x65	859	S[207]	10684	260	18x65
804	S[152]	11344	350	18x65	860	S[208]	10672	170	18x65
805	S[153]	11332	260	18x65	861	S[209]	10660	350	18x65
806	S[154]	11320	170	18x65	862	S[210]	10648	260	18x65
807	S[155]	11308	350	18x65	863	S[211]	10636	170	18x65
808	S[156]	11296	260	18x65	864	S[212]	10624	350	18x65
809	S[157]	11284	170	18x65	865	S[213]	10612	260	18x65
810	S[158]	11272	350	18x65	866	S[214]	10600	170	18x65
811	S[159]	11260	260	18x65	867	S[215]	10588	350	18x65
812	S[160]	11248	170	18x65	868	S[216]	10576	260	18x65
813	S[161]	11236	350	18x65	869	S[217]	10564	170	18x65
814	S[162]	11224	260	18x65	870	S[218]	10552	350	18x65
815	S[163]	11212	170	18x65	871	S[219]	10540	260	18x65
816	S[164]	11200	350	18x65	872	S[220]	10528	170	18x65
817	S[165]	11188	260	18x65	873	S[221]	10516	350	18x65
818	S[166]	11176	170	18x65	874	S[222]	10504	260	18x65
819	S[167]	11164	350	18x65	875	S[223]	10492	170	18x65
820	S[168]	11152	260	18x65	876	S[224]	10480	350	18x65
821	S[169]	11140	170	18x65	877	S[225]	10468	260	18x65
822	S[170]	11128	350	18x65	878	S[226]	10456	170	18x65
823	S[171]	11116	260	18x65	879	S[227]	10444	350	18x65
824	S[172]	11104	170	18x65	880	S[228]	10432	260	18x65
825	S[173]	11092	350	18x65	881	S[229]	10420	170	18x65
826	S[174]	11080	260	18x65	882	S[230]	10408	350	18x65
827	S[175]	11068	170	18x65	883	S[231]	10396	260	18x65
828	S[176]	11056	350	18x65	884	S[232]	10384	170	18x65
829	S[177]	11044	260	18x65	885	S[233]	10372	350	18x65
830	S[178]	11032	170	18x65	886	S[234]	10360	260	18x65
831	S[179]	11020	350	18x65	887	S[235]	10348	170	18x65
832	S[180]	11008	260	18x65	888	S[236]	10336	350	18x65
833	S[181]	10996	170	18x65	889	S[237]	10324	260	18x65
834	S[182]	10984	350	18x65	890	S[238]	10312	170	18x65
835	S[183]	10972	260	18x65	891	S[239]	10300	350	18x65
836	S[184]	10960	170	18x65	892	S[240]	10288	260	18x65
837	S[185]	10948	350	18x65	893	S[241]	10276	170	18x65
838	S[186]	10936	260	18x65	894	S[242]	10264	350	18x65
839	S[187]	10924	170	18x65	895	S[243]	10252	260	18x65
840	S[188]	10912	350	18x65	896	S[244]	10240	170	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
897	S[245]	10228	350	18x65	953	S[301]	9556	170	18x65
898	S[246]	10216	260	18x65	954	S[302]	9544	350	18x65
899	S[247]	10204	170	18x65	955	S[303]	9532	260	18x65
900	S[248]	10192	350	18x65	956	S[304]	9520	170	18x65
901	S[249]	10180	260	18x65	957	S[305]	9508	350	18x65
902	S[250]	10168	170	18x65	958	S[306]	9496	260	18x65
903	S[251]	10156	350	18x65	959	S[307]	9484	170	18x65
904	S[252]	10144	260	18x65	960	S[308]	9472	350	18x65
905	S[253]	10132	170	18x65	961	S[309]	9460	260	18x65
906	S[254]	10120	350	18x65	962	S[310]	9448	170	18x65
907	S[255]	10108	260	18x65	963	S[311]	9436	350	18x65
908	S[256]	10096	170	18x65	964	S[312]	9424	260	18x65
909	S[257]	10084	350	18x65	965	S[313]	9412	170	18x65
910	S[258]	10072	260	18x65	966	S[314]	9400	350	18x65
911	S[259]	10060	170	18x65	967	S[315]	9388	260	18x65
912	S[260]	10048	350	18x65	968	S[316]	9376	170	18x65
913	S[261]	10036	260	18x65	969	S[317]	9364	350	18x65
914	S[262]	10024	170	18x65	970	S[318]	9352	260	18x65
915	S[263]	10012	350	18x65	971	S[319]	9340	170	18x65
916	S[264]	10000	260	18x65	972	S[320]	9328	350	18x65
917	S[265]	9988	170	18x65	973	S[321]	9316	260	18x65
918	S[266]	9976	350	18x65	974	S[322]	9304	170	18x65
919	S[267]	9964	260	18x65	975	S[323]	9292	350	18x65
920	S[268]	9952	170	18x65	976	S[324]	9280	260	18x65
921	S[269]	9940	350	18x65	977	S[325]	9268	170	18x65
922	S[270]	9928	260	18x65	978	S[326]	9256	350	18x65
923	S[271]	9916	170	18x65	979	S[327]	9244	260	18x65
924	S[272]	9904	350	18x65	980	S[328]	9232	170	18x65
925	S[273]	9892	260	18x65	981	S[329]	9220	350	18x65
926	S[274]	9880	170	18x65	982	S[330]	9208	260	18x65
927	S[275]	9868	350	18x65	983	S[331]	9196	170	18x65
928	S[276]	9856	260	18x65	984	S[332]	9184	350	18x65
929	S[277]	9844	170	18x65	985	S[333]	9172	260	18x65
930	S[278]	9832	350	18x65	986	S[334]	9160	170	18x65
931	S[279]	9820	260	18x65	987	S[335]	9148	350	18x65
932	S[280]	9808	170	18x65	988	S[336]	9136	260	18x65
933	S[281]	9796	350	18x65	989	S[337]	9124	170	18x65
934	S[282]	9784	260	18x65	990	S[338]	9112	350	18x65
935	S[283]	9772	170	18x65	991	S[339]	9100	260	18x65
936	S[284]	9760	350	18x65	992	S[340]	9088	170	18x65
937	S[285]	9748	260	18x65	993	S[341]	9076	350	18x65
938	S[286]	9736	170	18x65	994	S[342]	9064	260	18x65
939	S[287]	9724	350	18x65	995	S[343]	9052	170	18x65
940	S[288]	9712	260	18x65	996	S[344]	9040	350	18x65
941	S[289]	9700	170	18x65	997	S[345]	9028	260	18x65
942	S[290]	9688	350	18x65	998	S[346]	9016	170	18x65
943	S[291]	9676	260	18x65	999	S[347]	9004	350	18x65
944	S[292]	9664	170	18x65	1000	S[348]	8992	260	18x65
945	S[293]	9652	350	18x65	1001	S[349]	8980	170	18x65
946	S[294]	9640	260	18x65	1002	S[350]	8968	350	18x65
947	S[295]	9628	170	18x65	1003	S[351]	8956	260	18x65
948	S[296]	9616	350	18x65	1004	S[352]	8944	170	18x65
949	S[297]	9604	260	18x65	1005	S[353]	8932	350	18x65
950	S[298]	9592	170	18x65	1006	S[354]	8920	260	18x65
951	S[299]	9580	350	18x65	1007	S[355]	8908	170	18x65
952	S[300]	9568	260	18x65	1008	S[356]	8896	350	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1009	S[357]	8884	260	18x65	1065	S[413]	8212	350	18x65
1010	S[358]	8872	170	18x65	1066	S[414]	8200	260	18x65
1011	S[359]	8860	350	18x65	1067	S[415]	8188	170	18x65
1012	S[360]	8848	260	18x65	1068	S[416]	8176	350	18x65
1013	S[361]	8836	170	18x65	1069	S[417]	8164	260	18x65
1014	S[362]	8824	350	18x65	1070	S[418]	8152	170	18x65
1015	S[363]	8812	260	18x65	1071	S[419]	8140	350	18x65
1016	S[364]	8800	170	18x65	1072	S[420]	8128	260	18x65
1017	S[365]	8788	350	18x65	1073	S[421]	8116	170	18x65
1018	S[366]	8776	260	18x65	1074	S[422]	8104	350	18x65
1019	S[367]	8764	170	18x65	1075	S[423]	8092	260	18x65
1020	S[368]	8752	350	18x65	1076	S[424]	8080	170	18x65
1021	S[369]	8740	260	18x65	1077	S[425]	8068	350	18x65
1022	S[370]	8728	170	18x65	1078	S[426]	8056	260	18x65
1023	S[371]	8716	350	18x65	1079	S[427]	8044	170	18x65
1024	S[372]	8704	260	18x65	1080	S[428]	8032	350	18x65
1025	S[373]	8692	170	18x65	1081	S[429]	8020	260	18x65
1026	S[374]	8680	350	18x65	1082	S[430]	8008	170	18x65
1027	S[375]	8668	260	18x65	1083	S[431]	7996	350	18x65
1028	S[376]	8656	170	18x65	1084	S[432]	7984	260	18x65
1029	S[377]	8644	350	18x65	1085	S[433]	7972	170	18x65
1030	S[378]	8632	260	18x65	1086	S[434]	7960	350	18x65
1031	S[379]	8620	170	18x65	1087	S[435]	7948	260	18x65
1032	S[380]	8608	350	18x65	1088	S[436]	7936	170	18x65
1033	S[381]	8596	260	18x65	1089	S[437]	7924	350	18x65
1034	S[382]	8584	170	18x65	1090	S[438]	7912	260	18x65
1035	S[383]	8572	350	18x65	1091	S[439]	7900	170	18x65
1036	S[384]	8560	260	18x65	1092	S[440]	7888	350	18x65
1037	S[385]	8548	170	18x65	1093	S[441]	7876	260	18x65
1038	S[386]	8536	350	18x65	1094	S[442]	7864	170	18x65
1039	S[387]	8524	260	18x65	1095	S[443]	7852	350	18x65
1040	S[388]	8512	170	18x65	1096	S[444]	7840	260	18x65
1041	S[389]	8500	350	18x65	1097	S[445]	7828	170	18x65
1042	S[390]	8488	260	18x65	1098	S[446]	7816	350	18x65
1043	S[391]	8476	170	18x65	1099	S[447]	7804	260	18x65
1044	S[392]	8464	350	18x65	1100	S[448]	7792	170	18x65
1045	S[393]	8452	260	18x65	1101	S[449]	7780	350	18x65
1046	S[394]	8440	170	18x65	1102	S[450]	7768	260	18x65
1047	S[395]	8428	350	18x65	1103	S[451]	7756	170	18x65
1048	S[396]	8416	260	18x65	1104	S[452]	7744	350	18x65
1049	S[397]	8404	170	18x65	1105	S[453]	7732	260	18x65
1050	S[398]	8392	350	18x65	1106	S[454]	7720	170	18x65
1051	S[399]	8380	260	18x65	1107	S[455]	7708	350	18x65
1052	S[400]	8368	170	18x65	1108	S[456]	7696	260	18x65
1053	S[401]	8356	350	18x65	1109	S[457]	7684	170	18x65
1054	S[402]	8344	260	18x65	1110	S[458]	7672	350	18x65
1055	S[403]	8332	170	18x65	1111	S[459]	7660	260	18x65
1056	S[404]	8320	350	18x65	1112	S[460]	7648	170	18x65
1057	S[405]	8308	260	18x65	1113	S[461]	7636	350	18x65
1058	S[406]	8296	170	18x65	1114	S[462]	7624	260	18x65
1059	S[407]	8284	350	18x65	1115	S[463]	7612	170	18x65
1060	S[408]	8272	260	18x65	1116	S[464]	7600	350	18x65
1061	S[409]	8260	170	18x65	1117	S[465]	7588	260	18x65
1062	S[410]	8248	350	18x65	1118	S[466]	7576	170	18x65
1063	S[411]	8236	260	18x65	1119	S[467]	7564	350	18x65
1064	S[412]	8224	170	18x65	1120	S[468]	7552	260	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1121	S[469]	7540	170	18x65	1177	S[525]	6868	260	18x65
1122	S[470]	7528	350	18x65	1178	S[526]	6856	170	18x65
1123	S[471]	7516	260	18x65	1179	S[527]	6844	350	18x65
1124	S[472]	7504	170	18x65	1180	S[528]	6832	260	18x65
1125	S[473]	7492	350	18x65	1181	S[529]	6820	170	18x65
1126	S[474]	7480	260	18x65	1182	S[530]	6808	350	18x65
1127	S[475]	7468	170	18x65	1183	S[531]	6796	260	18x65
1128	S[476]	7456	350	18x65	1184	S[532]	6784	170	18x65
1129	S[477]	7444	260	18x65	1185	S[533]	6772	350	18x65
1130	S[478]	7432	170	18x65	1186	S[534]	6760	260	18x65
1131	S[479]	7420	350	18x65	1187	S[535]	6748	170	18x65
1132	S[480]	7408	260	18x65	1188	S[536]	6736	350	18x65
1133	S[481]	7396	170	18x65	1189	S[537]	6724	260	18x65
1134	S[482]	7384	350	18x65	1190	S[538]	6712	170	18x65
1135	S[483]	7372	260	18x65	1191	S[539]	6700	350	18x65
1136	S[484]	7360	170	18x65	1192	S[540]	6688	260	18x65
1137	S[485]	7348	350	18x65	1193	S[541]	6676	170	18x65
1138	S[486]	7336	260	18x65	1194	S[542]	6664	350	18x65
1139	S[487]	7324	170	18x65	1195	S[543]	6652	260	18x65
1140	S[488]	7312	350	18x65	1196	S[544]	6640	170	18x65
1141	S[489]	7300	260	18x65	1197	S[545]	6628	350	18x65
1142	S[490]	7288	170	18x65	1198	S[546]	6616	260	18x65
1143	S[491]	7276	350	18x65	1199	S[547]	6604	170	18x65
1144	S[492]	7264	260	18x65	1200	S[548]	6592	350	18x65
1145	S[493]	7252	170	18x65	1201	S[549]	6580	260	18x65
1146	S[494]	7240	350	18x65	1202	S[550]	6568	170	18x65
1147	S[495]	7228	260	18x65	1203	S[551]	6556	350	18x65
1148	S[496]	7216	170	18x65	1204	S[552]	6544	260	18x65
1149	S[497]	7204	350	18x65	1205	S[553]	6532	170	18x65
1150	S[498]	7192	260	18x65	1206	S[554]	6520	350	18x65
1151	S[499]	7180	170	18x65	1207	S[555]	6508	260	18x65
1152	S[500]	7168	350	18x65	1208	S[556]	6496	170	18x65
1153	S[501]	7156	260	18x65	1209	S[557]	6484	350	18x65
1154	S[502]	7144	170	18x65	1210	S[558]	6472	260	18x65
1155	S[503]	7132	350	18x65	1211	S[559]	6460	170	18x65
1156	S[504]	7120	260	18x65	1212	S[560]	6448	350	18x65
1157	S[505]	7108	170	18x65	1213	S[561]	6436	260	18x65
1158	S[506]	7096	350	18x65	1214	S[562]	6424	170	18x65
1159	S[507]	7084	260	18x65	1215	S[563]	6412	350	18x65
1160	S[508]	7072	170	18x65	1216	S[564]	6400	260	18x65
1161	S[509]	7060	350	18x65	1217	S[565]	6388	170	18x65
1162	S[510]	7048	260	18x65	1218	S[566]	6376	350	18x65
1163	S[511]	7036	170	18x65	1219	S[567]	6364	260	18x65
1164	S[512]	7024	350	18x65	1220	S[568]	6352	170	18x65
1165	S[513]	7012	260	18x65	1221	S[569]	6340	350	18x65
1166	S[514]	7000	170	18x65	1222	S[570]	6328	260	18x65
1167	S[515]	6988	350	18x65	1223	S[571]	6316	170	18x65
1168	S[516]	6976	260	18x65	1224	S[572]	6304	350	18x65
1169	S[517]	6964	170	18x65	1225	S[573]	6292	260	18x65
1170	S[518]	6952	350	18x65	1226	S[574]	6280	170	18x65
1171	S[519]	6940	260	18x65	1227	S[575]	6268	350	18x65
1172	S[520]	6928	170	18x65	1228	S[576]	6256	260	18x65
1173	S[521]	6916	350	18x65	1229	S[577]	6244	170	18x65
1174	S[522]	6904	260	18x65	1230	S[578]	6232	350	18x65
1175	S[523]	6892	170	18x65	1231	S[579]	6220	260	18x65
1176	S[524]	6880	350	18x65	1232	S[580]	6208	170	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1233	S[581]	6196	350	18x65	1289	S[637]	5524	170	18x65
1234	S[582]	6184	260	18x65	1290	S[638]	5512	350	18x65
1235	S[583]	6172	170	18x65	1291	S[639]	5500	260	18x65
1236	S[584]	6160	350	18x65	1292	S[640]	5488	170	18x65
1237	S[585]	6148	260	18x65	1293	S[641]	5476	350	18x65
1238	S[586]	6136	170	18x65	1294	S[642]	5464	260	18x65
1239	S[587]	6124	350	18x65	1295	S[643]	5452	170	18x65
1240	S[588]	6112	260	18x65	1296	S[644]	5440	350	18x65
1241	S[589]	6100	170	18x65	1297	S[645]	5428	260	18x65
1242	S[590]	6088	350	18x65	1298	S[646]	5416	170	18x65
1243	S[591]	6076	260	18x65	1299	S[647]	5404	350	18x65
1244	S[592]	6064	170	18x65	1300	S[648]	5392	260	18x65
1245	S[593]	6052	350	18x65	1301	S[649]	5380	170	18x65
1246	S[594]	6040	260	18x65	1302	S[650]	5368	350	18x65
1247	S[595]	6028	170	18x65	1303	S[651]	5356	260	18x65
1248	S[596]	6016	350	18x65	1304	S[652]	5344	170	18x65
1249	S[597]	6004	260	18x65	1305	S[653]	5332	350	18x65
1250	S[598]	5992	170	18x65	1306	S[654]	5320	260	18x65
1251	S[599]	5980	350	18x65	1307	S[655]	5308	170	18x65
1252	S[600]	5968	260	18x65	1308	S[656]	5296	350	18x65
1253	S[601]	5956	170	18x65	1309	S[657]	5284	260	18x65
1254	S[602]	5944	350	18x65	1310	S[658]	5272	170	18x65
1255	S[603]	5932	260	18x65	1311	S[659]	5260	350	18x65
1256	S[604]	5920	170	18x65	1312	S[660]	5248	260	18x65
1257	S[605]	5908	350	18x65	1313	S[661]	5236	170	18x65
1258	S[606]	5896	260	18x65	1314	S[662]	5224	350	18x65
1259	S[607]	5884	170	18x65	1315	S[663]	5212	260	18x65
1260	S[608]	5872	350	18x65	1316	S[664]	5200	170	18x65
1261	S[609]	5860	260	18x65	1317	S[665]	5188	350	18x65
1262	S[610]	5848	170	18x65	1318	S[666]	5176	260	18x65
1263	S[611]	5836	350	18x65	1319	S[667]	5164	170	18x65
1264	S[612]	5824	260	18x65	1320	S[668]	5152	350	18x65
1265	S[613]	5812	170	18x65	1321	S[669]	5140	260	18x65
1266	S[614]	5800	350	18x65	1322	S[670]	5128	170	18x65
1267	S[615]	5788	260	18x65	1323	S[671]	5116	350	18x65
1268	S[616]	5776	170	18x65	1324	S[672]	5104	260	18x65
1269	S[617]	5764	350	18x65	1325	S[673]	5092	170	18x65
1270	S[618]	5752	260	18x65	1326	S[674]	5080	350	18x65
1271	S[619]	5740	170	18x65	1327	S[675]	5068	260	18x65
1272	S[620]	5728	350	18x65	1328	S[676]	5056	170	18x65
1273	S[621]	5716	260	18x65	1329	S[677]	5044	350	18x65
1274	S[622]	5704	170	18x65	1330	S[678]	5032	260	18x65
1275	S[623]	5692	350	18x65	1331	S[679]	5020	170	18x65
1276	S[624]	5680	260	18x65	1332	S[680]	5008	350	18x65
1277	S[625]	5668	170	18x65	1333	S[681]	4996	260	18x65
1278	S[626]	5656	350	18x65	1334	S[682]	4984	170	18x65
1279	S[627]	5644	260	18x65	1335	S[683]	4972	350	18x65
1280	S[628]	5632	170	18x65	1336	S[684]	4960	260	18x65
1281	S[629]	5620	350	18x65	1337	S[685]	4948	170	18x65
1282	S[630]	5608	260	18x65	1338	S[686]	4936	350	18x65
1283	S[631]	5596	170	18x65	1339	S[687]	4924	260	18x65
1284	S[632]	5584	350	18x65	1340	S[688]	4912	170	18x65
1285	S[633]	5572	260	18x65	1341	S[689]	4900	350	18x65
1286	S[634]	5560	170	18x65	1342	S[690]	4888	260	18x65
1287	S[635]	5548	350	18x65	1343	S[691]	4876	170	18x65
1288	S[636]	5536	260	18x65	1344	S[692]	4864	350	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1345	S[693]	4852	260	18x65	1401	S[749]	4180	350	18x65
1346	S[694]	4840	170	18x65	1402	S[750]	4168	260	18x65
1347	S[695]	4828	350	18x65	1403	S[751]	4156	170	18x65
1348	S[696]	4816	260	18x65	1404	S[752]	4144	350	18x65
1349	S[697]	4804	170	18x65	1405	S[753]	4132	260	18x65
1350	S[698]	4792	350	18x65	1406	S[754]	4120	170	18x65
1351	S[699]	4780	260	18x65	1407	S[755]	4108	350	18x65
1352	S[700]	4768	170	18x65	1408	S[756]	4096	260	18x65
1353	S[701]	4756	350	18x65	1409	S[757]	4084	170	18x65
1354	S[702]	4744	260	18x65	1410	S[758]	4072	350	18x65
1355	S[703]	4732	170	18x65	1411	S[759]	4060	260	18x65
1356	S[704]	4720	350	18x65	1412	S[760]	4048	170	18x65
1357	S[705]	4708	260	18x65	1413	S[761]	4036	350	18x65
1358	S[706]	4696	170	18x65	1414	S[762]	4024	260	18x65
1359	S[707]	4684	350	18x65	1415	S[763]	4012	170	18x65
1360	S[708]	4672	260	18x65	1416	S[764]	4000	350	18x65
1361	S[709]	4660	170	18x65	1417	S[765]	3988	260	18x65
1362	S[710]	4648	350	18x65	1418	S[766]	3976	170	18x65
1363	S[711]	4636	260	18x65	1419	S[767]	3964	350	18x65
1364	S[712]	4624	170	18x65	1420	S[768]	3952	260	18x65
1365	S[713]	4612	350	18x65	1421	Shielding_VSSA	3888	350	18x65
1366	S[714]	4600	260	18x65	1422	Shielding_VSSA	3816	350	18x65
1367	S[715]	4588	170	18x65	1423	Shielding_VSSA	3744	350	18x65
1368	S[716]	4576	350	18x65	1424	Shielding_VSSA	3672	350	18x65
1369	S[717]	4564	260	18x65	1425	Shielding_VSSA	3600	350	18x65
1370	S[718]	4552	170	18x65	1426	Shielding_VSSA	3528	350	18x65
1371	S[719]	4540	350	18x65	1427	Shielding_VSSA	3456	350	18x65
1372	S[720]	4528	260	18x65	1428	Shielding_VSSA	3384	350	18x65
1373	S[721]	4516	170	18x65	1429	Shielding_VSSA	3312	350	18x65
1374	S[722]	4504	350	18x65	1430	Shielding_VSSA	3240	350	18x65
1375	S[723]	4492	260	18x65	1431	Shielding_VSSA	3168	350	18x65
1376	S[724]	4480	170	18x65	1432	Shielding_VSSA	3096	350	18x65
1377	S[725]	4468	350	18x65	1433	Shielding_VSSA	3024	350	18x65
1378	S[726]	4456	260	18x65	1434	Shielding_VSSA	2952	350	18x65
1379	S[727]	4444	170	18x65	1435	Shielding_VSSA	2880	350	18x65
1380	S[728]	4432	350	18x65	1436	Shielding_VSSA	2808	350	18x65
1381	S[729]	4420	260	18x65	1437	Shielding_VSSA	2736	350	18x65
1382	S[730]	4408	170	18x65	1438	Shielding_VSSA	2664	350	18x65
1383	S[731]	4396	350	18x65	1439	Shielding_VSSA	2592	350	18x65
1384	S[732]	4384	260	18x65	1440	Shielding_VSSA	2520	350	18x65
1385	S[733]	4372	170	18x65	1441	Shielding_VSSA	2448	350	18x65
1386	S[734]	4360	350	18x65	1442	Shielding_VSSA	2376	350	18x65
1387	S[735]	4348	260	18x65	1443	Shielding_VSSA	2304	350	18x65
1388	S[736]	4336	170	18x65	1444	Shielding_VSSA	2232	350	18x65
1389	S[737]	4324	350	18x65	1445	Shielding_VSSA	2160	350	18x65
1390	S[738]	4312	260	18x65	1446	Shielding_VSSA	2088	350	18x65
1391	S[739]	4300	170	18x65	1447	Shielding_VSSA	2016	350	18x65
1392	S[740]	4288	350	18x65	1448	Shielding_VSSA	1944	350	18x65
1393	S[741]	4276	260	18x65	1449	Shielding_VSSA	1872	350	18x65
1394	S[742]	4264	170	18x65	1450	Shielding_VSSA	1800	350	18x65
1395	S[743]	4252	350	18x65	1451	Shielding_VSSA	1728	350	18x65
1396	S[744]	4240	260	18x65	1452	Shielding_VSSA	1656	350	18x65
1397	S[745]	4228	170	18x65	1453	Shielding_VSSA	1584	350	18x65
1398	S[746]	4216	350	18x65	1454	Shielding_VSSA	1512	350	18x65
1399	S[747]	4204	260	18x65	1455	Shielding_VSSA	1440	350	18x65
1400	S[748]	4192	170	18x65	1456	Shielding_VSSA	1368	350	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1457	Shielding_VSSA	1296	350	18x65	1513	Shielding_VSSA	-2736	350	18x65
1458	Shielding_VSSA	1224	350	18x65	1514	Shielding_VSSA	-2808	350	18x65
1459	Shielding_VSSA	1152	350	18x65	1515	Shielding_VSSA	-2880	350	18x65
1460	Shielding_VSSA	1080	350	18x65	1516	Shielding_VSSA	-2952	350	18x65
1461	Shielding_VSSA	1008	350	18x65	1517	Shielding_VSSA	-3024	350	18x65
1462	Shielding_VSSA	936	350	18x65	1518	Shielding_VSSA	-3096	350	18x65
1463	Shielding_VSSA	864	350	18x65	1519	Shielding_VSSA	-3168	350	18x65
1464	Shielding_VSSA	792	350	18x65	1520	Shielding_VSSA	-3240	350	18x65
1465	Shielding_VSSA	720	350	18x65	1521	Shielding_VSSA	-3312	350	18x65
1466	Shielding_VSSA	648	350	18x65	1522	Shielding_VSSA	-3384	350	18x65
1467	Shielding_VSSA	576	350	18x65	1523	Shielding_VSSA	-3456	350	18x65
1468	Shielding_VSSA	504	350	18x65	1524	Shielding_VSSA	-3528	350	18x65
1469	Shielding_VSSA	432	350	18x65	1525	Shielding_VSSA	-3600	350	18x65
1470	Shielding_VSSA	360	350	18x65	1526	Shielding_VSSA	-3672	350	18x65
1471	Shielding_VSSA	288	350	18x65	1527	Shielding_VSSA	-3744	350	18x65
1472	Shielding_VSSA	216	350	18x65	1528	Shielding_VSSA	-3816	350	18x65
1473	Shielding_VSSA	144	350	18x65	1529	Shielding_VSSA	-3888	350	18x65
1474	Shielding_VSSA	72	350	18x65	1530	S[769]	-4029	170	18x65
1475	Shielding_VSSA	0	350	18x65	1531	S[770]	-4041	350	18x65
1476	Shielding_VSSA	-72	350	18x65	1532	S[771]	-4053	260	18x65
1477	Shielding_VSSA	-144	350	18x65	1533	S[772]	-4065	170	18x65
1478	Shielding_VSSA	-216	350	18x65	1534	S[773]	-4077	350	18x65
1479	Shielding_VSSA	-288	350	18x65	1535	S[774]	-4089	260	18x65
1480	Shielding_VSSA	-360	350	18x65	1536	S[775]	-4101	170	18x65
1481	Shielding_VSSA	-432	350	18x65	1537	S[776]	-4113	350	18x65
1482	Shielding_VSSA	-504	350	18x65	1538	S[777]	-4125	260	18x65
1483	Shielding_VSSA	-576	350	18x65	1539	S[778]	-4137	170	18x65
1484	Shielding_VSSA	-648	350	18x65	1540	S[779]	-4149	350	18x65
1485	Shielding_VSSA	-720	350	18x65	1541	S[780]	-4161	260	18x65
1486	Shielding_VSSA	-792	350	18x65	1542	S[781]	-4173	170	18x65
1487	Shielding_VSSA	-864	350	18x65	1543	S[782]	-4185	350	18x65
1488	Shielding_VSSA	-936	350	18x65	1544	S[783]	-4197	260	18x65
1489	Shielding_VSSA	-1008	350	18x65	1545	S[784]	-4209	170	18x65
1490	Shielding_VSSA	-1080	350	18x65	1546	S[785]	-4221	350	18x65
1491	Shielding_VSSA	-1152	350	18x65	1547	S[786]	-4233	260	18x65
1492	Shielding_VSSA	-1224	350	18x65	1548	S[787]	-4245	170	18x65
1493	Shielding_VSSA	-1296	350	18x65	1549	S[788]	-4257	350	18x65
1494	Shielding_VSSA	-1368	350	18x65	1550	S[789]	-4269	260	18x65
1495	Shielding_VSSA	-1440	350	18x65	1551	S[790]	-4281	170	18x65
1496	Shielding_VSSA	-1512	350	18x65	1552	S[791]	-4293	350	18x65
1497	Shielding_VSSA	-1584	350	18x65	1553	S[792]	-4305	260	18x65
1498	Shielding_VSSA	-1656	350	18x65	1554	S[793]	-4317	170	18x65
1499	Shielding_VSSA	-1728	350	18x65	1555	S[794]	-4329	350	18x65
1500	Shielding_VSSA	-1800	350	18x65	1556	S[795]	-4341	260	18x65
1501	Shielding_VSSA	-1872	350	18x65	1557	S[796]	-4353	170	18x65
1502	Shielding_VSSA	-1944	350	18x65	1558	S[797]	-4365	350	18x65
1503	Shielding_VSSA	-2016	350	18x65	1559	S[798]	-4377	260	18x65
1504	Shielding_VSSA	-2088	350	18x65	1560	S[799]	-4389	170	18x65
1505	Shielding_VSSA	-2160	350	18x65	1561	S[800]	-4401	350	18x65
1506	Shielding_VSSA	-2232	350	18x65	1562	S[801]	-4413	260	18x65
1507	Shielding_VSSA	-2304	350	18x65	1563	S[802]	-4425	170	18x65
1508	Shielding_VSSA	-2376	350	18x65	1564	S[803]	-4437	350	18x65
1509	Shielding_VSSA	-2448	350	18x65	1565	S[804]	-4449	260	18x65
1510	Shielding_VSSA	-2520	350	18x65	1566	S[805]	-4461	170	18x65
1511	Shielding_VSSA	-2592	350	18x65	1567	S[806]	-4473	350	18x65
1512	Shielding_VSSA	-2664	350	18x65	1568	S[807]	-4485	260	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1569	S[808]	-4497	170	18x65	1625	S[864]	-5169	260	18x65
1570	S[809]	-4509	350	18x65	1626	S[865]	-5181	170	18x65
1571	S[810]	-4521	260	18x65	1627	S[866]	-5193	350	18x65
1572	S[811]	-4533	170	18x65	1628	S[867]	-5205	260	18x65
1573	S[812]	-4545	350	18x65	1629	S[868]	-5217	170	18x65
1574	S[813]	-4557	260	18x65	1630	S[869]	-5229	350	18x65
1575	S[814]	-4569	170	18x65	1631	S[870]	-5241	260	18x65
1576	S[815]	-4581	350	18x65	1632	S[871]	-5253	170	18x65
1577	S[816]	-4593	260	18x65	1633	S[872]	-5265	350	18x65
1578	S[817]	-4605	170	18x65	1634	S[873]	-5277	260	18x65
1579	S[818]	-4617	350	18x65	1635	S[874]	-5289	170	18x65
1580	S[819]	-4629	260	18x65	1636	S[875]	-5301	350	18x65
1581	S[820]	-4641	170	18x65	1637	S[876]	-5313	260	18x65
1582	S[821]	-4653	350	18x65	1638	S[877]	-5325	170	18x65
1583	S[822]	-4665	260	18x65	1639	S[878]	-5337	350	18x65
1584	S[823]	-4677	170	18x65	1640	S[879]	-5349	260	18x65
1585	S[824]	-4689	350	18x65	1641	S[880]	-5361	170	18x65
1586	S[825]	-4701	260	18x65	1642	S[881]	-5373	350	18x65
1587	S[826]	-4713	170	18x65	1643	S[882]	-5385	260	18x65
1588	S[827]	-4725	350	18x65	1644	S[883]	-5397	170	18x65
1589	S[828]	-4737	260	18x65	1645	S[884]	-5409	350	18x65
1590	S[829]	-4749	170	18x65	1646	S[885]	-5421	260	18x65
1591	S[830]	-4761	350	18x65	1647	S[886]	-5433	170	18x65
1592	S[831]	-4773	260	18x65	1648	S[887]	-5445	350	18x65
1593	S[832]	-4785	170	18x65	1649	S[888]	-5457	260	18x65
1594	S[833]	-4797	350	18x65	1650	S[889]	-5469	170	18x65
1595	S[834]	-4809	260	18x65	1651	S[890]	-5481	350	18x65
1596	S[835]	-4821	170	18x65	1652	S[891]	-5493	260	18x65
1597	S[836]	-4833	350	18x65	1653	S[892]	-5505	170	18x65
1598	S[837]	-4845	260	18x65	1654	S[893]	-5517	350	18x65
1599	S[838]	-4857	170	18x65	1655	S[894]	-5529	260	18x65
1600	S[839]	-4869	350	18x65	1656	S[895]	-5541	170	18x65
1601	S[840]	-4881	260	18x65	1657	S[896]	-5553	350	18x65
1602	S[841]	-4893	170	18x65	1658	S[897]	-5565	260	18x65
1603	S[842]	-4905	350	18x65	1659	S[898]	-5577	170	18x65
1604	S[843]	-4917	260	18x65	1660	S[899]	-5589	350	18x65
1605	S[844]	-4929	170	18x65	1661	S[900]	-5601	260	18x65
1606	S[845]	-4941	350	18x65	1662	S[901]	-5613	170	18x65
1607	S[846]	-4953	260	18x65	1663	S[902]	-5625	350	18x65
1608	S[847]	-4965	170	18x65	1664	S[903]	-5637	260	18x65
1609	S[848]	-4977	350	18x65	1665	S[904]	-5649	170	18x65
1610	S[849]	-4989	260	18x65	1666	S[905]	-5661	350	18x65
1611	S[850]	-5001	170	18x65	1667	S[906]	-5673	260	18x65
1612	S[851]	-5013	350	18x65	1668	S[907]	-5685	170	18x65
1613	S[852]	-5025	260	18x65	1669	S[908]	-5697	350	18x65
1614	S[853]	-5037	170	18x65	1670	S[909]	-5709	260	18x65
1615	S[854]	-5049	350	18x65	1671	S[910]	-5721	170	18x65
1616	S[855]	-5061	260	18x65	1672	S[911]	-5733	350	18x65
1617	S[856]	-5073	170	18x65	1673	S[912]	-5745	260	18x65
1618	S[857]	-5085	350	18x65	1674	S[913]	-5757	170	18x65
1619	S[858]	-5097	260	18x65	1675	S[914]	-5769	350	18x65
1620	S[859]	-5109	170	18x65	1676	S[915]	-5781	260	18x65
1621	S[860]	-5121	350	18x65	1677	S[916]	-5793	170	18x65
1622	S[861]	-5133	260	18x65	1678	S[917]	-5805	350	18x65
1623	S[862]	-5145	170	18x65	1679	S[918]	-5817	260	18x65
1624	S[863]	-5157	350	18x65	1680	S[919]	-5829	170	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1681	S[920]	-5841	350	18x65	1737	S[976]	-6513	170	18x65
1682	S[921]	-5853	260	18x65	1738	S[977]	-6525	350	18x65
1683	S[922]	-5865	170	18x65	1739	S[978]	-6537	260	18x65
1684	S[923]	-5877	350	18x65	1740	S[979]	-6549	170	18x65
1685	S[924]	-5889	260	18x65	1741	S[980]	-6561	350	18x65
1686	S[925]	-5901	170	18x65	1742	S[981]	-6573	260	18x65
1687	S[926]	-5913	350	18x65	1743	S[982]	-6585	170	18x65
1688	S[927]	-5925	260	18x65	1744	S[983]	-6597	350	18x65
1689	S[928]	-5937	170	18x65	1745	S[984]	-6609	260	18x65
1690	S[929]	-5949	350	18x65	1746	S[985]	-6621	170	18x65
1691	S[930]	-5961	260	18x65	1747	S[986]	-6633	350	18x65
1692	S[931]	-5973	170	18x65	1748	S[987]	-6645	260	18x65
1693	S[932]	-5985	350	18x65	1749	S[988]	-6657	170	18x65
1694	S[933]	-5997	260	18x65	1750	S[989]	-6669	350	18x65
1695	S[934]	-6009	170	18x65	1751	S[990]	-6681	260	18x65
1696	S[935]	-6021	350	18x65	1752	S[991]	-6693	170	18x65
1697	S[936]	-6033	260	18x65	1753	S[992]	-6705	350	18x65
1698	S[937]	-6045	170	18x65	1754	S[993]	-6717	260	18x65
1699	S[938]	-6057	350	18x65	1755	S[994]	-6729	170	18x65
1700	S[939]	-6069	260	18x65	1756	S[995]	-6741	350	18x65
1701	S[940]	-6081	170	18x65	1757	S[996]	-6753	260	18x65
1702	S[941]	-6093	350	18x65	1758	S[997]	-6765	170	18x65
1703	S[942]	-6105	260	18x65	1759	S[998]	-6777	350	18x65
1704	S[943]	-6117	170	18x65	1760	S[999]	-6789	260	18x65
1705	S[944]	-6129	350	18x65	1761	S[1000]	-6801	170	18x65
1706	S[945]	-6141	260	18x65	1762	S[1001]	-6813	350	18x65
1707	S[946]	-6153	170	18x65	1763	S[1002]	-6825	260	18x65
1708	S[947]	-6165	350	18x65	1764	S[1003]	-6837	170	18x65
1709	S[948]	-6177	260	18x65	1765	S[1004]	-6849	350	18x65
1710	S[949]	-6189	170	18x65	1766	S[1005]	-6861	260	18x65
1711	S[950]	-6201	350	18x65	1767	S[1006]	-6873	170	18x65
1712	S[951]	-6213	260	18x65	1768	S[1007]	-6885	350	18x65
1713	S[952]	-6225	170	18x65	1769	S[1008]	-6897	260	18x65
1714	S[953]	-6237	350	18x65	1770	S[1009]	-6909	170	18x65
1715	S[954]	-6249	260	18x65	1771	S[1010]	-6921	350	18x65
1716	S[955]	-6261	170	18x65	1772	S[1011]	-6933	260	18x65
1717	S[956]	-6273	350	18x65	1773	S[1012]	-6945	170	18x65
1718	S[957]	-6285	260	18x65	1774	S[1013]	-6957	350	18x65
1719	S[958]	-6297	170	18x65	1775	S[1014]	-6969	260	18x65
1720	S[959]	-6309	350	18x65	1776	S[1015]	-6981	170	18x65
1721	S[960]	-6321	260	18x65	1777	S[1016]	-6993	350	18x65
1722	S[961]	-6333	170	18x65	1778	S[1017]	-7005	260	18x65
1723	S[962]	-6345	350	18x65	1779	S[1018]	-7017	170	18x65
1724	S[963]	-6357	260	18x65	1780	S[1019]	-7029	350	18x65
1725	S[964]	-6369	170	18x65	1781	S[1020]	-7041	260	18x65
1726	S[965]	-6381	350	18x65	1782	S[1021]	-7053	170	18x65
1727	S[966]	-6393	260	18x65	1783	S[1022]	-7065	350	18x65
1728	S[967]	-6405	170	18x65	1784	S[1023]	-7077	260	18x65
1729	S[968]	-6417	350	18x65	1785	S[1024]	-7089	170	18x65
1730	S[969]	-6429	260	18x65	1786	S[1025]	-7101	350	18x65
1731	S[970]	-6441	170	18x65	1787	S[1026]	-7113	260	18x65
1732	S[971]	-6453	350	18x65	1788	S[1027]	-7125	170	18x65
1733	S[972]	-6465	260	18x65	1789	S[1028]	-7137	350	18x65
1734	S[973]	-6477	170	18x65	1790	S[1029]	-7149	260	18x65
1735	S[974]	-6489	350	18x65	1791	S[1030]	-7161	170	18x65
1736	S[975]	-6501	260	18x65	1792	S[1031]	-7173	350	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1793	S[1032]	-7185	260	18x65		1849	S[1088]	-7857	18x65
1794	S[1033]	-7197	170	18x65		1850	S[1089]	-7869	18x65
1795	S[1034]	-7209	350	18x65		1851	S[1090]	-7881	18x65
1796	S[1035]	-7221	260	18x65		1852	S[1091]	-7893	18x65
1797	S[1036]	-7233	170	18x65		1853	S[1092]	-7905	18x65
1798	S[1037]	-7245	350	18x65		1854	S[1093]	-7917	18x65
1799	S[1038]	-7257	260	18x65		1855	S[1094]	-7929	18x65
1800	S[1039]	-7269	170	18x65		1856	S[1095]	-7941	18x65
1801	S[1040]	-7281	350	18x65		1857	S[1096]	-7953	18x65
1802	S[1041]	-7293	260	18x65		1858	S[1097]	-7965	18x65
1803	S[1042]	-7305	170	18x65		1859	S[1098]	-7977	18x65
1804	S[1043]	-7317	350	18x65		1860	S[1099]	-7989	18x65
1805	S[1044]	-7329	260	18x65		1861	S[1100]	-8001	18x65
1806	S[1045]	-7341	170	18x65		1862	S[1101]	-8013	18x65
1807	S[1046]	-7353	350	18x65		1863	S[1102]	-8025	18x65
1808	S[1047]	-7365	260	18x65		1864	S[1103]	-8037	18x65
1809	S[1048]	-7377	170	18x65		1865	S[1104]	-8049	18x65
1810	S[1049]	-7389	350	18x65		1866	S[1105]	-8061	18x65
1811	S[1050]	-7401	260	18x65		1867	S[1106]	-8073	18x65
1812	S[1051]	-7413	170	18x65		1868	S[1107]	-8085	18x65
1813	S[1052]	-7425	350	18x65		1869	S[1108]	-8097	18x65
1814	S[1053]	-7437	260	18x65		1870	S[1109]	-8109	18x65
1815	S[1054]	-7449	170	18x65		1871	S[1110]	-8121	18x65
1816	S[1055]	-7461	350	18x65		1872	S[1111]	-8133	18x65
1817	S[1056]	-7473	260	18x65		1873	S[1112]	-8145	18x65
1818	S[1057]	-7485	170	18x65		1874	S[1113]	-8157	18x65
1819	S[1058]	-7497	350	18x65		1875	S[1114]	-8169	18x65
1820	S[1059]	-7509	260	18x65		1876	S[1115]	-8181	18x65
1821	S[1060]	-7521	170	18x65		1877	S[1116]	-8193	18x65
1822	S[1061]	-7533	350	18x65		1878	S[1117]	-8205	18x65
1823	S[1062]	-7545	260	18x65		1879	S[1118]	-8217	18x65
1824	S[1063]	-7557	170	18x65		1880	S[1119]	-8229	18x65
1825	S[1064]	-7569	350	18x65		1881	S[1120]	-8241	18x65
1826	S[1065]	-7581	260	18x65		1882	S[1121]	-8253	18x65
1827	S[1066]	-7593	170	18x65		1883	S[1122]	-8265	18x65
1828	S[1067]	-7605	350	18x65		1884	S[1123]	-8277	18x65
1829	S[1068]	-7617	260	18x65		1885	S[1124]	-8289	18x65
1830	S[1069]	-7629	170	18x65		1886	S[1125]	-8301	18x65
1831	S[1070]	-7641	350	18x65		1887	S[1126]	-8313	18x65
1832	S[1071]	-7653	260	18x65		1888	S[1127]	-8325	18x65
1833	S[1072]	-7665	170	18x65		1889	S[1128]	-8337	18x65
1834	S[1073]	-7677	350	18x65		1890	S[1129]	-8349	18x65
1835	S[1074]	-7689	260	18x65		1891	S[1130]	-8361	18x65
1836	S[1075]	-7701	170	18x65		1892	S[1131]	-8373	18x65
1837	S[1076]	-7713	350	18x65		1893	S[1132]	-8385	18x65
1838	S[1077]	-7725	260	18x65		1894	S[1133]	-8397	18x65
1839	S[1078]	-7737	170	18x65		1895	S[1134]	-8409	18x65
1840	S[1079]	-7749	350	18x65		1896	S[1135]	-8421	18x65
1841	S[1080]	-7761	260	18x65		1897	S[1136]	-8433	18x65
1842	S[1081]	-7773	170	18x65		1898	S[1137]	-8445	18x65
1843	S[1082]	-7785	350	18x65		1899	S[1138]	-8457	18x65
1844	S[1083]	-7797	260	18x65		1900	S[1139]	-8469	18x65
1845	S[1084]	-7809	170	18x65		1901	S[1140]	-8481	18x65
1846	S[1085]	-7821	350	18x65		1902	S[1141]	-8493	18x65
1847	S[1086]	-7833	260	18x65		1903	S[1142]	-8505	18x65
1848	S[1087]	-7845	170	18x65		1904	S[1143]	-8517	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
1905	S[1144]	-8529	170	18x65	1961	S[1200]	-9201	260	18x65
1906	S[1145]	-8541	350	18x65	1962	S[1201]	-9213	170	18x65
1907	S[1146]	-8553	260	18x65	1963	S[1202]	-9225	350	18x65
1908	S[1147]	-8565	170	18x65	1964	S[1203]	-9237	260	18x65
1909	S[1148]	-8577	350	18x65	1965	S[1204]	-9249	170	18x65
1910	S[1149]	-8589	260	18x65	1966	S[1205]	-9261	350	18x65
1911	S[1150]	-8601	170	18x65	1967	S[1206]	-9273	260	18x65
1912	S[1151]	-8613	350	18x65	1968	S[1207]	-9285	170	18x65
1913	S[1152]	-8625	260	18x65	1969	S[1208]	-9297	350	18x65
1914	S[1153]	-8637	170	18x65	1970	S[1209]	-9309	260	18x65
1915	S[1154]	-8649	350	18x65	1971	S[1210]	-9321	170	18x65
1916	S[1155]	-8661	260	18x65	1972	S[1211]	-9333	350	18x65
1917	S[1156]	-8673	170	18x65	1973	S[1212]	-9345	260	18x65
1918	S[1157]	-8685	350	18x65	1974	S[1213]	-9357	170	18x65
1919	S[1158]	-8697	260	18x65	1975	S[1214]	-9369	350	18x65
1920	S[1159]	-8709	170	18x65	1976	S[1215]	-9381	260	18x65
1921	S[1160]	-8721	350	18x65	1977	S[1216]	-9393	170	18x65
1922	S[1161]	-8733	260	18x65	1978	S[1217]	-9405	350	18x65
1923	S[1162]	-8745	170	18x65	1979	S[1218]	-9417	260	18x65
1924	S[1163]	-8757	350	18x65	1980	S[1219]	-9429	170	18x65
1925	S[1164]	-8769	260	18x65	1981	S[1220]	-9441	350	18x65
1926	S[1165]	-8781	170	18x65	1982	S[1221]	-9453	260	18x65
1927	S[1166]	-8793	350	18x65	1983	S[1222]	-9465	170	18x65
1928	S[1167]	-8805	260	18x65	1984	S[1223]	-9477	350	18x65
1929	S[1168]	-8817	170	18x65	1985	S[1224]	-9489	260	18x65
1930	S[1169]	-8829	350	18x65	1986	S[1225]	-9501	170	18x65
1931	S[1170]	-8841	260	18x65	1987	S[1226]	-9513	350	18x65
1932	S[1171]	-8853	170	18x65	1988	S[1227]	-9525	260	18x65
1933	S[1172]	-8865	350	18x65	1989	S[1228]	-9537	170	18x65
1934	S[1173]	-8877	260	18x65	1990	S[1229]	-9549	350	18x65
1935	S[1174]	-8889	170	18x65	1991	S[1230]	-9561	260	18x65
1936	S[1175]	-8901	350	18x65	1992	S[1231]	-9573	170	18x65
1937	S[1176]	-8913	260	18x65	1993	S[1232]	-9585	350	18x65
1938	S[1177]	-8925	170	18x65	1994	S[1233]	-9597	260	18x65
1939	S[1178]	-8937	350	18x65	1995	S[1234]	-9609	170	18x65
1940	S[1179]	-8949	260	18x65	1996	S[1235]	-9621	350	18x65
1941	S[1180]	-8961	170	18x65	1997	S[1236]	-9633	260	18x65
1942	S[1181]	-8973	350	18x65	1998	S[1237]	-9645	170	18x65
1943	S[1182]	-8985	260	18x65	1999	S[1238]	-9657	350	18x65
1944	S[1183]	-8997	170	18x65	2000	S[1239]	-9669	260	18x65
1945	S[1184]	-9009	350	18x65	2001	S[1240]	-9681	170	18x65
1946	S[1185]	-9021	260	18x65	2002	S[1241]	-9693	350	18x65
1947	S[1186]	-9033	170	18x65	2003	S[1242]	-9705	260	18x65
1948	S[1187]	-9045	350	18x65	2004	S[1243]	-9717	170	18x65
1949	S[1188]	-9057	260	18x65	2005	S[1244]	-9729	350	18x65
1950	S[1189]	-9069	170	18x65	2006	S[1245]	-9741	260	18x65
1951	S[1190]	-9081	350	18x65	2007	S[1246]	-9753	170	18x65
1952	S[1191]	-9093	260	18x65	2008	S[1247]	-9765	350	18x65
1953	S[1192]	-9105	170	18x65	2009	S[1248]	-9777	260	18x65
1954	S[1193]	-9117	350	18x65	2010	S[1249]	-9789	170	18x65
1955	S[1194]	-9129	260	18x65	2011	S[1250]	-9801	350	18x65
1956	S[1195]	-9141	170	18x65	2012	S[1251]	-9813	260	18x65
1957	S[1196]	-9153	350	18x65	2013	S[1252]	-9825	170	18x65
1958	S[1197]	-9165	260	18x65	2014	S[1253]	-9837	350	18x65
1959	S[1198]	-9177	170	18x65	2015	S[1254]	-9849	260	18x65
1960	S[1199]	-9189	350	18x65	2016	S[1255]	-9861	170	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
2017	S[1256]	-9873	350	18x65	2073	S[1312]	-10545	170	18x65
2018	S[1257]	-9885	260	18x65	2074	S[1313]	-10557	350	18x65
2019	S[1258]	-9897	170	18x65	2075	S[1314]	-10569	260	18x65
2020	S[1259]	-9909	350	18x65	2076	S[1315]	-10581	170	18x65
2021	S[1260]	-9921	260	18x65	2077	S[1316]	-10593	350	18x65
2022	S[1261]	-9933	170	18x65	2078	S[1317]	-10605	260	18x65
2023	S[1262]	-9945	350	18x65	2079	S[1318]	-10617	170	18x65
2024	S[1263]	-9957	260	18x65	2080	S[1319]	-10629	350	18x65
2025	S[1264]	-9969	170	18x65	2081	S[1320]	-10641	260	18x65
2026	S[1265]	-9981	350	18x65	2082	S[1321]	-10653	170	18x65
2027	S[1266]	-9993	260	18x65	2083	S[1322]	-10665	350	18x65
2028	S[1267]	-10005	170	18x65	2084	S[1323]	-10677	260	18x65
2029	S[1268]	-10017	350	18x65	2085	S[1324]	-10689	170	18x65
2030	S[1269]	-10029	260	18x65	2086	S[1325]	-10701	350	18x65
2031	S[1270]	-10041	170	18x65	2087	S[1326]	-10713	260	18x65
2032	S[1271]	-10053	350	18x65	2088	S[1327]	-10725	170	18x65
2033	S[1272]	-10065	260	18x65	2089	S[1328]	-10737	350	18x65
2034	S[1273]	-10077	170	18x65	2090	S[1329]	-10749	260	18x65
2035	S[1274]	-10089	350	18x65	2091	S[1330]	-10761	170	18x65
2036	S[1275]	-10101	260	18x65	2092	S[1331]	-10773	350	18x65
2037	S[1276]	-10113	170	18x65	2093	S[1332]	-10785	260	18x65
2038	S[1277]	-10125	350	18x65	2094	S[1333]	-10797	170	18x65
2039	S[1278]	-10137	260	18x65	2095	S[1334]	-10809	350	18x65
2040	S[1279]	-10149	170	18x65	2096	S[1335]	-10821	260	18x65
2041	S[1280]	-10161	350	18x65	2097	S[1336]	-10833	170	18x65
2042	S[1281]	-10173	260	18x65	2098	S[1337]	-10845	350	18x65
2043	S[1282]	-10185	170	18x65	2099	S[1338]	-10857	260	18x65
2044	S[1283]	-10197	350	18x65	2100	S[1339]	-10869	170	18x65
2045	S[1284]	-10209	260	18x65	2101	S[1340]	-10881	350	18x65
2046	S[1285]	-10221	170	18x65	2102	S[1341]	-10893	260	18x65
2047	S[1286]	-10233	350	18x65	2103	S[1342]	-10905	170	18x65
2048	S[1287]	-10245	260	18x65	2104	S[1343]	-10917	350	18x65
2049	S[1288]	-10257	170	18x65	2105	S[1344]	-10929	260	18x65
2050	S[1289]	-10269	350	18x65	2106	S[1345]	-10941	170	18x65
2051	S[1290]	-10281	260	18x65	2107	S[1346]	-10953	350	18x65
2052	S[1291]	-10293	170	18x65	2108	S[1347]	-10965	260	18x65
2053	S[1292]	-10305	350	18x65	2109	S[1348]	-10977	170	18x65
2054	S[1293]	-10317	260	18x65	2110	S[1349]	-10989	350	18x65
2055	S[1294]	-10329	170	18x65	2111	S[1350]	-11001	260	18x65
2056	S[1295]	-10341	350	18x65	2112	S[1351]	-11013	170	18x65
2057	S[1296]	-10353	260	18x65	2113	S[1352]	-11025	350	18x65
2058	S[1297]	-10365	170	18x65	2114	S[1353]	-11037	260	18x65
2059	S[1298]	-10377	350	18x65	2115	S[1354]	-11049	170	18x65
2060	S[1299]	-10389	260	18x65	2116	S[1355]	-11061	350	18x65
2061	S[1300]	-10401	170	18x65	2117	S[1356]	-11073	260	18x65
2062	S[1301]	-10413	350	18x65	2118	S[1357]	-11085	170	18x65
2063	S[1302]	-10425	260	18x65	2119	S[1358]	-11097	350	18x65
2064	S[1303]	-10437	170	18x65	2120	S[1359]	-11109	260	18x65
2065	S[1304]	-10449	350	18x65	2121	S[1360]	-11121	170	18x65
2066	S[1305]	-10461	260	18x65	2122	S[1361]	-11133	350	18x65
2067	S[1306]	-10473	170	18x65	2123	S[1362]	-11145	260	18x65
2068	S[1307]	-10485	350	18x65	2124	S[1363]	-11157	170	18x65
2069	S[1308]	-10497	260	18x65	2125	S[1364]	-11169	350	18x65
2070	S[1309]	-10509	170	18x65	2126	S[1365]	-11181	260	18x65
2071	S[1310]	-10521	350	18x65	2127	S[1366]	-11193	170	18x65
2072	S[1311]	-10533	260	18x65	2128	S[1367]	-11205	350	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
2129	S[1368]	-11217	260	18x65	2185	S[1424]	-11889	350	18x65
2130	S[1369]	-11229	170	18x65	2186	S[1425]	-11901	260	18x65
2131	S[1370]	-11241	350	18x65	2187	S[1426]	-11913	170	18x65
2132	S[1371]	-11253	260	18x65	2188	S[1427]	-11925	350	18x65
2133	S[1372]	-11265	170	18x65	2189	S[1428]	-11937	260	18x65
2134	S[1373]	-11277	350	18x65	2190	S[1429]	-11949	170	18x65
2135	S[1374]	-11289	260	18x65	2191	S[1430]	-11961	350	18x65
2136	S[1375]	-11301	170	18x65	2192	S[1431]	-11973	260	18x65
2137	S[1376]	-11313	350	18x65	2193	S[1432]	-11985	170	18x65
2138	S[1377]	-11325	260	18x65	2194	S[1433]	-11997	350	18x65
2139	S[1378]	-11337	170	18x65	2195	S[1434]	-12009	260	18x65
2140	S[1379]	-11349	350	18x65	2196	S[1435]	-12021	170	18x65
2141	S[1380]	-11361	260	18x65	2197	S[1436]	-12033	350	18x65
2142	S[1381]	-11373	170	18x65	2198	S[1437]	-12045	260	18x65
2143	S[1382]	-11385	350	18x65	2199	S[1438]	-12057	170	18x65
2144	S[1383]	-11397	260	18x65	2200	S[1439]	-12069	350	18x65
2145	S[1384]	-11409	170	18x65	2201	S[1440]	-12081	260	18x65
2146	S[1385]	-11421	350	18x65	2202	S[1441]	-12093	170	18x65
2147	S[1386]	-11433	260	18x65	2203	S[1442]	-12105	350	18x65
2148	S[1387]	-11445	170	18x65	2204	S[1443]	-12117	260	18x65
2149	S[1388]	-11457	350	18x65	2205	S[1444]	-12129	170	18x65
2150	S[1389]	-11469	260	18x65	2206	S[1445]	-12141	350	18x65
2151	S[1390]	-11481	170	18x65	2207	S[1446]	-12153	260	18x65
2152	S[1391]	-11493	350	18x65	2208	S[1447]	-12165	170	18x65
2153	S[1392]	-11505	260	18x65	2209	S[1448]	-12177	350	18x65
2154	S[1393]	-11517	170	18x65	2210	S[1449]	-12189	260	18x65
2155	S[1394]	-11529	350	18x65	2211	S[1450]	-12201	170	18x65
2156	S[1395]	-11541	260	18x65	2212	S[1451]	-12213	350	18x65
2157	S[1396]	-11553	170	18x65	2213	S[1452]	-12225	260	18x65
2158	S[1397]	-11565	350	18x65	2214	S[1453]	-12237	170	18x65
2159	S[1398]	-11577	260	18x65	2215	S[1454]	-12249	350	18x65
2160	S[1399]	-11589	170	18x65	2216	S[1455]	-12261	260	18x65
2161	S[1400]	-11601	350	18x65	2217	S[1456]	-12273	170	18x65
2162	S[1401]	-11613	260	18x65	2218	S[1457]	-12285	350	18x65
2163	S[1402]	-11625	170	18x65	2219	S[1458]	-12297	260	18x65
2164	S[1403]	-11637	350	18x65	2220	S[1459]	-12309	170	18x65
2165	S[1404]	-11649	260	18x65	2221	S[1460]	-12321	350	18x65
2166	S[1405]	-11661	170	18x65	2222	S[1461]	-12333	260	18x65
2167	S[1406]	-11673	350	18x65	2223	S[1462]	-12345	170	18x65
2168	S[1407]	-11685	260	18x65	2224	S[1463]	-12357	350	18x65
2169	S[1408]	-11697	170	18x65	2225	S[1464]	-12369	260	18x65
2170	S[1409]	-11709	350	18x65	2226	S[1465]	-12381	170	18x65
2171	S[1410]	-11721	260	18x65	2227	S[1466]	-12393	350	18x65
2172	S[1411]	-11733	170	18x65	2228	S[1467]	-12405	260	18x65
2173	S[1412]	-11745	350	18x65	2229	S[1468]	-12417	170	18x65
2174	S[1413]	-11757	260	18x65	2230	S[1469]	-12429	350	18x65
2175	S[1414]	-11769	170	18x65	2231	S[1470]	-12441	260	18x65
2176	S[1415]	-11781	350	18x65	2232	S[1471]	-12453	170	18x65
2177	S[1416]	-11793	260	18x65	2233	S[1472]	-12465	350	18x65
2178	S[1417]	-11805	170	18x65	2234	S[1473]	-12477	260	18x65
2179	S[1418]	-11817	350	18x65	2235	S[1474]	-12489	170	18x65
2180	S[1419]	-11829	260	18x65	2236	S[1475]	-12501	350	18x65
2181	S[1420]	-11841	170	18x65	2237	S[1476]	-12513	260	18x65
2182	S[1421]	-11853	350	18x65	2238	S[1477]	-12525	170	18x65
2183	S[1422]	-11865	260	18x65	2239	S[1478]	-12537	350	18x65
2184	S[1423]	-11877	170	18x65	2240	S[1479]	-12549	260	18x65

No.	Name	X	Y	Bump size(um)	No.	Name	X	Y	Bump size(um)
2241	S[1480]	-12561	170	18x65	2297	S[1536]	-13233	260	18x65
2242	S[1481]	-12573	350	18x65	2298	S[1537]	-13245	170	18x65
2243	S[1482]	-12585	260	18x65	2299	DUMMY	-13257	350	18x65
2244	S[1483]	-12597	170	18x65	2300	DUMMY	-13293	350	18x65
2245	S[1484]	-12609	350	18x65	2301	DUMMY	-13329	350	18x65
2246	S[1485]	-12621	260	18x65	2302	DUMMY	-13365	350	18x65
2247	S[1486]	-12633	170	18x65	2303	DUMMY	-13401	350	18x65
2248	S[1487]	-12645	350	18x65	2304	DUMMY	-13437	350	18x65
2249	S[1488]	-12657	260	18x65	2305	DUMMY	-13473	350	18x65
2250	S[1489]	-12669	170	18x65	2306	DUMMY	-13509	350	18x65
2251	S[1490]	-12681	350	18x65	2307	DUMMY	-13545	350	18x65
2252	S[1491]	-12693	260	18x65	2308	DUMMY	-13581	350	18x65
2253	S[1492]	-12705	170	18x65	2309	PASS1_R	-13617	350	18x65
2254	S[1493]	-12717	350	18x65	2310	PASS1_R	-13653	350	18x65
2255	S[1494]	-12729	260	18x65	2311	PASS1_R	-13689	350	18x65
2256	S[1495]	-12741	170	18x65	2312	PASS1_R	-13725	350	18x65
2257	S[1496]	-12753	350	18x65	2313	DUMMY	-13761	350	18x65
2258	S[1497]	-12765	260	18x65	2314	PASS2_R	-13797	350	18x65
2259	S[1498]	-12777	170	18x65	2315	PASS2_R	-13833	350	18x65
2260	S[1499]	-12789	350	18x65	2316	PASS2_R	-13869	350	18x65
2261	S[1500]	-12801	260	18x65	2317	PASS2_R	-13905	350	18x65
2262	S[1501]	-12813	170	18x65	2318	DUMMY	-13941	350	18x65
2263	S[1502]	-12825	350	18x65	2297	S[1536]	-13233	260	18x65
2264	S[1503]	-12837	260	18x65	2298	S[1537]	-13245	170	18x65
2265	S[1504]	-12849	170	18x65	2299	DUMMY	-13257	350	18x65
2266	S[1505]	-12861	350	18x65	2300	DUMMY	-13293	350	18x65
2267	S[1506]	-12873	260	18x65	2301	DUMMY	-13329	350	18x65
2268	S[1507]	-12885	170	18x65	2302	DUMMY	-13365	350	18x65
2269	S[1508]	-12897	350	18x65	2303	DUMMY	-13401	350	18x65
2270	S[1509]	-12909	260	18x65	2304	DUMMY	-13437	350	18x65
2271	S[1510]	-12921	170	18x65	2305	DUMMY	-13473	350	18x65
2272	S[1511]	-12933	350	18x65	2306	DUMMY	-13509	350	18x65
2273	S[1512]	-12945	260	18x65	2307	DUMMY	-13545	350	18x65
2274	S[1513]	-12957	170	18x65	2308	DUMMY	-13581	350	18x65
2275	S[1514]	-12969	350	18x65	2309	PASS1_R	-13617	350	18x65
2276	S[1515]	-12981	260	18x65	2310	PASS1_R	-13653	350	18x65
2277	S[1516]	-12993	170	18x65	2311	PASS1_R	-13689	350	18x65
2278	S[1517]	-13005	350	18x65	2312	PASS1_R	-13725	350	18x65
2279	S[1518]	-13017	260	18x65	2313	DUMMY	-13761	350	18x65
2280	S[1519]	-13029	170	18x65	2314	PASS2_R	-13797	350	18x65
2281	S[1520]	-13041	350	18x65	2315	PASS2_R	-13833	350	18x65
2282	S[1521]	-13053	260	18x65	2316	PASS2_R	-13869	350	18x65
2283	S[1522]	-13065	170	18x65	2317	PASS2_R	-13905	350	18x65
2284	S[1523]	-13077	350	18x65	2318	DUMMY	-13941	350	18x65
2285	S[1524]	-13089	260	18x65					
2286	S[1525]	-13101	170	18x65					
2287	S[1526]	-13113	350	18x65					
2288	S[1527]	-13125	260	18x65					
2289	S[1528]	-13137	170	18x65					
2290	S[1529]	-13149	350	18x65					
2291	S[1530]	-13161	260	18x65					
2292	S[1531]	-13173	170	18x65					
2293	S[1532]	-13185	350	18x65					
2294	S[1533]	-13197	260	18x65					
2295	S[1534]	-13209	170	18x65					
2296	S[1535]	-13221	350	18x65					

14. Revision History

Reversion	Content	Date
0.0.1	New SPEC	2023/11/27
0.0.2	Remove VDD18V_BPS function(p12)	2024/04/02