JADARD

JD9365DA-H3

User Guide

Preliminary Version 0.00
2020/8/27

INDEX LIST:

Table List:

1. Revision History

Version	Date	Description of modification
0.00	2020/08/27	New setup

2. Jadard Command List

2.1. ALL page

Index	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
E0	SET_PAGE	R/W	-	-	-	-	-	PAGE[2:0]			**00**
E1	SET_PASSWD	R/W	PASSWD1[7:0]								**00**
E2		R/W	PASSWD2[7:0]								**00**
E3		R/W	PASSWD3[7:0]								**00**
E4	AUTO_DISP_SETTING	R/W	-	-	-	-	GON	DTE	DISP[1:0]		**08**
E5		R/W	-	-	DISP_SW_OPT[1:0]		-	BLK_DISABLE	BLK_MODE[1:0]		**01**
E6	SET_WD	R/W	-	-	-	-	-	-	WD_MODE[1:0]		**02**
E7		R/W	-	-	-	WD_off	WD_Timer[3:0]				**0C**
E8		R	-	-	-	-	-	-	WD_FMS	WD_FBLK	**00**
E9	OTP_PROG	R/W	OTP_MASK[7:0]								00
EA		R/W	-	-	-	-	-	-	OTP_INDEX[9:8]		00
EB		R/W	OTP_INDEX[7:0]								00
EC		R/W	-	-	-	OTP_READ_SINGLE	OTP_WRITE_SINGLE	OTP_LOAD_DISABLE	OTP_INT_VPP	OTP_AUTO_PROG	00
ED		R	OTP_RDATA[7:0]								-
EE		R/W	OTP_WDATA[7:0]								00
EF		R/W	OTP_PPROG	OTP_VPP_SEL	OTP_PRD	OTP_PWE	-	-	OTP_PTM[1:0]		00
F0	SELF_DIAG	R	regload_detec	func_detec	attach_detec	gbreak_detec	-	-	-	-	**00**
F1	SPI_CMD	R/W	SPI_CMD_INDEX[7:0]								**00**
F2	SPI_READ	R	SPI_READ_DATA[7:0]								**00**
F8	DSI_RESERVED2	W	DSI_RES2[7:0]								**00**
F9	DSI_RESERVED3	W	DSI_RES3[7:0]								**00**

TABLE 2.1: JADARD ALL PAGE COMMAND LIST

2.2. Jadard page 0 command

Index	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
1B	RDCUSTM_ID	R	CUSTM1[7:0]								FF
		R	CUSTM2[7:0]								FF
		R	CUSTM3[7:0]								FF
		R	CUSTM4[7:0]								FF
		R	CUSTM5[7:0]								FF
		R	CUSTM6[7:0]								FF
		R	CUSTM7[7:0]								FF
		R	CUSTM8[7:0]								FF
70	SEQUENCE_CTRL	R/W	-	DC0H[2:0]			-	DC1H[2:0]			01
71		R/W	-	DC2H[2:0]			-	DC3H[2:0]			23
72		R/W	-	-	-	-	-	DC7H[2:0]			06
73		R/W	DC0L	DC1L	DC2L	DC3L	DC4L	DC5L	DC6L	DC7L	88
74		R/W	T0P[1:0]		T1P[1:0]		T8P[1:0]		-	-	64
75		R/W	-	SOFT0H[2:0]			-	SOFT0L[2:0]			06
76		R	-	-	-	-	-	-	-	POW_ON_STATE	00
77	SETID(OTP*5)	R/W	-	-	-	-	-	-	-	-	00
78		R/W	ID1[7:0]								00
79		R/W	ID2[7:0]								00
7A		R/W	ID3[7:0]								00
7B		R/W	ID4[7:0]								00
7C		R	-	-	-	-	-	ID_OTP_TIMES[2:0]			00
80	SETDSISETUP	R/W	-	DSI_INIT0[6:0]							03
81		R/W	DSI_INIT1[7:0]								28
82		R/W	DSI_INIT2[7:0]								07
83	SETDSISETUP2	R/W	-	DSI_INIT3[6:0]							0F
84	UP_START_CTRL	R/W	UP_KEY1[7:0]								00
85		R/W	UP_KEY2[7:0]								00
86		R/W	UP_START_EN[7:0]								00
87		R/W	PWR_KEY[7:0]								00
88	SET_ALS	R/W	ALS[31:24]								00

89		R/W	ALS[23:16]	**00**
8A		R/W	ALS[15:8]	**00**
8B		R/W	ALS[7:0]	**00**

TABLE 2.2: JADARD PAGE 0 COMMAND LIST

2.3. Jadard page 1 command

Index	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
00	VCOM_SET(OTP*5)	R/W	-	-	-	VCOMS_BP	-	-	VCOM_S[9:8]		00
01		R/W	VCOM_S[7:0]								46
02		R	-	-	-	-	-	VCOM_OTP_TIMES[2:0]			00
03	VCOM_R_SET(OTP*5)	R/W	-	-	-	VCOM_R_SEN	-	-	VCOM_R_S[9:8]		00
04		R/W	VCOM_R_S[7:0]								32
05		R	-	-	-	-	-	VCOM_R_OTP_TIMES[2:0]			00
0A	PWRIC_SET	R/W	-	-	JD_RELD	VCSW_SWAP	EN_VREF_S[3:0]				08
0B		R/W	PWRIC_SET[7:0]								00
0C		R/W	-	PWRIC_CLK1[2:0]			-	PWRIC_IDLE_CLK1[2:0]			54
0D		R/W	HX_SOFT	PWRIC_CLK2[2:0]			PWRIC_HXCLK[3:0]				E3
0E		R/W	HX_DT_AVDD	-	-	-	-	-	LED_PWR_S[1:0]		00
17	GAMMA_SET	R/W	-	-	-	VGMP_S[8]	-	-	-	VGSP_S[8]	00
18		R/W	VGMP_S[7:0]								BF
19		R/W	VGSP_S[7:0]								11
1A		R/W	-	-	-	VGMN_S[8]	-	-	-	VGSN_S[8]	00
1B		R/W	VGMN_S[7:0]								BF
1C		R/W	VGSN_S[7:0]								11
1D	OTP_SET	R/W	-	-	VPP_DT[1:0]		-	VPP_VGH_RT[2:0]			01
1E		R/W	-	VPP_VGH_S[6:0]							03
1F	GATE_POWER	R/W	-	VGH_REG_S[6:0]							34
20		R/W	-	-	VGL_REG_S[5:0]						23
21		R/W	-	-	VGL_REG2_S[5:0]						19
22		R/W	-	VGH_REG_SHT	VGL_REG_SHT	VGL_REG2_SHT	VGH_REG_EN	VGL_REG_EN	VGL_REG2_EN	SHT_VGL_REG	0E
23	DCDC_CTRL	R/W	-	-	GAS_VGH_EN	GAS_VGL_EN	VGH_NC	VGL_NC	VCLREG_OP_CEN	VCL_NC	30
24		R/W	VGHEN	VGLEN	AVDDEN	AVEEEN	VCLEN	VDDAEN	VCLREG_EN	VCL2VDDN	FE
25	POWAMP_CTRL	R/W	-	AP[2:0]			-	-	-	-	30
26		R/W	VCOM_EN	VGM_EN	-	GAS_DET_SEL	GAS_IOVCC_EN	GAS_VCI_EN	GAS_AVEE_EN	GAS_OUT_EN	CF

27		R/W	UP_VDD_1P8_EN	VDDD_S1[2:0]			-	VDDD_S2[2:0]			**33**
28	DCDC_CTRL2	R/W	-	PWR_SW_EN	VGH_MSF_EN	VGH_CHG2AVDD_EH	VGH_GAS_PWS_EN	VGH_PWS	VGH_PWS_GND	VGH_PWS_POS	**04**
29		R/W			GAS_T8P[1:0]		VGH_SGL_C41	VGH_SGL_C42	-	-	**00**
2A		R/W	DDS[7:0]								**00**
35	SETSTBA	R/W	-	GAP[2:0]			SAP[3:0]				**23**
36		R/W	SAP_Temp[3:0]				SAP2[3:0]				**53**
37	SETPANEL	R/W	-	Z_line	ENZ[1:0]		SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	**00**
38	SETRGBCYC	R/W	-	-	-	-	-	RGB_JDT[2:0]			**04**
39		R/W	RGB_N_EQ1[7:0]								**0C**
3A		R/W	RGB_N_EQ2[7:0]								**18**
3B		R/W	RGB_N_EQ2_Temp[7:0]								**18**
3C		R/W	RGB_N_EQ3[7:0]								**80**
3D		R/W	RGB_CHGEN_ON[7:0]								**0C**
3E		R/W	RGB_CHGEN_OFF[7:0]								**80**
3F		R/W	RGB_CHGEN_OFF2[7:0]								**4E**

40	SET_TCON	R/W	-	IP750_1	LN[1:0]		IP750_0	RSO[2:0]					**04**
41		R/W	LN[9:2]										**A0**
42		R/W	SLT[7:0]										**81**
43		R/W	VFP[7:0]										**0E**
44		R/W	VBP[7:0]										**0A**
45		R/W	HBP[7:0]										**16**
46		R/W	TE_Delay[10:3]										**00**
47		R/W	BlkinF_num[7:0]										**00**
48		R/W	BlkinF_STR[7:0]										**00**
49		R/W	BlkinFrame	BlkinF_hsync	-	-	-	TE_Delay[2:0]					**40**
4A		R/W	FRAME_NUM[1:0]		Auto_Test_en	TEST_PAT_EN	TEST_PATTERN[3:0]						**80**
4B		R/W	TCON_OPT1[15:8]										**00**
4C		R/W	TCON_OPT1[7:0]										**00**
4D	SET_TE_PAD	R/W	-	-	-	-	-	-	-	-			**00**
4E		R/W	-	-	-	-	TP_VS_EN	TP_VS_WIDTH[10:8]					**0D**
4F		R/W	TP_VS_WIDTH[7:0]										**00**
50		R/W	TP_VS_SHIFT[7:0]										**14**
51		R/W	-	-	-	-	-	-	TP_HS_BLK_EN	TP_HS_DIS_EN			**01**
52		R/W	TP_HS_ON[7:0]										**48**
53		R/W	TP_HS_OFF[7:0]										**70**
54	POWER_STATE	R/W	-	-	-	-	-	-	-	DSTBY			**00**
55	DCDC_SEL	R/W	-	-	-	-	DCDCM[3:0]						**05**
56		R/W	-	-	-	-	AUTO_RT	-	AVDD_RT[1:0]				**01**
57		R/W	VGH_RT[2:0]			VGL_RT[2:0]			VCL_RT[1:0]				**29**
58		R/W	-	-	-	AVDD_S[4:0]							**0A**
59		R/W	VCL_S[2:0]			AVEE_S[4:0]							**0A**
5A		R/W	-	VGH_S[6:0]									**28**
5B		R/W	-	-	VGL_S[5:0]								**19**
5C		R/W	-	-	VDDA_CLK[1:0]	VCL_CLK[1:0]	VGHVGL_CLK[1:0]						**15**
5D	SET_GAMMA	R/W	-	RPA18[6:0]									**7C**
5E		R/W	-	RPA17[6:0]									**6D**

5F		R/W	-	RPA16[6:0]	63
60		R/W	-	RPA15[6:0]	59
61		R/W	-	RPA14[6:0]	57
62		R/W	-	RPA13[6:0]	4A
63		R/W	-	RPA12[6:0]	51
64		R/W	-	RPA11[6:0]	3A
65		R/W	-	RPA10[6:0]	55
66		R/W	-	RPA9[6:0]	53
67		R/W	-	RPA8[6:0]	55
68		R/W	-	RPA7[6:0]	7A
69		R/W	-	RPA6[6:0]	6F
6A		R/W	-	RPA5[6:0]	7F
6B		R/W	-	RPA4[6:0]	75
6C		R/W	-	RPA3[6:0]	72
6D		R/W	-	RPA2[6:0]	62
6E		R/W	-	RPA1[6:0]	2D
6F		R/W	-	RPA0[6:0]	06
70		R/W	-	RNA18[6:0]	7C
71		R/W	-	RNA17[6:0]	6D
72		R/W	-	RNA16[6:0]	63
73		R/W	-	RNA15[6:0]	59
74		R/W	-	RNA14[6:0]	57
75		R/W	-	RNA13[6:0]	4A
76		R/W	-	RNA12[6:0]	51
77		R/W	-	RNA11[6:0]	3A
78		R/W	-	RNA10[6:0]	55
79		R/W	-	RNA9[6:0]	53
7A		R/W	-	RNA8[6:0]	55
7B		R/W	-	RNA7[6:0]	7A
7C		R/W	-	RNA6[6:0]	6F
7D		R/W	-	RNA5[6:0]	7F
7E		R/W	-	RNA4[6:0]	75
7F		R/W	-	RNA3[6:0]	72
80		R/W	-	RNA2[6:0]	62
81		R/W	-	RNA1[6:0]	2D

82		R/W	-	RNA0[6:0]							**06**
83	SETDDB	R/W	-	-	-	-	-	-	-	-	**00**
84		R/W	DDB1[7:0]								**00**
85		R/W	DDB2[7:0]								**00**
86		R/W	DDB3[7:0]								**00**
87		R/W	DDB4[7:0]								**00**
88	SETECO	R/W	-	-	-	-	-	-	-	-	**00**
89		R/W	ECO0[7:0]								**03**
8A		R/W	ECO1[7:0]								**00**
8B		R/W	-	ECO2[6:0]							**00**
8C		R/W	-	ECO3[6:0]							**00**
8D	GET_ID_VERSION	R	JD_ID1[7:0]								**93**
8E		R	JD_ID2[7:0]								**65**
8F		R	JD_ID3[7:0]								**0E**
93	DCS_CMD_OPT	R/W	-	-	-	-	-	-	-	NOKIA_CMD_EN	**00**
94		R/W	-	-	-	-	-	-	-	RDCTMOTP_EN	**00**
95	CTM_OTP	R/W	-	-	-	OTP_WR_FLAG	OTP_RD_LENGTH[3:0]				**0E**
96		R/W	CTM_OTP0[7:0]								**00**
97		R/W	CTM_OTP1[7:0]								**00**
98		R/W	CTM_OTP2[7:0]								**00**
99		R/W	CTM_OTP3[7:0]								**00**
9A		R/W	CTM_OTP4[7:0]								**00**
9B		R/W	CTM_OTP5[7:0]								**00**
9C		R/W	CTM_OTP6[7:0]								**00**
9D		R/W	CTM_OTP7[7:0]								**00**
9E		R/W	CTM_OTP8[7:0]								**00**
9F		R/W	CTM_OTP9[7:0]								**00**
A0		R/W	CTM_OTP10[7:0]								**00**
A1		R/W	CTM_OTP11[7:0]								**00**
A2		R/W	CTM_OTP12[7:0]								**00**
A3		R/W	CTM_OTP13[7:0]								**00**
A4		R/W	CTM_OTP14[7:0]								**00**
A5		R/W	CTM_OTP15[7:0]								**00**
A6	SETCUSTM_	R/W	-	-	-	-	-	-	-	-	**00**

A7	ID	R/W	CUSTM1[7:0]						**FF**
A8		R/W	CUSTM2[7:0]						**FF**
A9		R/W	CUSTM3[7:0]						**FF**
AA		R/W	CUSTM4[7:0]						**FF**
AB		R/W	CUSTM5[7:0]						**FF**
AC		R/W	CUSTM6[7:0]						**FF**
AD		R/W	CUSTM7[7:0]						**FF**
AE		R/W	CUSTM8[7:0]						**FF**
AF	SET_TE_PAD2	R/W	-	-	-	VHS_TEON_OPT	TP_VS_EN2	TP_VS_WIDTH2[10:8]	**05**
B0		R/W	TP_VS_WIDTH2[7:0]						**00**
B1		R/W	TP_VS_SHIFT2[7:0]						**01**
B2	OTP_REPAIR		-	-	-	-	REPAIR_PAGE[3:0]		**00**
B3			REPAIR_INDEX[7:0]						**00**
B4			REPAIR_PAR[7:0]						**00**
B5			REPAIR_VALUE[7:0]						**00**
B6	SETRGBCYC3		-	RES_MUX_ON[6:0]					**00**
B7			-	RES_MUX_OFF[6:0]					**20**
B8			DYNBIAS_ON[7:0]						**00**
B9			DYNBIAS_OFF[7:0]						**20**
BA			DYNCHGEN_ON[7:0]						**10**
BB			DYNCHGEN_OFF[7:0]						**30**

TABLE 2.3: JADARD PAGE 1 COMMAND LIST

2.4. Jadard page 2 command

Index	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
00	SET_GIP_L	R/W	-	CGO1_PH_L	CGO1_INV_L	CGOUT1_L[4:0]					0A
01		R/W	-	CGO2_PH_L	CGO2_INV_L	CGOUT2_L[4:0]					08
02		R/W	-	CGO3_PH_L	CGO3_INV_L	CGOUT3_L[4:0]					06
03		R/W	-	CGO4_PH_L	CGO4_INV_L	CGOUT4_L[4:0]					04
04		R/W	-	CGO5_PH_L	CGO5_INV_L	CGOUT5_L[4:0]					00
05		R/W	-	CGO6_PH_L	CGO6_INV_L	CGOUT6_L[4:0]					1F
06		R/W	-	CGO7_PH_L	CGO7_INV_L	CGOUT7_L[4:0]					1F
07		R/W	-	CGO8_PH_L	CGO8_INV_L	CGOUT8_L[4:0]					1F
08		R/W	-	CGO9_PH_L	CGO9_INV_L	CGOUT9_L[4:0]					1F
09		R/W	-	CGO10_PH_L	CGO10_INV_L	CGOUT10_L[4:0]					1F
0A		R/W	-	CGO11_PH_L	CGO11_INV_L	CGOUT11_L[4:0]					1F
0B		R/W	-	CGO12_PH_L	CGO12_INV_L	CGOUT12_L[4:0]					1F
0C		R/W	-	CGO13_PH_L	CGO13_INV_L	CGOUT13_L[4:0]					1F
0D		R/W	-	CGO14_PH_L	CGO14_INV_L	CGOUT14_L[4:0]					1F
0E		R/W	-	CGO15_PH_L	CGO15_INV_L	CGOUT15_L[4:0]					1F
0F		R/W	-	CGO16_PH_L	CGO16_INV_L	CGOUT16_L[4:0]					1F
10		R/W	-	CGO17_PH_L	CGO17_INV_L	CGOUT17_L[4:0]					1F
11		R/W	-	CGO18_PH_L	CGO18_INV_L	CGOUT18_L[4:0]					1F
12		R/W	-	CGO19_PH_L	CGO19_INV_L	CGOUT19_L[4:0]					17
13		R/W	-	CGO20_PH_L	CGO20_INV_L	CGOUT20_L[4:0]					18
14		R/W	-	CGO21_PH_L	CGO21_INV_L	CGOUT21_L[4:0]					1F
15		R/W	-	CGO22_PH_L	CGO22_INV_L	CGOUT22_L[4:0]					1F
16	SET_GIP_R	R/W	-	CGO1_PH_R	CGO1_INV_R	CGOUT1_R[4:0]					0B
17		R/W	-	CGO2_PH_R	CGO2_INV_R	CGOUT2_R[4:0]					09
18		R/W	-	CGO3_PH_R	CGO3_INV_R	CGOUT3_R[4:0]					07
19		R/W	-	CGO4_PH_R	CGO4_INV_R	CGOUT4_R[4:0]					05
1A		R/W	-	CGO5_PH_R	CGO5_INV_R	CGOUT5_R[4:0]					01
1B		R/W	-	CGO6_PH_R	CGO6_INV_R	CGOUT6_R[4:0]					1F
1C		R/W	-	CGO7_PH_R	CGO7_INV_R	CGOUT7_R[4:0]					1F
1D		R/W	-	CGO8_PH_R	CGO8_INV_R	CGOUT8_R[4:0]					1F
1E		R/W	-	CGO9_PH_R	CGO9_INV_R	CGOUT9_R[4:0]					1F
1F		R/W	-	CGO10_PH_R	CGO10_INV_R	CGOUT10_R[4:0]					1F
20		R/W	-	CGO11_PH_R	CGO11_INV_R	CGOUT11_R[4:0]					1F
21		R/W	-	CGO12_PH_R	CGO12_INV_R	CGOUT12_R[4:0]					1F
22		R/W	-	CGO13_PH_R	CGO13_INV_R	CGOUT13_R[4:0]					1F

23		R/W	-	CGO14_PH_R	CGO14_INV_R	CGOUT14_R[4:0]	**1F**
24		R/W	-	CGO15_PH_R	CGO15_INV_R	CGOUT15_R[4:0]	**1F**
25		R/W	-	CGO16_PH_R	CGO16_INV_R	CGOUT16_R[4:0]	**1F**
26		R/W	-	CGO17_PH_R	CGO17_INV_R	CGOUT17_R[4:0]	**1F**
27		R/W	-	CGO18_PH_R	CGO18_INV_R	CGOUT18_R[4:0]	**1F**
28		R/W	-	CGO19_PH_R	CGO19_INV_R	CGOUT19_R[4:0]	**17**
29		R/W	-	CGO20_PH_R	CGO20_INV_R	CGOUT20_R[4:0]	**18**
2A		R/W	-	CGO21_PH_R	CGO21_INV_R	CGOUT21_R[4:0]	**1F**
2B		R/W	-	CGO22_PH_R	CGO22_INV_R	CGOUT22_R[4:0]	**1F**
2C	SET_GIP_L_GS	R/W	-	-	-	CGOUT1_L_GS[4:0]	**09**
2D		R/W	-	-	-	CGOUT2_L_GS[4:0]	**0B**
2E		R/W	-	-	-	CGOUT3_L_GS[4:0]	**05**
2F		R/W	-	-	-	CGOUT4_L_GS[4:0]	**07**
30		R/W	-	-	-	CGOUT5_L_GS[4:0]	**1F**
31		R/W	-	-	-	CGOUT6_L_GS[4:0]	**01**
32		R/W	-	-	-	CGOUT7_L_GS[4:0]	**1F**
33		R/W	-	-	-	CGOUT8_L_GS[4:0]	**1F**
34		R/W	-	-	-	CGOUT9_L_GS[4:0]	**1F**
35		R/W	-	-	-	CGOUT10_L_GS[4:0]	**1F**
36		R/W	-	-	-	CGOUT11_L_GS[4:0]	**1F**
37		R/W	-	-	-	CGOUT12_L_GS[4:0]	**1F**
38		R/W	-	-	-	CGOUT13_L_GS[4:0]	**1F**
39		R/W	-	-	-	CGOUT14_L_GS[4:0]	**1F**
3A		R/W	-	-	-	CGOUT15_L_GS[4:0]	**1F**
3B		R/W	-	-	-	CGOUT16_L_GS[4:0]	**1F**
3C		R/W	-	-	-	CGOUT17_L_GS[4:0]	**1F**
3D		R/W	-	-	-	CGOUT18_L_GS[4:0]	**1F**
3E		R/W	-	-	-	CGOUT19_L_GS[4:0]	**17**
3F		R/W				CGOUT20_L_GS[4:0]	**18**
40		R/W				CGOUT21_L_GS[4:0]	**1F**
41		R/W	-	-	-	CGOUT22_L_GS[4:0]	**1F**

42	SET_GIP_R_GS	R/W	-	-	-	CGOUT1_R_GS[4:0]		08
43		R/W	-	-	-	CGOUT2_R_GS[4:0]		0A
44		R/W	-	-	-	CGOUT3_R_GS[4:0]		04
45		R/W	-	-	-	CGOUT4_R_GS[4:0]		06
46		R/W	-	-	-	CGOUT5_R_GS[4:0]		1F
47		R/W	-	-	-	CGOUT6_R_GS[4:0]		00
48		R/W	-	-	-	CGOUT7_R_GS[4:0]		1F
49		R/W	-	-	-	CGOUT8_R_GS[4:0]		1F
4A		R/W	-	-	-	CGOUT9_R_GS[4:0]		1F
4B		R/W	-	-	-	CGOUT10_R_GS[4:0]		1F
4C		R/W	-	-	-	CGOUT11_R_GS[4:0]		1F
4D		R/W	-	-	-	CGOUT12_R_GS[4:0]		1F
4E		R/W	-	-	-	CGOUT13_R_GS[4:0]		1F
4F		R/W	-	-	-	CGOUT14_R_GS[4:0]		1F
50		R/W	-	-	-	CGOUT15_R_GS[4:0]		1F
51		R/W	-	-	-	CGOUT16_R_GS[4:0]		1F
52		R/W	-	-	-	CGOUT17_R_GS[4:0]		1F
53		R/W	-	-	-	CGOUT18_R_GS[4:0]		1F
54		R/W	-	-	-	CGOUT19_R_GS[4:0]		17
55		R/W	-	-	-	CGOUT20_R_GS[4:0]		18
56		R/W	-	-	-	CGOUT21_R_GS[4:0]		1F
57		R/W	-	-	-	CGOUT22_R_GS[4:0]		1F
58	SETGIP1	R/W	-	GIP_GAS_OPT	TGEQL	GIP_RST_EN	INIT_PORCH[3:0]	40
59		R/W	INIT_W[3:0]			-	INIT[10:8]	00
5A		R/W	INIT[7:0]					00
5B		R/W	-	-	STV_NUM[1:0]	-	- - - -	10
5C		R/W	STV_S0[7:0]					02
5D		R/W	STV_W[3:0]			-	STV_S1[2:0]	10
5E		R/W	-	-	-	STV_S2[4:0]		01
5F		R/W	-	-	-	STV_S3[4:0]		02
60		R/W	ETV_W[3:0]			-	ETV_S1[2:0]	00
61		R/W	-	-	-	ETV_S2[4:0]		01
62		R/W	-	-	-	ETV_S3[4:0]		02
63		R/W	SETV_ON[7:0]					03
64		R/W	SETV_OFF[7:0]					7B
65		R/W		ETV_EN	ETV_NUM[1:0]	-	ETV_S0[10:8]	15
66		R/W	ETV_S0[7:0]					00

67		R/W	CKV0_NUM[3:0]					CKV0_W[3:0]			**71**
68		R/W	CKV0_S0[7:0]								**04**
69		R/W	CKV0_ON[7:0]								**06**
6A		R/W	CKV0_OFF[7:0]								**7B**
6B		R/W	CKV0_DUM[7:0]								**10**
6C	SETGIP2	R/W	-	-	FLM_MODE	GEQ_LINE	GEQ_W[3:0]				**00**
6D		R/W	-	-	GEQ_GGND1[5:0]						**04**
6E		R/W	-	-	GEQ_GGND2[5:0]						**04**
6F		R/W	GIPDR[1:0]		VGHO_SEL	VGLO_SEL	VGLO_SEL2	CKV_GROUP	CKV1_CON	CKV0_CON	**88**
70		R/W	CKV1_NUM[3:0]					CKV1_W[3:0]			**00**
71		R/W	CKV1_S0[7:0]								**00**
72		R/W	CKV1_ON[7:0]								**06**
73		R/W	CKV1_OFF[7:0]								**7B**
74		R/W	CKV1_DUM[7:0]								**00**
75		R/W	FLM_EN	FLM_W[6:0]							**87**
76		R/W	FLM_ON[7:0]								**00**
77		R/W	VEN_EN	VEN_W[10:8]			FLM_NUM	FLM_OFF[10:8]			**5D**
78		R/W	FLM_OFF[7:0]								**17**
79		R/W	VEN_W[7:0]								**1F**
7A		R/W	VEN_S0[7:0]								**00**
7B		R/W	VEN_S1[7:0]								**00**
7C		R/W	VEN_DUM[7:0]								**00**
7D		R/W	VEN_ON[7:0]								**03**
7E		R/W	VEN_OFF[7:0]								**7B**
7F	SET_GIP_OPT	R/W	-	GIP_OPT0[6:0]							**00**
80		R/W	GIP_OPT1[7:0]								**00**

81	SET_GIP_TEMP	R/W	-	FLM_EQ	ETV_BLK_S0[10:8]	STV_BLK_S0[10:8]	**00**
82		R/W	STV_BLK_S0[7:0]				**00**
83		R/W	ETV_BLK_S0[7:0]				**00**
84		R/W	STV_BLK_S2[3:0]		STV_BLK_S1[3:0]		**00**
85		R/W	STV_OPT[3:0]		STV_BLK_S3[3:0]		**00**
86		R/W	ETV_BLK_S2[3:0]		ETV_BLK_S1[3:0]		**00**
87		R/W	ETV_OPT[3:0]		ETV_BLK_S3[3:0]		**00**
88		R/W	FLM_ON_TU[7:0]				**00**
89		R/W	FLM_OFF_TU[7:0]				**00**
8B	SET_GIP_BIF	R/W	-	GIP_OPT2[4:0]		CKV_BIF_S[9:8]	**00**
8C		R/W	CKV_BIF_S[7:0]				**00**
8D		R/W	CKV_BIF_W[7:0]				**00**
8E	SETGIP3	R/W	-	GIP_OPT3[4:0]		FLM_ON_LRN_EN / FLM_OFF_LRN_EN	**01**
8F		R/W	AGON_EN	AGON_OPT	AGON_LINE0	AGON_LINE1 / AGON_DLY[3:0]	**02**
90		R/W	AGON_S[3:0]			AGON_W[3:0]	**03**
91		R/W	AGON_ON0[7:0]				**08**
92		R/W	AGON_ON1[7:0]				**08**

TABLE 2.4: JADARD PAGE 2 COMMAND LIST

2.5. Jadard page 3 command

Index	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
00	CE_CTRL0	R/W	-	-	-	-	-	-	-	CE_OTP_ROM_VLD	01
01	CE_CTRL1	R/W	-	-	-	-	CE_EDG_MODE[1:0]		CE_SAT_MODE[1:0]		00
02	CE_PRM	R/W	-	-	-	CE_EDG_SP_PROT	CE_SAT_SP_PROT	CE_COL_EN	CE_HUE_EN	CE_VV_EN	-
03		R/W	-	CE_THREF[2:0]			-	CE_THSAT[2:0]			-
04		R/W	-	CE_THGREY[2:0]			-	CE_THCOLOR[2:0]			-
05		R/W	CE_SAT_OFFS[7:0]								-
06		R/W	CE_REF_OFFS[7:0]								-
07		R/W	-	-	-	-	-	CE_THCOLOR2[2:0]			-
08		R/W	CE_COL_OFFS[7:0]								-
09		R/W	CE_SG016[3:0]				CE_SG000[3:0]				-
0A		R/W	CE_SG048[3:0]				CE_SG032[3:0]				-
0B		R/W	CE_SG080[3:0]				CE_SG064[3:0]				-
0C		R/W	CE_SG112[3:0]				CE_SG096[3:0]				-
0D		R/W	CE_SG144[3:0]				CE_SG128[3:0]				-
0E		R/W	CE_SG176[3:0]				CE_SG160[3:0]				-
0F		R/W	CE_SG208[3:0]				CE_SG192[3:0]				-
10		R/W	CE_SG240[3:0]				CE_SG224[3:0]				-
11		R/W	-	-	-	-	CE_SG255[3:0]				-
12		R/W	-	-	CE_HUE_TBL00[5:0]						-
13		R/W	-	-	CE_HUE_TBL01[5:0]						-
14		R/W	-	-	CE_HUE_TBL02[5:0]						-
15		R/W	-	-	CE_HUE_TBL03[5:0]						-
16		R/W	-	-	CE_HUE_TBL04[5:0]						-
17		R/W	-	-	CE_HUE_TBL05[5:0]						-
18		R/W	-	-	CE_HUE_TBL06[5:0]						-
19		R/W	-	-	CE_HUE_TBL07[5:0]						-
1A		R/W	-	-	CE_HUE_TBL08[5:0]						-
1B		R/W	-	-	CE_HUE_TBL09[5:0]						-
1C		R/W	-	-	CE_HUE_TBL10[5:0]						-
1D		R/W	-	-	CE_HUE_TBL11[5:0]						-
1E		R/W	-	-	CE_HUE_TBL12[5:0]						-

1F		R/W	-	-	CE_HUE_TBL13[5:0]						**-**
20		R/W	-	-	CE_HUE_TBL14[5:0]						**-**
21		R/W	-	-	CE_HUE_TBL15[5:0]						**-**
22		R/W	-	-	CE_HUE_TBL16[5:0]						**-**
23		R/W	-	-	CE_HUE_TBL17[5:0]						**-**
24		R/W	-	-	CE_HUE_TBL18[5:0]						**-**
25		R/W	-	-	CE_HUE_TBL19[5:0]						**-**
26		R/W	-	-	CE_HUE_TBL20[5:0]						**-**
27		R/W	-	-	CE_HUE_TBL21[5:0]						**-**
28		R/W	-	-	CE_HUE_TBL22[5:0]						**-**
29		R/W	-	-	CE_HUE_TBL23[5:0]						**-**
2A		R/W	CE_EDG_FAC2[3:0]				CE_EDG_FAC1[3:0]				**-**
2B	DGC_CTRL	R/W	-	-	-	-	-	-	-	DGC_EN	**00**
2C		R/W	-	-	-	-	-	-	DGC_SELECT[1:0]		**01**
2D		R/W	-	-	-	DTR_EN	DGC_CHKSUM_EN[2:0]			DGC_REG_SYNC_GT	**11**
2E		R/W	DGC_GT_BYTE0[7:0]								**FF**
2F		R/W	DGC_GT_BYTE1[7:0]								**FF**
30	SET_DIGITAL_GAMMA1	R/W	-	DGC_GAMMA1_GAIN[6:0]							**-**
31		R/W	DGC_GAMMA1_OFFSET[3:0]				DGC_GAMMA1_000[3:0]				**-**
32		R/W	DGC_GAMMA1_004[3:0]				DGC_GAMMA1_008[3:0]				**-**
33		R/W	DGC_GAMMA1_012[3:0]				DGC_GAMMA1_016[3:0]				**-**
34		R/W	DGC_GAMMA1_020[3:0]				DGC_GAMMA1_024[3:0]				**-**
35		R/W	DGC_GAMMA1_028[3:0]				DGC_GAMMA1_032[3:0]				**-**
36		R/W	DGC_GAMMA1_036[3:0]				DGC_GAMMA1_040[3:0]				**-**
37		R/W	DGC_GAMMA1_044[3:0]				DGC_GAMMA1_048[3:0]				**-**
38		R/W	DGC_GAMMA1_052[3:0]				DGC_GAMMA1_056[3:0]				**-**
39		R/W	DGC_GAMMA1_060[3:0]				DGC_GAMMA1_064[3:0]				**-**
3A		R/W	DGC_GAMMA1_068[3:0]				DGC_GAMMA1_072[3:0]				**-**
3B		R/W	DGC_GAMMA1_076[3:0]				DGC_GAMMA1_080[3:0]				**-**
3C		R/W	DGC_GAMMA1_084[3:0]				DGC_GAMMA1_088[3:0]				**-**
3D		R/W	DGC_GAMMA1_092[3:0]				DGC_GAMMA1_096[3:0]				**-**
3E		R/W	DGC_GAMMA1_100[3:0]				DGC_GAMMA1_104[3:0]				**-**
3F		R/W	DGC_GAMMA1_108[3:0]				DGC_GAMMA1_112[3:0]				**-**
40		R/W	DGC_GAMMA1_116[3:0]				DGC_GAMMA1_120[3:0]				**-**
41		R/W	DGC_GAMMA1_124[3:0]				DGC_GAMMA1_128[3:0]				**-**
42		R/W	DGC_GAMMA1_132[3:0]				DGC_GAMMA1_136[3:0]				**-**

43		R/W	DGC_GAMMA1_140[3:0]	DGC_GAMMA1_144[3:0]	-
44		R/W	DGC_GAMMA1_148[3:0]	DGC_GAMMA1_152[3:0]	-
45		R/W	DGC_GAMMA1_156[3:0]	DGC_GAMMA1_160[3:0]	-
46		R/W	DGC_GAMMA1_164[3:0]	DGC_GAMMA1_168[3:0]	-
47		R/W	DGC_GAMMA1_172[3:0]	DGC_GAMMA1_176[3:0]	-
48		R/W	DGC_GAMMA1_180[3:0]	DGC_GAMMA1_184[3:0]	-
49		R/W	DGC_GAMMA1_188[3:0]	DGC_GAMMA1_192[3:0]	-
4A		R/W	DGC_GAMMA1_196[3:0]	DGC_GAMMA1_200[3:0]	-
4B		R/W	DGC_GAMMA1_204[3:0]	DGC_GAMMA1_208[3:0]	-
4C		R/W	DGC_GAMMA1_212[3:0]	DGC_GAMMA1_216[3:0]	-
4D		R/W	DGC_GAMMA1_220[3:0]	DGC_GAMMA1_224[3:0]	-
4E		R/W	DGC_GAMMA1_228[3:0]	DGC_GAMMA1_232[3:0]	-
4F		R/W	DGC_GAMMA1_236[3:0]	DGC_GAMMA1_240[3:0]	-
50		R/W	DGC_GAMMA1_244[3:0]	DGC_GAMMA1_248[3:0]	-
51		R/W	DGC_GAMMA1_252[3:0]	DGC_GAMMA1_253[3:0]	-
52		R/W	DGC_GAMMA1_254[3:0]	DGC_GAMMA1_255[3:0]	-
53		R/W		DGC_GAMMA1_OFFSET_MAG[1:0] / DGC_GAMMA1_DELTA_MAG[1:0]	-
54	SET_DIGITAL_GAMMA2	R/W	-	DGC_GAMMA2_GAIN[6:0]	-
55		R/W	DGC_GAMMA2_OFFSET[3:0]	DGC_GAMMA2_000[3:0]	-
56		R/W	DGC_GAMMA2_004[3:0]	DGC_GAMMA2_008[3:0]	-
57		R/W	DGC_GAMMA2_012[3:0]	DGC_GAMMA2_016[3:0]	-
58		R/W	DGC_GAMMA2_020[3:0]	DGC_GAMMA2_024[3:0]	-
59		R/W	DGC_GAMMA2_028[3:0]	DGC_GAMMA2_032[3:0]	-
5A		R/W	DGC_GAMMA2_036[3:0]	DGC_GAMMA2_040[3:0]	-
5B		R/W	DGC_GAMMA2_044[3:0]	DGC_GAMMA2_048[3:0]	-
5C		R/W	DGC_GAMMA2_052[3:0]	DGC_GAMMA2_056[3:0]	-
5D		R/W	DGC_GAMMA2_060[3:0]	DGC_GAMMA2_064[3:0]	-
5E		R/W	DGC_GAMMA2_068[3:0]	DGC_GAMMA2_072[3:0]	-
5F		R/W	DGC_GAMMA2_076[3:0]	DGC_GAMMA2_080[3:0]	-
60		R/W	DGC_GAMMA2_084[3:0]	DGC_GAMMA2_088[3:0]	-
61		R/W	DGC_GAMMA2_092[3:0]	DGC_GAMMA2_096[3:0]	-
62		R/W	DGC_GAMMA2_100[3:0]	DGC_GAMMA2_104[3:0]	-
63		R/W	DGC_GAMMA2_108[3:0]	DGC_GAMMA2_112[3:0]	-
64		R/W	DGC_GAMMA2_116[3:0]	DGC_GAMMA2_120[3:0]	-
65		R/W	DGC_GAMMA2_124[3:0]	DGC_GAMMA2_128[3:0]	-
66		R/W	DGC_GAMMA2_132[3:0]	DGC_GAMMA2_136[3:0]	-
67		R/W	DGC_GAMMA2_140[3:0]	DGC_GAMMA2_144[3:0]	-

68		R/W	DGC_GAMMA2_148[3:0]				DGC_GAMMA2_152[3:0]			**-**
69		R/W	DGC_GAMMA2_156[3:0]				DGC_GAMMA2_160[3:0]			**-**
6A		R/W	DGC_GAMMA2_164[3:0]				DGC_GAMMA2_168[3:0]			**-**
6B		R/W	DGC_GAMMA2_172[3:0]				DGC_GAMMA2_176[3:0]			**-**
6C		R/W	DGC_GAMMA2_180[3:0]				DGC_GAMMA2_184[3:0]			**-**
6D		R/W	DGC_GAMMA2_188[3:0]				DGC_GAMMA2_192[3:0]			**-**
6E		R/W	DGC_GAMMA2_196[3:0]				DGC_GAMMA2_200[3:0]			**-**
6F		R/W	DGC_GAMMA2_204[3:0]				DGC_GAMMA2_208[3:0]			**-**
70		R/W	DGC_GAMMA2_212[3:0]				DGC_GAMMA2_216[3:0]			**-**
71		R/W	DGC_GAMMA2_220[3:0]				DGC_GAMMA2_224[3:0]			**-**
72		R/W	DGC_GAMMA2_228[3:0]				DGC_GAMMA2_232[3:0]			**-**
73		R/W	DGC_GAMMA2_236[3:0]				DGC_GAMMA2_240[3:0]			**-**
74		R/W	DGC_GAMMA2_244[3:0]				DGC_GAMMA2_248[3:0]			**-**
75		R/W	DGC_GAMMA2_252[3:0]				DGC_GAMMA2_253[3:0]			**-**
76		R/W	DGC_GAMMA2_254[3:0]				DGC_GAMMA2_255[3:0]			**-**
77		R/W					DGC_GAMMA2_OFFSET_MAG[1:0]	DGC_GAMMA2_DELTA_MAG[1:0]		**-**
98	PWM_CTRL	R/W	-	-		LEDON_EN	LEDON_POL	VCSW_VOL	LEDPWM_POL	LED_VOL	**1A**
99		R/W	-	-	PWM_SYNC2VS	PWM_OFFSET[4:0]					**00**
9A		R/W	SEL_CLK_DIV[7:0]								**01**
9B		R/W	N_VAL[7:0]								**06**
9C		R/W	PWM_FRAC[7:0]								**80**
A0	BC_DIM_FT_CTRL	R/W	-	DEC_STP_FT[2:0]			-	INC_STP_FT[2:0]			**33**
A1		R/W	DEC_FPS_FT[3:0]				INC_FPS_FT[3:0]				**11**

TABLE 2.5: JADARD PAGE 3 COMMAND LIST

2.6. Jadard page 4 command

Index	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
00	POWER_OPT	R/W	-	PDS[30:24]							02
01		R/W	PDS[23:16]								18
02		R/W	PDS[15:8]								23
03		R/W	PDS[7:0]								8E
06	GAS_CTRL	R/W	-	GAS_DBS_CLR	GAS_IN_DBS_EN	GAS_OUT_DBS_EN	GAS_VCOM_EN	GAS_DBS_VEN	GAS_DBS_GEN	GAS_DBS_SEN	77
07		R/W	GAS_DBS_LTH[7:0]								18
08		R	GAS_SLPIN_EN	GAS_RE_SLPOUT	GAS_RE_SLPOUT_OTP_RELOAD	GAS_POR_OPT	GAS_POR_MASK	GAS_BLK_NUM[2:0]			0A
09	SETRGBCYC2	R/W	-	SDPRDUM	SDDUM[1:0]		SDSW[1:0]		SDPORCH[1:0]		10
0C	SETSTBA2	R/W	-	-	VTEST[5:0]						00
0D		R/W	-	SDS[22:16]							06
0E		R/W	SDS[15:8]								6A
0F		R/W	SDS[7:0]								85
1E	SET_OSCD	R/W	-	-	OSCD_EN	OSCD_BIAS_EN	-	OSCD_ADJ[2:0]			03
1F		R/W	OSCD_OFFSET_SS	-	-	OSCD_SS_EN	OSCD_SS_F[2:0]			OSCD_SS_R	09
29	SETMIPI1	R/W	-	TX_LDO_SEL[2:0]			PHY_VDC0_D3	RX_LDO_SEL[2:0]			33
35	SETMIPI4	R/W	-	DSI_CTL7[6:0]							0A
36	SETMIPI5	R/W	-	DSI_CTL8[6:0]							11
37		R/W	DSI_CTL9[7:0]								00

97	REG_CHKSUM	R/W	-	-	SLPIN_RST_EN	CHKSUM_OFF	-	CHKSUM_SEL[2:0]			**12**
98	SET_INH_CHKSUM	R/W	-	-	-	SLPIN_RESET_EN	INH_CHKSUM_OFF	INH_CHKSUM_SEL[2:0]			**1A**
99	SET_GPO	R/W	-	GPO0_REV	GPO0_OE	GPO0_SEL[4:0]					**21**
9A		R/W	-	GPO1_REV	GPO1_OE	GPO1_SEL[4:0]					**26**
9B		R/W	-	GPO2_REV	GPO2_OE	GPO2_SEL[4:0]					**25**
9C		R/W	-	GPO3_REV	GPO3_OE	GPO3_SEL[4:0]					**00**
9D		R/W	-	GPO4_REV	GPO4_OE	GPO4_SEL[4:0]					**00**
9E		R/W	VCSW1_OE	GPO5_REV	GPO5_OE	GPO5_SEL[4:0]					**80**
9F		R/W	VCSW2_OE	GPO6_REV	GPO6_OE	GPO6_SEL[4:0]					**80**
A0		R/W	-	INTERNAL_SEL2[2:0]			-	INTERNAL_SEL1[2:0]			**00**
A3	STD_SEL	R/W	-	RX0F_DCS_B0_MIX	RX0F_B0_SEL	-	RX0A_B2_MIX	RX0A_B0_MIX	CMPR_MIX_EN[1:0]		**00**
A4	RX0A_OTP	R/W	-	-	DSI_F8F9_EN	DISPON_SEL	-	-	-	RX0A_EN	**00**
A5		R/W	RX0A[7:0]								**00**
A6	DSI_SMRP	R/W	-	-	-	-	-	-	-	DSI_SMRP_TYPE	**00**
A7		R/W	DSI_SMRP[15:8]								**00**
A8		R/W	DSI_SMRP[7:0]								**01**

TABLE 2.6: JADARD PAGE 4 COMMAND LIST

2.7. All page command description

2.7.1. SET_PAGE(ALL Page-RE0h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RE0h	**R/W**	-	-	-	-	-	PAGE[2:0]			
Description	This command is used to change page. **PAGE[2:0]:** Register page select.									
Restriction	-									

2.7.2. SET_PASSWORD(ALL Page-RE1h~RE3h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	0	1	1	1	1	1	1	BF
RE1h	**R/W**	PASSWD1[7:0]								
RE2h	**R/W**	PASSWD2[7:0]								
RE3h	**R/W**	PASSWD3[7:0]								
Description	This command is used to set password to access inhouse register. When {PASSED1, PASSWD2, PASSWD3}= {93h, 65, F8} => Enable STD CMD and all in-house registers {5Ah, A5h, FFh} => Enable STD CMD and Page0~3 registers {09h, B1h, 7Fh} => Enable ESD protection machine, no comamnd access permission {69h, 96h, 55h} => Exist ESD protection machine, only STD CMD can access. Others => Enable STD CMD only (Default)									
Restriction	-									

2.7.3. AUTO_DISP_SETTING(ALL Page -RE4h~RE5h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RE4h	**R/W**	-	-	-	-	GON	DTE	DISP[1:0]		
RE5h	**R/W**	-	-	DISP_SW_OPT[1:0]		-	BLK_DISABLE	BLK_MODE[1:0]		

Description

This command is used to set display sequence Related Setting.

DISP[1:0]: Source output setting.

DISP1	DISP0	Internal Display Operations	Source Output
0	0	Halt	VSSD
0	1	Inhibit	Inhibit
1	0	Operate	V255
1	1	Operate	Display

DTE, GON: Gate / SD output setting.

GON	Gate Output
0	VGL
1	VGH/VGL

DTE	SD Output
0	Off (Hi-Z)
1	ON

BLK_DISABLE: When this bit is 1, no blanking frame is displayed after SLPIN/SLPOUT. When this bit is 0, 2blanking frame are displayed after SLPIN/SLPOUT.

BLK_MODE[1:0]: When BLK_DISABLE=0,

BLK_MODE [1:0]	Blank mode
00	Turn off blanking after 2 blanking frame
01	Keep blanking after 2 blanking frames
10	Inhibit
11	Inhibit

DISP_SW_OPT[1:0]: Define status of DISP[1:0] after SW reset command receivered.

Restriction

-

2.7.4. SET_WD: Setup watch dog (ALL Page -RE6h~RE8h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RE6h	**R/W**	-				-	-	WD_MODE[1:0]		
RE7h	**R/W**	-	-	-	WD_off	WD_Timer[3:0]				
RE8h	**R/W**	-	-	-	-	-	-	WD_FMS	WD_FBLK	

Description

WD_MODE[1:0]: Watch dog mode select.

WD_MODE[1:0]		WD Alarm start	WD Alarm stop
0	0	Inhibit	Inhibit
0	1	Inhibit	Inhibit
1	0	Display off	Display on
1	1	Inhibit	Inhibit

WD_off: Bit=1, disable watch dog function.

WD_Timer[3:0]: Set watch dog timer. When external HSYNC stop, watch dog timer start to count. Send alarm signal to watch dog if timer counting value is the same as WD_Timer[3:0] setting. When HSYNC resume, alarm signal is stoped.

WD_Timer[3:0]	Time to alarm
0x00	0 x 512osc(Inhibit)
0x01	1 x 512osc
:	:
0x0E	14 x 512osc
0x0F	15 x 512osc

WD_FMS: Force Mode Switch when WDT occurs(not release)

WD_FBLK: Force Blanking when WDT or Hwreset occurs(not release)

Restriction: -

2.7.5. OTP PROG: OTP Program (ALL Page -RE9h~REFh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RE9h	R/W	OTP_MASK[7:0]								
REAh	R/W	-	-	-	-	-	OTP_INDEX[10:8]			
REBh	R/W	OTP_INDEX[7:0]								
RECh	R/W	-	-	-	OTP_READ_SINGLE	OTP_WRITE_SINGLE	OTP_LOAD_DISABLE	OTP_INT_VPP	OTP_AUTO_PROG	
REDh	R	OTP_RDATA[7:0]								
REEh	R/W	OTP_WDATA[7:0]								
REFh	R/W	OTP_PROG	OTP_VPP_SEL	OTP_PCE	OTP_PWE	-	-	OTP_PTM[1:0]		

Description

OTP_MASK[7:0]: Bit programming mask, if 1, means this bit can't be programmed.

OTP_INDEX[10:0] : Set index of OTP table for programming.

OTP_WRITE_READ_SINGLE: Read 1 byte OTP value.

0: Disable.

1: Enable.

EX: set INDEX[9:0], READ_SINGLE=1 and AUTO_PROG=1, then read OTP_RDATA[7:0]

OTP_WRITE_PROG_SINGLE: For 1 byte OTP programing only.(Not release to customer)

0: Disable.

1: Enable.

EX: set MASK[7:0], INDEX[9:0] ,WDATA[7:0] and WRITE_SINGLE=1 first then set AUTO_PROG=1, the WDATA will write to INDEX.

OTP_LOAD_DISABLE: Auto reload OTP value.

0: Enable auto reload OTP value after SLPOUT command send.

1: Disable auto reload OTP value after SLPOUT command send.

OTP_INT_VPP: Select VPP voltage from external or internal.

0: VPP voltage from external power supply.

1: VPP voltage from internal power supply (VGH).

OTP_AUTO_PROG: When set to 1, the register content of OTP index is programmed.

OTP_ RDATA [7:0]: Read back the OTP index data. (Not release to customer)

Following description is for OTP manual mode. (Not release to customer)

OTP_WDATA: Set OTP data for programming when OTP_PROG_SINGLE=1.

OTP_PPROG: Program mode enable. 0:disable, 1:enable.

OTP_VPP_SEL: When written to 1, VPP voltage is fed to OTP.

OTP_POR: Pin for read operation

OTP_PWE: Define program cycle. 1: means OTP is able to be programmed.

OTP_PTM[1:0]: Test mode.

Operating Mode Truth Table

User Mode		PTM[1]	PTM[0]	PPROG	PWE	POR
Stand-by		L	L	L	L	L
Read Access		L	L	L	L	H
Program	Entry	L	L	H	L	L
(PGM)	Access	L	L	H	H	L
Test Mode						
Margin-1 Read Mode		H	L	L	L	H
Margin-2 Read Mode		H	H	L	L	H
IPP Mode		L	H	H	H	L

Notes

1. H stands for logic High level. L stands for logic Low level.
2. PTM[1] = H and PTM[0] = L is for Margin-1 Read Mode. Margin-1 Read Mode provides a critical read condition to filter out "weak programmed" bits during CP1 sort in the testing flow. To cover all worse corners, customer should implement Margin-1 Read Mode during testing.
3. PTM[1] = H and PTM[0] = H is for Margin-2 Read Mode. Margin-2 Read Mode setup another critical read condition to filter out "weak retention" bits during CP2 sort in the testing flow.
4. PTM[1] = L and PTM[0] = H is for IPP Mode. IPP Mode is implemented for bit cell current measurement. Customer should design in IPP mode, which allow to measure OTP cell current. It's for debug purpose in case of malfunction happen in merged product.

Restriction	-

2.7.6. SELF_DIAG(ALL Page -RF0h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RF0h	**R**	regload_detec	func_detec	attach_detec	gbreak_detec	-	-	-	-	**HEX**
Description	This command is used to for up debug									
Restriction	-									

2.7.7. SPI_CMD: Set SPI command index (ALL Page -RF1h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RF1h	**R/W**	SPI_CMD_INDEX[7:0]								
Description	This command is used to set SPI command index. **SPI_CMD_INDEX[7:0]:** SET SPI READ Command Address for Jadard Command.									
Restriction	-									

2.7.8. SPI_READ(ALL Page -RF2h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	1	1	0	0	1	0	F2
Parameter 1	**R**	SPI_CMD_DATA1[7:0]								
:	:	:								
Parameter n	**R**	SPI_CMD_DATAn[7:0]								
Description	This command is used to get SPI command data. **SPI_CMD_DATA[7:0]:** GET SPI READ Command data for Jadard Command.									
Restriction	-									

2.7.9. DSI_RESERVED:DSI Reserved (ALL Page -RF7h~RF9h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RF7h	**R/W**	DSI_RES1[7:0]								
RF8h	**R/W**	DSI_RES2[7:0]								
RF9h	**R/W**	DSI_RES3[7:0]								
Description	RF7h comamnd: Continuous write/read function used. RF8h comamnd: While DDIC received RF7h comamnd, DDIC will excute SLPIN + DISPLAY OFF sequqnce automaticaly. RF9h comamnd: While DDIC received RF8h comamnd, DDIC will excute SLPOUT + DISPLAY ON sequence automaticaly. Both RF7h and RF8h are vaild under page1_R89h[7](ECO0[7])=1. ECO0[7]:0:disable dsi F8/F9 command. (Default) 1:enable dsi F8/F9 command.									
Restriction	-									

2.8. Jadard page 0 command description

2.8.1. RDCUSTMID: Read Customer ID (Page0-R1Bh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R1Bh	R	CUSTM1[7:0]								
	R	CUSTM2[7:0]								
	R	CUSTM3[7:0]								
	R	CUSTM4[7:0]								
	R	CUSTM5[7:0]								
	R	CUSTM6[7:0]								
	R	CUSTM7[7:0]								
	R	CUSTM7[7:0]								
Description	This command is used to read customer ID. Read the value of page1_RA7h to RAEh CUSTM1[7:0] mapping to Page1_RA7h CUSTM2[7:0] mapping to Page1_RA8h CUSTM3[7:0] mapping to Page1_RA9h CUSTM4[7:0] mapping to Page1_RAAh CUSTM5[7:0] mapping to Page1_RABh CUSTM6[7:0] mapping to Page1_RACh CUSTM7[7:0] mapping to Page1_RADh CUSTM8[7:0] mapping to Page1_RAEh									
Restriction	-									

2.8.2. SEQUENCE CTRL: Power on sequence control (Page0-R70h~R76h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R70h	R/W	X	DC0H[2:0]			X	DC1H[2:0]			
R71h	R/W	X	DC2H[2:0]			X	DC3H[2:0]			
R72h	R/W	X	X	X	X	X	DC7H[2:0]			
R73h	R/W	DC0L	DC1L	DC2L	DC3L	DC4L	DC5L	DC6L	DC7L	
R74h	R/W	T0P[1:0]		T1P[1:0]		T8P[1:0]		X	X	
R75h	R/W	X	SOFT0H[2:0]			X	SOFT0L[2:0]			
R76h	R/W	X	X	X	X	X	X	X	POW_ON_STATE	

Description

This command is used to set power on sequence Related Setting.

DC0H[2:0]: Select the AVDD power on timing(P1~P8).

DC1H[2:0]: Select the VCL power on timing(P1~P8).

DC2H[2:0]: Select the AVEE power on timing(P1~P8).

DC3H[2:0]: Select the VGL power on timing(P1~P8).

DC4H[2:0]: Fix the VGH power on timing at P5.

DC5H[2:0]: Fix the Gamma reference voltage power on timing at P6.

DC6H[2:0]: Fix the VCOM power on timing at P7.

DC7H[2:0]: Option.

Power-on Sequence option		
DCxH[2:0]	Go High	
0	P1	DC0H default
1	P2	DC1H default
2	P3	DC2H default
3	P4	DC3H default
4	P5	DC4H fixed
5	P6	DC5H fixed
6	P7	DC6H fixed / DC7H default
7	P8	

DC0L: Select the AVDD power off timing(P10~P11).

DC1L: Select the VCL power off timing(P10~P11)

DC2L: Select the AVEE/VDDN power off timing(P10~P11)

DC3L: Select the VGL power off timing(P10~P11)

DC4L: Select the VGH power off timing(P10~P11)

DC5L: Select the Gamma reference voltage power off timing(P10~P11)

DC6L: Select the VCOM power off timing(P10~P11)

DC7L: Option

Power-off Sequence option		
DCxL	Go Low	
0	P10	DC1-3L,DC5-7L default
1	P11	DC0/4L default

TP0[1:0]: Slecet the period time for T0.

TP1[1:0]: Slecet the period time for T1.

TP8[1:0]: Slecet the period time for T8.

Power-on Period option		
TxP[1:0]	Period	
0	0.1ms	
1	3ms	T0 / T8 defualt
2	6ms	T1 default
3	10ms	

SOFT0H[2:0]: Select the AVDD soft pump start timing(P0~P7).

Soft Start Option		
SOFTxH[2:0]	Go High	
0	P0	SOFT0H default
1	P1	
2	P2	
3	P3	
4	P4	
5	P5	
6	P6	
7	P7	

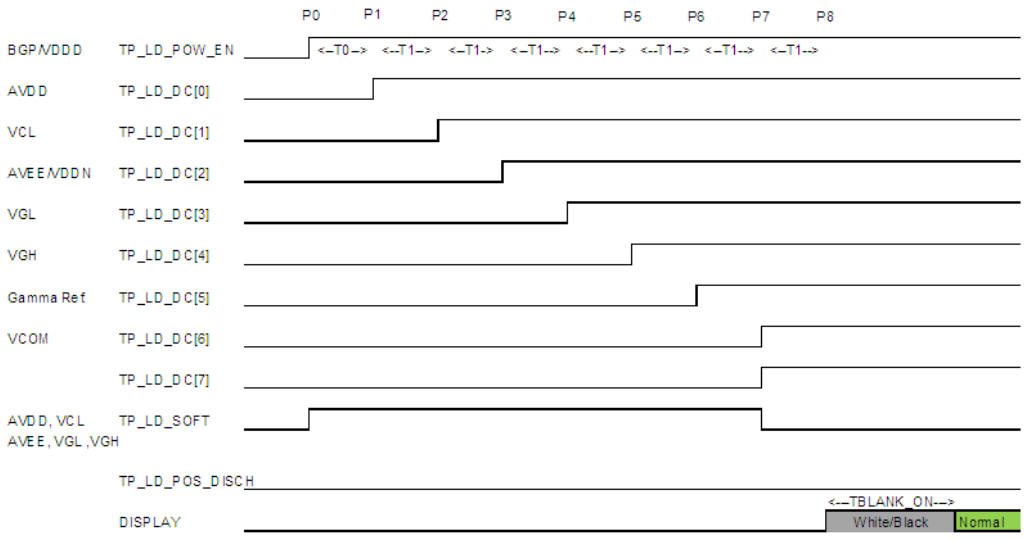
SOFT0L[2:0]: Select the AVDD soft pump stop timing(P1~P8).

Soft End Option		
SOFTxL[2:0]	Go Low	
0	P1	
1	P2	
2	P3	
3	P4	
4	P5	
5	P6	

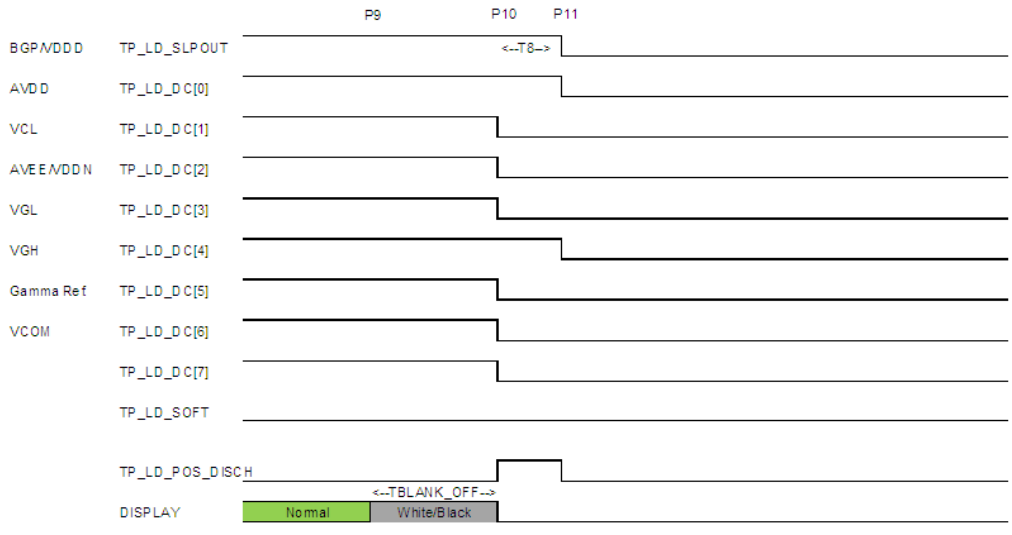
6	P7	SOFT0L default
7	P8	

POW_ON_STATE: All power ready when this bit is high.

- Power-on Sequence Flow



- Power-off Sequence Flow



Restriction	-

2.8.3. SET ID: SETID(OTP*5) (Page0-R77h~R7Ch)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R77h	**R**	X	X	X	X	X	X	X	X	
R78h	**R/W**	ID1[7:0]								
R79h	**R/W**	ID2[7:0]								
R7Ah	**R/W**	ID3[7:0]								
R7Bh	**R/W**	ID4[7:0]								
R7Ch	**R**	X	X	X	X	X	ID_OTP_TIMES[2:0]			
Description	**ID1[7:0]:** This is used to set ID1 and read value from DAh. **ID2[7:0]:** This is used to set ID2 and read value from DBh. **ID3[7:0]:** This is used to set ID3 and read value from DCh. **ID4[7:0]:** This is used to set ID4. **ID_OTP_TIMES [2:0]:** Read the OTP program times of ID. (Not release to customer) 0: No valid SETID in OTP, use register default value. 1: SETID is programmed once in OTP. Reload 1st valid one. 5: SETID is programmed 5 times in OTP. Reload 5th valid one.									
Restriction	-									

2.8.4. SETDSISETUP: Set DSI Setup (Page0-R80h~R82h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R80h	**R/W**	X	DSI_INIT0[6:0]							
R81h	**R/W**	DSI_INIT1[7:0]								
R82h	**R/W**	DSI_ INIT2[7:0]								

Description

This command is used to set DSI Related Setting.

//DSI_INIT0

//DSI_INIT0[1:0]: Lane Num.

2'b00	1 lane
2'b01	2 lane
2'b10	3 lane
2'b11	4 lane

DSI_INIT0[3:2]: VC_ID, virtual channel identifier of RX.Default is 2'b00.

DSI_INIT0[4]: EoT_pkt_en.

0: Rx doesn't care the EOT packet (default)(protocol_error disable),

1: Rx must receive the EOT packet before entering the stop state

DSI_INIT0[5]: ERR_rpt_en.

0: disable the all error detector

1: enable (default)

//DSI_INIT1

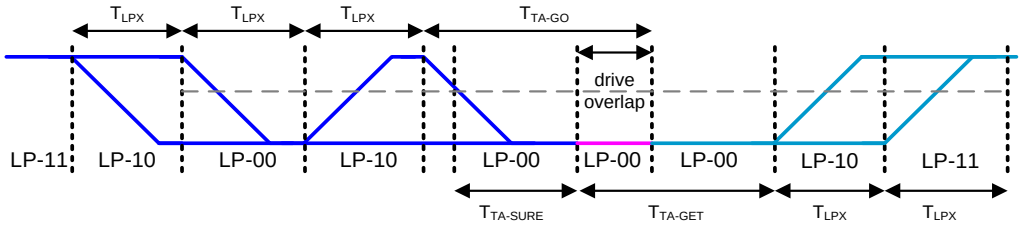
DSI_INIT1[1:0]: TX_s_wait. T_{TA_SURE} + T_{TA_GET} (spec. definition:min is 6 T_{LPX}, max is 7 T_{LPX}.)

Note:T_{TA_SURE} time is fixed by osc_on_time+OSC_div_setup_time，the TX_s_wait only affect the T_{TA_GET} time

2'b00	$7T_{LPX}$
2'b01	$8T_{LPX}$
2'b10	$9T_{LPX}$
2'b11	$12T_{LPX}$

DSI_INIT1[4:2]: TX_e_wait. $T_{TA\text{-}GO}$ (spec. definition: 4 T_{LPX}.)

3'b000	$1T_{LPX}$
3'b001	$2T_{LPX}$
3'b010	$3T_{LPX}$
3'b011	$4T_{LPX}$
3'b100	$5T_{LPX}$
3'b101	$6T_{LPX}$
3'b110	$7T_{LPX}$
3'b111	$8T_{LPX}$



DSI_INIT1 [6:5]: TX_OSC_DIV[1:0].

2'b00	OSCM_CLK_DIV2
2'b01	OSCM_CLK_DIV3
2'b10	OSCM_CLK_DIV4
2'b11	OSCM_CLK

DSI_INIT1[7]: CD_disable.

0: Enable contention detector flag(default).

1: disable

//DSI_INIT2

DSI_INIT2[0]: RST_trigger_EN.

0: Disable the reset function of the escape entry code.

1: Enable(Whole chip level), function as SW_RST. (default)

DSI_INIT2[1]: ECC_dis.

1: Ignore the ECC error and don't replace the received data with relative ECC (default),

0: normal function

DSI_INIT2[2]: CRC_chk_en.

0: Don't report the CRC error.

1: Report the CRC error. (default)

Restriction	-

2.8.5. SETDSISETUP: Set DSI Setup2 (Page0-R83h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R83h	**R/W**	X	DSI_INIT3[6:0]							

Description

This command is used to set DSI Related Setting.

//DSI_INIT3

DSI_INIT3[2:0]: DSWAP[2:0].

Below tabl show the mapping while PN is not swap.

DSWAP [2:0]	HS_ D0N	HS_ D0P	HS_ D1N	HS_ D1P	HS_ CN	HS_ CP	HS_ D2N	HS_ D2P	HS_ D3N	HS_ D3P
3'b000	D2-	D2+	D1-	D1+	CLK-	CLK+	D0-	D0+	D3-	D3+
3'b001	D2-	D2+	D0-	D0+	CLK-	CLK+	D1-	D1+	D3-	D3+
3'b010	D3-	D3+	D1-	D1+	CLK-	CLK+	D0-	D0+	D2-	D2+
3'b011	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+
3'b100	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+
3'b101	D3-	D3+	D1-	D1+	CLK-	CLK+	D2-	D2+	D0-	D0+
3'b110	D0-	D0+	D2-	D2+	CLK-	CLK+	D1-	D1+	D3-	D3+
3'b111	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+

DSI_INIT3 [3]: PN_SWAPX.

1: PN no swap(default).

0: swap.

Restriction: -

2.8.6. UP_START_CTRL (Page0-R84h~R87h)

<table>
<tr><th>CMD_ADD</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>R84h</td><td>R/W</td><td colspan="8">UP_KEY1[7:0]</td><td></td></tr>
<tr><td>R85h</td><td>R/W</td><td colspan="8">UP_KEY2[7:0]</td><td></td></tr>
<tr><td>R86h</td><td>R/W</td><td colspan="8">UP_START_EN[7:0]</td><td></td></tr>
<tr><td>R87h</td><td>R/W</td><td colspan="8">PWR_KEY[7:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="10">
OTP_KEY1/KEY2[7:0]: This command is used to enter or leave OTP program mode.
Before OTP programming, setting OTP_KEY1=5Ah and OTP_KEY2=A5h first. Otherwise OTP programming will fail.

<table>
<tr><th>OTP_KEY1[7:0]</th><th>OTP_KEY2[7:0]</th><th>Description</th></tr>
<tr><td>0x5Ah</td><td>0xA5h</td><td>Enter OTP program mode</td></tr>
<tr><td>0x00h</td><td>0x00h</td><td>Leave OTP program mode</td></tr>
</table>

(Not release to customer)
<table>
<tr><th>OTP_KEY1[7:0]</th><th>OTP_KEY2[7:0]</th><th>Description</th></tr>
<tr><td>0x55h</td><td>0xAAh</td><td>Control OTP directly</td></tr>
<tr><td>0xA7h</td><td>0x7Eh</td><td>Direct access to ROM</td></tr>
<tr><td>0x3Fh</td><td>0XE6h</td><td>ROM BIST</td></tr>
</table>

UP_START_EN[7:0]: AFh= UP_DISABLE. (Not release to customer)
PWR_KEY [7:0]: AA to enable direct power sequence control. (Not release to customer)
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

2.8.7. ALS: SET_ALS (Page0-R88h~R8Bh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R88h	**R/W**	ALS[31:24]								
R89h	**R/W**	ALS[23:16]								
R8Ah	**R/W**	ALS[15:08]								
R8Bh	**R/W**	ALS[07:00]								
Description	32bits ambient value (Unit: LUX) Use for “SLR Auto” mode. IEC 0x7									
Restriction	-									

2.8.8. RDCTMOTP: Read customer OTP value (Page0-RB1h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
	R									
Description	Refer to page1_R95h~A5h, CTM_OTP description									
Restriction	-									

2.9. Jadard page 1 command description

2.9.1. VCOM_SET: Set VCOM Voltage (Page1-R00h~R02h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R00h	R/W	X			VCOMS_BP	X		VCOM_S[9:8]		
R01h	R/W	VCOM_S[7:0]								
R02h	R/W	X					VCOM_OTP_TIMES[2:0]			

Description

This command is used to set VCOM voltage and read OTP writing times for VCOM. The setting is vaild by GIP is forward scan.

VCOMS_BP: Select VCOM operation range.

0: The maximum of VCOM operation range is up to VCOM_S[8:0].

1: The maximum of VCOM operation range is up to VCOM_S[:0].

VCOMS_BP=0(default value), VCOM operation range table as below:

VCOM_S[8:0]: Set VCOM voltage while normal light on.

VCOM_S[8:0]	Volatge (V)
000h	-0.3
001h	-0.31
002h	-0.32
003h	-0.33
004h	-0.34
:	-10mv/step
0x4E	1.77
:	-10mv/step
171h	-3.99
172h	-4
173h ~ 1FCh	Inhibit
0x1FD	VCOMR
0x1FE	AVSS
0x1FF	Hi-Z

VCOMS_BP=1, VCOM operation range table as below:

VCOM_S[9:0]: Set VCOM voltage while normal light on.

VCOM_S[9:0]	Volatge (V)
000h	Inhibit
000h ~ 04Ah	Inhibit
04Bh	1.8
04Ch	1.79
04Dh	1.78
04Eh	1.77
:	-10mv/step
163h	-1
164h	-1.01
~	-10mv/step
1F4h	-2.45
1F5h	-2.46
:	-10mv/step
28Eh	-3.99
28Fh	-4
290h ~ 3FCh	Inhibit
3FDh	VCOMR
3Feh	AVSS
3FFh	Hi-Z

VCOM_OTP_TIMES[2:0]: This register just can be written by up.
Due to VCOM is belonging to MTP, VCOM_OTP_TIMES[2:0] is used to record OTP being programmed times of VOCM.

Restriction	-

2.9.2. VCOM_R_SET: Set VCOM Voltage when reverse scan (Page1-R03h~R05h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R03h	R/W	X			VCOM_R_SEN	X		VCOM_R_S[9:8]		
R04h	R/W	VCOM_R_S[7:0]								
R05h	R	X					VCOM_R_OTP_TIMES[2:0]			

Description

This command is used to set VCOM voltage and read OTP writing times for VCOM. The setting is vaild by GIP is backward scan.

VCOMS_R_SEN, Set VCOM setting source while GIP is backword scan.

Under GIP is backword scan,

0: VCOM setting is follow VCOM_S. (Default)

1: VCOM setting is follow VCOM_R_S.

VCOMS_BP(Page0_R00h[4])=0, VCOM operation range table as below:

VCOM_R_S[8:0]: Set VCOM voltage while normal light on.

VCOM_R_S[8:0]	Volatge (V)
000h	-0.3
001h	-0.31
002h	-0.32
003h	-0.33
004h	-0.34
:	-10mv/step
0x4E	1.77
:	-10mv/step
171h	-3.99
172h	-4
173h ~ 1FCh	Inhibit
0x1FD	VCOMR
0x1FE	AVSS
0x1FF	Hi-Z

VCOMS_BP(Page0_R00h[4])=1, VCOM operation range table as below:

VCOM_S[9:0]: Set VCOM voltage while normal light on.

VCOM_R_S[9:0]	Volatge (V)
000h	Inhibit
000h ~ 04Ah	Inhibit
04Bh	1.8
04Ch	1.79
04Dh	1.78
04Eh	1.77
:	-10mv/step
163h	-1
164h	-1.01
~	-10mv/step
1F4h	-2.45
1F5h	-2.46
:	-10mv/step
28Eh	-3.99
28Fh	-4
290h ~ 3FCh	Inhibit
3FDh	VCOMR
3Feh	AVSS
3FFh	Hi-Z

VCOM_R_OTP_TIMES[2:0]: This register just can be written by up.
Due to VCOM is belonging to MTP, VCOM_R_OTP_TIMES[2:0] is used to record OTP being programmed times of VOCM_R.

Restriction	-

2.9.3. PWRIC SET: External Power IC timing setting (Page1-R0Ah~R0Eh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R0Ah	**R/W**	X	X	JD_ RELD	VCSW_ SWAP	ENVREF_S[3:0]				
R0Bh	**R/W**	PWRIC_SET[7:0]								
R0Ch	**R/W**	X	PWRIC_CLK1[2:0]			X	PWRIC_IDLE_CLK1[2:0]			
R0Dh	**R/W**	HX_ SOFT	PWRIC_CLK2[2:0]			PWRIC_HXCLK[3:0]				
R0Eh	**R/W**	HX_DT _AVDD	X	X	X	X	X	LED_PWR_S[1:0]		

Description

This command is used to set frequency of charge/pump of AVDD/AVEE for external Power IC.

JD_RELD: During blanking area, driver ic will re-send new pumping ratio to external power ic(JD5xxx), set this bit 1 to enable this function.

VCSW_SWAP: Swap VCSW1 and VCSW2 for power ic, set this bit 1 to enable this function.

ENVREF_S[3:0]: Set voltage level of VCSW1 to JD power IC. The register is valid at DCDCM[2:0]=001.

ENVREF_S[3:0]	ENVREF(V)	ENVREF_S[3:0]	ENVREF(V)
0h	1.55	7h	1.90
1h	1.60	8h	1.95
2h	1.65	9h	2.00
3h	1.70	Ah	2.05
4h	1.75	Bh	2.10
5h	1.80	Ch	2.15
6h	1.85	Other	Inhibitt

PWRIC_SET[7:0]: Set refernce clock number to detect pumping ratio of JD power IC. The register is valid at DCDCM[2:0]=001.

PWRIC_SET[7:0]	AVDD / AVEEPumping ratio
0 reference clocks	2 x
9 reference clocks	3 x
17 reference clocks	1.5 x

PWRIC_CLK1 [2:0]: Set frequency of pumping clock to JD pwoer IC at normal mode operation.
PWRIC_IDLE_CLK1 [2:0]: Set frequency of pumping clock to JD pwoer IC at Idle mode operation.
The registers are valid at DCDCM[2:0]=001.

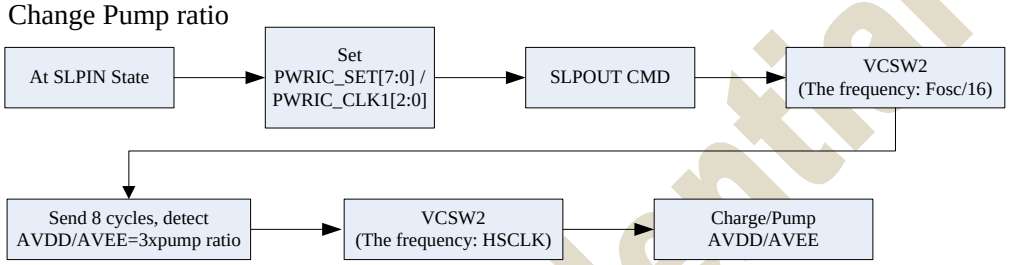
PWRIC_CLK1[2:0]/ PWRIC_IDLE_CLK1[2:0]	VCSW2	PWRIC_CLK1[2:0]/ PWRIC_IDLE_CLK1[2:0]	VCSW2
0h	HSCLK / 16	4h	HSCLK
1h	HSCLK / 8	5h	HSCLK x 2
2h	HSCLK / 4	6h	HSCLK x 4
3h	HSCLK / 2	7h	HSCLK x 8

PWRIC_CLK2 [2:0]: Set frequency of refernce clock.
The register is valid at DCDCM[2:0]=001.

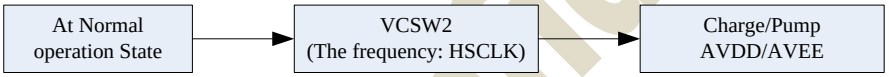
PWRIC_CLK2[2:0]	VCSW2	PWRIC_CLK2[2:0]	VCSW2
0h	Fosc / 256	4h	Fosc / 16
1h	Fosc / 128	5h	Fosc / 8
2h	Fosc / 64	6h	Fosc / 4
3h	Fosc / 32	7h	Fosc / 4

Example:
PWRIC_SET[7:0]=9, PWRIC_CLK1[2:0]=4, PWRIC_CLK2[2:0]=4

Change Pump ratio



Change charge/Pump frequency



HX_SOFT: For HX5186 soft start function, set this bit 1 to enable this function.

PWRIC_HXCLK[3:0]: Set frequency of pumping clock of HX5186 power IC, the register is valid at DCDCM[2:0]=011.

PWRIC_CLK1 [2:0]	Pumping ratio	PWRIC_CLK1 [2:0]	Pumping ratio
0h	Fosc / 8	8h	Fosc / 224
1h	Fosc / 16	9h	Fosc / 256
2h	Fosc / 32	Ah	Fosc / 288
3h	Fosc / 64	Bh	Fosc / 320
4h	Fosc / 96	Ch	Fosc / 352
5h	Fosc / 128	Dh	Fosc / 384
6h	Fosc / 160	Eh	Fosc / 416
7h	Fosc / 192	Fh	Fosc / 448

HX_DT_AVDD: For HX5186 PWRIC used.

LED_PWR_S[1:0]: Select LED_ON pin function.

LED_PWR_S[1:0]	LED_ON frunction
0h	LEDON
1h	VCSW2
2h	DC[0]
3h	VCSW2

Restriction	-

2.9.4. GAMMA_SET: Set Gama Reference Voltage(Page1-R17h~R1Ch)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R17h	**R/W**	X			VGMP_S[8]	X			VGSP_S[8]	
R18h	**R/W**	VGMP_S[7:0]								
R19h	**R/W**	VGSP_S[7:0]								
R1Ah	**R/W**				VGMN_S[8]	X			VGSN_S[8]	
R1Bh	**R/W**	VGMN_S[7:0]								
R1Ch	**R/W**	VGSN_S[7:0]								

Description

This command is used to set postive / Negative reference volatge of Gamma.

VGMP_S[8:0]: Set power source volatge of postive polarity.

VGMP_S [8:0]	VGMP (V)
0h	0 (GND)
:	Inhibit
27h	2.6
28h	2.6125
:	12.5mv/step
11Eh	5.6875
11Fh	5.7
Others	Inhibit

VGSP_S [8:0]: Set refernce volatge of postive polarity.

VGMP_S [8:0]	VGSP (V)
0h	0 (GND)
1h	0.3
2h	0.3125
:	12.5mv/step
110h	3.6875
111h	3.7
Others	Inhibit

VGMN_S [8:0]: Set power source volatge of negative polarity.

VGMP_S [8:0]	VGMN (V)
0h	0 (GND)
:	Inhibit
27h	-2.6
28h	-2.6125
:	12.5mv/step
11Eh	-5.6875
11Fh	-5.7
Others	Inhibit

VGSN_S [8:0]: Set refernce volatge of negative polarity.

VGMP_S[8:0]	**VGSN (V)**
0h	**0 (GND)**
1h	**-0.3**
2h	**-0.3125**
:	**12.5mv/step**

		110h	**-3.6875**	
		111h	**-3.7**	
		Others	**Inhibit**	
Restriction	-			

2.9.5. OTP_SET(Page1-R1Dh~R1Eh)

<table>
<tr><th>CMD_ADD</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>R1Dh</td><td>R/W</td><td>-</td><td>-</td><td colspan="2">VPP_DT[1:0]</td><td>-</td><td colspan="3">VPP_VGH_RT[2:0]</td><td>-</td></tr>
<tr><td>R1Eh</td><td>R/W</td><td>-</td><td colspan="7">VPP_VGH_S[6:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to set internal OTP program relaetd setting.

VPP_DT[1:0]:When INT_VPP=1(ECh), internal OTP will program 2bit step by step until 1 byte program finished. VPP_DT[1:0] can define delay time between each cycle.
<table>
<tr><th>VPP_DT[2:0]</th><th>Delaytime (ms)</th></tr>
<tr><td>0h</td><td>0.25</td></tr>
<tr><td>1h</td><td>0.5</td></tr>
<tr><td>2h</td><td>1</td></tr>
<tr><td>3h</td><td>2</td></tr>
</table>
VPP_VGH_RT[2:0]: Set VGH DC/DC charge/pump ratio of internal OTP program.
<table>
<tr><th>VPP_VGH _RT[2:0]</th><th>Charge pump Ratio</th></tr>
<tr><td>0</td><td>AVDD-VCL</td></tr>
<tr><td>1</td><td>2*AVDD</td></tr>
<tr><td>2</td><td>2*AVDD-VCL</td></tr>
<tr><td>3</td><td>2*AVDD-AVEE</td></tr>
<tr><td>4</td><td>3*AVDD-VCL</td></tr>
<tr><td>5</td><td>3*AVDD-AVEE</td></tr>
<tr><td>6</td><td>3*AVDD-AVEE-VCL</td></tr>
<tr><td>7</td><td>3*AVDD-2*AVEE</td></tr>
</table>
VPP_VGH_S[6:0]: Set VGH voltage level of internal OTP program.
Internal OTP power, INT_VPP = VPP_VGH_S + VPP_VGH_SFT[2:0]

VPP_VGH_SFT[2:0]=0x04 (default)
<table>
<tr><th>VPP_VGH _S[6:0]</th><th>INT_VGH_S</th><th>VGH (V)</th></tr>
<tr><td>000_0011</td><td>0000_0111</td><td>8.6</td></tr>
<tr><td>Others</td><td>Inhibit</td><td>Inhibit</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

2.9.6. GATE_POWER_SET: Set GIP Output High Level (Page1-R1Fh~R22h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R1Fh	R/W	X	VGH_REG[6:0]							
R20h	R/W	X		VGL_REG[5:0]						
R21h	R/W	X		VGL_REG2[5:0]						
R22h	R/W		VGH_REG_SHT	VGL_REG_SHT	VGL_REG2_SHT	VGH_REG_EN	VGL_REG_EN	VGL_REG2_EN	SHT_VGL_REG	

Description

This command is used to set GIP output voltage level.

VGH_REG[6:0]: Set VGH regulator volatge level.

VGH_REG[6]	VGH_REG[5:0]	VGH_REG(V)
0	00h	2.6
0	01h	2.8
0	02h	3.0
:	:	200mv/step
0	3Dh	14.8
0	3Eh	15.0
0	3Fh	15.2
1	00h	6.6
1	01h	6.8
1	02h	7.0
:	:	200mv/step
1	3Dh	18.8
1	3Eh	19.0
1	3Fh	19.2

VGL_REG[5:0]: Set VGL_REG regulator volatge level.

VGL_REG[5:0] / VGL_REG2[5:0]	VGL_REG(V) / VGL_REG2(V)
00h	-3.0
01h	-3.2
02h	-3.4
:	200mv/step
3Dh	-15.2
3Eh	-15.4
3Fh	-15.6

VGL_REG2[5:0]: reversed

VGH_REG_SHT: Define V(VGH_REG) conenct to VGH.
VGL_REG_SHT: Define V(VGL_REG) conenct to VGL.

XX_SHT	Connect V(VGH_REG),V(VGL_REG)/V(VGL_REG2) to VGH/VGL
0	Disbale
1	Enable

VGL_REG2_SHT: reversed.

VGH_REG_EN: Set VGH_REG output state.
VGL_REG_EN: Set VGL_REG output state.

XX_EN	Output Level
1	Regulator
0	Hi-Z

	VGL_REG2_EN: reversed. **SHT_VGL_REG:** reversed.
Restriction	-

2.9.7. DCDC_CTRL(Page1-R23h~R24h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R23h	**R/W**	-	-	GAS_ VGH_ EN	GAS_ VGL_ EN	VGH_ NC	VGL_ NC	VCLREG_OP_CEN	VCL_ NC	-
R24h	**R/W**	VGH EN	VGL EN	AVDD EN	AVEE EN	VCL EN	VDDA_EN	VCLREG_EN	VCL2 VDDN	-

Description

This command is used to control engineer mode of power related setting.

GAS_VGH_EN: Control VGH pumping clock state during GAS state

GAS_VGH_EN	VGH DC/DC circuit operation
0	Stop
1	Keep

GAS_VGL_EN: Control VGL pumping clock state during GAS state

GAS_VGL_EN	VGL DC/DC circuit operation
0	Stop
1	Keep

VGH_NC: Set VGH output state.

VGH_NC	VGH output
0	Clamping
1	No clamping

VGL_NC: Set VGL otuptut state

VGL_NC	VGH output
0	Clamping
1	No clamping

VCLREG_OP_CEN: VCL stable cap

VCLREG_OP_CEN	VCL
0	Need stable Cap
1	No need stable Cap

VCL_NC: Reversed.

VGH_EN: Control VGH DC/DC circuit On/Off.

VGH_EN	VGH DC/DC circuit
0	Disbale
1	Enable

VGL_EN: Control VGL DC/DC circuit On/Off.

VGL_EN	VGL DC/DC circuit
0	Disbale
1	Enable

AVDD_EN: Control AVDD DC/DC circuit On/Off.

AVDD_EN	AVDD DC/DC circuit
0	Disbale
1	Enable

AVEE_EN: Control AVEE DC/DC circuit On/Off.

AVEE_EN	AVEE DC/DC circuit
0	Disbale
1	Enable

VCL_EN: Control VCL DC/DC circuit On/Off.

VCL_EN	VCL DC/DC circuit
0	Disbale
1	Enable

VDDA_EN: Control VDDN DC/DC circuit On/Off.

VDDA_EN	VDDA DC/DC circuit
0	Disbale
1	Enable

VCLREG_EN: When VCLEN=1, set VCL circuit source

VCLREG_EN	VCL Source
0	VCL from DCDC
1	VCL from regulator

VCL2VDDN: Control source of VDDN output.

VCL2VDDN	VDDN
0	VDDN DC/DC Circuit
1	VCL

Restriction	-

2.9.8. POWAMP_CTRL: Set Power Function Related Setting (Page1-R25h~R27h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R25h	R/W	X	AP[2:0]			X				
R26h	R/W	VCOM_EN	VGM_EN	-	GAS_DET_SEL	GAS_IOVCC_EN	GAS_VCI_EN	GAS_AVEE_EN	GAS_OUT_EN	
R27h	R/W	UP_VDD_1P8_EN	VDDD_S1[2:0]			X	VDDD_S2[2:0]			

Description

This command is used to control engineer mode of power related setting.

AP[2:0]: Adjust the ratio of fixed current for the operatinal amplifier in the power circuit.

AP[2:0]	Biase Current
0h	25%
1h	50%
2h	75%
3h	100%
4h	125%
5h	150%
6h	175%
7h	200%

VCOM_EN: Control VCOM regulator On/Off

VCOM_EN	VCOM
0	Disable
1	Enable

VGM_EN: Control Postive/Negative regulator of Source output On/Off.

VGM_EN	VGMP/VGSP VGMN/VGSN
0	Disable
1	Enable

GAS_DET_SEL: Switch GAS detect level between 2 power and 3 power mode.

GAS_DET_SEL	2 power (Detect level)	3 power (Detect level)
0	VCI level	AVDD level
1	AVDD level	VCI level

GAS_IOVCC_EN: Enable IOVCC abnormal power off detect function.

GAS_IOVCC_EN	IOVCC detect function
0	Disbale
1	Enable

GAS_VCI_EN: Enable VCI abnormal power off detect function.

GAS_VCI_EN	VCI detect function
0	Disbale
1	Enable

GAS_AVEE_EN: Enable AVEE abnormal power off detect function.

GAS_AVEE_EN	AVEE detect function
0	Disbale
1	Enable

GAS_OUT_EN: Enable abnormal power off detect function.

GAS_OUT_EN	Abnormal power off function
0	Disbale (All GAS_XXX_EN is non-valid)
1	Enable

UP_VDDD_1P8_EN: Reserved.

VDDD_S1[2:0]: Set VDDD operation voltage.

VDDD_S1[2:0]	VDDD (V)	VDDD_S1[2:0]	VDDD (V)
0h	1.35	4h	1.55
1h	1.40	5h	1.60
2h	1.45	6h	1.65
3h	1.50	7h	1.70

VDDD_S2[2:0]: Set internal IOVCC regulator voltage during abnormla power off state.
Condiion: The function is valid at AVDD > VDDD_S2 setting volatge.

VDDD_S2[2:0]	IOVCC_GAS (V)	VDDD_S2[2:0]	IOVCC_GAS(V)
0h	1.10	4h	1.30
1h	1.15	5h	1.35
2h	1.20	6h	1.40
3h	1.25	7h	1.45

Restriction	-

2.9.9. DCDC_CTRL2: Set DCDC control function2 (Page1- R28h~R2Ah)

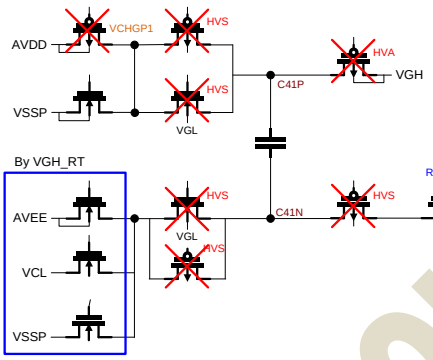
CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R28h	**R/W**	X	PWR_SW_EN	VGH_MSF_EN	VGH_CHG2AVDD_EH	VGH_GAS_PWS_EN	VGH_PWS	VGH_PWS_GND	VGH_PWS_POS	
R29h	**R/W**	X	X	GAS_T8P[1:0]		VGH_SGL_C41	VGH_SGL_C42	X	X	
R2Ah	**R/W**	DDS[7:0]								

Description

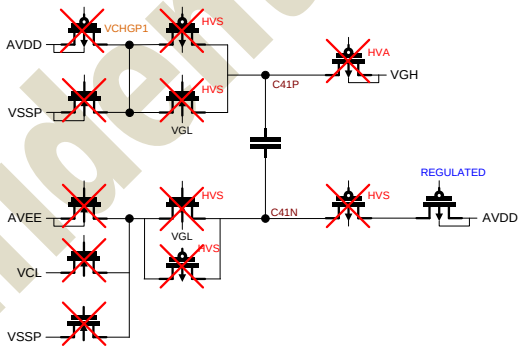
This command is used to set DCDC control 2.

PWR_SW_EN: Reserved.
VGH_MSF_EN: Control VGH SW floating state under VGH_EN=0.

VGH_EN=L ; VGH_MSF_EN=L

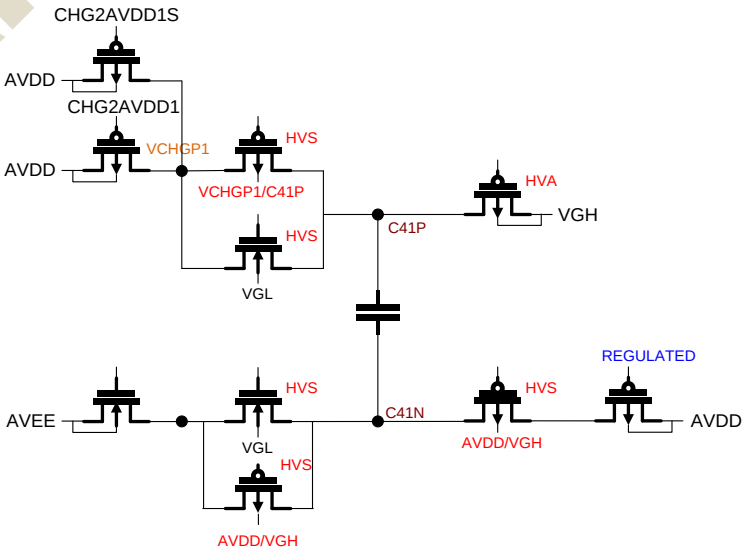


VGH_EN=L ; VGH_MSF_EN=H



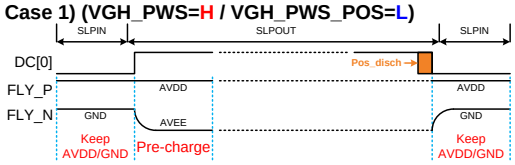
VGH_CHG2AVDD_EH: Enable VGH SW enhance under SLPIN state.

	VGH_CHG2AVDD_EH=L		VGH_CHG2AVDD_EH=H	
	SLPIN	SLPOUT	SLPIN	SLPOUT
CHG2AVDD1S	V	V	V	V
CHG2AVDD1	X	V	V	V

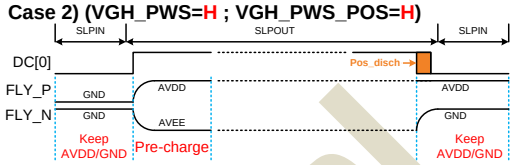


VGH_GAS_PWS_EN: Control VGH DCDC flying capcitance state between FLY_P and FLY_N during abnormal power off state.
VGH_PWS_EN: Control VGH DCDC flying capcitance state between FLY_P and FLY_N during SLPIN state.
VGH_PWS_GND: Reserved.
VGH_PWS_POS: Reserved.

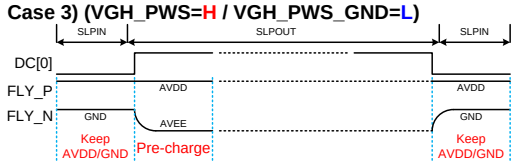
Case 1) (VGH_PWS=H / VGH_PWS_POS=L)



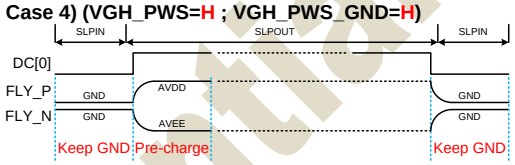
Case 2) (VGH_PWS=H ; VGH_PWS_POS=H)



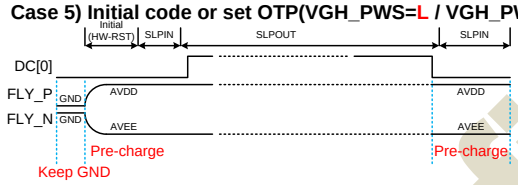
Case 3) (VGH_PWS=H / VGH_PWS_GND=L)



Case 4) (VGH_PWS=H ; VGH_PWS_GND=H)



Case 5) Initial code or set OTP(VGH_PWS=L / VGH_PWS_GND=X)



GAS_T8P[1:0]: Set T8P[1:0] time at SLPIN state while abnormal power off recoverd.
VGHSGL_C41: Control VGH DCDC flying SW state for C41P/N.
VGHSGL_C42: Control VGH DCDC flying SW state for C42P/N.

VGH_SGL_C41	VGH_SGL_C42	C41P/N	C42P/N	Note
0	0	V	V	Pump by C41/C42
0	1	X	V	Pump by C42
1	0	V	X	Pump by C41
1	1	off	off	Inhibit

DDS[7:0]: Reserved.

Restriction	-

2.9.10.SETSTBA: Set Source Option (Page1- R35h~R36h)

<table>
<tr><th>CMD_ADD</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>R35h</td><td>R/W</td><td>X</td><td colspan="3">GAP[2:0]</td><td colspan="4">SAP[3:0]</td><td></td></tr>
<tr><td>R36h</td><td>R/W</td><td colspan="4">-</td><td colspan="4">SAP2[3:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command is used to panel related setting.

GAP[2:0]:Set Gamma OP output driving ability. The output current is multiple of fixed current(IREF).
<table>
<tr><th>GAP[2:0]</th><th>Biase current</th></tr>
<tr><td>0h</td><td>1*IREF</td></tr>
<tr><td>1h</td><td>2*IREF</td></tr>
<tr><td>2h</td><td>3*IREF</td></tr>
<tr><td>3h</td><td>4*IREF</td></tr>
<tr><td>4h</td><td>5*IREF</td></tr>
<tr><td>5h</td><td>6*IREF</td></tr>
<tr><td>6h</td><td>7*IREF</td></tr>
<tr><td>7h</td><td>8*IREF</td></tr>
</table>
SAP[3:0]/SAP2[3:0]: Set channel OP output driving ability. The otuptu current is multiple of fixed current(IREF).
<table>
<tr><th>GAP[2:0]</th><th>Biase current</th></tr>
<tr><td>0h</td><td>1*IREF</td></tr>
<tr><td>1h</td><td>2*IREF</td></tr>
<tr><td>2h</td><td>3*IREF</td></tr>
<tr><td>3h</td><td>4*IREF</td></tr>
<tr><td>4h</td><td>5*IREF</td></tr>
<tr><td>5h</td><td>6*IREF</td></tr>
<tr><td>6h</td><td>7*IREF</td></tr>
<tr><td>7h</td><td>8*IREF</td></tr>
<tr><td>8h</td><td>9*IREF</td></tr>
<tr><td>9h</td><td>10*IREF</td></tr>
<tr><td>Ah</td><td>11*IREF</td></tr>
<tr><td>Bh</td><td>12*IREF</td></tr>
<tr><td>Ch</td><td>13*IREF</td></tr>
<tr><td>Dh</td><td>14*IREF</td></tr>
<tr><td>Eh</td><td>15*IREF</td></tr>
<tr><td>Fh</td><td>16*IREF</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

2.9.11.SETPANEL: Set Panel Related (Page1-R37h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R37h	**R/W**	X	Z_line	ENZ[1:0]		SS_ PANEL	GS_ PANEL	REV_ PANEL	BGR_ PANEL	

Description

This command is used to panel related setting.

Z_line: Set SZ output line

Z_line	SZ otuptu line
0	Odd line(1st line)
1	Even line(2nd line)

ENZ[1:0]: Set SZ output of Zag-Zag inversion.

ENZ[1:0]	SD Dummy outptu
01	SZ[2]
10	SZ[3]

SS_Panel: Set Source scan output direction.

SS_Panel	S/D scan direction
0	S1 -> S2400
1	S2400 -> S1

GS_Panel: Set Gate scan output direction.

GS_Panel	G/D scan direction
0	Top -> Bottom Scan (G1->G1280)
1	Bottom -> Top Scan (G1280 -> G1)

Note: Exmaple, resolution is 800RGB x 1280.

REV_Panel: Set the display of the same data on both normally-white and normally-black panels.

REV_Panel	Panel (Normally-type)
0	Normal Black panel
1	Normal White panel

BGR_Panel: This bit is control the order of <R><G><B> dot color for module supplier.

BGR_Panel	Color fliter alignment
0	<S1><S2><S3> align to <R><G><B>
1	<S1><S2><S3> align to <B><G><R>

Restriction

-

2.9.12.SETRGBCYC: Set Display Waveform Cycles of RGB Mode (Page1- R38h~R3Fh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R38h	R/W	X	interlace _line	X			RGB_JDT[2:0]			
R39h	R/W	RGB_N_EQ1[7:0]								
R3Ah	R/W	RGB_N_EQ2[7:0]								
R3Bh	R/W	RGB_N_EQ2_Temp[7:0]								
R3Ch	R/W	RGB_N_EQ3[7:0]								
R3Dh	R/W	RGB_CHGEN_ON[7:0]								
R3Eh	R/W	RGB_CHGEN_OFF[7:0]								
R3Fh	R/W	RGB_CHGEN_OFF2[7:0]								

Description

This command is used to set internal SD outptu timing.

Interalce_line: Set Even or Odd flag between SD and GIP.

RGB_JDT[2:0]: Set source dot inversion type at normal mode.

RGB_JDT[2:0]	Dot inversion type
000	1-dot
001	1+2-dot
010	2-dot
011	4-dot
100	Column
101	Zig-Zag
110	interlace
Others	Inhibit

RGB _N_EQ1[7:0]: Set SD EQ1 time. (Pull GND)

RGB _N_EQ1[7:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
02h	2 timing clock
:	1 timing clock /step
FEh	254 timing clock
FFh	255 timing clock

Note: 1 timing clock = 4 multiple of Fosc.

RGB _N_EQ2[7:0]: Set SD EQ2 time. (VCI or Hi-Z)

RGB _N_EQ2[7:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
02h	2 timing clock
:	1 timing clock /step
FEh	254 timing clock
FFh	255 timing clock

Note: 1 timing clock = 4 multiple of Fosc.

RGB_N_EQ2_Temp[7:0]: Set SD EQ2 time for low temperature. (VCI or Hi-Z)

RGB _N_EQ2[7:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
02h	2 timing clock

:	1 timing clock /step
FEh	254 timing clock
FFh	255 timing clock

Note: 1 timing clock = 4 multiple of Fosc.

RGB _N_EQ3[7:0]: Set SD EQ3 time. (VCI or Hi-Z)

RGB _N_EQ3[7:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
02h	2 timing clock
:	1 timing clock /step
FEh	254 timing clock
FFh	255 timing clock

Note: 1 timing clock = 4 multiple of Fosc.

RGB _CHGEN_ON[7:0]: Set SD output time.

RGB _CHGEN_ON[7:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
02h	2 timing clock
:	1 timing clock /step
FEh	254 timing clock
FFh	255 timing clock

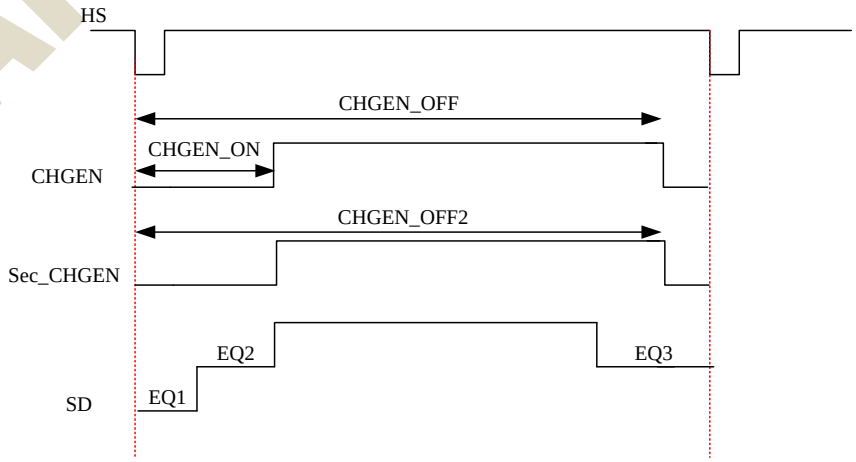
Note: 1 timing clock = 4 multiple of Fosc.

RGB _CHGEN_OFF[7:0]: Set 1st SD OP output time.

RGB _CHGEN_OFF[7:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
02h	2 timing clock
:	1 timing clock /step
FEh	254 timing clock
FFh	255 timing clock

Note: 1 timing clock = 4 multiple of Fosc.

RGB _CHGEN_OFF2[7:0]: Reversed



Note: 1. EQ1 < EQ2 < EQ2_Temp < EQ3.
2. EQ2 = EQ3=0xFF, CHGEN will always turn on.

Restriction	-

2.9.13.SET TCON: Timing control setting (Page1-R40h~R4Ch)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R40h	R/W	X	IP750_1	LN[1:0]		IP750_0	RSO[2:0]			
R41h	R/W	LN[9:2]								
R42h	R/W	SLT[7:0]								
R43h	R/W	VFP[7:0]								
R44h	R/W	VBP[7:0]								
R45h	R/W	HBP[7:0]								
R46h	R/W	TE_Delay[10:3]								
R47h	R/W	BlkinF_num[7:0]								
R48h	R/W	BlkinF_STR[7:0]								
R49h	R/W	BlkinFrame	X	X	X	X	TE_Delay[2:0]			
R4Ah	R/W	FRAME_NUM[1:0]		Auto_Test_en	TEST_PAT_EN	TEST_PATTERN[3:0]				
R4Bh	R/W	TCON_OPT1[15:8]								
R4Ch	R/W	TCON_OPT1[7:0]								

Description

This command is used to set timing control.

RSO[1:0]: Resolution select.

RSO[2:0]	Resolution	Source channels
000	Inhibit	Inhibit
001	750RGB x LN*2 dot	Refer to {IP750_1,IP750_0}
010	600RGBx LN*2 dot	S1~S900, S1501~S2400
011	640RGB x LN*2 dot	S1~S960, S1441~S2400
100	720RGB x LN*2 dot	S1 ~ S1080, S1321~S2400
101	768RGB x LN*2 dot	S1 ~ S1152, S1249~S2400
110	800RGB x LN*2 dot	S1 ~ S2400
111	Inhibit	Inhibit

RSO[2:0]	{IP750_1,IP750_0}	Source channels
001	00	S1~S1125, S1276~S2400
	01	S1~S1152, S1249~S2346
	10	S55~S1152, S1249~S2400

LN[9:0]: Sets the gate line number to drive LCD panel. The number of lines must be equal or more than the gate line number of LCD panel. Gate line number = LN*2.

NL[9:0]	Gate Line

0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	0	1	0	4
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
1	0	0	1	1	1	1	1	1	1	1278
1	0	1	0	0	0	0	0	0	0	1280
1	0	1	0	0	0	0	0	0	1	1282
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	1	1	0	1	2042
1	1	1	1	1	1	1	1	1	0	2044
1	1	1	1	1	1	1	1	1	1	2046

SLT[7:0]: Sets the scan line time width. Scan line time width = osc*4.

STL[7:0]								Scan Line time(osc)
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	4
0	0	0	0	0	0	1	0	8
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
0	1	1	1	1	1	1	1	508
1	0	0	0	0	0	0	0	512
1	0	0	0	0	0	0	1	516
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	1	1012
1	1	1	1	1	1	1	0	1016
1	1	1	1	1	1	1	1	1020

VBP[7:0]: Vertical back porch number setting.

VFP[7:0]: Vertical front porch number setting.

HBP[7:0]: Horizontal front porch number setting.

VBP[7:0] / VFP[7:0] / HBP[7:0]	Number of VBP / VFP (line)	Number of HBP(PCLK)
0x00	Inhibit	Inhibit
0x01	1	1

0x02	2	2
:	:	:
0xFE	254	254
0xFF	255	255

Note: VFP/VBP set 4 line unless, HBP set 2 PCLK unless.

TE_Delay[7:0]: TE delay setting.

TE_Delay[10:0]	TE output position (line)
0x000	VFP start position
0x001	1 gate line
0x002	2 gate line
:	:
0x500	1280 gate line
Others	Inhibit

TEST_PAT_EN: AGING mode enable/ disable, 1=>Enable, 0=>Disable.

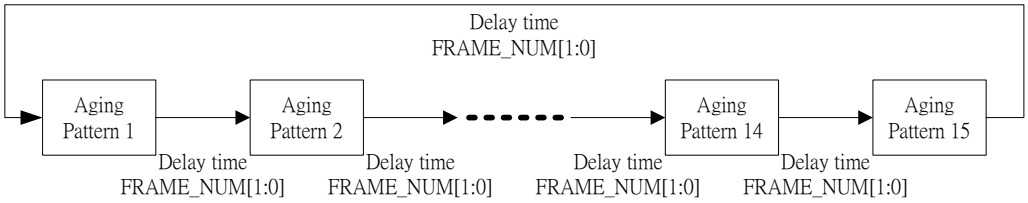
Auto_Test_en: Automatically executed aging cycle. 1=>Enable, 0=>Disable(display data by PATTERN_SELECT[3:0]).

Test Flow:

Step 1: Send slpout command

Step 2: Set Auto_Test_EN=1 & Test_PAT_EN=1.

Internal pattern will run differential pattern automatically.



FRAME_NUM[1:0]: Interval of each pattern when Automatically executed aging cycle.

FRAME_NUM[1:0]		Frame number
0	0	32
0	1	96
1	0	160
1	1	224

TEST_PATTERN[3:0]: Display pattern select when AGING_EN=1 and AUTO_EN=0.

PATTERN_SELECT[3:0]				Display pattern
0	0	0	0	Full Black
0	0	0	1	Full White
0	0	1	0	Full Red
0	0	1	1	Ful Green
0	1	0	0	Full Blue
0	1	0	1	Color bar(H)
0	1	1	0	Grayscale(V)
0	1	1	1	Grayscale(H)
1	0	0	0	Pixel 64x64
1	0	0	1	Crosstalk with G0
1	0	1	0	Crosstalk with G255
1	0	1	1	Flciker pattern for column inversion
1	1	0	0	Flicker pattern for 1 dot inversion
1	1	0	1	Flicker pattern for 2 dot inversion
1	1	1	0	Parity complement(for CP test)
1	1	1	1	Border(external : red, middle: blue internal: black)

BlkinFrame: Reserved.

BlkinF_num [7:0]: Reserved.

BlkinF_STR [7:0]: Reserved..

TCON_OPT1[15:8]: TCON option.

TCON_OPT1[7:0]: TCON option.

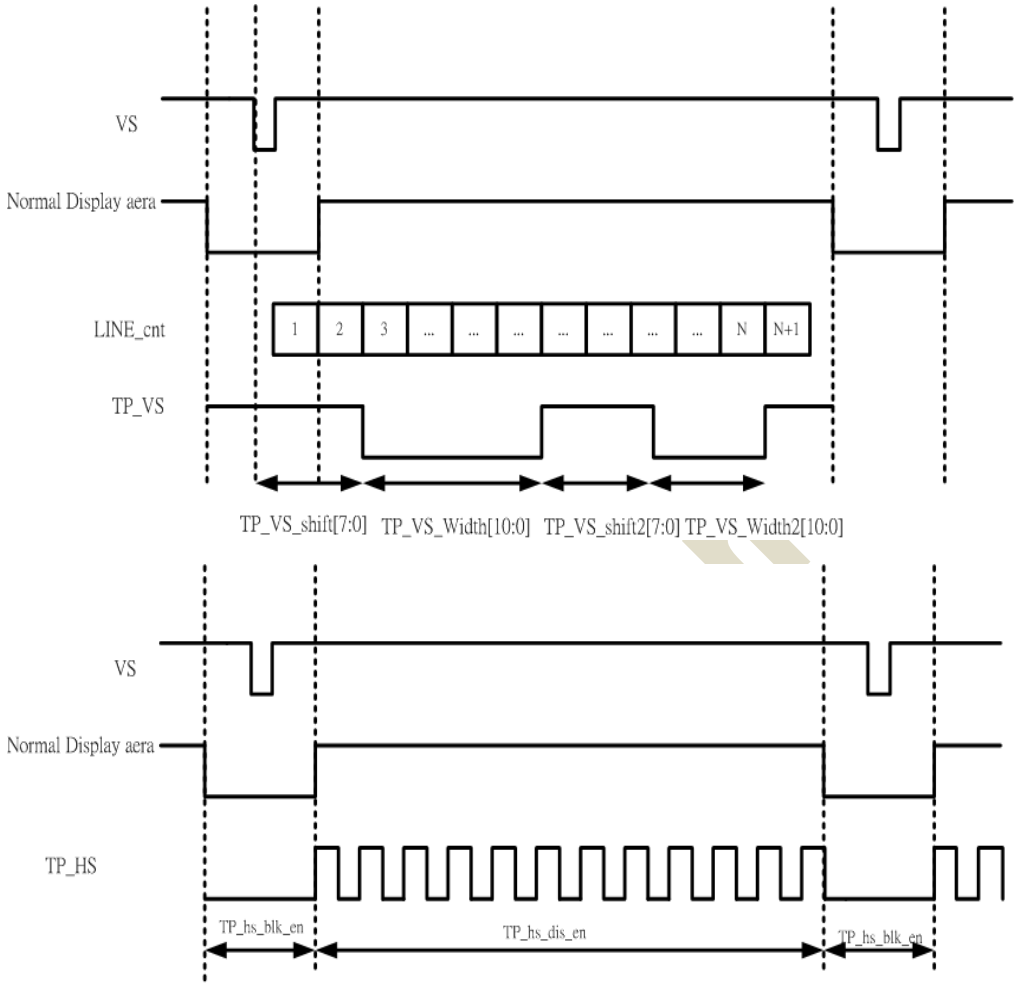
TCON_OPT [0]:GIP Learn function disable. 0: GIP learn enable, 1: GIP learn disable.

TCON_OPT [10]: Source EQ off. 0: Source EQ on, 1: Source EQ off.

Restriction	-

2.9.14.SET TE PAD: TE pad function setting (Page1-R4Dh~R53h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R4Dh	**R/W**	X	X	X	X	X	X	X	X	
R4Eh	**R/W**	X	X	X	X	TP_VS_EN	TP_VS_WIDTH[10:8]			
R4Fh	**R/W**	TP_VS_WIDTH[7:0]								
R50h	**R/W**	TP_VS_SHIFT[7:0]								
R51h	**R/W**	X	X	X	X	X	X	TP_HS_BLK_EN	TP_HS_DIS_EN	
R52h	**R/W**	TP_HS_ON[7:0]								
R53h	**R/W**	TP_HS_OFF[7:0]								
Description	This command is used to set TE and TE1 output state. **TP_VS_EN:** Set VS outptu enable/Disable. 0: When TE/TE1=10, TE/TE1 will outptu at Low. 1: Normal output **TP_VS_WIDTH[10:0]:** Set width of output low. **TP_VS_SHIFT[7:0]:** Set width of output high. TP_VS_WIDTH[10:0]=0 is inhibited. TP_VS_WIDTH[10:0]+ TP_VS_SHIFT[7:0]<VFP+VS+VBP+DISP AREA **TP_HS_BLK_EN:** Set HS output enable/disable at blanking area. **TP_HS_DIS_EN:** Set HS output enable/disable at disaply area. **TP_HS_ON[7:0]:** Set HS output low time. **TP_HS_OFF[7:0]:** Set HS output high time. TP_HS_ON[7:0] must small than TP_HS_OFF[7:0] **Related diagram chart as below**:									



Restriction	-

2.9.15.POWER_STATE: Power status setting (Page1-R54h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R54h	**R/W**	-	-	-	-	-	-	-	DSTBY	
Description	This command is used to set power state. **DSTBY:** Standby mode select. DSTBY=1, driver IC enters the deep standby mode when POW_EN=0. DSTBY=0, driver IC enters the standby mode when POW_EN=0. When DSTBY=1, all the display operation stops, All the internal operations and R-C oscillators are suspended. Driver IC should receive reset pull low 3ms at leats to exist deep standby mode.									
Restriction	-									

2.9.16.DCDC_SEL: Power Mode and Charge Pump Setting (Page1-R55h~ R5Ch)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R55h	R/W	X	X	X	X	DCDCM[3:0]				
R56h	R/W	X	X	X	X	AUTO_RT	X	AVDD_RT[1:0]		
R57h	R/W	VGH_RT[2:0]			VGL_RT[2:0]			VCL_RT[1:0]		
R58h	R/W	X	X	X	AVDD[4:0]					
R59h	R/W	VCL[2:0]			AVEE[4:0]					
R5Ah	R/W	X	VGH[6:0]							
R5Bh	R/W	X	X	VGL[5:0]						
R5Ch	R/W	X	X	VDDA_CLK[1:0]		VCL_CLK[1:0]		VGHVGL_CLK[1:0]		

Description

This command is used to Trimming HS Data Lane 0/1 Delay.

DCDCM[3:0]:The bits just valid under BOOSTM[1:0]=00

DCDCM[3:0]	AVDD	AVEE	VCL
0000	Internal Charge Pump(CP)		
0001	No output		CP
0010	NT power IC		CP
0011	HX power IC		CP
0100~1001	No output		CP
1010	NT power IC		
1011	No output		CP
1100	AVDD/AVEE external when SLPOUT		CP
1101	AVDD external when SLPOUT		CP
1110	AVEE external when SLPOUT		CP
1111	No output		CP

Note:
1. The connection between JD power IC / PFM mode1~3 and JD9311 could refer PXXX.
2. CP: Dr.IC Internal charge pump.

AUTO_RT: Inhibit
set AUTO_RT=0.

AVDD_RT[1:0]: Specify the charge pump ratio of AVDD under BOOSTM[1:0]=00.(Internal charge pump)

AVDD_RT[1:0]	Charge pump Ratio
0h	1.5 x VCIP
1h	2.0 x VCIP
2h	2.0 x VCIP
3h	3.0 x VCIP

VGH_RT[2:0]: Specify the charge pump ratio of VGH.
VGL_RT[2:0]: Specify the charge pump ratio of VGL.

VGH _RT[2:0]	Charge pump Ratio	VGL _RT[2:0]	Charge pump Ratio
0h	AVDD-VCL	0h	VCL-AVDD
1h	2*AVDD	1h	AVEE-AVDD
2h	2*AVDD-VCL	2h	AVEE+VCL-AVDD
3h	2*AVDD-AVEE	3h	2*AVEE-AVDD

4h	3*AVDD-VCL	4h	inhibit
5h	3*AVDD-AVEE	5h	inhibit
6h	3*AVDD-AVEE-VCL	6h	inhibit
7h	3*AVDD-2*AVEE	7h	inhibit

Note: If VGH_RT[2:0]=100, VGL_RT[1:0] can only be set 01 or 11.

VCL_RT[1:0]: Specify the charge pump ratio of VGL.

VCL_RT[1:0]	Charge pump Ratio
0h	inhibit
1h	- VCIP
2h	inhibit
3h	inhibit

AVDD_S[4:0]: Set clamping voltage levle of AVDD.
AVEE_S[4:0]: Set clamping voltage levle of AVEE.

AVDD _S[4:0]	AVDD (V)	AVEE_S[4:0]	AVEE (V)
0x00	6.5	0x00	-6.5
0x01	6.4	0x01	-6.4
: :	100mv / step	: :	100mv / step
0x1E	3.5	0x1E	-3.5
0x1F	3.4	0x1F	-3.4

VCL_S[1:0]: Set clamping voltage levle of VCL.

VCL _S[1:0]	VCL (V)	VCL _S[2:0]	VCL (V)
0x00	-2.5	0x04	-3.3
0x01	-2.7	0x05	-3.5
0x02	-2.9	0x06	-3.7
0x03	-3.1	0x07	-3.9

VGH_S[6:0]: Set clamping voltage levle of VGH.

VGH _S[6]	VGH _S[5:0]	VGH (V)
0	00h	7.0
0	01h	7.2
0	02h	7.4
0	. . .	200mv / step
0	3Dh	19.2
0	3Eh	19.4
0	3Fh	19.6
1	00h	7.8
1	01h	8.0
1	02h	8.2
1	. . .	200mv / step
1	3Dh	20.0
1	3Eh	20.2
1	3Fh	20.4

VGL_S[5:0]: Set clamping voltage levle of VGL.

VGL _S[5:0]	VGL (V)
0	-7.0

1	-7.2
2	-7.4
. . .	200mv / step
2Eh	-15.6
2Fh	-15.8
2Dh	-16.0
Others	Inhibit

VGHVGL _CLK[1:0]: Set frequency of pumping clock of VGH/VGL under normal mode. mode.

VGHVGL_CLK[1:0]	Ratio
0x00	HSCLK / 4
0x01	HSCLK / 2
0x02	HSCLK
0x03	HSCLK x 2

Note: HSCLK is define frequency of 1-line.

VCL _CLK[1:0]: Set frequency of pumping clock of VCL under normal mode.

VCL_CLK[1:0]	Ratio
0x00	HSCLK / 4
0x01	HSCLK / 2
0x02	HSCLK
0x03	HSCLK x 2

Note: HSCLK is define frequency of 1-line.

VDDA _CLK[1:0]: Set frequency of pumping clock of VDDA under normal mode.

VCL_CLK[1:0]	Ratio
0x00	HSCLK / 4
0x01	HSCLK / 2
0x02	HSCLK
0x03	HSCLK x 2

Note: HSCLK is define frequency of 1-line.

Restriction	-

2.9.17.SET_GAMMA: Set Gamma output voltage (Page1-R5Dh~ R82h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R5Dh	R/W	X	RPA18[6:0]							
R5Eh	R/W	X	RPA17[6:0]							
R5Fh	R/W	X	RPA16[6:0]							
R60h	R/W	X	RPA15[6:0]							
R61h	R/W	X	RPA14[6:0]							
R62h	R/W	X	RPA13[6:0]							
R63h	R/W	X	RPA12[6:0]							
R64h	R/W	X	RPA11[6:0]							
R65h	R/W	X	RPA10[6:0]							
R66h	R/W	X	RPA9[6:0]							
R67h	R/W	X	RPA8[6:0]							
R68h	R/W	X	RPA7[6:0]							
R69h	R/W	X	RPA6[6:0]							
R6Ah	R/W	X	RPA5[6:0]							
R6Bh	R/W	X	RPA4[6:0]							
R6Ch	R/W	X	RPA3[6:0]							
R6Dh	R/W	X	RPA2[6:0]							
R6Eh	R/W	X	RPA1[6:0]							
R6Fh	R/W	X	RPA0[6:0]							
R70h	R/W	X	RNA18[6:0]							
R71h	R/W	X	RNA17[6:0]							
R72h	R/W	X	RNA16[6:0]							
R73h	R/W	X	RNA15[6:0]							
R74h	R/W	X	RNA14[6:0]							
R75h	R/W	X	RNA13[6:0]							
R76h	R/W	X	RNA12[6:0]							
R77h	R/W	X	RNA11[6:0]							
R78h	R/W	X	RNA10[6:0]							
R79h	R/W	X	RNA9[6:0]							
R7Ah	R/W	X	RNA8[6:0]							
R7Bh	R/W	X	RNA7[6:0]							
R7Ch	R/W	X	RNA6[6:0]							
R7Dh	R/W	X	RNA5[6:0]							
R7Eh	R/W	X	RNA4[6:0]							

R7Fh	**R/W**	X	RNA3[6:0]	
R80h	**R/W**	X	RNA2[6:0]	
R81h	**R/W**	X	RNA1[6:0]	
R82h	**R/W**	X	RNA0[6:0]	
Description	This command is used to set postive /neagative volatge of source output. The related illustration can refer “8.1 Grayscale-Level adjustment control” of JD9366 Datasheet.			
Restriction	-			

2.9.18.SET DDB: Set Device Descriptor Block (Page1-R83h~R87h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R83h	**R**	X	X	X	X	X	X	X	X	
R84h	**R/W**	DDB1[7:0]								
R85h	**R/W**	DDB2[7:0]								
R86h	**R/W**	DDB3[7:0]								
R87h	**R/W**	DDB4[7:0]								
Description	This command is used to set DDB value and read form A1h and A8h.									
Restriction	-									

2.9.19.SETECO(Page1-R88h~ R8Ch)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R88h	**R**	-	-	-	-	-	-	-	-	
R89h	**R/W**	ECO1[7:0]								
R8Ah	**R/W**	ECO2[7:0]								
R8Bh	**R/W**	-	ECO3[6:0]							
R8Ch	**R/W**	-	ECO4[6:0]							
Description	This command is used to set ECO. ECO1~4[7:0]: Internal option. **ECO0[0]:**RG_CABC_TP2_CRV_FIX **ECO0[1]:**RG_CABC_TP1_PWM_FIX **ECO0[7]:** Enable DSI F8/ F9 command function. - DSI F8 command: Sleep in + display off - DSI F9 command: Sleep out + display on. 0:Disable 1: Enable **ECO2[0]:**for TEST_EN HW pin function 0:Enable. 1:Disable **ECO3[0]:**for HW BIST pin function 0:Enable. 1:Disable									
Restriction	-									

2.9.20.GET_ID_VERSION(Page1-R8Dh~ R92h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R8Dh	**R/W**	JD_ID1[7:0]								
R8Eh	**R/W**	JD_ID2[7:0]								
R8Fh	**R/W**	JD_ID3[7:0]								
Description	**JD_ID1[7:0]:** 0x93. IC production number. **JD_ID2[7:0]:** 0x65. IC production number. **JD_ID3[7:0]:** IC Version									
Restriction	-									

2.9.21.DCS_CMD_OPT (Page1-R93h~ R94h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R93h	**R/W**	-	-	-	-	-	-	-	NOKIA_CMD_EN	
R94h	**R/W**	-	-	-	-	-	-	-	RDCTMOTP_EN	
Description	**NOKIA_CMD_EN:** Set the read out value of standard command is based on Nokia SPEC or DCS SPEC 0: DCS SPEC, 1: Nokia SPEC **RDCTMOTP_EN:** Enable CTM_OTP R/W access 0: Disable RDCTMOTP read and write, 1: Enable RDCTMOTP read and write									
Restriction	-									

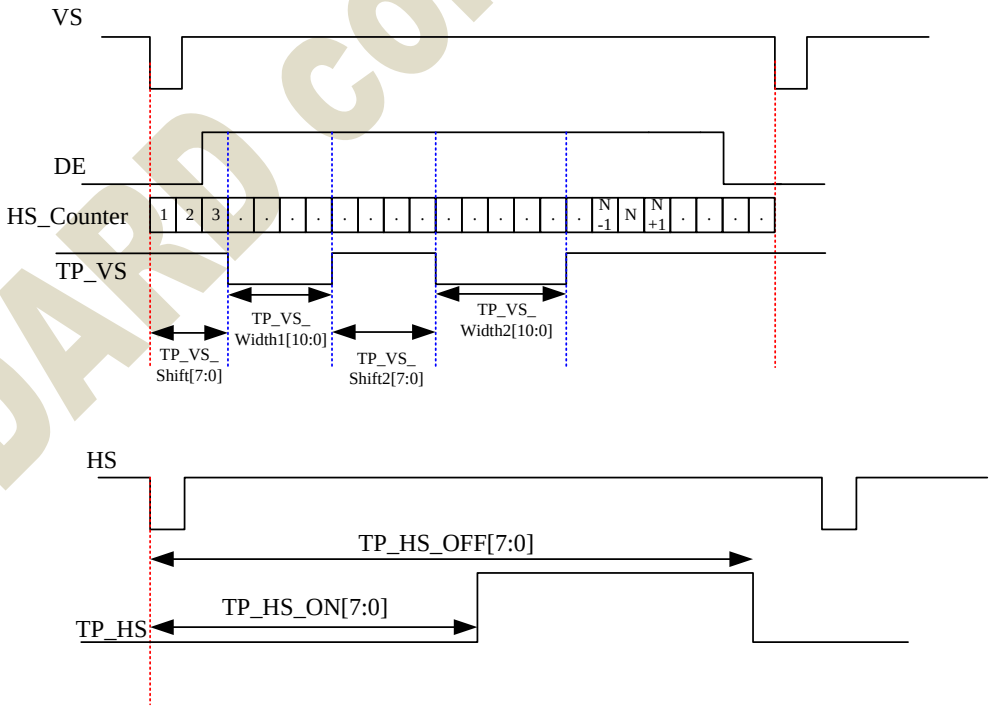
2.9.22.CTM_OTP (Page1-R95h~ RA5h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R95h	**R/W**	-	-	-	OTP_ WR_ FLAG	OTP_RD_LENGTH[3:0]				
R96h	**R/W**	CTM_OTP0[7:0]								
R97h	**R/W**	CTM_OTP1[7:0]								
R98h	**R/W**	CTM_OTP2[7:0]								
R99h	**R/W**	CTM_OTP3[7:0]								
R9Ah	**R/W**	CTM_OTP4[7:0]								
R9Bh	**R/W**	CTM_OTP5[7:0]								
R9Ch	**R/W**	CTM_OTP6[7:0]								
R9Dh	**R/W**	CTM_OTP7[7:0]								
R9Eh	**R/W**	CTM_OTP8[7:0]								
R9Fh	**R/W**	CTM_OTP9[7:0]								
RA0h	**R/W**	CTM_OTP10[7:0]								
RA1h	**R/W**	CTM_OTP11[7:0]								
RA2h	**R/W**	CTM_OTP12[7:0]								
RA3h	**R/W**	CTM_OTP13[7:0]								
RA4h	**R/W**	CTM_OTP14[7:0]								
RA5h	**R/W**	CTM_OTP15[7:0]								
Description	This command is used to set customer OTP value **OTP_WR_FLAG:** Determine page0_RB1h return size 0: default,follow SMRP setting 1: write OTP table,(OTP_RD_LENGTH[3:0] used as SMRP) **OTP_RD_LENGTH[3:0]:** Set maximum return packed size, when OTP_WR_FLAG=1, DSI will always return same packed size as OTP_RD_LENGTH(for standard command B1), (4'b0000 means 1;4'b1111 means 16) **CTM_OTP0~CTM_OTP15:** Customer OTP return value refer to standard command RB1h..									
Restriction	-									

2.9.23.SETCUSTM_ID (Page1-RA6h~ RAEh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RA6h	**R**	-	-	-	-	-	-	-	-	
RA7h	**R/W**	CUSTM1[7:0]								
RA8h	**R/W**	CUSTM2[7:0]								
RA9h	**R/W**	CUSTM3[7:0]								
RAAh	**R/W**	CUSTM4[7:0]								
RABh	**R/W**	CUSTM5[7:0]								
RACh	**R/W**	CUSTM6[7:0]								
RADh	**R/W**	CUSTM7[7:0]								
RAEh	**R/W**	CUSTM8[7:0]								
Description	This command is used to set custom ID. This register mapping to standard command R1Bh.									
Restriction	-									

2.9.24.SET_TE_PAD2(Page1-RAFh~ RB1h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAFh	**R/W**	-	-	-	VHS_ TEON _OPT	TP_VS _EN2	TP_VS_WIDTH2[10:8]			
RB0h	**R/W**	TP_VS_WIDTH2[7:0]								
RB1h	**R/W**	TP_VS_SHIFT2[7:0]								
Description	**VHS_TEON_OPT:** 1'b0:TP_VS and TP_HS don't use TEON 1'b1:TP_VS and TP_HS use TEON **TP_VS_EN2:** Set 2nd TE_VS output enable/Disable. This function can be used when TP_VS_EN=1. 0: When TE/TE1=10, TE/TE1 2nd VS will output at Low. 1: Normal output **TP_VS_WIDTH2[10:0]:** Set width2 of output low. **TP_VS_SHIFT2[7:0]:** Set width2 of output high.  										
Restriction	-									

2.9.25.OTP_REPAIR(Page1-RB2h~ RB5h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RB2h	**R/W**	-	-	-	-	REPAIR_PAGE[3:0]				
RB3h	**R/W**	REPAIR_INDEX[7:0]								
RB4h	**R/W**	REPAIR_PAR[7:0]								
RB5h	**R/W**	REPAIR_VALUE[7:0]								
Description	**REPAIR_PAGE[3:0]:** Set register page for repaire used. **REPAIR_PAGE[7:0]:** Set register index for repaire used. **REPAIR_PAR[7:0]:** Set register parameter for repaire used . - The setting is always fix at 1. **REPAIR_VALUE[7:0]:** Set value of register index for repaire used.									
Restriction	-									

2.9.26.SETRGBCYC3(Page1-RB6h~ RBBh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RB6h	**R/W**	-	RES_MUX_ON[6:0]							
RB7h	**R/W**	-	RES_MUX_OFF[6:0]							
RB8h	**R/W**	DYNBIAS_ON[7:0]								
RB9h	**R/W**	DYNBIAS_OFF[7:0]								
RBAh	**R/W**	DYNCHGEN_ON[7:0]								
RBBh	**R/W**	DYNCHGEN_OFF[7:0]								

Description

RES_MUX_ON[6:0]: Enable differential MUX output reisitor between EQ and Source output.

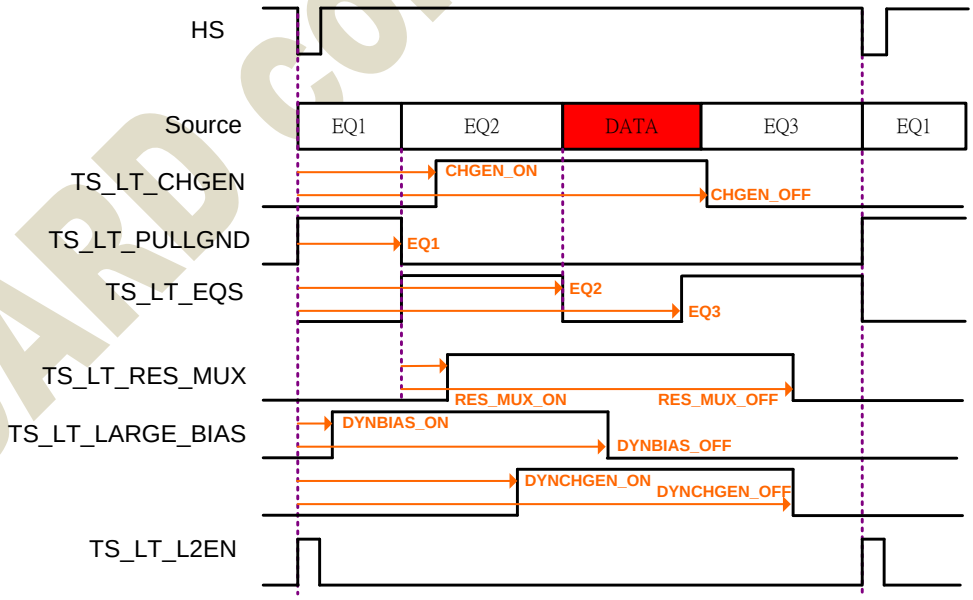
RES_MUX_OFF[6:0]: Disbable differential MUX output reisitor between EQ and Source output.

DYNBIAS_ON[7:0]: Set larger source bias current on time.

DYNBIAS_OFF[7:0]: Set larger source bias current off time.

DYNCHGEN_ON[7:0]: Set pre-open function for source channel op on time.

DYNCHGEN_OFF[7:0]: Set pre-open function of source channel op off time.



Restriction

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2.10. Jadard page 2 command description

2.10.1.SET_GIP_L: SET CGOUTx_L Signal Mapping, GS_Panel=0 (Page2-R00~15h)

CMD Add	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
00	**R/W**	X	CGO1_PH_L	CGO1_INV_L	CGOUT1_L[4:0]					
01	**R/W**	X	CGO2_PH_L	CGO2_INV_L	CGOUT2_L[4:0]					
02	**R/W**	X	CGO3_PH_L	CGO3_INV_L	CGOUT3_L[4:0]					
03	**R/W**	X	CGO4_PH_L	CGO4_INV_L	CGOUT4_L[4:0]					
04	**R/W**	X	CGO5_PH_L	CGO5_INV_L	CGOUT5_L[4:0]					
05	**R/W**	X	CGO6_PH_L	CGO6_INV_L	CGOUT6_L[4:0]					
06	**R/W**	X	CGO7_PH_L	CGO7_INV_L	CGOUT7_L[4:0]					
07	**R/W**	X	CGO8_PH_L	CGO8_INV_L	CGOUT8_L[4:0]					
08	**R/W**	X	CGO9_PH_L	CGO9_INV_L	CGOUT9_L[4:0]					
09	**R/W**	X	CGO10_PH_L	CGO10_INV_L	CGOUT10_L[4:0]					
0A	**R/W**	X	CGO11_PH_L	CGO11_INV_L	CGOUT11_L[4:0]					
0B	**R/W**	X	CGO12_PH_L	CGO12_INV_L	CGOUT12_L[4:0]					
0C	**R/W**	X	CGO13_PH_L	CGO13_INV_L	CGOUT13_L[4:0]					
0D	**R/W**	X	CGO14_PH_L	CGO14_INV_L	CGOUT14_L[4:0]					
0E	**R/W**	X	CGO15_PH_L	CGO15_INV_L	CGOUT15_L[4:0]					
0F	**R/W**	X	CGO16_PH_L	CGO16_INV_L	CGOUT16_L[4:0]					
10	**R/W**	X	CGO17_PH_L	CGO17_INV_L	CGOUT17_L[4:0]					
11	**R/W**	X	CGO18_PH_L	CGO18_INV_L	CGOUT18_L[4:0]					
12	**R/W**	X	CGO19_PH_L	CGO19_INV_L	CGOUT19_L[4:0]					
13	**R/W**	X	CGO20_PH_L	CGO20_INV_L	CGOUT20_L[4:0]					
14	**R/W**	X	CGO21_PH_L	CGO21_INV_L	CGOUT21_L[4:0]					
15	**R/W**	X	CGO22_PH_L	CGO22_INV_L	CGOUT22_L[4:0]					

Description

This command sets GIP CGOUTx_L signal mapping when XOR(GS_Panel, GS)=0.

CGOx_PH_L:CGOUT voltage level while abnormal power off @ GIP_GAS_OPT='1'.
0: Pull to VGL.1: Pull to VGH.

CGOx_INV_L: 0: CGOUT normal drive. 1: CGOUT drive inverse voltage level(VGH↔VGL)

CGOUTx(x=1~22**)_L[4:0]:** Please refer to below table.

CGOUTx_L	Output	CGOUTx_L	Output	CGOUTx_L	Output	CGOUTx_L	Output
0_0000	STV0	**0**_1000	CKV4	**1**_0000	ETV0	**1**_1000	FLM2
0_0001	STV1	**0**_1001	CKV5	**1**_0001	ETV1	**1**_1001	CKV12
0_0010	STV2	**0**_1010	CKV6	**1**_0010	ETV2	**1**_1010	CKV13
0_0011	STV3	**0**_1011	CKV7	**1**_0011	ETV3	**1**_1011	CKV14
0_0100	CKV0	**0**_1100	CKV8	**1**_0100	INT	**1**_1100	CKV15
0_0101	CKV1	**0**_1101	CKV9	**1**_0101	VEN0	**1**_1101	Floating
0_0110	CKV2	**0**_1110	CKV10	**1**_0110	VEN1	**1**_1110	VGH
0_0111	CKV3	**0**_1111	CKV11	**1**_0111	FLM1	**1**_1111	VGL

Restriction: -

2.10.2.SET_GIP_R: SET CGOUTx_R Signal Mapping, GS_Panel=0 (Page2-R16~2Bh)

CMD Add	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
16	**R/W**	X	CGO1_PH_R	CGO1_INV_R	CGOUT1_R[4:0]					
17	**R/W**	X	CGO2_PH_R	CGO2_INV_R	CGOUT2_R[4:0]					
18	**R/W**	X	CGO3_PH_R	CGO3_INV_R	CGOUT3_R[4:0]					
19	**R/W**	X	CGO4_PH_R	CGO4_INV_R	CGOUT4_R[4:0]					
1A	**R/W**	X	CGO5_PH_R	CGO5_INV_R	CGOUT5_R[4:0]					
1B	**R/W**	X	CGO6_PH_R	CGO6_INV_R	CGOUT6_R[4:0]					
1C	**R/W**	X	CGO7_PH_R	CGO7_INV_R	CGOUT7_R[4:0]					
1D	**R/W**	X	CGO8_PH_R	CGO8_INV_R	CGOUT8_R[4:0]					
1E	**R/W**	X	CGO9_PH_R	CGO9_INV_R	CGOUT9_R[4:0]					
1F	**R/W**	X	CGO10_PH_R	CGO10_INV_R	CGOUT10_R[4:0]					
20	**R/W**	X	CGO11_PH_R	CGO11_INV_R	CGOUT11_R[4:0]					
21	**R/W**	X	CGO12_PH_R	CGO12_INV_R	CGOUT12_R[4:0]					
22	**R/W**	X	CGO13_PH_R	CGO13_INV_R	CGOUT13_R[4:0]					
23	**R/W**	X	CGO14_PH_R	CGO14_INV_R	CGOUT14_R[4:0]					
24	**R/W**	X	CGO15_PH_R	CGO15_INV_R	CGOUT15_R[4:0]					
25	**R/W**	X	CGO16_PH_R	CGO16_INV_R	CGOUT16_R[4:0]					
26	**R/W**	X	CGO17_PH_R	CGO17_INV_R	CGOUT17_R[4:0]					
27	**R/W**	X	CGO18_PH_R	CGO18_INV_R	CGOUT18_R[4:0]					
28	**R/W**	X	CGO19_PH_R	CGO19_INV_R	CGOUT19_R[4:0]					
29	**R/W**	X	CGO20_PH_R	CGO20_INV_R	CGOUT20_R[4:0]					
2A	**R/W**	X	CGO21_PH_R	CGO21_INV_R	CGOUT21_R[4:0]					
2B	**R/W**	X	CGO22_PH_R	CGO22_INV_R	CGOUT22_R[4:0]					

Description

This command sets GIP CGOUTx_R signal mapping when XOR(GS_Panel, GS)=0.

CGOx_PH_R: CGOUT voltage level while abnormal power off @ GIP_GAS_OPT='1'.

0: Pull to VGL. 1: Pull to VGH.

CGOx_INV_R: 0: CGOUT normal drive. 1: CGOUT drive inverse voltage level(VGH↔VGL).

CGOUTx(x=1~22**)_R[4:0]:** Please refer to below table.

CGOUTx_R	Output	CGOUTx_R	Output Signal	CGOUTx_R	Output Signal	CGOUTx_R	Output Signal
0_0000	STV0	**0**_1000	CKV4	**1**_0000	ETV0	**1**_1000	FLM2
0_0001	STV1	**0**_1001	CKV5	**1**_0001	ETV1	**1**_1001	CKV12
0_0010	STV2	**0**_1010	CKV6	**1**_0010	ETV2	**1**_1010	CKV13
0_0011	STV3	**0**_1011	CKV7	**1**_0011	ETV3	**1**_1011	CKV14
0_0100	CKV0	**0**_1100	CKV8	**1**_0100	INT	**1**_1100	CKV15
0_0101	CKV1	**0**_1101	CKV9	**1**_0101	VEN0	**1**_1101	Floating
0_0110	CKV2	**0**_1110	CKV10	**1**_0110	VEN1	**1**_1110	VGH
0_0111	CKV3	**0**_1111	CKV11	**1**_0111	FLM1	**1**_1111	VGL

Restriction: -

SET_GIP_L_GS: SET CGOUTx_L Mapping, GS_Panel=1 (Page2-R2C~41h)

CMD Add	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
2C	R/W	X	X	X	CGOUT1_L_GS [4:0]					
2D	R/W	X	X	X	CGOUT2_L_GS [4:0]					
2E	R/W	X	X	X	CGOUT3_L_GS [4:0]					
2F	R/W	X	X	X	CGOUT4_L_GS [4:0]					
30	R/W	X	X	X	CGOUT5_L_GS [4:0]					
31	R/W	X	X	X	CGOUT6_L_GS [4:0]					
32	R/W	X	X	X	CGOUT7_L_GS [4:0]					
33	R/W	X	X	X	CGOUT8_L_GS [4:0]					
34	R/W	X	X	X	CGOUT9_L_GS [4:0]					
35	R/W	X	X	X	CGOUT10_L_GS [4:0]					
36	R/W	X	X	X	CGOUT11_L_GS [4:0]					
37	R/W	X	X	X	CGOUT12_L_GS [4:0]					
38	R/W	X	X	X	CGOUT13_L_GS [4:0]					
39	R/W	X	X	X	CGOUT14_L_GS [4:0]					
3A	R/W	X	X	X	CGOUT15_L_GS [4:0]					
3B	R/W	X	X	X	CGOUT16_L_GS [4:0]					
3C	R/W	X	X	X	CGOUT17_L_GS [4:0]					
3D	R/W	X	X	X	CGOUT18_L_GS [4:0]					
3E	R/W	X	X	X	CGOUT19_L_GS [4:0]					
3F	R/W	X	X	X	CGOUT20_L_GS [4:0]					
40	R/W	X	X	X	CGOUT21_L_GS [4:0]					
41	R/W	X	X	X	CGOUT22_L_GS [4:0]					

Description

This command sets GIP CGOUTx_L signal mapping when either XOR(GS_Panel, GS)=1.

CGOUTx_L_GS[4:0]: Please refer to below table.

x=1~22

CGOUTx_L_GS	Output	CGOUTx_L_GS	Output	CGOUTx_L_GS	Output	CGOUTx_L_GS	Output
0_0000	STV0	**0**_1000	CKV4	**1**_0000	ETV0	**1**_1000	FLM2
0_0001	STV1	**0**_1001	CKV5	**1**_0001	ETV1	**1**_1001	CKV12
0_0010	STV2	**0**_1010	CKV6	**1**_0010	ETV2	**1**_1010	CKV13
0_0011	STV3	**0**_1011	CKV7	**1**_0011	ETV3	**1**_1011	CKV14
0_0100	CKV0	**0**_1100	CKV8	**1**_0100	INT	**1**_1100	CKV15
0_0101	CKV1	**0**_1101	CKV9	**1**_0101	VEN0	**1**_1101	Floating
0_0110	CKV2	**0**_1110	CKV10	**1**_0110	VEN1	**1**_1110	VGH
0_0111	CKV3	**0**_1111	CKV11	**1**_0111	FLM1	**1**_1111	VGL

Restriction

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2.10.3.SET_GIP_R_GS: SET CGOUTx_R Mapping, GS_Panel=1 (Page2-R42~57h)

CMD Add	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
42	R/W	X	X	X	CGOUT1_R_GS [4:0]					
43	R/W	X	X	X	CGOUT2_R_GS [4:0]					
44	R/W	X	X	X	CGOUT3_R_GS [4:0]					
45	R/W	X	X	X	CGOUT4_R_GS [4:0]					
46	R/W	X	X	X	CGOUT5_R_GS [4:0]					
47	R/W	X	X	X	CGOUT6_R_GS [4:0]					
48	R/W	X	X	X	CGOUT7_R_GS [4:0]					
49	R/W	X	X	X	CGOUT8_R_GS [4:0]					
4A	R/W	X	X	X	CGOUT9_R_GS [4:0]					
4B	R/W	X	X	X	CGOUT10_R_GS [4:0]					
4C	R/W	X	X	X	CGOUT11_R_GS [4:0]					
4D	R/W	X	X	X	CGOUT12_R_GS [4:0]					
4E	R/W	X	X	X	CGOUT13_R_GS [4:0]					
4F	R/W	X	X	X	CGOUT14_R_GS [4:0]					
50	R/W	X	X	X	CGOUT15_R_GS [4:0]					
51	R/W	X	X	X	CGOUT16_R_GS [4:0]					
52	R/W	X	X	X	CGOUT17_R_GS [4:0]					
53	R/W	X	X	X	CGOUT18_R_GS [4:0]					
54	R/W	X	X	X	CGOUT19_R_GS [4:0]					
55	R/W	X	X	X	CGOUT20_R_GS [4:0]					
56	R/W	X	X	X	CGOUT21_R_GS [4:0]					
57	R/W	X	X	X	CGOUT22_R_GS [4:0]					

Description

This command sets GIP CGOUTx_R signal mapping when either XOR(GS_Panel, GS)=1.

CGOUTx_R_GS[4:0]: Please refer to below table.

x=1~22

CGOUTx_R_GS	Output	CGOUTx_R_GS	Output	CGOUTx_R_GS	Output	CGOUTx_R_GS	Output
0_0000	STV0	**0**_1000	CKV4	**1**_0000	ETV0	**1**_1000	FLM2
0_0001	STV1	**0**_1001	CKV5	**1**_0001	ETV1	**1**_1001	CKV12
0_0010	STV2	**0**_1010	CKV6	**1**_0010	ETV2	**1**_1010	CKV13
0_0011	STV3	**0**_1011	CKV7	**1**_0011	ETV3	**1**_1011	CKV14
0_0100	CKV0	**0**_1100	CKV8	**1**_0100	INT	**1**_1100	CKV15
0_0101	CKV1	**0**_1101	CKV9	**1**_0101	VEN0	**1**_1101	Floating
0_0110	CKV2	**0**_1110	CKV10	**1**_0110	VEN1	**1**_1110	VGH
0_0111	CKV3	**0**_1111	CKV11	**1**_0111	FLM1	**1**_1111	VGL

Restriction

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2.10.4.SETGIP1: Set GIP Signal Timing_1 (Page2-R58~6Bh)

CMD Add	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
58	R/W	X	GIP_GAS_OPT	TGEQL	GIP_RST_EN	INIT_PORCH[3:0]				40
59	R/W	INIT_W[3:0]				X	INIT[10:8]			00
5A	R/W	INIT[7:0]								00
5B	R/W	X	X	STV_NUM[1:0]		X	X	X	X	10
5C	R/W	STV_S0[7:0]								02
5D	R/W	STV_W[3:0]				X	STV_S1[2:0]			10
5E	R/W	X	X	X	STV_S2[4:0]					01
5F	R/W	X	X	X	STV_S3[4:0]					02
60	R/W	ETV_W[3:0]				X	ETV_S1[2:0]			00
61	R/W	X	X	X	ETV_S2[4:0]					01
62	R/W	X	X	X	ETV_S3[4:0]					02
63	R/W	SETV_ON[7:0]								03
64	R/W	SETV_OFF[7:0]								7B
65	R/W		ETV_EN	ETV_NUM[1:0]		X	ETV_S0[10:8]			00
66	R/W	ETV_S0 [7:0]								00
67	R/W	CKV0_NUM[3:0]				CKV0_W[3:0]				71
68	R/W	CKV0_S0[7:0]								04
69	R/W	CKV0_ON[7:0]								06
6A	R/W	CKV0_OFF[7:0]								7B
6B	R/W	CKV0_DUM[7:0]								10

SETGIP2: Set GIP Signal Timing_2 (Page2-R6C~7Eh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
6C	R/W	-	-	FLM_MODE	GEQ_LINE	GEQ_W[3:0]				00
6D	R/W	-	-	GEQ_GGND1[5:0]						00
6E	R/W	-	-	GEQ_GGND2[5:0]						00
6F	R/W	GIPDR[1:0]		-	-	-	CKV_GROUP	CKV1_CON	CKV0_CON	00
70	R/W	CKV1_NUM[3:0]				CKV1_W[3:0]				00
71	R/W	CKV1_S0[7:0]								00
72	R/W	CKV1_ON[7:0]								06
73	R/W	CKV1_OFF[7:0]								86
74	R/W	CKV1_DUM[7:0]								00
75	R/W	FLM_EN	FLM_W[6:0]							00
76	R/W	FLM_ON[7:0]								00
77	R/W	VEN_EN	VEN_W[10:8]			FLM_NUM	FLM_OFF[10:8]			55
78	R/W	FLM_OFF[7:0]								00
79	R/W	VEN_W[7:0]								00
7A	R/W	VEN_S0[7:0]								05
7B	R/W	VEN_S1[7:0]								05
7C	R/W	VEN_DUM[7:0]								00
7D	R/W	VEN_ON[7:0]								03
7E	R/W	VEN_OFF[7:0]								86

Description

This command is used to Setting GIP Signal Timing.

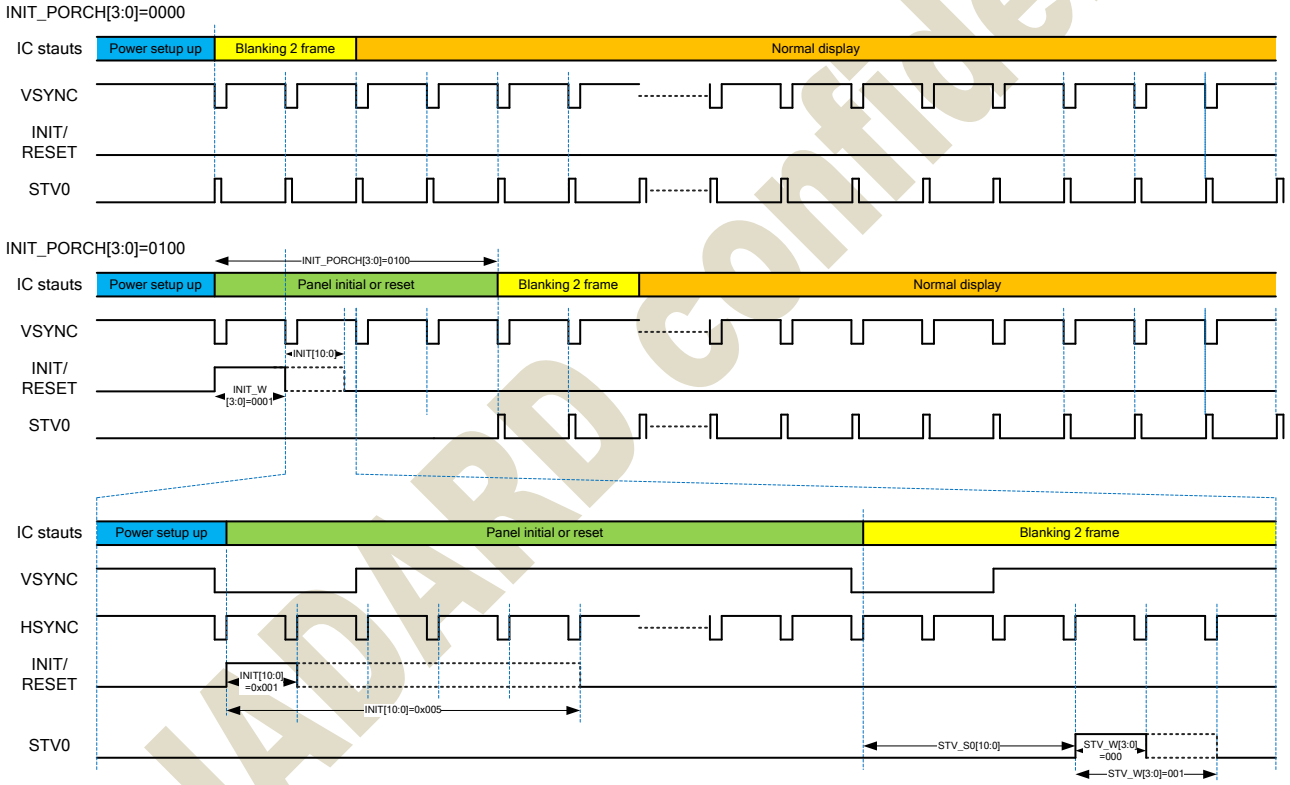
//INIT, Note:INIT signal has no EQ function.

INIT_PORCH[3:0]: INIT signal porch setting(Unit: frame).

INIT_W[3:0]: INIT signal frame width setting (Unit: frame).

INIT[10:0]: INIT signal line width setting (Unit: line).

INIT/RESET setting



//STV

STV_NUM[1:0]: Start pulse number.

STV_W[3:0]: Start pulse line width setting(Unit: line).

STV_S0[10:0]: Vsync to 1st Start pulse porch (Unit: line).

STV_S1 [2:0]: 1st Start pulse to 2nd Start pulse porch (Unit: line).

STV_S2 [4:0]: 1st Start pulse to 3rd Start pulse porch (Unit: line).

STV_S3 [4:0]: 1st Start pulse to 4th Start pulse porch (Unit: line).

SETV_ON[7:0]: Start pulse and End pulse turn on setting (Unit: OSC CLK).

SETV_OFF[7:0]: Start pulse and End pulse turn off setting (Unit: OSC CLK).

//GIP GAS_OPT

GIP_GAS_OPT: Set CGOUT behavior while abnormal power off. (OTP is need for using this bit.)

0: When abnormal power off occurs, scan blanking frame with higher speed continuously.

1: Pull CGOUTx to VGH or VGL depends on CGOx_PH_x setting.(PH=1 keep VGH, PH=0 keep VGL)

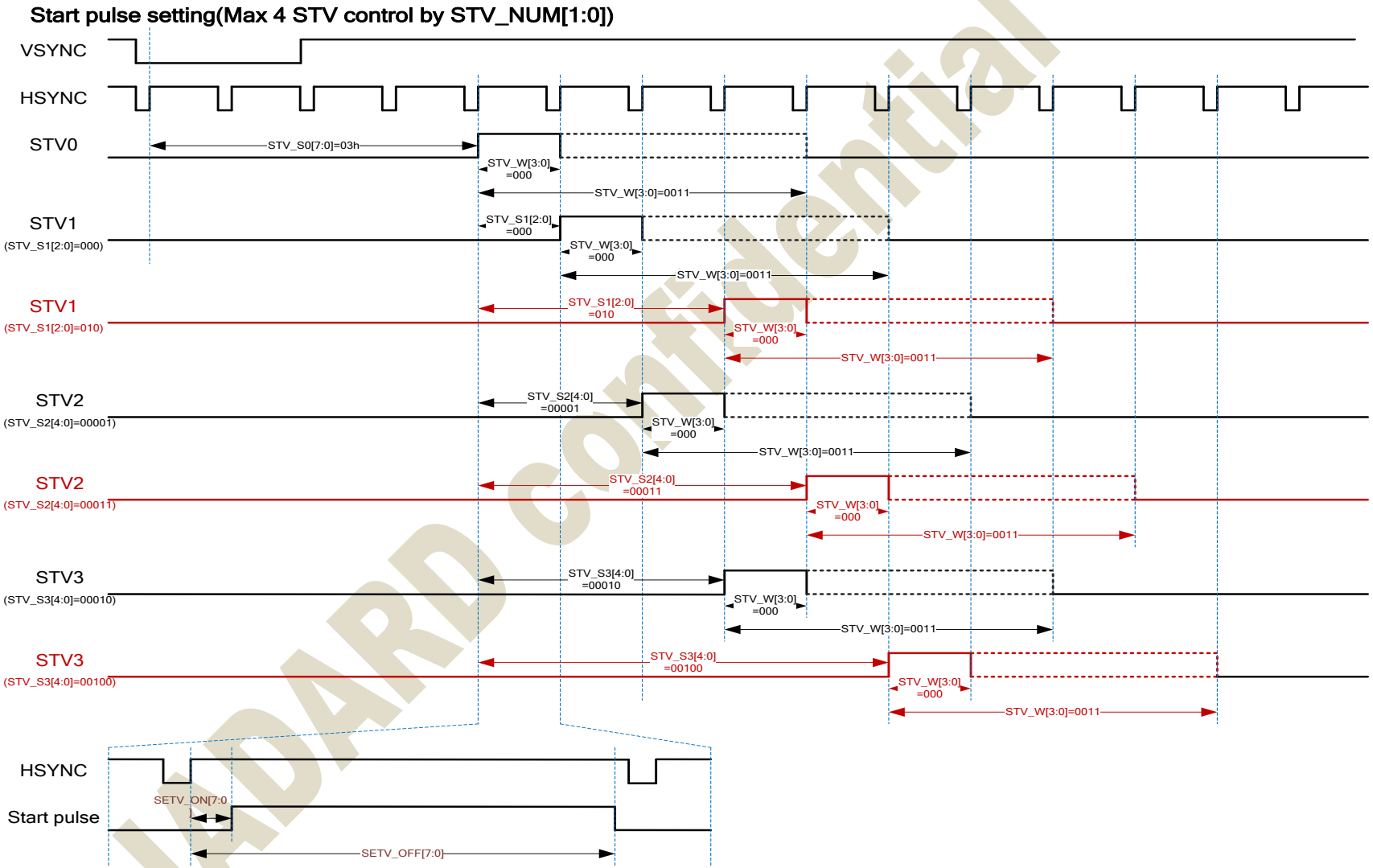
//GIP_RST_EN

GIP_RST_EN: GIP discharge behavior while HW_RST occurs.

When sleep in mode, if GIP_RST_EN=1, JD9161 will keep CGOUTx will as VGH or GND level via CGOn_PH_L/R bit

0: VGL level.

1: VGH level.



//CKV

CKV_GROUP: GIP clock group select,

'0'= Only group 0(CKV0~CKV12) ,

'1'=group 0(CKV0~CKV7) & group 1(CKV8~CKV11).

//CKV0

CKV0_NUM[3:0]: GIP clock pulse number of group 0.

CKV0_W[3:0]: GIP clock pulse line width setting of group 0(Unit: line) .

CKV0_S0[7:0]: VSYNC to 1st GIP clock pulse porch of group 0 (Unit: line).

CKV0_ON[7:0]: GIP clock pulse turn on setting of group 0(Unit: OSC CLK).

CKV0_OFF[7:0]: GIP clock pulse turn off setting of group 0(Unit: OSC CLK).

CKV0_CON: GIP clock pulse continuous Output in blanking area of group 1(CKV0~7). 0: non-continuous, 1: Continuous.

CKV0_DUM[7:0]: GIP clock pulse dummy line setting of group 0(Unit: line).

//CKV1

CKV1_NUM[3:0]: GIP clock pulse number of group 1(CKV8~11).

CKV1_W[3:0]: GIP clock pulse line width setting of group 1(CKV8~11)(Unit: line).

CKV1_S0 [7:0]: VSYNC to 1st GIP clock pulse porch of group 1(CKV8~11)(Unit: line).

CKV1_ON [7:0]: GIP clock pulse turn on setting of group 1(CKV8~11)(Unit: OSC CLK).

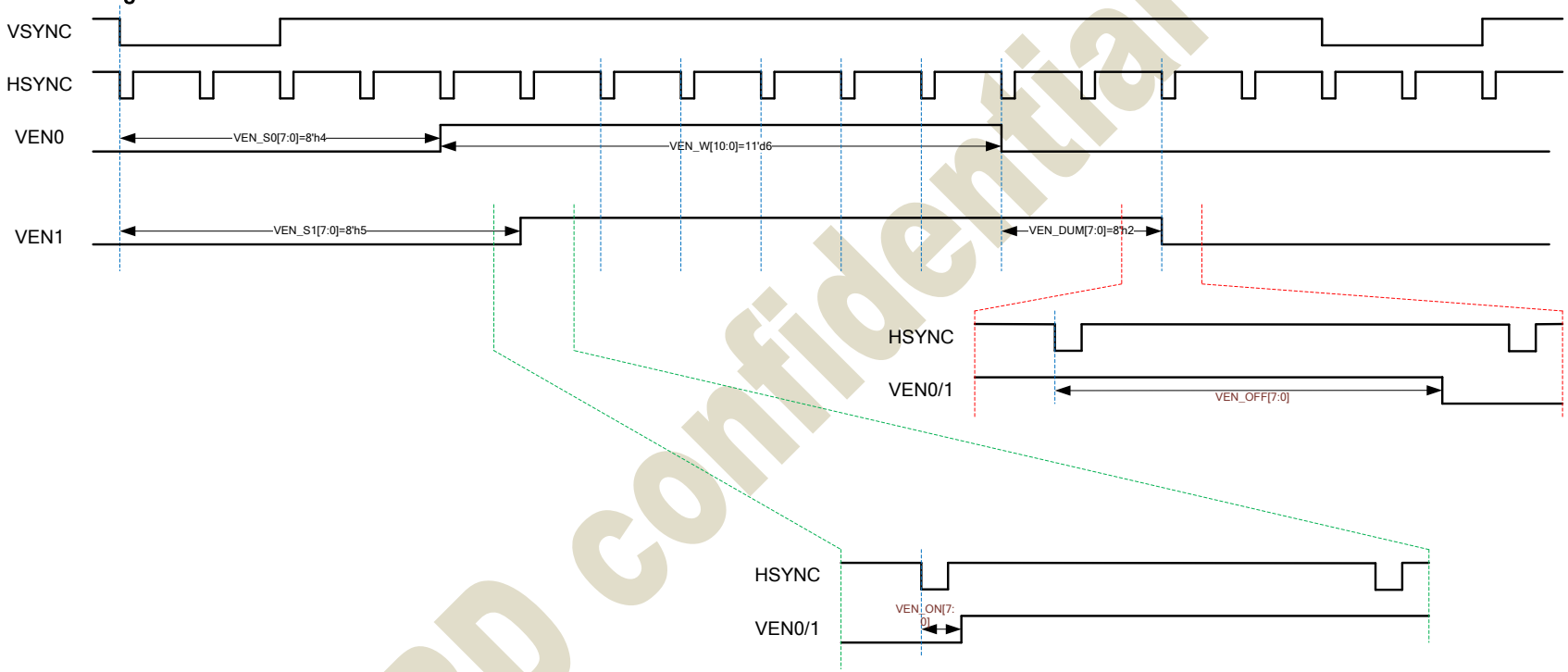
CKV1_OFF [7:0]: GIP clock pulse turn off setting of group 1(CKV8~11)(Unit: OSC CLK).

CKV1_CON: GIP clock pulse continuous Output in blanking area of group 1(CKV8~11). 0: non-continuous, 1: Continuous.

CKV1_DUM [7:0]: GIP clock pulse dummy line setting of group 1(CKV8~11)(Unit: line).

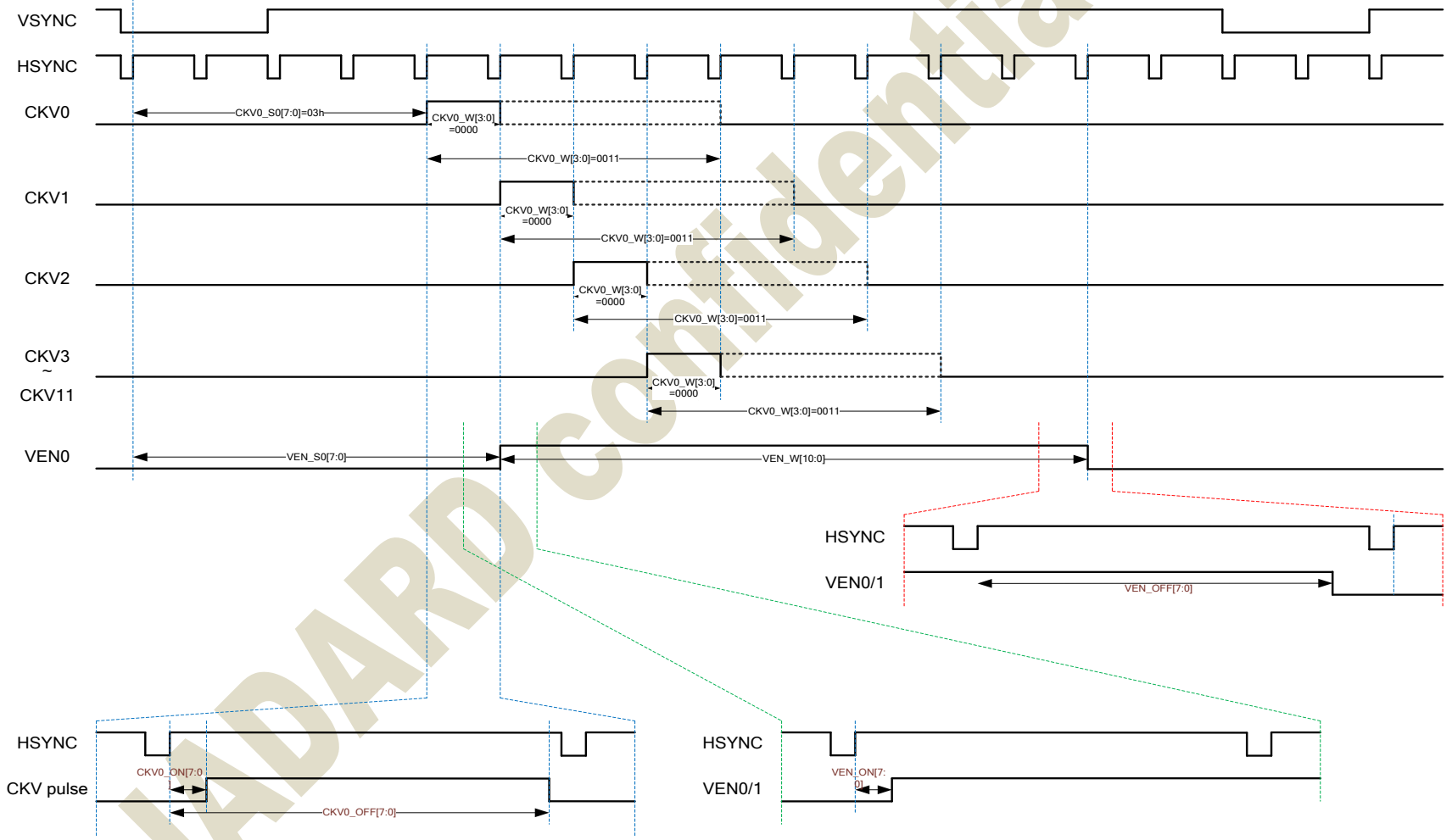
	//VEN
	VEN_W[10:0]: VEN0 pulse width setting (Unit: line)
	VEN_S0[7:0]: VSYNC to VEN0 pulse porch of rising (Unit: line)
	VEN_S1[7:0]: VSYNC to VEN1 pulse porch of rising (Unit: line)
	VEN_DUM[7:0]: VEN0 falling to VEN1 falling setting (Unit: line)
	VEN_ON[7:0]: VEN0/1 period turn on setting(Unit: OSC CLK).
	VEN_OFF[7:0]: VEN0/1 period turn off setting(Unit: OSC CLK).
	//VEN0 and VEN1

VEN setting



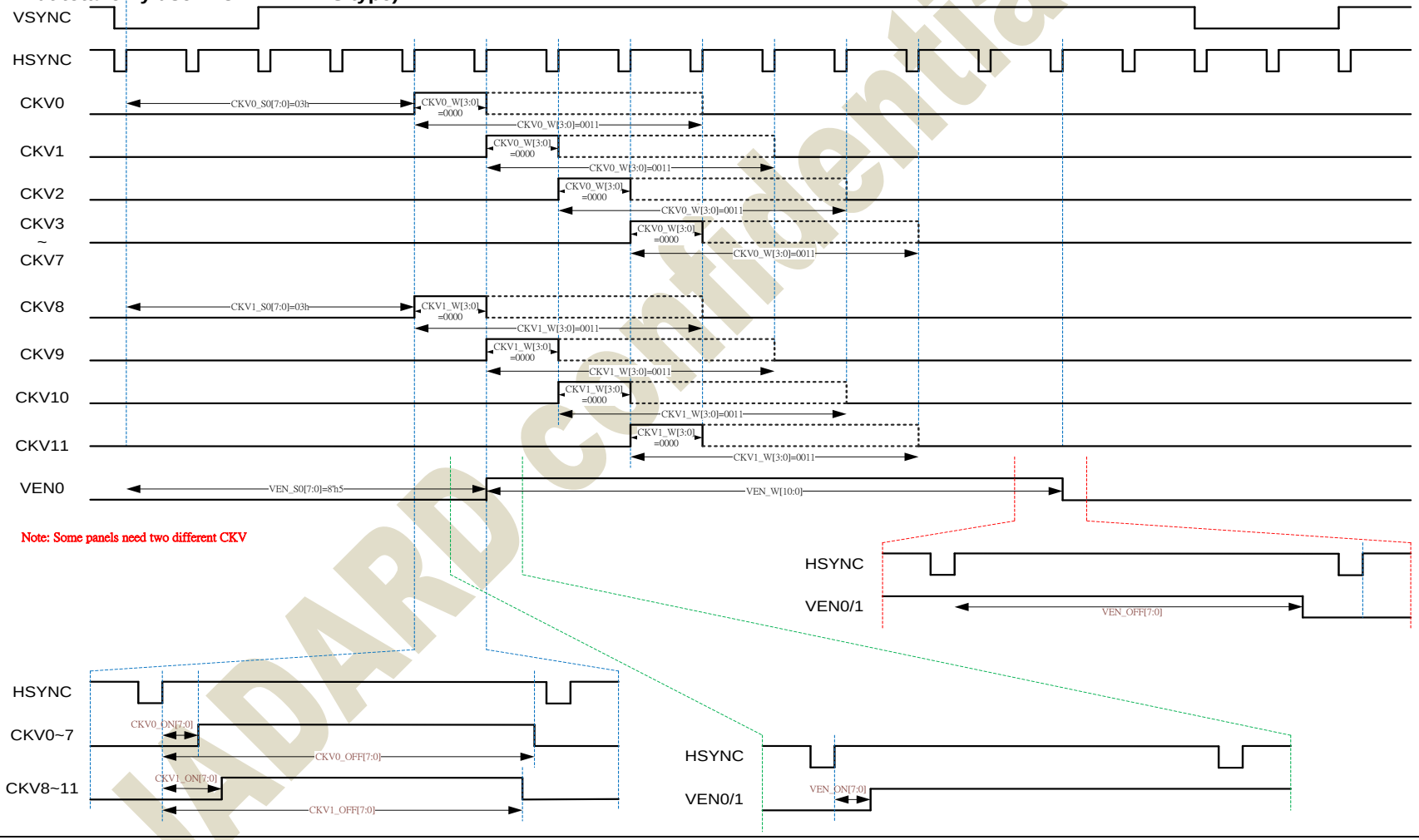
//CKV0 and VEN

CKV setting(Max 16 CKV control by CKV0_NUM[3:0], but only use 12CKV in LTPS type)

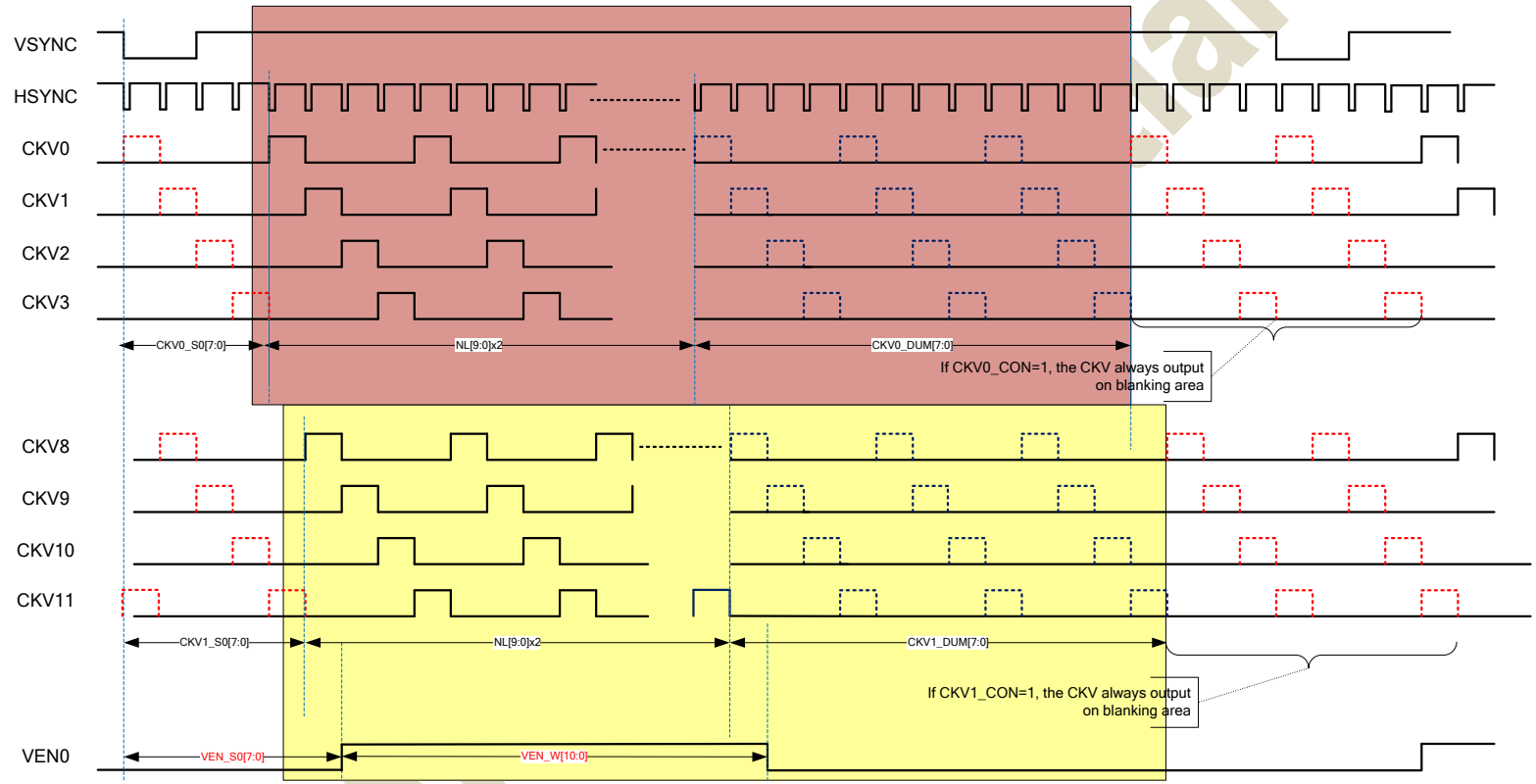


//CKV0, CKV1 and VEN

CKV setting(Max 8 CKV control by CKV0_NUM[3:0], and also max 8 CKV control by CKV1_NUM[3:0]
But total only use 12CKV in LTPS type)



//CKV Dummy and CKV_CON



//ETV

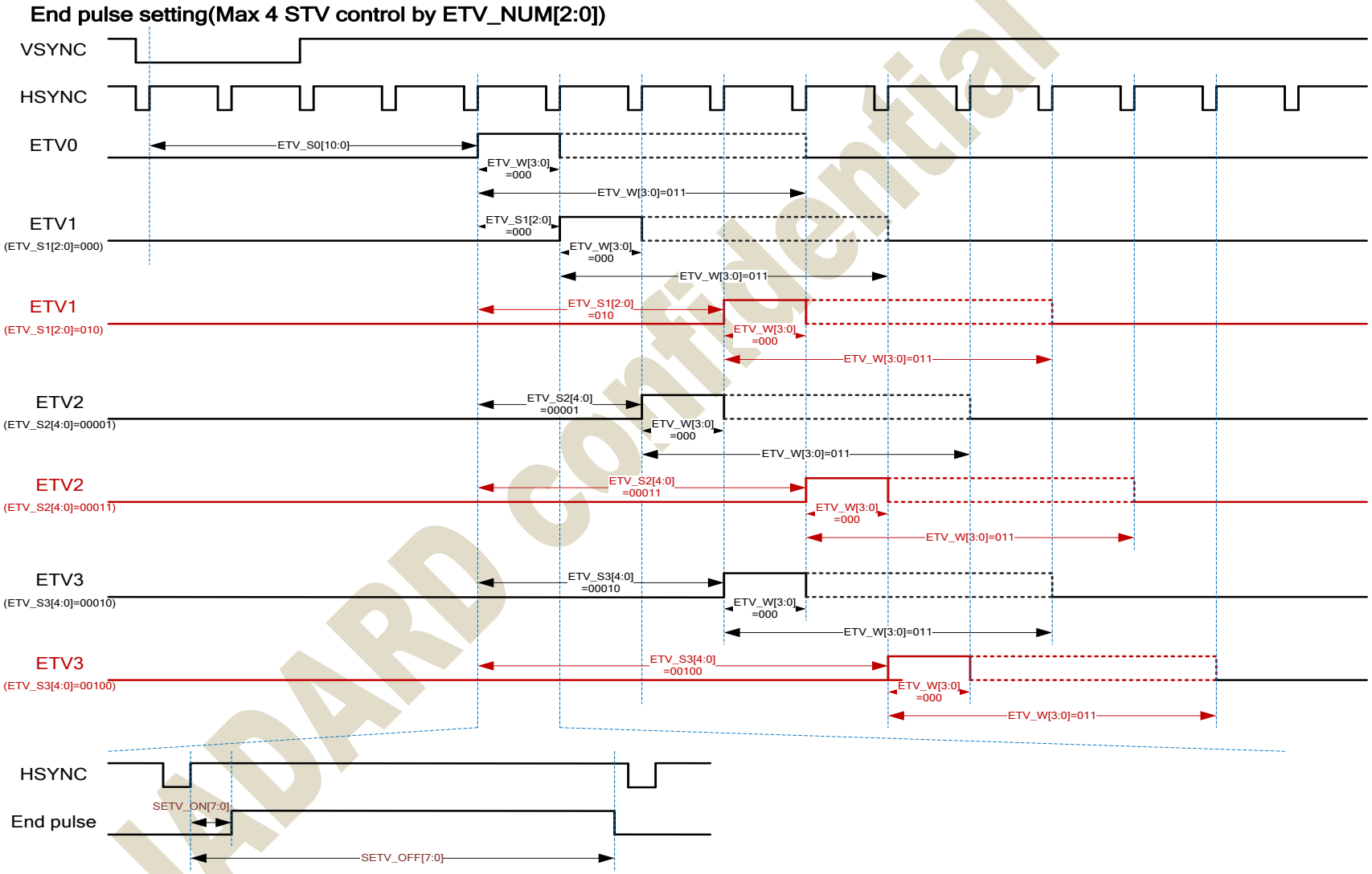
ETV_NUM[1:0]: End pulse number.

ETV_W[3:0]: End pulse line width setting (Unit: line).

ETV_S0 [10:0]: VSYNC to 1st End pulse porth (Unit: line).

ETV_S1[2:0]: 1st End pulse to 2nd End pulse porth (Unit: line)..

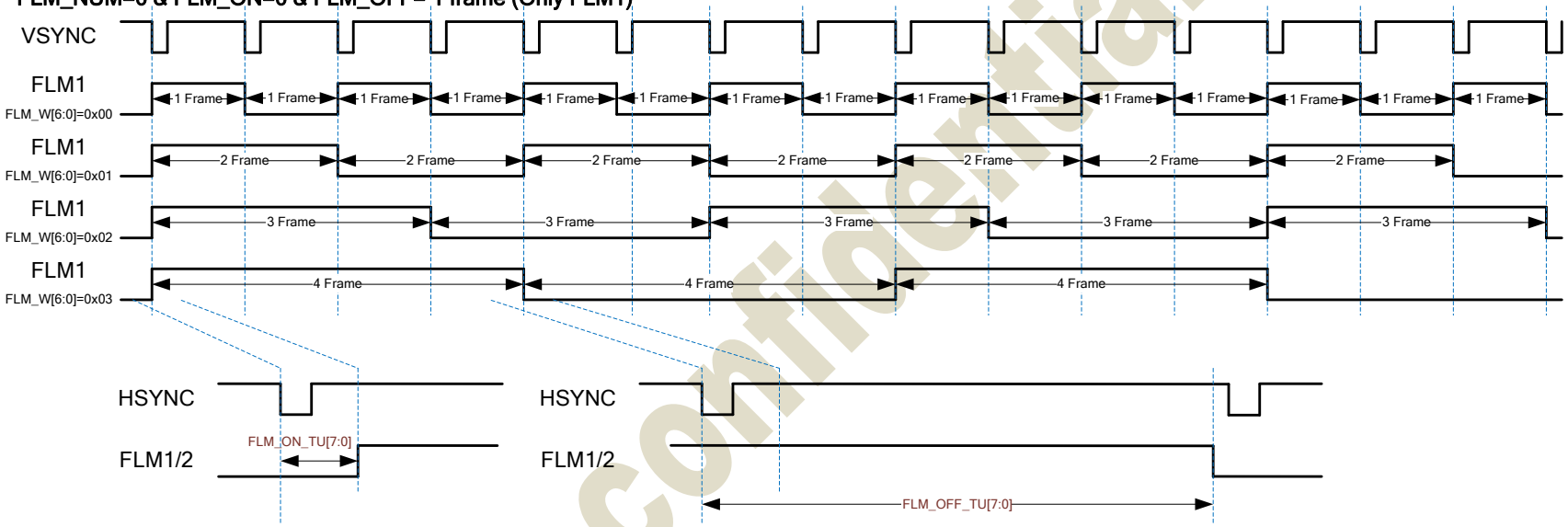
	ETV_S2 [4:0]: 1st End pulse to 3rd End pulse porth (Unit: line).. **ETV_S3 [4:0]:** 1st End pulse to 4th End pulse porth (Unit: line). **//ETV_EN** **ETV_EN:** ETV signal block enable. 0: Stop ETV signal control block, saving power. 1: Enable ETV signal control block.



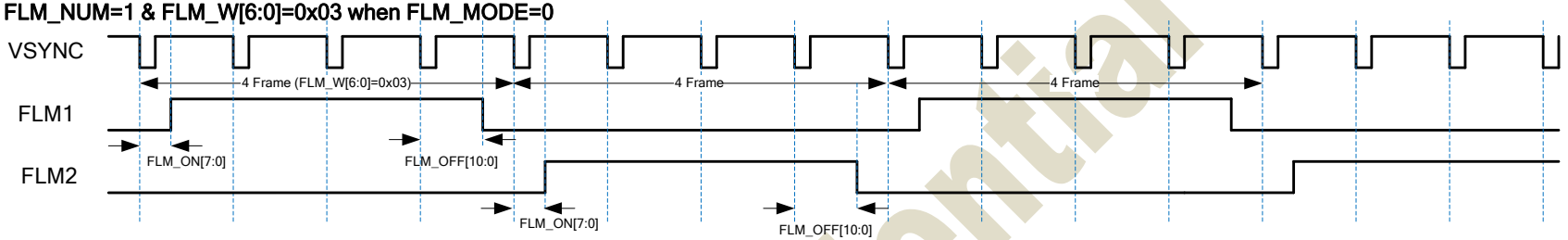
	//FLM **FLM_NUM:** FLM pulse number(0 or 1). **FLM_W[6:0]:** Frame number setting for FLM signal (Unit: frame). **FLM_ON[7:0]:** FLM pulse turn on setting (Unit: line). **FLM_OFF[10:0]:** FLM pulse turn off setting (Unit: line). **FLM_ON_TU[7:0]:** FLM pulse turn on setting (Unit: 8*osc). **FLM_OFF_TU[8:0]:** FLM pulse turn off setting (Unit: 8*osc). **FLM_EN:** FLM signal block enable. **FLM_MODE:** FLM signal mode select. 0: Stop FLM signal control block, saving power. 1: Enable FLM signal control block. Note:FLM signal has no EQ function.

FLM setting

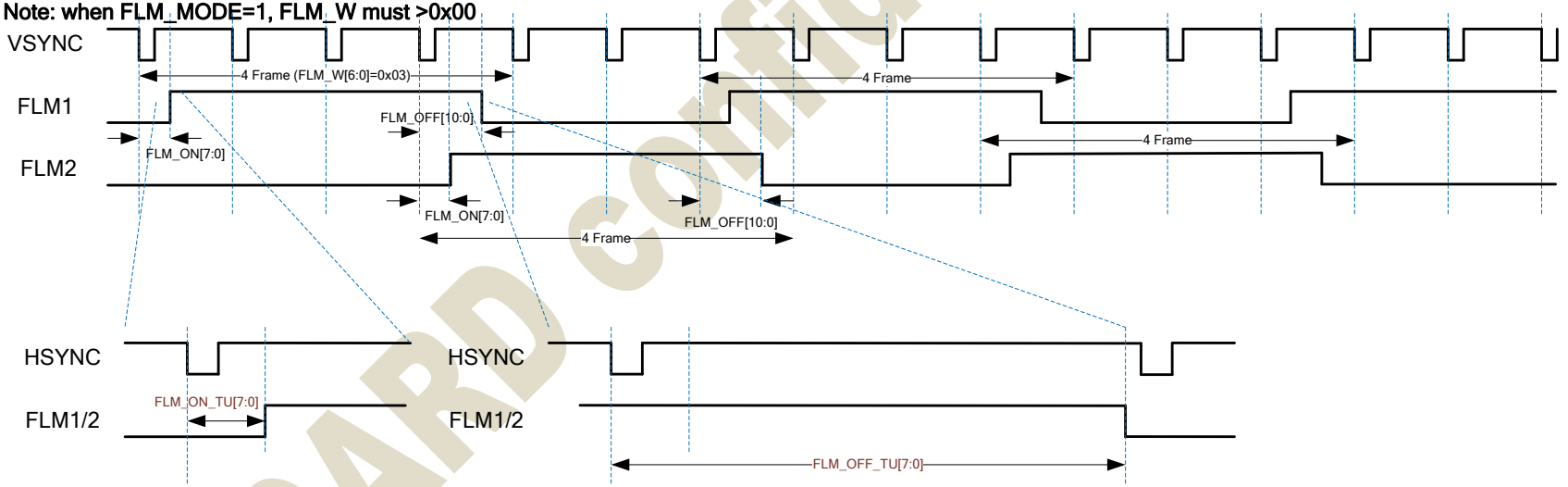
FLM_NUM=0 & FLM_ON=0 & FLM_OFF= 1 frame (Only FLM1)



FLM_NUM=1 & FLM_W[6:0]=0x03 when FLM_MODE=0



FLM_NUM=1 & FLM_W[6:0]=0x03 when FLM_MODE=1
Note: when FLM_MODE=1, FLM_W must >0x00



//GIP EQ

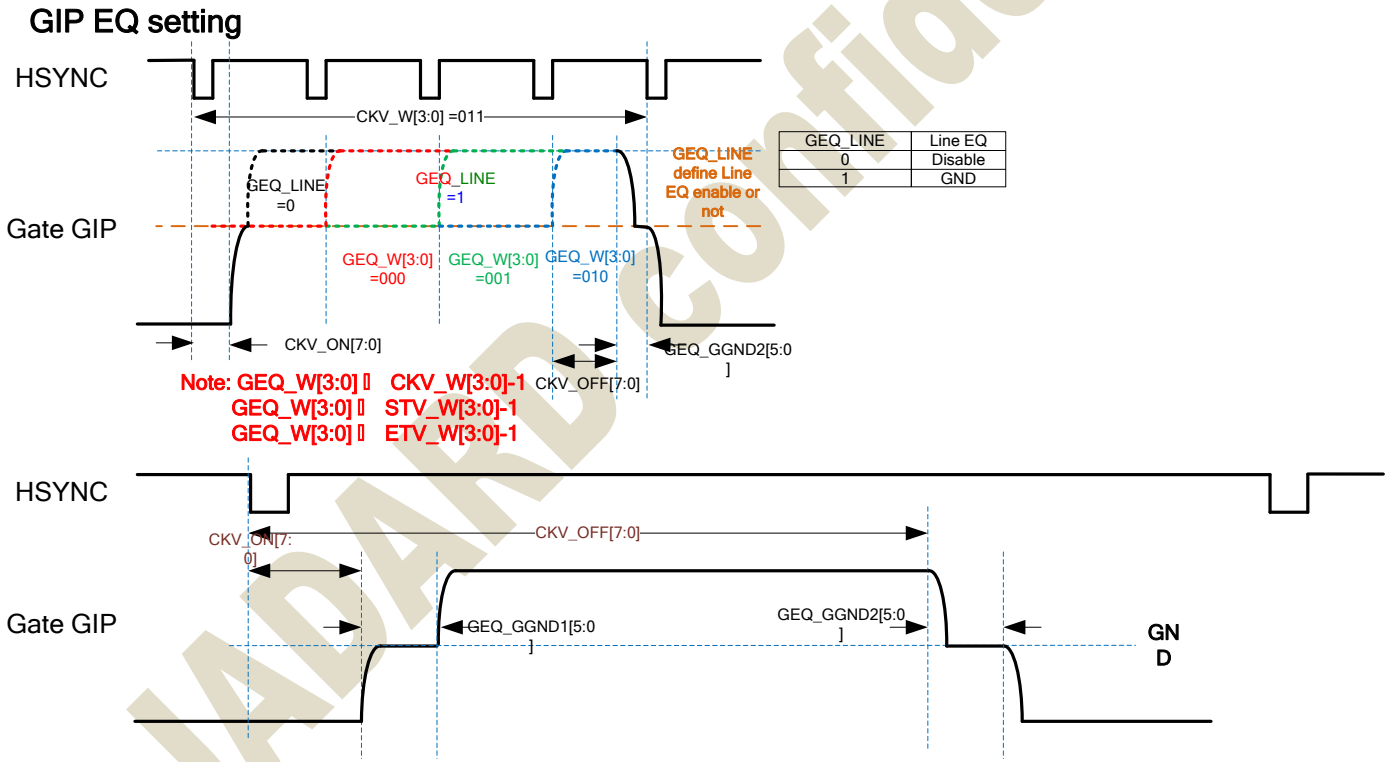
GEQ_W[3:0]: Set gate dis-charge line (Unit: line).

GEQ_GGND1[7:0]: Set gate EQ GND period for turn on(Unit: OSC CLK).

GEQ_GGND2[7:0]: Set gate EQ GND period for turn off(Unit: OSC CLK).

GEQ_LINE: Set gate line enable, 0:Line EQ disable, 1:EQ to GND(Unit: line).

EQ function for STV,ETV,CKV0,CKV1,VEN



GEQ_LINE	Line EQ
0	Disable
1	GND

	//GIPDR[1:0] **GPIDR[1:0]:** GIP CGOx PAD driving ability 00: 25% driving ability. 01: 50% driving ability. 10: 75% driving ability. 11: 100% driving ability.
Restriction	-

2.10.5.SET_GIP_OPT: Set GIP Option (Page2-R7F~80h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
7F	R/W	X	GIP_OPT0 [6:0]							
80	R/W	GIP_OPT1 [7:0]								

Description

This command is used to set additional GIP timing option.

	Function	Default
GIP_OPT0[1:0]	N/A	
GIP_OPT0[2]	vgz for gas when GIP_GAS_OPT = 1 1'b1: CGOx_PH_GAS_L/R 1'b0: keep floating if CGOUTx_L/R = 29	1'b0
GIP_OPT0[3]	Even/Odd line exchange 1'b1:exchanged 1'b0:not exchanged	1'b0
GIP_OPT0[4]	N/A	1'b0
GIP_OPT0[5]	Enable BOE timing, which resets CKVs when STV0 is asserted 1'b1:enable BOE timing 1'b0:disable BOE timing	1'b0
GIP_OPT0[6]	N/A	1'b0
GIP_OPT1[0]	MTK_INTERLACE_OPT	1'b0
GIP_OPT1[1]	Enable END_W1 / END_W23 region setting (PANDA_EN = 1, CGOx_END_W1/W2[1:0]) 1'b1:enable 1'b0:disable	1'b0
GIP_OPT1[2]	Enable U2D region setting 1'b1:enable 1'b0:disable	1'b0
GIP_OPT1[3]	Enable GAS for panda mode level 1'b1:enable 1'b0:disable	1'b0
GIP_OPT1[4]	Enable GIP start 1'b1: Original (TP_LD_DC3/4) 1'b0: Pwr_slpout	1'b0
GIP_OPT1[7:5]	N/A	3'h0

Restriction

-

2.10.6.SETGIP5: SET GIP Signal Timing_5(Page2-R81~89h)

CMD/Pas	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
81	R/W	-	FLM_EQ	ETV_BLK_S0[10:8]			STV_BLK_S0[10:8]			00
82	R/W	STV_BLK_S0[7:0]								00
83	R/W	ETV_BLK_S0[7:0]								00
84	R/W	STV_BLK_S2[3:0]				STV_BLK_S1[3:0]				00
85	R/W	STV_OPT[3:0]				STV_BLK_S3[3:0]				00
86	R/W	ETV_BLK_S2[3:0]				ETV_BLK_S1[3:0]				00
87	R/W	ETV_OPT[3:0]				ETV_BLK_S3[3:0]				00
88	R/W	FLM_ON_TU[7:0]								00
89	R/W	FLM_OFF_TU[7:0]								00

Description

This command sets GIP Signal .

STV_OPT[3:0]: 2nd STV pulse control.

STV_BLK_S0[10:0]: 2nd STV0 to 1st STV0 porch (Unit: line).

STV_ BLK_S1 [3:0]: 2nd STV1 to 2nd STV0 porch (Unit: line).

STV_ BLK_S2 [3:0]: 2nd STV2 to 2nd STV0 porch (Unit: line).

STV_ BLK_S3 [3:0]: 2nd STV3 to 2nd STV0 porch (Unit: line).

ETV_OPT[3:0]: 2nd ETV pulse control.

ETV_BLK_S0[10:0]: 2nd ETV0 to 1st ETV0 porch (Unit: line).

ETV_ BLK_S1 [3:0]: 2nd ETV1 to 2nd ETV0 porch (Unit: line).

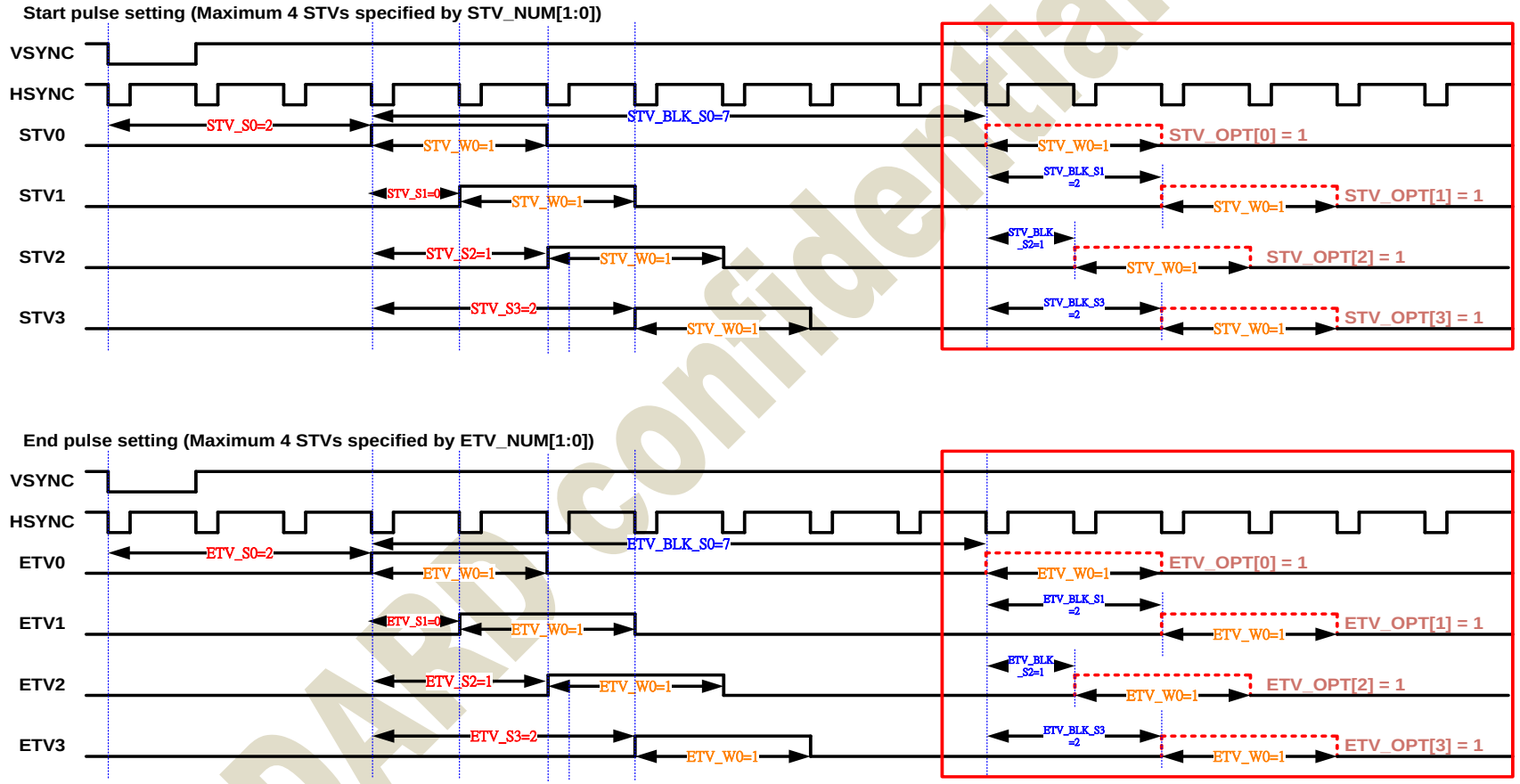
ETV_ BLK_S2 [3:0]: 2nd ETV2 to 2nd ETV0 porch (Unit: line).

ETV_ BLK_S3 [3:0]: 2nd ETV3 to 2nd ETV0 porch (Unit: line).

FLM_EQ: FLM EQ function control. **1**:Enable EQ funtion.

FLM_ON_TU[7:0]: FLM pulse turn on setting (Unit: 4*osc).

FLM_OFF_TU[7:0]: FLM pulse turn off setting (Unit: 4*osc).

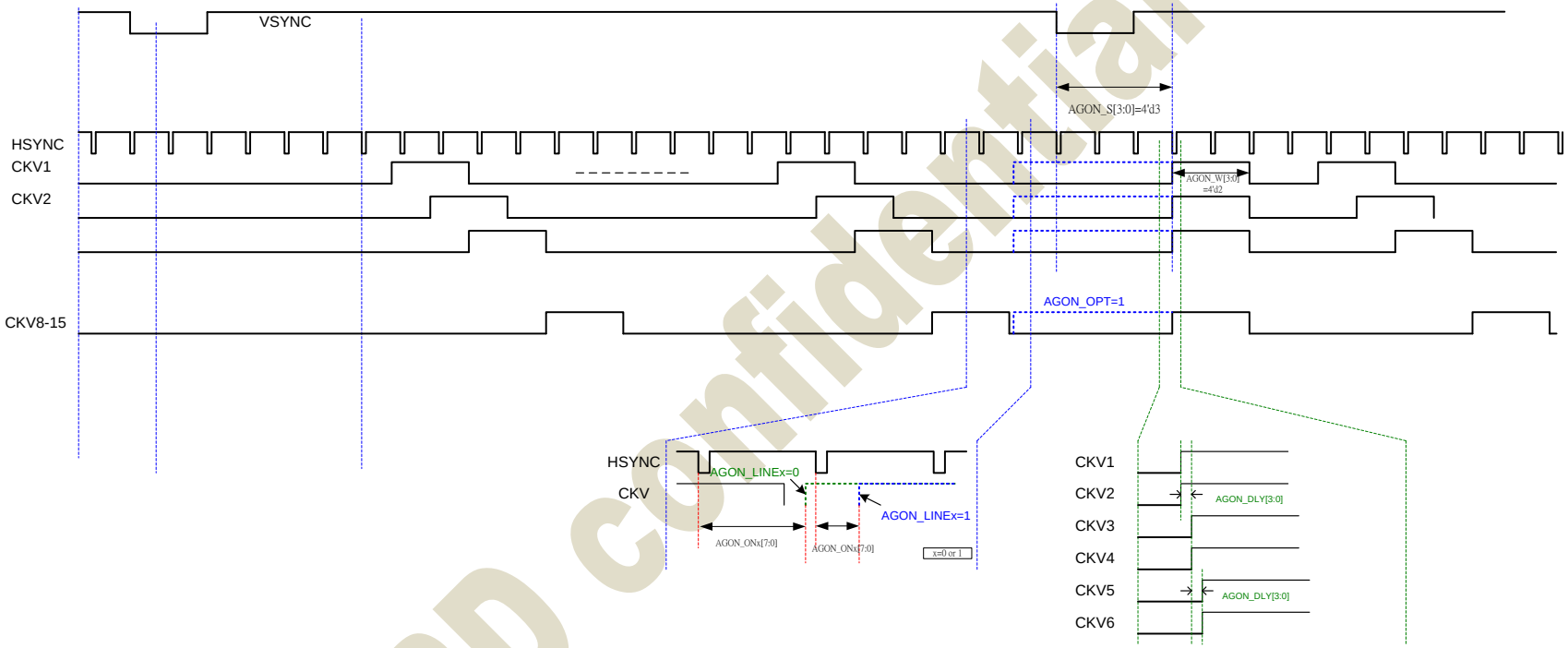
Restriction	
Restriction	-

2.10.7.SET_GIP_BIF: SET GIP Blanking In Frame (Page2-R8B~8Dh)

CMD/Pas	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
8B	**R/W**	-	GIP_OPT2[4:0]					CKV_BIF_S [9:8]		00
8C	**R/W**	CKV_BIF_S[7:0]								00
8D	**R/W**	CKV_BIF_W[7:0]								00
Description	This command sets GIP Signal for Tianma blanking in frame function. **GIP_OPT2[4:0]:** internal used, not open **CKV_BIF_S[9:0]:** revsered. **CKV_BIF_W[7:0]:** reversed.									
Restriction	-									

2.10.8.SETGIP3: SET GIP Signal Timing_3(Page2-R8E~92h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
8E	**R/W**	X	X	X	X	X	X	FLM_ON_LRN_EN	FLM_OFF_LRN_EN	01
8F	**R/W**	AGON_EN	AGON_OPT	AGON_LINE0	AGON_LINE1	AGON_DLY[3:0]				02
90	**R/W**	AGON_S[3:0]				AGON_W[3:0]				03
91	**R/W**	AGON_ON0[7:0]								08
92	**R/W**	AGON_ON1[7:0]								08
Restriction	This command sets GIP Signal width setting during different temprature. **FLM_ON_LRN_EN:** FLM signal on edge learning function enable. **FLM_OFF_LRN_EN:** FLM signal off edge learning function enable **AGON_EN:** All gate on function enable. **AGON_OPT:** All gate on function option. **AGON_LINE0:** All gate on function control for gruop 0 **AGON_LINE1:** All gate on function control for gruop 1 **AGON_DLY[3:0]:** All gate on function delay control, 200 ns/step **AGON_S[3:0]:** All gate on function shift **AGON_W[3:0]:** All gate on function width **AGON_ON0[7:0]:** All gate on function on time for group 0 **AGON_ON1[7:0]:** All gate on function on time for group 1.									

Description	CKV setting(Max 16 CKV control by CKV0_NUM[3:0], but only use 12CKV in LTPS type) 
Restriction	-

2.11. Jadard page 3 command description

2.11.1.CE CTRL0: Color Enhancement Control 0 (Page3-R 00h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
00h	R/W	X	X	X	X	X	X	X	CE_OTPROM_VLD	
Description	This command is used to control the color enhancement function. **CE_OTP_ROM_VLD:** Set CE reload register is come rom internal ROM code or OTP or keep initial setting. 0: Keep initial setting 1: Reload from OTP or internal ROM code.									
Restriction	-									

2.11.2.CE CTRL1 : Color Enhancement Control 1 (Page3-R01h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
01h	R/W	X	X	X	X	ce_edg_mode[1:0]		ce_sat_mode[1:0]		

Description

ce_sat_mode[1:0]: SATURATION enhance mode;

ce_sat_mode[1:0]	Mode
00	OFF
01	LOW
10	MED
11	HIGH

ce_edg_mode[1:0]: EDGE enhance mode;

ce_edg_mode[1:0]	Mode
00	OFF
01	LOW
10	MED
11	HIGH

Restriction: -

2.11.3.CE PRM: CE Related Parameter Setting (Page3-R02h~R2Ah)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R02h	R/W	X	X	X	CE_EDG_SP_PROT	CE_SAT_SP_PROT	CE_COL_EN	CE_HUE_EN	CE_VV_EN	
R03h	R/W	X	CE_THREF[2:0]			X	CE_THSAT[2:0]			
R04h	R/W	X	CE_THGREY[2:0]			X	CE_THCOLOR[2:0]			
R05h	R/W	CE_SAT_OFFS[7:0]								
R06h	R/W	CE_REF_OFFS[7:0]								
R07h	R/W	X	X	X	X	X	CE_THCOLOR2[2:0]			
R08h	R/W	CE_COL_OFFS[7:0]								
R09h	R/W	CE_SG016[3:0]				CE_SG000[3:0]				
R0Ah	R/W	CE_SG048[3:0]				CE_SG032[3:0]				
R0Bh	R/W	CE_SG080[3:0]				CE_SG064[3:0]				
R0Ch	R/W	CE_SG112[3:0]				CE_SG096[3:0]				
R0Dh	R/W	CE_SG144[3:0]				CE_SG128[3:0]				
R0Eh	R/W	CE_SG176[3:0]				CE_SG160[3:0]				
R0Fh	R/W	CE_SG208[3:0]				CE_SG192[3:0]				
R10h	R/W	CE_SG240[3:0]				CE_SG224[3:0]				
R11h	R/W	X	X	X	X	CE_SG255[3:0]				
R12h	R/W	X	X	CE_HUE_TBL00[5:0]						
R13h	R/W	X	X	CE_HUE_TBL01[5:0]						
R14h	R/W	X	X	CE_HUE_TBL02[5:0]						
R15h	R/W	X	X	CE_HUE_TBL03[5:0]						
R16h	R/W	X	X	CE_HUE_TBL04[5:0]						
R17h	R/W	X	X	CE_HUE_TBL05[5:0]						
R18h	R/W	X	X	CE_HUE_TBL06[5:0]						
R19h	R/W	X	X	CE_HUE_TBL07[5:0]						
R1Ah	R/W	X	X	CE_HUE_TBL08[5:0]						
R1Bh	R/W	X	X	CE_HUE_TBL09[5:0]						
R1Ch	R/W	X	X	CE_HUE_TBL10[5:0]						
R1Dh	R/W	X	X	CE_HUE_TBL11[5:0]						
R1Eh	R/W	X	X	CE_HUE_TBL12[5:0]						
R1Fh	R/W	X	X	CE_HUE_TBL13[5:0]						
R20h	R/W	X	X	CE_HUE_TBL14[5:0]						
R21h	R/W	X	X	CE_HUE_TBL15[5:0]						
R22h	R/W	X	X	CE_HUE_TBL16[5:0]						
R23h	R/W	X	X	CE_HUE_TBL17[5:0]						

R24h	R/W	X	X	CE_HUE_TBL18[5:0]	
R25h	R/W	X	X	CE_HUE_TBL19[5:0]	
R26h	R/W	X	X	CE_HUE_TBL20[5:0]	
R27h	R/W	X	X	CE_HUE_TBL21[5:0]	
R28h	R/W	X	X	CE_HUE_TBL22[5:0]	
R29h	R/W	X	X	CE_HUE_TBL23[5:0]	
R2Ah	R/W	CE_EDG_FAC2[3:0]		CE_EDG_FAC1[3:0]	

Description

This command is used to control the image enhancement function.

ce_edg_sp_prot: If special pattern be detected, edge enhancement will be disabled with the protection is active.
0: no protect 1: protect

ce_sat_sp_prot: If special pattern be detected, saturation enhancement will be disabled with the protection is active.
0: no protect
1: protect

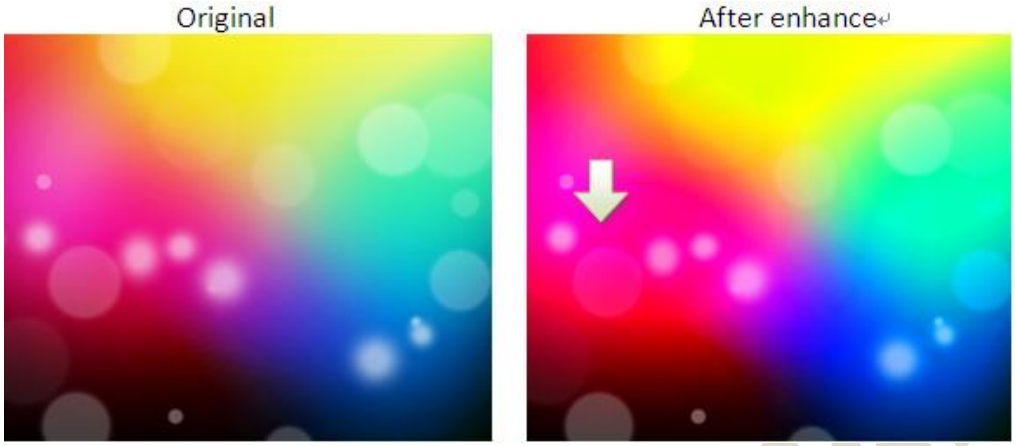
ce_col_en: Enable second color threshold of color protect in color enhancement.
0: disable
1: enable

ce_hue_en: Enable hue factor of local gain in color enhancement.
0: disable
1: enable

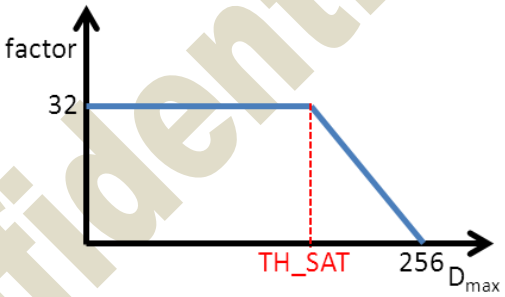
ce_vv_en: Enable reflection protect and saturation protect in color enhancement.
0: disable
1: enable

ce_THSAT[2:0]: Saturation local gain factor threshold.
Factor decreases when per pixel saturation (RGB_{max}-RGB_{min}) is greater than this threshold.

ce_SAT_OFFS[7:0]: Saturation local gain factor offset.
1. Let the TH_SAT to higher gray
2. factor' = factor *(256-TH-OFFS) / (256-TH)
   SAT_OFFS should be less than (256- TH_SAT)



ce_THREF[2:0]	Threshold
0x0	0
0x1	248
0x2	240
0x3	224
0x4	192
0x5	128
Others	0



A. Shift the TH_SAT to higher gray.

$$NEW\_TH = TH\_SAT + SAT\_OFFS \quad (2\text{-}1)$$

B. Reduce max factor.

$$NEW\_factor = factor \times \frac{256 - TH\_SAT - SAT\_OFFS}{256 - TH\_SAT} \quad (2\text{-}2)$$

In follow figure, there are three curves:

Assume fac = 16,

Blue curve: TH = 128, OFFS = 0

NEW_TH = 128 + 0 = 128

NEW_factor = fac*(256-128-0)/(256-128) = 16

Red curve: TH = 128, OFFS = 20

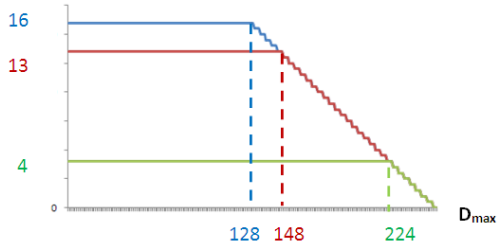
NEW_TH = 128 + 20 = 148,

NEW_factor = fac*(256-128-20)/(256-128) = 13

Green curve: TH = 128, OFFS = 96

NEW_TH = 128 + 96 = 224

NEW_factor = fac*(256-128-96)/(256-128) =4



ce_THREF[2:0]: Saturation local gain factor threshold.

Factor decreases when per pixel reflection (RGB_{max}) is greater than this threshold.

ce_REF_OFFS[7:0]: Saturation local gain factor offset.

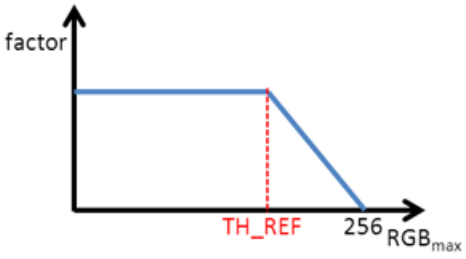
1. Let the TH_REF to higher gray
2. factor' = factor *(256-TH-OFFS) / (256-TH)

REF_OFFS should be less than (256- TH_REF)

Original

After Enhance

ce_THREF[2:0]	Threshold
0x0	0
0x1	248
0x2	240
0x3	224
0x4	192
0x5	128
Others	0



A. Shift the TH_REF to higher gray.

$$NEW\_TH = TH\_REF + REF\_OFFS \quad (2\text{-}3)$$

B. Reduce max factor.

$$NEW\_factor = factor \times \frac{256 - TH\_REF - REF\_OFFS}{256 - TH} \quad (2\text{-}4)$$

In follow figure, there are three curves:

Assume fac = 16,

Blue curve: TH = 128, OFFS = 0

NEW_TH = 128 + 0 = 128

NEW_factor = fac*(256-128-0)/(256-128) =16

Red curve: TH = 128, OFFS = 20

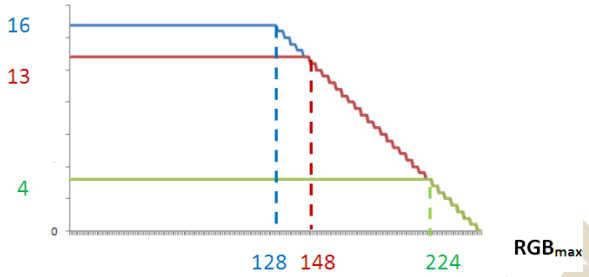
NEW_TH = 128 + 20 = 148,

NEW_factor = fac*(256-128-20)/(256-128) =13

Green curve: TH = 128, OFFS = 96

NEW_TH = 128 + 96 = 224

NEW_factor = fac*(256-128-96)/(256-128) =4



ce_THCOLOR[2:0]: Saturation local gain factor threshold.

Factor decreases when per pixel colorful (RGB_{min}) is smaller than this threshold.

ce_THCOLOR2[2:0]: Saturation local gain factor threshold.

Factor decreases when per pixel colorful (RGB_{min}) is smaller than this threshold.

Second threshold to protect special range

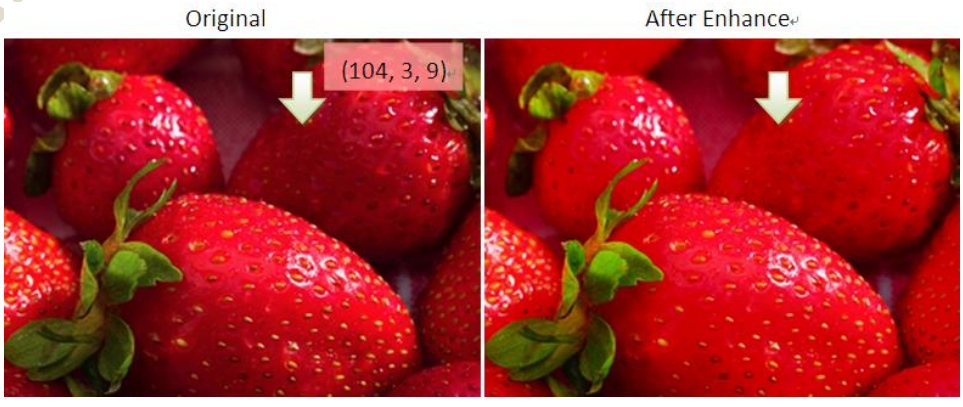
value range : 0x0: 0, 0x1: 008, 0x2: 016, 0x3: 032, 0x4: 064, 0x5: 128, others: 0

TH_COLOR2 should be greater than TH_COLOR

ce_COL_OFFS[7:0]: Saturation local gain factor offset.

Let the TH_COLOR2 to lower gray

COL_OFFS should be less than (TH_COLOR2 - TH_COLOR)



ce_THCOLOR[2:0]/	Threshold	factor ↑

ce_THCOLOR2[2:0]	
0x0	0
0x1	008
0x2	016
0x3	032
0x4	064
0x5	128
Others	0

A. Shift the TH_COLOR2 to lower gray.

$$NEW\_TH2 = TH\_COLOR2 - COL\_OFFS \quad (2\text{-}5)$$

B. Raise the lowest factor

$$Lowest\_point = 32 \times \frac{TH\_COLOR + COL\_OFFS}{TH\_COLOR2} \quad (2\text{-}6)$$

In follow figure, there are three curves:

Assume fac = 16,

Blue curve: rg_ce_THCOLOR = 64, Not second turning point.

rg_col_en = 0, rg_ce_THCOLOR2 = don't care, rg_ce_COL_OFFS = don't care

Red curve: rg_ce_THCOLOR = 64,

rg_col_en = 1, rg_ce_THCOLOR2 = 128, rg_ce_COL_OFFS = 0

Second turning point = 128 – 0 = 128

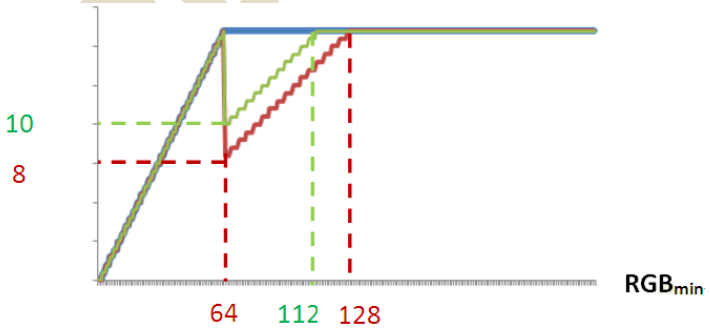
Lowest point = fac*(64+0)/(128) =8

Green curve: rg_ce_THCOLOR = 64,

rg_col_en = 1, rg_ce_THCOLOR2 = 128, rg_ce_COL_OFFS = 16

Second turning point = 128 – 16 = 112

Lowest point = fac*(64+16)/(128) =10



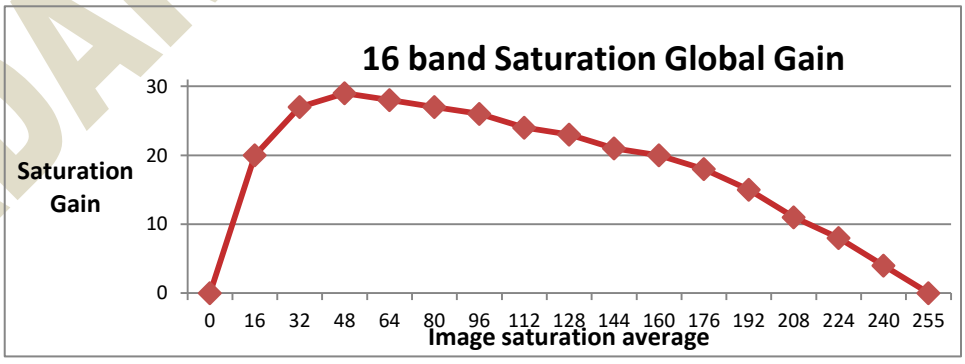
ce_THGREY[2:0]: Saturation local gain factor threshold.

Factor decreases when per pixel gray (RGBmax-RGBmin) is smaller than this threshold.

ce_TH_GREY [2:0]	Threshold
0x0	0
0x1	008
0x2	016
0x3	032
0x4	064
0x5	128
Others	0

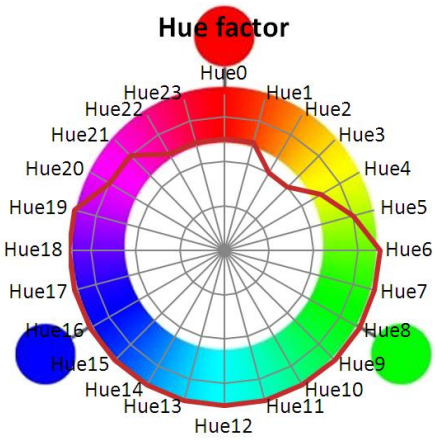
ce_SGXXX[4:0]: Saturation global gain. Gain = 1 + (value/16)

Algorithm will calculate whole image saturation average to select the global saturation gain. And then check per pixel characteristic to give it a local gain factor to avoid over enhancement. It's also allowed different gain factor in different hue angles.



CE_HUE_TBLXX[5:0]: Hue factor of saturation gain.Don't be set 0.

Use user definition to decide different gain factors in different hue angles.



CE_EDG_FAC1[3:0]: Edge enhance gain k_1.

0 for largest enhance, 7 for smallest enhance

CE_EDG_FAC2[3:0]: Edge enhance gain k_2.

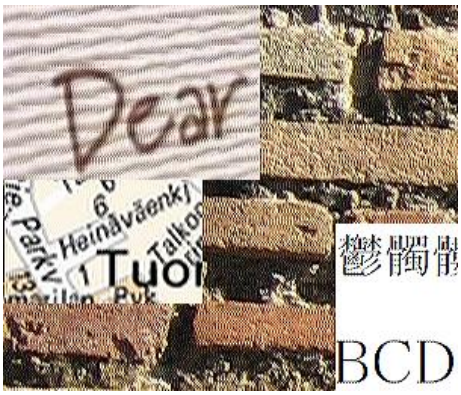
0 for largest enhance, 7 for smallest enhance

See function

Value >7, edge enhance OFF

$$\text{Gain} = \begin{cases} 1 \quad , & rg\_ce\_EDG\_FAC = 0 \\ 1/2, & rg\_ce\_EDG\_FAC = 1 \\ 1/4, & rg\_ce\_EDG\_FAC = 2 \\ 1/8, & rg\_ce\_EDG\_FAC = 3 \\ 1/16, & rg\_ce\_EDG\_FAC = 4 \\ 1/32, & rg\_ce\_EDG\_FAC = 5 \\ 1/64, & rg\_ce\_EDG\_FAC = 6 \\ 1/128, & rg\_ce\_EDG\_FAC = 7 \\ 0, & rg\_ce\_EDG\_FAC = Others \end{cases}$$

(a) rg_ce_EDG_FAC1=8, OFF



(b) rg_ce_EDG_FAC1=0,

	rg_ce_EDG_FAC2=8  (c) rg_ce_EDG_FAC1=1, rg_ce_EDG_FAC2=8 rg_ce_EDG_FAC2=8  (d) rg_ce_EDG_FAC1=2, rg_ce_EDG_FAC2=8
Restriction	-

2.11.4.DGC_CTRL: DGC Control Register (Page3- R2Bh~ R2Fh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>R2Bh</td><td>R/W</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>DGC_EN</td><td></td></tr>
<tr><td>R2Ch</td><td>R/W</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td colspan="2">DGC_SELECT[1:0]</td><td></td></tr>
<tr><td>R2Dh</td><td>R/W</td><td>-</td><td>-</td><td>-</td><td>DTR_EN</td><td colspan="3">DGC_CHKSUM_EN[2:0]</td><td>DGC_REG
_SYNC_GT</td><td></td></tr>
<tr><td>R2Eh</td><td>R/W</td><td colspan="8">DGC_GT_BYTE0[7:0]</td><td></td></tr>
<tr><td>R2Fh</td><td>R/W</td><td colspan="8">DGC_GT_BYTE1[7:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command is used to set DGC control setting.
DGC_EN: Digital gamma control enable/disable.
DGC_SELECT[1:0]: Mux selection for DGC.
<table>
<tr><td>DGC_SELECT[1:0]</td><td>By Pass</td><td>DGC1</td><td>DGC2</td></tr>
<tr><td>0h</td><td>R</td><td>G</td><td>B</td></tr>
<tr><td>1h</td><td>G</td><td>R</td><td>B</td></tr>
<tr><td>2h</td><td>B</td><td>G</td><td>R</td></tr>
<tr><td>3h</td><td>R</td><td>G</td><td>B</td></tr>
</table>
DTR_EN: Dithering enable.
DGC_CHKSUM_EN[2:0]: Set internal checksum function enable/disable.
DGC_REG_SYNC_GT: Set register sync with external VSYNC enable/disable.
DGC_GT_BYTE0[7:0]: Clock gating enable for DGC block
DGC_GT_BYTE1[7:0]: Clock gating enable for DGC block</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
</table>

2.11.5.SET_DIGITAL_GAMMA1: Set Gamma Curve 1 (Page3-R30h~ R53h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R30h	R/W	-	DGC_GAMMA1_GAIN[6:0]							-
R31h	R/W	DGC_GAMMA1_OFFSET[3:0]				DGC_GAMMA1_000[3:0]				-
R32h	R/W	DGC_GAMMA1_004[3:0]				DGC_GAMMA1_008[3:0]				
R33h	R/W	DGC_GAMMA1_012[3:0]				DGC_GAMMA1_016[3:0]				
R34h	R/W	DGC_GAMMA1_020[3:0]				DGC_GAMMA1_024[3:0]				
R35h	R/W	DGC_GAMMA1_028[3:0]				DGC_GAMMA1_032[3:0]				
R36h	R/W	DGC_GAMMA1_036[3:0]				DGC_GAMMA1_040[3:0]				
R37h	R/W	DGC_GAMMA1_044[3:0]				DGC_GAMMA1_048[3:0]				
R38h	R/W	DGC_GAMMA1_052[3:0]				DGC_GAMMA1_056[3:0]				
R39h	R/W	DGC_GAMMA1_060[3:0]				DGC_GAMMA1_064[3:0]				
R3Ah	R/W	DGC_GAMMA1_068[3:0]				DGC_GAMMA1_072[3:0]				
R3Bh	R/W	DGC_GAMMA1_076[3:0]				DGC_GAMMA1_080[3:0]				
R3Ch	R/W	DGC_GAMMA1_084[3:0]				DGC_GAMMA1_088[3:0]				
R3Dh	R/W	DGC_GAMMA1_092[3:0]				DGC_GAMMA1_096[3:0]				
R3Eh	R/W	DGC_GAMMA1_100[3:0]				DGC_GAMMA1_104[3:0]				
R3Fh	R/W	DGC_GAMMA1_108[3:0]				DGC_GAMMA1_112[3:0]				
R40h	R/W	DGC_GAMMA1_116[3:0]				DGC_GAMMA1_120[3:0]				
R41h	R/W	DGC_GAMMA1_124[3:0]				DGC_GAMMA1_128[3:0]				
R42h	R/W	DGC_GAMMA1_132[3:0]				DGC_GAMMA1_136[3:0]				
R43h	R/W	DGC_GAMMA1_140[3:0]				DGC_GAMMA1_144[3:0]				
R44h	R/W	DGC_GAMMA1_148[3:0]				DGC_GAMMA1_152[3:0]				
R45h	R/W	DGC_GAMMA1_156[3:0]				DGC_GAMMA1_160[3:0]				
R46h	R/W	DGC_GAMMA1_164[3:0]				DGC_GAMMA1_168[3:0]				
R47h	R/W	DGC_GAMMA1_172[3:0]				DGC_GAMMA1_176[3:0]				
R48h	R/W	DGC_GAMMA1_180[3:0]				DGC_GAMMA1_184[3:0]				
R49h	R/W	DGC_GAMMA1_188[3:0]				DGC_GAMMA1_192[3:0]				
R4Ah	R/W	DGC_GAMMA1_196[3:0]				DGC_GAMMA1_200[3:0]				
R4Bh	R/W	DGC_GAMMA1_204[3:0]				DGC_GAMMA1_208[3:0]				
R4Ch	R/W	DGC_GAMMA1_212[3:0]				DGC_GAMMA1_216[3:0]				
R4Dh	R/W	DGC_GAMMA1_220[3:0]				DGC_GAMMA1_224[3:0]				
R4Eh	R/W	DGC_GAMMA1_228[3:0]				DGC_GAMMA1_232[3:0]				
R4Fh	R/W	DGC_GAMMA1_236[3:0]				DGC_GAMMA1_240[3:0]				
R50h	R/W	DGC_GAMMA1_244[3:0]				DGC_GAMMA1_248[3:0]				
R51h	R/W	DGC_GAMMA1_252[3:0]				DGC_GAMMA1_253[3:0]				
R52h	R/W	DGC_GAMMA1_254[3:0]				DGC_GAMMA1_255[3:0]				

R53h	R/W	-	-	-	-	DGC_GAMMA1_OFFSET_MAG[1:0]	DGC_GAMMA1_ DELTA_MAG[1:0]	-

Description

This command is used to set DGC2 dithering mapping control.

Register can set LUT point with 67 point. (0, 4, 8, 12….252, 4/step, have 64 points. Other 3 point = 253, 254, 255. Totally 67 points.)

DGC_GAMMA1_GAIN[6:0]: Change slop of LUT, range= 0 ~ 1. All LUT points will apply same gain setting.

Formula: LUT_Gain = Gain [6:0] / 64.

Example:

Gain[6:0]=0x00, LUT_Gain = 0

Gain[6:0]=0x40, LUT_Gain = 1

DGC_GAMMA1_OFFSET[3:0]: Set same center offset value for all LUT points.

When DGC_GAMMA1_OFFSET_MAG[1:0]=00, offset = { [3:0] } = { -8 ~ 7 }

Example:

DGC_GAMMA1_OFFSET[3:0]	Offset Value	DGC_GAMMA1_OFFSET[3:0]	Offset Value
4'b0000	0	4'b1000	-8
4'b0001	1	4'b1001	-7
4'b0010	2	4'b1010	-6
4'b0011	3	4'b1011	-5
4'b0100	4	4'b1100	-4
4'b0101	5	4'b1101	-3
4'b0110	6	4'b1110	-2
4'b0111	7	4'b1111	-1

DGC_GAMMA1_xxx[3:0] : Each LUT point can increase / decrease delta value.

When DGC_GAMMA1_DELTA_MAG [1:0]=00, Delta = { [3:0] } = { -8 ~ 7 }

DGC_GAMMA1_OFFSET_MAG[1:0] : Set ratio of multiplication for Offset.

When DGC_ GAMMA1_OFFSET_MAG [1:0]=00/01/10/11 (The ratio of multiplication = 1 / 2/ 4 / 8)

DGC_GAMMA1_ DELTA _MAG[1:0] : Set ratio of multiplication for Delta.

When DGC_ GAMMA1_ DELTA_MAG [1:0]=00/01/10/11 (The ratio of multiplication = 1 / 2/ 4 / 8)

Restriction: -

2.11.6.SET_DIGITAL_GAMMA2: Set Gamma Curve 2 (Page3-R54h~ R77h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R54h	R/W	-	DGC_GAMMA2_GAIN[6:0]							-
R55h	R/W	DGC_GAMMA2_OFFSET[3:0]				DGC_GAMMA2_000[3:0]				-
R56h	R/W	DGC_GAMMA2_004[3:0]				DGC_GAMMA2_008[3:0]				
R57h	R/W	DGC_GAMMA2_012[3:0]				DGC_GAMMA2_016[3:0]				
R58h	R/W	DGC_GAMMA2_020[3:0]				DGC_GAMMA2_024[3:0]				
R59h	R/W	DGC_GAMMA2_028[3:0]				DGC_GAMMA2_032[3:0]				
R5Ah	R/W	DGC_GAMMA2_036[3:0]				DGC_GAMMA2_040[3:0]				
R5Bh	R/W	DGC_GAMMA2_044[3:0]				DGC_GAMMA2_048[3:0]				
R5Ch	R/W	DGC_GAMMA2_052[3:0]				DGC_GAMMA2_056[3:0]				
R5Dh	R/W	DGC_GAMMA2_060[3:0]				DGC_GAMMA2_064[3:0]				
R5Eh	R/W	DGC_GAMMA2_068[3:0]				DGC_GAMMA2_072[3:0]				
R5Fh	R/W	DGC_GAMMA2_076[3:0]				DGC_GAMMA2_080[3:0]				
R60h	R/W	DGC_GAMMA2_084[3:0]				DGC_GAMMA2_088[3:0]				
R61h	R/W	DGC_GAMMA2_092[3:0]				DGC_GAMMA2_096[3:0]				
R62h	R/W	DGC_GAMMA2_100[3:0]				DGC_GAMMA2_104[3:0]				
R63h	R/W	DGC_GAMMA2_108[3:0]				DGC_GAMMA2_112[3:0]				
R64h	R/W	DGC_GAMMA2_116[3:0]				DGC_GAMMA2_120[3:0]				
R65h	R/W	DGC_GAMMA2_124[3:0]				DGC_GAMMA2_128[3:0]				
R66h	R/W	DGC_GAMMA2_132[3:0]				DGC_GAMMA2_136[3:0]				
R67h	R/W	DGC_GAMMA2_140[3:0]				DGC_GAMMA2_144[3:0]				
R68h	R/W	DGC_GAMMA2_148[3:0]				DGC_GAMMA2_152[3:0]				
R69h	R/W	DGC_GAMMA2_156[3:0]				DGC_GAMMA2_160[3:0]				
R6Ah	R/W	DGC_GAMMA2_164[3:0]				DGC_GAMMA2_168[3:0]				
R6Bh	R/W	DGC_GAMMA2_172[3:0]				DGC_GAMMA2_176[3:0]				
R6Ch	R/W	DGC_GAMMA2_180[3:0]				DGC_GAMMA2_184[3:0]				
R6Dh	R/W	DGC_GAMMA2_188[3:0]				DGC_GAMMA2_192[3:0]				
R6Eh	R/W	DGC_GAMMA2_196[3:0]				DGC_GAMMA2_200[3:0]				
R6Fh	R/W	DGC_GAMMA2_204[3:0]				DGC_GAMMA2_208[3:0]				
R70h	R/W	DGC_GAMMA2_212[3:0]				DGC_GAMMA2_216[3:0]				
R71h	R/W	DGC_GAMMA2_220[3:0]				DGC_GAMMA2_224[3:0]				
R72h	R/W	DGC_GAMMA2_228[3:0]				DGC_GAMMA2_232[3:0]				
R73h	R/W	DGC_GAMMA2_236[3:0]				DGC_GAMMA2_240[3:0]				
R74h	R/W	DGC_GAMMA2_244[3:0]				DGC_GAMMA2_248[3:0]				
R75h	R/W	DGC_GAMMA2_252[3:0]				DGC_GAMMA2_253[3:0]				
R76h	R/W	DGC_GAMMA2_254[3:0]				DGC_GAMMA2_255[3:0]				
R77h	R/W	-	-	-	-	DGC_GAMMA2_OF		DGC_GAMMA2_		-

							FSET_MAG[1:0]	DELTA_MAG[1:0]	

Description

This command is used to set DGC1 dithering mapping control.

Register can set LUT point with 67 point. (0, 4, 8, 12….252, 4/step, have 64 points. Other 3 point = 253, 254, 255. Totally 67 points.)

DGC_GAMMA2_GAIN[6:0]: Change slop of LUT, range= 0 ~ 1. All LUT points will apply same gain setting.

Formula: LUT_Gain = Gain [6:0] / 64.

Example:

Gain[6:0]=0x00, LUT_Gain = 0

Gain[6:0]=0x40, LUT_Gain = 1

DGC_GAMMA2_OFFSET[3:0]: Set same center offset value for all LUT points.

When DGC_GAMMA2_OFFSET_MAG[1:0]=00, offset = { [3:0] } = { -8 ~ 7 }

Example:

DGC_GAMMA2_OFFSET[3:0]	Offset Value	DGC_GAMMA2_OFFSET[3:0]	Offset Value
4'b0000	0	4'b1000	-8
4'b0001	1	4'b1001	-7
4'b0010	2	4'b1010	-6
4'b0011	3	4'b1011	-5
4'b0100	4	4'b1100	-4
4'b0101	5	4'b1101	-3
4'b0110	6	4'b1110	-2
4'b0111	7	4'b1111	-1

DGC_GAMMA2_xxx[3:0] : Each LUT point can increase / decrease delta value.

When DGC_GAMMA2_DELTA_MAG[1:0]=00, Delta = { [3:0] } = { -8 ~ 7 }

DGC_GAMMA2_OFFSET_MAG[1:0] : Set ratio of multiplication for Offset.

When DGC_ GAMMA2_OFFSET_MAG [1:0]=00/01/10/11 (The ratio of multiplication = 1 / 2/ 4 / 8)

DGC_GAMMA2_ DELTA _MAG[1:0] : Set ratio of multiplication for Delta.

When DGC_ GAMMA2_ DELTA_MAG [1:0]=00/01/10/11 (The ratio of multiplication = 1 / 2/ 4 / 8)

Restriction: -

2.11.7.PWM_CTRL: PWM Control (Page3-R98h~R9Ch)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R98h	**R/W**	X	X	LEDON_OE	LEDON_EN	LEDON_POL	VCSW_VOL	LEDPWM_POL	LED_VOL	
R99h	**R/W**	X	X	PWM_SYNC2VS	PWM_OFFSET[4:0]					
R9Ah	**R/W**	SEL_CLK_DIV[7:0]								
R9Bh	**R/W**	N_VAL[7:0]								
R9Ch	**R/W**	PWM_FRAC[7:0]								

Description

LED_VOL: Voltage level for LEDON and LEDPWM pins

LEDPWM_POL: Active polarity for LEDPWM pin.

LEDON_POL: Active polarity for LEDON pin.

VCSW_VOL: Voltage level for VCSW1/2 pin.

LEDON_EN: On/Off control for LEDON pin.

LEDON_OE: Enable output enable for LEDON pin

LEDON_EN	LEDON_POL	Status of LEDON Pin
0	0	Keep “high”
0	1	Keep “low”
1	0	Keep “low”
1	1	Keep “high”

LED_VOL	Voltage level of LEDON/LEDPWM
0	IOGND to IOVCC
1	IOGND to VCI

PWM_SYNC2VS: PWM sync control.

1: Sync to Vsync.

0: Not sync.

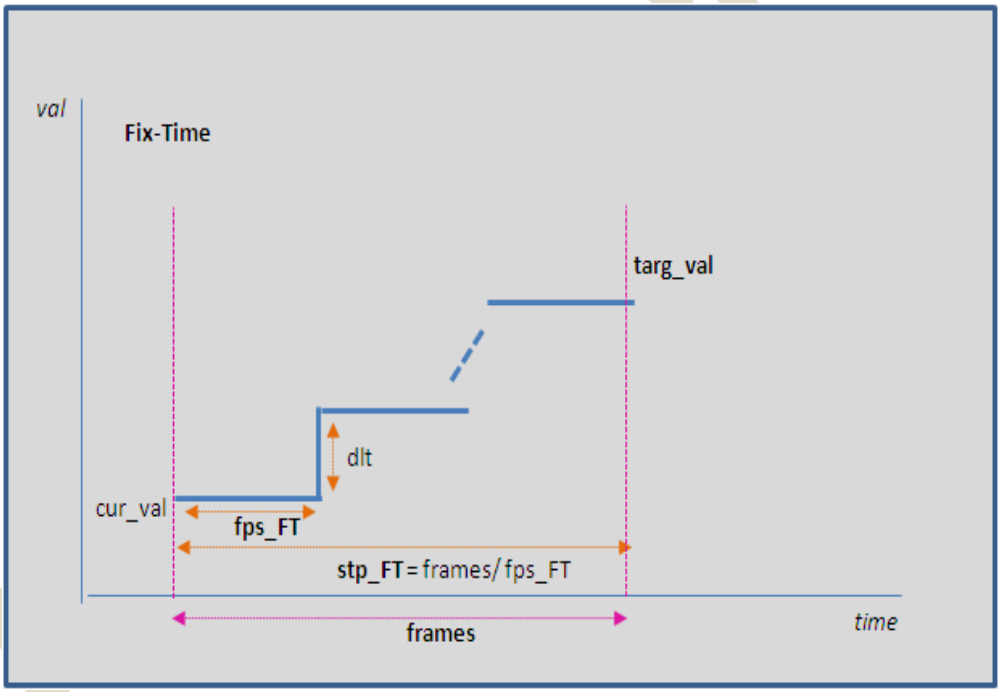
PWM_OFFSET[4:0]: Compensate the effective PWM duty for LEDPWM pin.

PWM_OFFSET[4:0]	PWM Duty Offset
0x01	+0
0x02	+1
:	:
0x1E	+30
0x1F	+31

SEL_CLK_DIV[7:0] : PWM clock select.

	Value : 0x01 / 0x02 / 0x04 / 0x08 / 0x10 / 0x20 / 0x40 / 0x80. The formula is as follows for the PWM_f formula. **N_VAL[7:0]:** PWM Frequency output. OSC default is 40MHz. $\mathrm{PWM_f} = \frac{\mathrm{OSC}}{256 \times (\mathrm{N\_VAL}[7:0] + 1) \times \mathrm{SEL\_CLK\_DIV}[7:0]}$
Restriction	-

2.11.8.BC_DIM_FT_CTRL: Backlight Dimming Fixed Time Control(Page3-RA0h~RA1h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RA0h	**R/W**	X	DEC_STP_FT			X	INC_STP_FT			
RA1h	**R/W**	DEC_FPS_FT				INC_FPS_FT				
Description	When 53h DD=1，Backlight dimming is control by BC_DIM_FT_CTRL. **DEC/INC_STP_FT [2:0]:** Fix-Time dimming steps for a target value. 2^{STP_FT} steps. (Value:1~7) **DEC/INC_FPS_FT[3:0]:** Fix-Time dimming frames for each step. Per step FPS_FT frames (Value:1~15) The Fix-Time Dimming behavior is as follow  									
Restriction	-									

2.12. Jadard page 4 command description

2.12.1.POWER_OPT: Power option (Page4-R00h~ R03h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R00h	**R/W**	-	PDS[30:24]							
R01h	**R/W**	PDS[23:16]								
R02h	**R/W**	PDS[15:8]								
R03h	**R/W**	PDS[7:0]								
Description	The command is use to set power option. **PDS[27:25]**: Enhance gamma power drivering ability option 1. **PDS[12]**: Enhance gamma power drivering ability option 2. **PDS[15]**: VGMP/ VGMN output to external capacitance. 0: VGMP/ VGMN do not output to external capacitance. 1: VGMP/ VGMN output to external capacitance. **Others**: Internal option used, not open.									
Restriction	-									

2.12.2.TEMP_TEST: Testing for Temperature Sensor (Page4-R06h~ R08h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R06h	**R/W**	-	GAS_DBS_CLR	GAS_IN_DBS_EN	GAS_OUT_DBS_EN	GAS_VCOM_EN	GAS_DBS_VEN	GAS_DBS_GEN	GAS_DBS_CLR	
R07h	**R/W**	GAS_DBS_LTH[7:0]								
R08h	**R/W**	GAS_SLPIN_EN	GAS_RE_SLPOUT	GAS_RE_SLPOUT_OTP_RELOAD	GAS_POR_OPT	GAS_POR_MASK	GAS_BLK_NUM[2:0]			

Description

The command is use to set display state while abnormal power off happen, or power recover during abnormal power off state.

GAS_DBS_CLR: Enable GAS flag was clear after abnormal power off state recovered.
0: The internal GAS flag just could clear by HW RESET.
1: The internal GAS flag was clear by power recovered.

GAS_IN_DBS_EN: Enable input power drop debounce function.
0: Disable
1: Enable

GAS_OUT_DBS_EN: Enable input power recover debounce function during abnormal power off event.
0: Disable
1: Enable

GAS_DBS_LTH[7:0]: Set Dounce time.
Debounce time = (1 / OSC) * 16 * GAS_DBS_LTH[7:0].
Ex: OSC = 40MHZ, GAS_DBS_LTH[7:0] = 0x18, Debounce time = 9.6us.
Note: GAS_OUT_DBS time = 2 * GAS_DBS_LTH[7:0] setting.

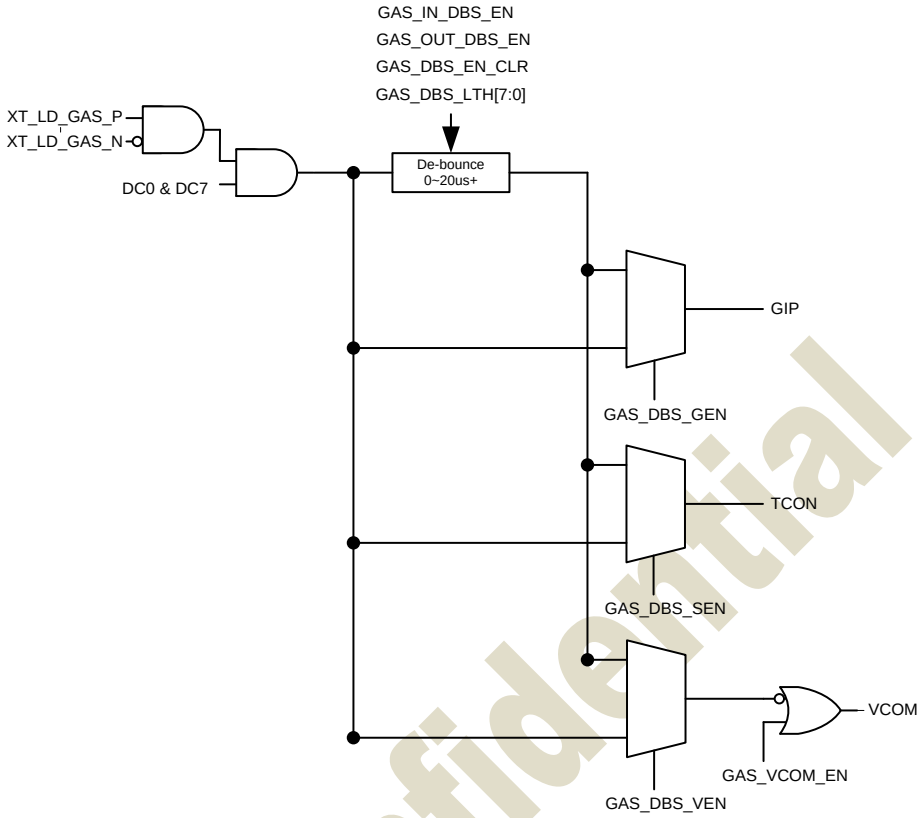
GAS_VCOM_EN: Enable VCOM output state after abnormal power off happen.

GAS_DBS_VEN: Enable VCOM output state while abnormal power off happen, the triiger event is through debounce function.

GAS_DBS_GEN: Enable GIP output state while abnormal power off happen, the triiger event is through debounce function.

GAS_DBS_SEN: Enable SOURCE output state while abnormal power off happen, the triiger event is through debounce function.

GAS_DBS_VEN GAS_DBS_GEN GAS_DBS_SEN	Abnormal power off event source
0	Bypass debounce function
1	**Through debounce function**



GAS_SLPIN_EN: Enable final display state is parking at SLPIN after abnormal power off happen.
0: Disable
1: Enable
GAS_RE_SLPOUT: Enable display state is re-start SLPOUT seqnecne while power recoverd during abnormal power off state.
0: Disbale
1: Enable

GAS_SLPOUT_OTP_RELOAD: Enable reload OTP during re-start SLPOUT sequence.
0: Disbale
1: Enable
Note: The setting is valid at GAS_RE_SLPOUT=1.

GAS_POR_OPT: Set internal display state is need refer POR signal while power recover during abnormal power off state.
0: Disbale
1: Enable

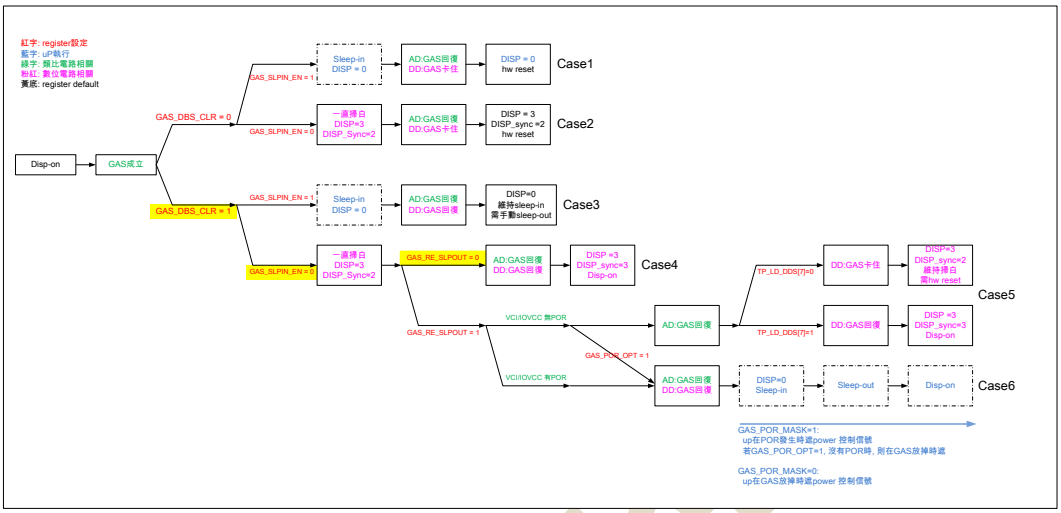
GAS_POR_MASK: Set analog power discharge time.
0: During abnormal power off happen.
1: Power recovered during abnormal power off state.

GAS_POR_OPT	GAS_POR_MASK	Discharge time
0	0	GAS event happen
0	1	GAS event clear
1	X	GAS event clear

Note:
1) GAS event happen: abnormal power off happen.
2) GAS event clear: Power recovered during abnormal power off state.

GAS_BLK_NUM[2:0]: Set blanking frame number during abnormal power off happen. The frme number is from 0 to 7.

Internal GAS case as below flow chart:



Restriction	-

2.12.3.SETRGBCYC2: Set RGB IF Source Switch Control Timing (Page4-R09h~ R0Bh)

<table>
<tr><th>CMD_ADD</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>R09h</td><td>R/W</td><td>X</td><td>SDPRDUM</td><td colspan="2">SDDUM[1:0]</td><td colspan="2">SDSW[1:0]</td><td colspan="2">SDPORCH[1:0]</td><td>15</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to set SD relative control timing.

SDPRDUM: Set SD dummy function enable/disable.
0:Disable
1: Enable

SDDUM[1:0]: Set SD output at dummy line.
SDSW[1:0]: Set SD output at sweep white case.
SDPORCH[1:0]: Set SD output at blanking area.
<table>
<tr><th>SDPORCH[1:0]/SDSW [1:0]/SDDUM [1:0]</th><th>SD Output</th></tr>
<tr><td>00</td><td>PullGND</td></tr>
<tr><td>01</td><td>V0</td></tr>
<tr><td>10</td><td>V255</td></tr>
<tr><td>11</td><td>Hi-Z</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

2.12.4.SETSTBA2: Set RGB IF Source Switch Control Timing (Page4-R0Ch~ R0Fh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R0Ch	R/W	X		VTEST[5:0]						
R0Dh	R/W	X	SDS[22:16]							
R0Eh	R/W	SDS[15:8]								
R0Fh	R/W	SDS[7:0]								

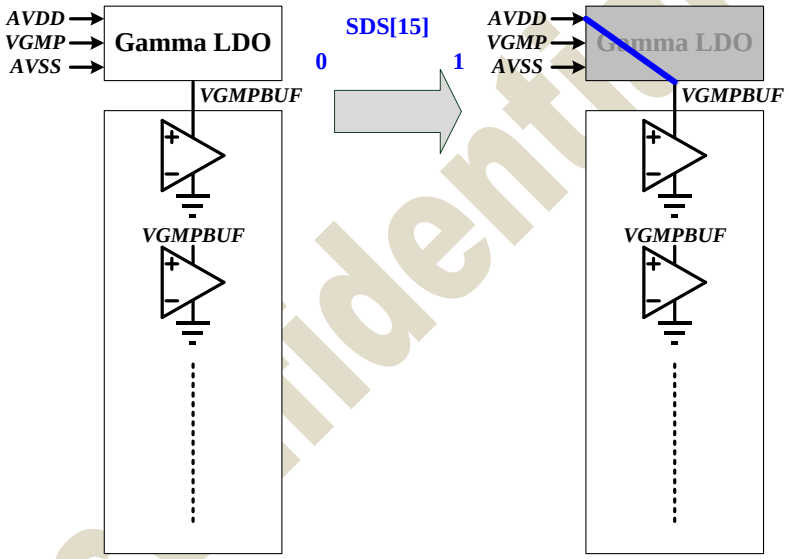
Description

This command is used to set internal source option control at engineer mode .

VTEST[5:0]: Bypass SD internal output to VTEST_P/N pin.

VTEST[5]	VTEST[4:0]	VTEST_P	VTEST_N
0	XXXXX	Hi-Z	Hi-Z
1	00000	VO0	VO0
1	00001	VO4	VO4
1	00010	VO8	VO8
1	00011	VO12	VO12
1	00100	VO20	VO20
1	00101	VO28	VO28
1	00110	VO44	VO44
1	00111	VO64	VO64
1	01000	VO96	VO96
1	01001	VO128	VO128
1	01010	VO159	VO159
1	01011	VO191	VO191
1	01100	VO211	VO211
1	01101	VO227	VO227
1	01110	VO235	VO235
1	01111	VO243	VO243
1	10000	VO247	VO247
1	10001	VO251	VO251
1	10010	VO255	VO255
1	10011	VO253	VO253
1	10100	VO239	VO239
1	10101	VO175	VO175
1	10110	VO144	VO144
1	10111	VO112	VO112
1	11000	VO80	VO80
1	11001	VO16	VO16
1	11010	VO2	VO2

SDS[22:0]: Source option setting.

SDS[22]	No use
SDS[21]	Right channel op off. (1=off)
SDS[20]	Left channel op off. (1=off)
SDS[19]	OPM release delay option. (0=delay;1=no delay)
SDS[18:16]	No use
SDS[15]	Disable Gamma LDO 0: Ref. SDS[8] 1: VGMPBUF=AVDD 
SDS[14:13]	PEQ power selection : SDS[14:13] / PEQ power source 00 / Hi-Z 01 / IOVCC 10 / PCAP 11 / VCI
SDS[12]	NEQ power selection : SDS[12] / NEQ power source 0 / NCAP 1 / VCL
SDS[11]	No use
SDS[10]	Chopper clamp option for channel op (1=opm clamp)
SDS[9]	No use
SDS[8]	Gamma LDO VGMPBUF 0: 1.02xVGMP regulator (default) 1: 1xVGMP regulator
SDS[7:4]	No use

	SDS[3:1]	Chop bias ratio setting (class-AB stage).	
	SDS[0]	Increasing output SW size (1: increasing;0: decreasing)	
Restriction	-		

2.12.5.SET_OSCD: Set OSCD Relative Register (Page4-R1Eh~ R1Fh)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R1Eh	**R/W**	X		OSCD_ EN	OSCD_ BIAS_EN	X	OSCD_ADJ[2:0]			
R1Fh	**R/W**	OSCD_ OFFSET_SS	X		OSCD_ SS_EN	OSCD_SS_F[2:0]			OSCD_ SS_R	

Description

This command is used to set OSCD relative setting.

OSCD_EN: Enable(1)/disable(0) OSCD

OSCD_BIAS_EN: OSCD bias setting

OSCD_BIAS_EN	
0	Bias turn on only when OSCD_EN=1
1	Enable R path bias for fast start-up

OSCD_ADJ[2:0]: Adjust OSCD frequency

OSCD_ADJ[2:0]	OSCD Frequency(MHz)
0	31.32
1	34.31
2	37.29
3	40.23
4	43.14
5	46.02
6	48.92
7	51.79

OSCD_OFFSET_SS: Enable(1)/ Disable(0) offset function.

OSCD_SS_EN: Enable(1)/disable(0) spread spectrum function.

OSCD_SS_F [2:0]: Adjust the time for spread spectrum frequency change.

SS_F[2:0]			SS_SEL[3:0] change cycle	time (ns)
0	0	0	4 osc	100
0	0	1	8 osc	200
0	1	0	16 osc	400
0	1	1	32 osc	800
1	0	0	64 osc	1600
1	0	1	128 osc	3200

	1	1	0	256 osc	6400
	1	1	1	1 Line	13000

OSCD_SS_R: Spread spectrum frequency range setting.

Restriction	-

2.12.6.SETMIPI1: Set MIPI Setup1 (Page4-R29h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R29h	**R/W**	X	TX_LDO_SEL[2:0]			PHY_VDC0_D3	RX_LDO_SEL[2:0]			

Description

This command is used to set DSI Related Setting.

TX_LDO_SEL[2:0]: TX_LDO_SEL[2:0]. VDDHL voltage for LP-TX,

3'b000	1.125 V
3'b001	1.150 V
3'b010	1.175 V
3'b011	1.200 V (default)
3'b100	1.225 V
3'b101	1.250 V
3'b110	1.275 V
3'b111	1.300 V

PHY_VDC0_D3: reserved

RX_LDO_SEL[2:0]: RX_LDO_SEL[2:0]. VDDH voltage for LP/HS-RX,

3'b000	1.350 V
3'b001	1.400 V
3'b010	1.450 V
3'b011	1.500 V
3'b100	1.550 V (default)
3'b101	1.600 V
3'b110	1.650 V
3'b111	1.700 V

Restriction: -

2.12.7.SETMIPI4: Set MIPI Setup4 (Page4-R35h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R35h	**R/W**	X	DSI_CTL7[6:0]							
Description	**//DSI_CTL7. Internal signal control, for debug.** **DSI_CTL7 [0]:** HS_d4_inv_END **0** : (default) XOR with HS_d4_inv to stop the PHY D4_CLK at posedge or nedge **1** : **DSI_CTL7 [1]:** ESD_PROTECT_CLK **0:** ESD protect use MIPI spec. **1:** ESD protect use DP/N==2'b11 **DSI_CTL7 [2]:** HS_USE_D4_CLK **0:** normal case **1:** iphone case VS/tcon_lline use OSCD, other ues HS_D4 CLK **DSI_CTL7 [3]:** READ_RPT_PKT **0:** as below DCS Read Request 1. Maximum Return =1, 時回 0x21 2. Maximum Return =2, 時回 0x22 3. Maximum Return >=3, 時回 0x1C Generic Short Read 1. Maximum Return =1, 時回 0x11 2. Maximum Return =2, 時回 0x12 3. Maximum Return >=3, 時回 0x1A **1:** DCS Read Request 只回 1C; Generic Short Read 只回 1A **DSI_CTL7 [7:4]:** Reserved										
Restriction										

2.12.8.SETMIPI5: Set MIPI Setup5 (Page4-R36h~R37h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R36h	**R/W**	X	DSI_CTL8[6:0]							
R37h	**R/W**	DSI_CTL9[7:0]								
Description	This command is used to set DSI Related Setting. **//DSI_CTL8. Internal signal control, for debug.** **DSI_CTL8 [2:0]:** HBP_CLK_NUM[2:0] Internal function add HBP OSCD clk number, HBP_CLK_NUM*4 **DSI_CTL8 [3]:** HFP_AT_DE **0:** after hs packet, HFP-> HS -> HBP **1:** after DE -> HFP ; after hs packet HS -> HBP **DSI_CTL8 [6:4]:** HFP_CLK_NUM[2:0] Internal function add HFP OSCD clk number, HFP_CLK_NUM*4 **//DSI_CTL9. Internal signal control, for debug.** **DSI_CTL9 [7:0]:** Reserved									
Restriction										

2.12.9.REG_CHKSUM: Standard Register Checksum (Page4-R97h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R97h	**R/W**	X	X	SLPIN_RST_EN	CHKSUM_OFF	X	CHKSUM_SEL[2:0]			
Description	**SLPIN_RST_EN:** 1: Enable the function of reset Nokia checksum in Sleep-in 0: Disable the function of reset Nokia checksum in Sleep-in **CHKSUM_OFF:** 1: Standard register checksum function OFF 0: Standard register checksum function ON **CHKSUM_SEL[2:0]: The interval between each checksum calculation** 5: 64 Frames 4: 32 Frames 3: 16 Frames 2: 8 Frames 1: 4 Frames 0: 2 Frames									
Restriction	-									

2.12.10. SET_INH_CHKSUM: Inhouse Register Checksum(Page4-R98h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R98h	**R/W**	X	X	X	SLPIN_RESET_EN	INH_CHKSUM_OFF	INH_CHKSUM_SEL[2:0]			
Description	**INH_CHKSUM_OFF:** 1: inhouse register checksum function OFF 0: inhouse register checksum function ON **INH_CHKSUM_SEL[2:0]: The interval between each checksum calculation** 5: 64 Frames 4: 32 Frames 3: 16 Frames 2: 8 Frames 1: 4 Frames 0: 2 Frames **note:only P0~P3 will be calculated** **SLPIN_RESET_EN:**reset in slpin 0:disable 1:enable									
Restriction	-									

2.12.11. SET_GPO: GPO Function Select (Page4-R99h~RA0h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R99h	**R/W**	X	GPO0_REV	GPO0_OE	GPO0_SEL[4:0]					
R9Ah	**R/W**	X	GPO1_REV	GPO1_OE	GPO1_SEL[4:0]					
R9Bh	**R/W**	X	GPO2_REV	GPO2_OE	GPO2_SEL[4:0]					
R9Ch	**R/W**	X	GPO3_REV	GPO3_OE	GPO3_SEL[4:0]					
R9Dh	**R/W**	X	GPO4_REV	GPO4_OE	GPO4_SEL[4:0]					
R9Eh	**R/W**	VCSW1_OE	GPO5_REV	GPO5_OE	GPO5_SEL[4:0]					
R9Fh	**R/W**	VCSW2_OE	GPO6_REV	GPO6_OE	GPO6_SEL[4:0]					
RA0h	**R/W**	X	INTERNAL_SEL2[2:0]			X	INTERNAL_SEL1[2:0]			

Description

Select GPO0~GPO6 function

XX_REV: Reverse Signal polarity
(XX= GPO0~GPO6)
0: Keep polarity
1: Reverse Polarity

XX_OE: Signal output enable
(XX= GPO0~GPO6, VCSW1/2)
0: Do not output signal
1: Output signal.

XX_SEL: Output signal type select
(XX= GPO0~GPO6)

4'b0000	GND
4'b0001	TE
4'b0010	TP_HS
4'b0011	TP_VS
4'b0100	TP_HVS
4'b0101	LEDPWM
4'b0110	LEDON
4'b0111	ERR_FLAG
4'b1000	POW_EN
4'b1001	DC2
4'b1010	INT_VS1
4'b1011	INT_HS1
4'b1100	INT_DE1
4'b1101	INT_VS2

4’b1110	INT_HS2
4’b1111	INT_DE2

INTERNAL_SEL1/2:

SEL [2:0]	INT_VS1 INT_VS 2	INT_HS1 INT_HS 2	INT_DE1 INT_DE 2
3’b000	DSI_VS	DSI_HS	DSI_DE
3’b001	IF_VS	IF_HS	IF_DE
3’b010	CE2PIE_VS	CE2PIE_HS	CE2PIE_DE
3’b011	PIE2LE_VS	PIE2LE_HS	PIE2LE_DE
3’b100	DGC2TCON_VS	DGC2TCON_HS	DGC2TCON_DE
3’b101	TP_VS &(!CS_CMPR_MIX)	CS_CMPR_MIX	dsi_ESD_err_st_lvl
3’b110	DISP_sync[1]	DISP_sync[0]	0
Others	UP_START	PWRIC_CLK	EXT_AVDD_AVEE_EN

Restriction	-

2.12.12. STD_SEL: Standard Command Option Select(Page4-RA3h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RA3h	**R/W**	X	RX0F_DCS_B0_MIX	RX0F_B0_SEL	X	RX0A_B2_MIX	RX0A_B0_MIX	CMPR_MIX_EN[1:0]		
Description	**CMPR_MIX_EN:** 00:nokia 01:inhouse 10:nokia+inhouse 11:disable **RX0A_B2_MIX:mix Rx0A bit2 with chksum error flag** 0:disable 1:enable **RX0A_B0_MIX:mix Rx0A bit0 with chksum error flag** 0:disable 1:enable **RX0F_DCS_B0_MIX:DCS 0F bit 0 select** 0:disable 1:chksum error flag **RX0F_B0_SEL** 0:cs_cmpr 1:cs_cmpr/inh_cs_cmpr									
Restriction	-									

2.12.13. RX0A_OTP: (Page4-RA4h~RA5h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RA4h	**R/W**	X		DSI_F8F9_EN	DISPON_SEL				RX0A_EN	
RA5h	**R/W**	RX0A[7:0]								
Description	**DSI_F8F9_EN:** Internal used, not open. **DSIPON_SEL:** It is used to set STD_R0A[2] bit state. 0: DDIC receive SLPUT + Display ON command, - Video off, R0A[2] will be “0”. - Video on, R0A[2] will be “1”. 1: No matter video on/off. if DDIC receive SLPUT + Display ON command, the R0A[2] will be “1”. **when RX0A_EN=1,STD 0A value will switch to RX0A[7:0]**									
Restriction	-									

2.12.14. DSI_SMRP: (Page4-RA6h~RA8h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RA6h	**R/W**	X	X	X	X	X	X	X	DSI_SMRP_ TYPE	
RA7h	**R/W**	DSI_SMRP[15:8]								
RA8h	**R/W**	DSI_SMRP[7:0]								
Description	**DSI_SMRP_TYPE** 0：Update SMRP value at 1st OTP reload event 1：Update SMRP value when OTP reload event occur **DSI_SMRP[15:0]:** SMRP OTP for Maintenance market									
Restriction	-									

3. OTP Programming

3.1. OTP Table

OTP_INDEX (HEX)	Ref. Command	Ref. Page	Ref. Index	Duplicate	B7	B6	B5	B4	B3	B2	B1	B0
0	SEQUENCE_CTRL	P0	70	1	NVALID	DC0H[2:0]			-	DC1H[2:0]		
1			71		-	DC2H[2:0]			-	DC3H[2:0]		
2			72		-	-	-	-	-	DC7H[2:0]		
3			73		DC0L	DC1L	DC2L	DC3L	DC4L	DC5L	DC6L	DC7L
4			74		T0P[1:0]		T1P[1:0]		T8P[1:0]		-	-
5			75		-	SOFT0H[2:0]			-	SOFT0L[2:0]		
6	SETID(OTP*5)	P0	77	1	NVALID	-	-	-	-	-	-	-
7			78		ID1[7:0]							
8			79		ID2[7:0]							
9			7A		ID3[7:0]							
A			7B		ID4[7:0]							
B			77	2	NVALID	-	-	-	-	-	-	-
C			78		ID1[7:0]							
D			79		ID2[7:0]							
E			7A		ID3[7:0]							
F			7B		ID4[7:0]							
10			77	3	NVALID	-	-	-	-	-	-	-
11			78		ID1[7:0]							
12			79		ID2[7:0]							
13			7A		ID3[7:0]							
14			7B		ID4[7:0]							
15			77	4	NVALID	-	-	-	-	-	-	-
16			78		ID1[7:0]							
17			79		ID2[7:0]							
18			7A		ID3[7:0]							
19			7B		ID4[7:0]							
1A			77	5	NVALID	-	-	-	-	-	-	-
1B			78		ID1[7:0]							
1C			79		ID2[7:0]							
1D			7A		ID3[7:0]							
1E			7B		ID4[7:0]							
1F	SETDSISETUP	P0	80	1	NVALID	DSI_INIT06:0]						
20			81		DSI_INIT1[7:0]							
21			82		DSI_INIT2[7:0]							
22	SETDSISETUP2	P0	83	1	NVALID	DSI_INIT3[6:0]						

24	SET_WD	PA	E6	1	NVALID	-	-	-	-	-	WD_MODE[1:0]	
25			E7		-	-	-	WD_off	WD_Timer[3:0]			
26	VCOM_SET(OTP*5)	P1	00	1	NVALID	-	-	VCOMS_BP	-	-	VCOM_S[9:8]	
27			01		VCOM_S[7:0]							
28			00	2	NVALID	-	-	VCOMS_BP	-	-	VCOM_S[9:8]	
29			01		VCOM_S[7:0]							
2A			00	3	NVALID	-	-	VCOMS_BP	-	-	VCOM_S[9:8]	
2B			01		VCOM_S[7:0]							
2C			00	4	NVALID	-	-	VCOMS_BP	-	-	VCOM_S[9:8]	
2D			01		VCOM_S[7:0]							
2E			00	5	NVALID	-	-	VCOMS_BP	-	-	VCOM_S[9:8]	
2F			01		VCOM_S[7:0]							
30	VCOM_R_SET(OTP*5)	P1	03	1	NVALID	-	-	VCOM_R_SEN	-	-	VCOM_R_S[9:8]	
31			04		VCOM_R_S[7:0]							
32			03	2	NVALID	-	-	VCOM_R_SEN	-	-	VCOM_R_S[9:8]	
33			04		VCOM_R_S[7:0]							
34			03	3	NVALID	-	-	VCOM_R_SEN	-	-	VCOM_R_S[9:8]	
35			04		VCOM_R_S[7:0]							
36			03	4	NVALID	-	-	VCOM_R_SEN	-	-	VCOM_R_S[9:8]	
37			04		VCOM_R_S[7:0]							
38			03	5	NVALID	-	-	VCOM_R_SEN	-	-	VCOM_R_S[9:8]	
39			04		VCOM_R_S[7:0]							
3A	OTP_REPAIR	P1	B2	1	NVALID	-	-	-	REPAIR_PAGE[3:0]			
3B			B3		REPAIR_INDEX[7:0]							
3C			B4		REPAIR_PAR[7:0]							
3D			B5		REPAIR_VALUE[7:0]							
3E	PWRIC_SET	P1	0A	1	NVALID	-	JD_RELD	VCSW_SWAP	EN_VREF_S[3:0]			
3F			0B		PWRIC_SET[7:0]							
40			0C		-	PWRIC_CLK1[2:0]			-	PWRIC_IDLE_CLK1[2:0]		
41			0D		HX_SOFT	PWRIC_CLK2[2:0]			PWRIC_HXCLK[3:0]			
42			0E		HX_DT_AVDD	-	-	-	-	-	LED_PWR_S[1:0]	
4B	GAMMA_SET	P1	17	1	NVALID	-	-	VGMP_S[8]	-	-	-	VGSP_S[8]
4C			18		VGMP_S[7:0]							
4D			19		VGSP_S[7:0]							
4E			1A		-	-	-	VGMN_S[8]	-	-	-	VGSN_S[8]
4F			1B		VGMN_S[7:0]							
50			1C		VGSN_S[7:0]							
51	OTP_SET	P1	1D	1	NVALID	-	VPP_DT[1:0]		-	VPP_VGH_RT[2:0]		
52			1E		-	VPP_VGH_S[6:0]						

53	GATE_POWER	P1	1F	1	NVALID	VGH_REG_S[6:0]							
54			20		-	-	VGL_REG_S[5:0]						
55			21		-	-	VGL_REG2_S[5:0]						
56			22		-	VGH_REG_SHT	VGL_REG_SHT	VGL_REG2_SHT	VGH_REG_EN	VGL_REG_EN	VGL_REG2_EN	SHT_VGL_REG	
57	DCDC_CTRL	P1	23	1	NVALID	-	GAS_VGH_EN	GAS_VGL_EN	VGH_NC	VGL_NC	VCLREG_OP_CEN	VCL_NC	
58			24		VGHEN	VGLEN	AVDDEN	AVEEEN	VCLEN	VDDAEN	VCLREG_EN	VCL2VDDN	
59	POWAMP_CTRL	P1	25	1	NVALID	AP[2:0]			-	-	-	-	
5A			26		VCOM_EN	VGM_EN	-	GAS_DET_SEL	GAS_IOVCC_EN	GAS_VCI_EN	GAS_AVE_EN	GAS_OUT_EN	
5B			27		UP_VDD_1P8_EN	VDDD_S1[2:0]			-	VDDD_S4[2:0]			
5C	DCDC_CTRL2	P1	28	1	NVALID	PWR_SW_EN	VGH_MSF_EN	VGH_CHG2AVDD_EH	VGH_GAS_PWS_EN	VGH_PWS	VGH_PWS_GND	VGH_PWS_POS	
5D			29		-	-	GAS_T8P[1:0]		VGH_SGL_C41	VGH_SGL_C42	-	-	
5E			2A		DDS[7:0]								
5F	SETRGBCYC3	P1	B6	1	NVALID	RES_MUX_ON[6:0]							
60			B7		-	RES_MUX_OFF[6:0]							
61			B8		DYNBIAS_ON[7:0]								
62			B9		DYNBIAS_OFF[7:0]								
63			BA		DYNCHGEN_ON[7:0]								
64			BB		DYNCHGEN_OFF[7:0]								
68	SETSTBA	P1	35	1	NVALID	GAP[2:0]			SAP[3:0]				
69			36		-	-	-	-	SAP2[3:0]				
6A	SETPANEL	P1	37	1	NVALID	Z_line	ENZ[1:0]		SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	
6B	SETRGBCYC	P1	38	1	NVALID	interlace_line	-	-	-	RGB_JDT[2:0]			
6C			39		RGB_N_EQ1[7:0]								
6D			3A		RGB_N_EQ2[7:0]								
6E			3B		RGB_N_EQ2_Temp[7:0]								
6F			3C		RGB_N_EQ3[7:0]								
70			3D		RGB_CHGEN_ON[7:0]								
71			3E		RGB_CHGEN_OFF[7:0]								
72			3F		RGB_CHGEN_OFF2[7:0]								
73	SET_TCON	P1	40	1	NVALID	IP750_1	LN[1:0]		IP750_0	RSO[2:0]			
74			41		LN[9:2]								
75			42		SLT[7:0]								
76			43		VFP[7:0]								
77			44		VBP[7:0]								
78			45		HBP[7:0]								
79			46		TE_Delay[10:3]								
7A			47		BlkinF_num[7:0]								
7B			48		BlkinF_STR[7:0]								
7C			49		-	-	-	-	-	TE_Delay[2:0]			

7D			4A		FRAME_NUM[1:0]		Auto_Test_en	TEST_PAT_EN	TEST_PATTERN[3:0]				
7E			4B		TCON_OPT1[15:8]								
7F			4C		TCON_OPT1[7:0]								
80	SET_TE_PAD	P1	4D	1	NVALID	-	-	-	-	-	-	-	
81			4E		-	-	-	-	TP_VS_EN	TP_VS_WIDTH[10:8]			
82			4F		TP_VS_WIDTH[7:0]								
83			50		TP_VS_SHIFT[7:0]								
84			51		-	-	-	-	-	-	TP_HS_BLK_EN	TP_HS_DIS_EN	
85			52		TP_HS_ON[7:0]								
86			53		TP_HS_OFF[7:0]								
87	DCDC_SEL	P1	55	1	NVALID	-	-	-	DCDCM[3:0]				
88			56		-	-	-	-	AUTO_RT	-	AVDD_RT[1:0]		
89			57		VGH_RT[2:0]			VGL_RT[2:0]			VCL_RT[1:0]		
8A			58		-	-	-	AVDD_S[4:0]					
8B			59		VCL_S[2:0]			AVEE_S[4:0]					
8C			5A		-	VGH_S[6:0]							
8D			5B		-	-	VGL_S[5:0]						
8E			5C		-	-	VDDA_CLK[1:0]		VCL_CLK[1:0]		VGHVGL_CLK[1:0]		
8F	SETDDB	P1	83	1	NVALID	-	-	-	-	-	-	-	
90			84		DDB1[7:0]								
91			85		DDB2[7:0]								
92			86		DDB3[7:0]								
93			87		DDB4[7:0]								
94	SETECO	P1	88	1	NVALID	-	-	-	-	-	-	-	
95			89		ECO0[7:0]								
96			8A		ECO1[7:0]								
97			8B		NVALID	ECO2[6:0]							
98			8C		NVALID	ECO3[6:0]							
99	DCS_CMD_OPT	P1	93	1	NVALID	-	-	-	-	-	-	NOKIA_CMD_EN	
9A	CTM_OTP	P1	95	1	NVALID	-	-	OTP_WR_FLAG	OTP_RD_LENGTH[3:0]				
9B			96		CTM_OTP0[7:0]								
9C			97		CTM_OTP1[7:0]								
9D			98		CTM_OTP2[7:0]								
9E			99		CTM_OTP3[7:0]								
9F			9A		CTM_OTP4[7:0]								
A0			9B		CTM_OTP5[7:0]								
A1			9C		CTM_OTP6[7:0]								
A2			9D		CTM_OTP7[7:0]								
A3			9E		CTM_OTP8[7:0]								
A4			9F		CTM_OTP9[7:0]								

A5			A0		CTM_OTP10[7:0]					
A6			A1		CTM_OTP11[7:0]					
A7			A2		CTM_OTP12[7:0]					
A8			A3		CTM_OTP13[7:0]					
A9			A4		CTM_OTP14[7:0]					
AA			A5		CTM_OTP15[7:0]					
AB			95		NVALID	-	-	OTP_WR_FLAG	OTP_RD_LENGTH[3:0]	
AC			96		CTM_OTP0[7:0]					
AD			97		CTM_OTP1[7:0]					
AE			98		CTM_OTP2[7:0]					
AF			99		CTM_OTP3[7:0]					
B0			9A		CTM_OTP4[7:0]					
B1			9B		CTM_OTP5[7:0]					
B2			9C		CTM_OTP6[7:0]					
B3			9D	2	CTM_OTP7[7:0]					
B4			9E		CTM_OTP8[7:0]					
B5			9F		CTM_OTP9[7:0]					
B6			A0		CTM_OTP10[7:0]					
B7			A1		CTM_OTP11[7:0]					
B8			A2		CTM_OTP12[7:0]					
B9			A3		CTM_OTP13[7:0]					
BA			A4		CTM_OTP14[7:0]					
BB			A5		CTM_OTP15[7:0]					
BC			95		NVALID	-	-	OTP_WR_FLAG	OTP_RD_LENGTH[3:0]	
BD			96		CTM_OTP0[7:0]					
BE			97		CTM_OTP1[7:0]					
BF			98		CTM_OTP2[7:0]					
C0			99		CTM_OTP3[7:0]					
C1			9A		CTM_OTP4[7:0]					
C2			9B		CTM_OTP5[7:0]					
C3			9C		CTM_OTP6[7:0]					
C4			9D	3	CTM_OTP7[7:0]					
C5			9E		CTM_OTP8[7:0]					
C6			9F		CTM_OTP9[7:0]					
C7			A0		CTM_OTP10[7:0]					
C8			A1		CTM_OTP11[7:0]					
C9			A2		CTM_OTP12[7:0]					
CA			A3		CTM_OTP13[7:0]					
CB			A4		CTM_OTP14[7:0]					
CC			A5		CTM_OTP15[7:0]					

CD	SETCUSTM_ID	P1	A6	1	NVALID	-	-	-	-	-	-	-	
CE			A7		CUSTM1[7:0]								
CF			A8		CUSTM2[7:0]								
D0			A9		CUSTM3[7:0]								
D1			AA		CUSTM4[7:0]								
D2			AB		CUSTM5[7:0]								
D3			AC		CUSTM6[7:0]								
D4			AD		CUSTM7[7:0]								
D5			AE		CUSTM8[7:0]								
D6	SET_TE_PAD2	P1	AF	1	NVALID	-	-	VHS_TEON_OPT	TP_VS_EN2	TP_VS_WIDTH2[10:8]			
D7			B0		TP_VS_WIDTH2[7:0]								
D8			B1		TP_VS_SHIFT2[7:0]								
FB	LE_DBV_CTRL	P3	96	1	NVALID	-	-	-	LE_DBV_SEL[3:0]				
FC	LE_ECO_SWITCH	P3	97	1	NVALID	-	PWM_PULSE_SAMPLE_D2	LE_BC_ALLP_CTRL	LE_SLPIN_LE_OFF	UNI_GAIN_SEL	MANU_CUT_SEL	LE_OFF_CMB_CHK	
100	SET_GAMMA(OTP*3)	P1	5D	1	NVALID	RPA18[6:0]							
101			5E		-	RPA17[6:0]							
102			5F		-	RPA16[6:0]							
103			60		-	RPA15[6:0]							
104			61		-	RPA14[6:0]							
105			62		-	RPA13[6:0]							
106			63		-	RPA12[6:0]							
107			64		-	RPA11[6:0]							
108			65		-	RPA10[6:0]							
109			66		-	RPA9[6:0]							
10A			67		-	RPA8[6:0]							
10B			68		-	RPA7[6:0]							
10C			69		-	RPA6[6:0]							
10D			6A		-	RPA5[6:0]							
10E			6B		-	RPA4[6:0]							
10F			6C		-	RPA3[6:0]							
110			6D		-	RPA2[6:0]							
111			6E		-	RPA1[6:0]							
112			6F		-	RPA0[6:0]							
113			70		-	RNA18[6:0]							
114			71		-	RNA17[6:0]							
115			72		-	RNA16[6:0]							
116			73		-	RNA15[6:0]							
117			74		-	RNA14[6:0]							
118			75		-	RNA13[6:0]							
119			76		-	RNA12[6:0]							

11A			77		-	RNA11[6:0]
11B			78		-	RNA10[6:0]
11C			79		-	RNA9[6:0]
11D			7A		-	RNA8[6:0]
11E			7B		-	RNA7[6:0]
11F			7C		-	RNA6[6:0]
120			7D		-	RNA5[6:0]
121			7E		-	RNA4[6:0]
122			7F		-	RNA3[6:0]
123			80		-	RNA2[6:0]
124			81		-	RNA1[6:0]
125			82		-	RNA0[6:0]
126			5D		NVALID	RPA18[6:0]
127			5E		-	RPA17[6:0]
128			5F		-	RPA16[6:0]
129			60		-	RPA15[6:0]
12A			61		-	RPA14[6:0]
12B			62		-	RPA13[6:0]
12C			63		-	RPA12[6:0]
12D			64		-	RPA11[6:0]
12E			65		-	RPA10[6:0]
12F			66		-	RPA9[6:0]
130			67		-	RPA8[6:0]
131			68		-	RPA7[6:0]
132			69		-	RPA6[6:0]
133			6A	2	-	RPA5[6:0]
134			6B		-	RPA4[6:0]
135			6C		-	RPA3[6:0]
136			6D		-	RPA2[6:0]
137			6E		-	RPA1[6:0]
138			6F		-	RPA0[6:0]
139			70		-	RNA18[6:0]
13A			71		-	RNA17[6:0]
13B			72		-	RNA16[6:0]
13C			73		-	RNA15[6:0]
13D			74		-	RNA14[6:0]
13E			75		-	RNA13[6:0]
13F			76		-	RNA12[6:0]
140			77		-	RNA11[6:0]
141			78		-	RNA10[6:0]

142			**79**		-	RNA9[6:0]
143			**7A**		-	RNA8[6:0]
144			**7B**		-	RNA7[6:0]
145			**7C**		-	RNA6[6:0]
146			**7D**		-	RNA5[6:0]
147			**7E**		-	RNA4[6:0]
148			**7F**		-	RNA3[6:0]
149			**80**		-	RNA2[6:0]
14A			**81**		-	RNA1[6:0]
14B			**82**		-	RNA0[6:0]
14C			**5D**		**NVALID**	RPA18[6:0]
14D			**5E**		-	RPA17[6:0]
14E			**5F**		-	RPA16[6:0]
14F			**60**		-	RPA15[6:0]
150			**61**		-	RPA14[6:0]
151			**62**		-	RPA13[6:0]
152			**63**		-	RPA12[6:0]
153			**64**		-	RPA11[6:0]
154			**65**		-	RPA10[6:0]
155			**66**		-	RPA9[6:0]
156			**67**		-	RPA8[6:0]
157			**68**		-	RPA7[6:0]
158			**69**		-	RPA6[6:0]
159			**6A**		-	RPA5[6:0]
15A			**6B**	3	-	RPA4[6:0]
15B			**6C**		-	RPA3[6:0]
15C			**6D**		-	RPA2[6:0]
15D			**6E**		-	RPA1[6:0]
15E			**6F**		-	RPA0[6:0]
15F			**70**		-	RNA18[6:0]
160			**71**		-	RNA17[6:0]
161			**72**		-	RNA16[6:0]
162			**73**		-	RNA15[6:0]
163			**74**		-	RNA14[6:0]
164			**75**		-	RNA13[6:0]
165			**76**		-	RNA12[6:0]
166			**77**		-	RNA11[6:0]
167			**78**		-	RNA10[6:0]
168			**79**		-	RNA9[6:0]
169			**7A**		-	RNA8[6:0]

16A			7B		-	RNA7[6:0]		
16B			7C		-	RNA6[6:0]		
16C			7D		-	RNA5[6:0]		
16D			7E		-	RNA4[6:0]		
16E			7F		-	RNA3[6:0]		
16F			80		-	RNA2[6:0]		
170			81		-	RNA1[6:0]		
171			82		-	RNA0[6:0]		
172	SET_GIP_L	P2	00	1	NVALID	CGO1_PH_L	CGO1_INV_L	CGOUT1_L[4:0]
173			01		-	CGO2_PH_L	CGO2_INV_L	CGOUT2_L[4:0]
174			02		-	CGO3_PH_L	CGO3_INV_L	CGOUT3_L[4:0]
175			03		-	CGO4_PH_L	CGO4_INV_L	CGOUT4_L[4:0]
176			04		-	CGO5_PH_L	CGO5_INV_L	CGOUT5_L[4:0]
177			05		-	CGO6_PH_L	CGO6_INV_L	CGOUT6_L[4:0]
178			06		-	CGO7_PH_L	CGO7_INV_L	CGOUT7_L[4:0]
179			07		-	CGO8_PH_L	CGO8_INV_L	CGOUT8_L[4:0]
17A			08		-	CGO9_PH_L	CGO9_INV_L	CGOUT9_L[4:0]
17B			09		-	CGO10_PH_L	CGO10_INV_L	CGOUT10_L[4:0]
17C			0A		-	CGO11_PH_L	CGO11_INV_L	CGOUT11_L[4:0]
17D			0B		-	CGO12_PH_L	CGO12_INV_L	CGOUT12_L[4:0]
17E			0C		-	CGO13_PH_L	CGO13_INV_L	CGOUT13_L[4:0]
17F			0D		-	CGO14_PH_L	CGO14_INV_L	CGOUT14_L[4:0]
180			0E		-	CGO15_PH_L	CGO15_INV_L	CGOUT15_L[4:0]
181			0F		-	CGO16_PH_L	CGO16_INV_L	CGOUT16_L[4:0]
182			10		-	CGO17_PH_L	CGO17_INV_L	CGOUT17_L[4:0]
183			11		-	CGO18_PH_L	CGO18_INV_L	CGOUT18_L[4:0]
184			12		-	CGO19_PH_L	CGO19_INV_L	CGOUT19_L[4:0]
185			13		-	CGO20_PH_L	CGO20_INV_L	CGOUT20_L[4:0]
186			14		-	CGO21_PH_L	CGO21_INV_L	CGOUT21_L[4:0]
187			15		-	CGO22_PH_L	CGO22_INV_L	CGOUT22_L[4:0]
188	SET_GIP_R	P2	16	1	NVALID	CGO1_PH_R	CGO1_INV_R	CGOUT1_R[4:0]
189			17		-	CGO2_PH_R	CGO2_INV_R	CGOUT2_R[4:0]
18A			18		-	CGO3_PH_R	CGO3_INV_R	CGOUT3_R[4:0]
18B			19		-	CGO4_PH_R	CGO4_INV_R	CGOUT4_R[4:0]
18C			1A		-	CGO5_PH_R	CGO5_INV_R	CGOUT5_R[4:0]
18D			1B		-	CGO6_PH_R	CGO6_INV_R	CGOUT6_R[4:0]
18E			1C		-	CGO7_PH_R	CGO7_INV_R	CGOUT7_R[4:0]

18F			1D		-	CGO8_PH_R	CGO8_INV_R	CGOUT8_R[4:0]
190			1E		-	CGO9_PH_R	CGO9_INV_R	CGOUT9_R[4:0]
191			1F		-	CGO10_PH_R	CGO10_INV_R	CGOUT10_R[4:0]
192			20		-	CGO11_PH_R	CGO11_INV_R	CGOUT11_R[4:0]
193			21		-	CGO12_PH_R	CGO12_INV_R	CGOUT12_R[4:0]
194			22		-	CGO13_PH_R	CGO13_INV_R	CGOUT13_R[4:0]
195			23		-	CGO14_PH_R	CGO14_INV_R	CGOUT14_R[4:0]
196			24		-	CGO15_PH_R	CGO15_INV_R	CGOUT15_R[4:0]
197			25		-	CGO16_PH_R	CGO16_INV_R	CGOUT16_R[4:0]
198			26		-	CGO17_PH_R	CGO17_INV_R	CGOUT17_R[4:0]
199			27		-	CGO18_PH_R	CGO18_INV_R	CGOUT18_R[4:0]
19A			28		-	CGO19_PH_R	CGO19_INV_R	CGOUT19_R[4:0]
19B			29		-	CGO20_PH_R	CGO20_INV_R	CGOUT20_R[4:0]
19C			2A		-	CGO21_PH_R	CGO21_INV_R	CGOUT21_R[4:0]
19D			2B		-	CGO22_PH_R	CGO22_INV_R	CGOUT22_R[4:0]
19E	SET_GIP_L_GS	P2	2C	1	NVALID	-	-	CGOUT1_L_GS[4:0]
19F			2D		-	-	-	CGOUT2_L_GS[4:0]
1A0			2E		-	-	-	CGOUT3_L_GS[4:0]
1A1			2F		-	-	-	CGOUT4_L_GS[4:0]
1A2			30		-	-	-	CGOUT5_L_GS[4:0]
1A3			31		-	-	-	CGOUT6_L_GS[4:0]
1A4			32		-	-	-	CGOUT7_L_GS[4:0]
1A5			33		-	-	-	CGOUT8_L_GS[4:0]
1A6			34		-	-	-	CGOUT9_L_GS[4:0]
1A7			35		-	-	-	CGOUT10_L_GS[4:0]
1A8			36		-	-	-	CGOUT11_L_GS[4:0]
1A9			37		-	-	-	CGOUT12_L_GS[4:0]
1AA			38		-	-	-	CGOUT13_L_GS[4:0]
1AB			39		-	-	-	CGOUT14_L_GS[4:0]
1AC			3A		-	-	-	CGOUT15_L_GS[4:0]
1AD			3B		-	-	-	CGOUT16_L_GS[4:0]
1AE			3C		-	-	-	CGOUT17_L_GS[4:0]
1AF			3D		-	-	-	CGOUT18_L_GS[4:0]
1B0			3E		-	-	-	CGOUT19_L_GS[4:0]
1B1			3F					CGOUT20_L_GS[4:0]
1B2			40					CGOUT21_L_GS[4:0]
1B3			41		-	-	-	CGOUT22_L_GS[4:0]
1B4	SET_GIP_R_GS	P2	42	1	NVALID	-	-	CGOUT1_R_GS[4:0]
1B5			43		-	-	-	CGOUT2_R_GS[4:0]

1B6			44		-	-	-	CGOUT3_R_GS[4:0]						
1B7			45		-	-	-	CGOUT4_R_GS[4:0]						
1B8			46		-	-	-	CGOUT5_R_GS[4:0]						
1B9			47		-	-	-	CGOUT6_R_GS[4:0]						
1BA			48		-	-	-	CGOUT7_R_GS[4:0]						
1BB			49		-	-	-	CGOUT8_R_GS[4:0]						
1BC			4A		-	-	-	CGOUT9_R_GS[4:0]						
1BD			4B		-	-	-	CGOUT10_R_GS[4:0]						
1BE			4C		-	-	-	CGOUT11_R_GS[4:0]						
1BF			4D		-	-	-	CGOUT12_R_GS[4:0]						
1C0			4E		-	-	-	CGOUT13_R_GS[4:0]						
1C1			4F		-	-	-	CGOUT14_R_GS[4:0]						
1C2			50		-	-	-	CGOUT15_R_GS[4:0]						
1C3			51		-	-	-	CGOUT16_R_GS[4:0]						
1C4			52		-	-	-	CGOUT17_R_GS[4:0]						
1C5			53		-	-	-	CGOUT18_R_GS[4:0]						
1C6			54		-	-	-	CGOUT19_R_GS[4:0]						
1C7			55		-	-	-	CGOUT20_R_GS[4:0]						
1C8			56		-	-	-	CGOUT21_R_GS[4:0]						
1C9			57		-	-	-	CGOUT22_R_GS[4:0]						
1CA	SETGIP1	P2	58	1	NVALID	GIP_GAS_OPT	TGEQL	GIP_RST_EN	INIT_PORCH[3:0]					
1CB			59		INIT_W[3:0]				-	INIT[10:8]				
1CC			5A		INIT[7:0]									
1CD			5B		-	-	STV_NUM[1:0]		-	-	-	-		
1CE			5C		STV_S0[7:0]									
1CF			5D		STV_W[3:0]				-	STV_S1[2:0]				
1D0			5E		-	-	-	STV_S2[4:0]						
1D1			5F		-	-	-	STV_S3[4:0]						
1D2			60		ETV_W[3:0]				-	ETV_S1[2:0]				
1D3			61		-	-	-	ETV_S2[4:0]						
1D4			62		-	ETV_ON_OPT	ETV_OFF_OPT	ETV_S3[4:0]						
1D5			63		SETV_ON[7:0]									
1D6			64		SETV_OFF[7:0]									
1D7			65		-	ETV_EN	ETV_NUM[1:0]		-	ETV_S0[10:8]				
1D8			66		ETV_S0[7:0]									
1D9			67		CKV0_NUM[3:0]				CKV0_W[3:0]					
1DA			68		CKV0_S0[7:0]									
1DB			69		CKV0_ON[7:0]									
1DC			6A		CKV0_OFF[7:0]									
1DD			6B		CKV0_DUM[7:0]									

1DE	SETGIP2	P2	6C	1	NVALID	EOLR	FLM_MODE	GEQ_LINE	GEQ_W[3:0]				
1DF			6D		-	-	GEQ_GGND1[5:0]						
1E0			6E		-	-	GEQ_GGND2[5:0]						
1E1			6F		GIPDR[1:0]		VGHO_SEL	VGLO_SEL	VGLO_SEL2	CKV_GROUP	CKV1_CON	CKV0_CON	
1E2			70		CKV1_NUM[3:0]				CKV1_W[3:0]				
1E3			71		CKV1_S0[7:0]								
1E4			72		CKV1_ON[7:0]								
1E5			73		CKV1_OFF[7:0]								
1E6			74		CKV1_DUM[7:0]								
1E7			75		FLM_EN	FLM_W[6:0]							
1E8			76		FLM_ON[7:0]								
1E9			77		VEN_EN	VEN_W[10:8]			FLM_NUM	FLM_OFF[10:8]			
1EA			78		FLM_OFF[7:0]								
1EB			79		VEN_W[7:0]								
1EC			7A		VEN_S0[7:0]								
1ED			7B		VEN_S1[7:0]								
1EE			7C		VEN_DUM[7:0]								
1EF			7D		VEN_ON[7:0]								
1F0			7E		VEN_OFF[7:0]								
1F1	SET_GIP_OPT	P2	7F	1	NVALID	GIP_OPT0[6:0]							
1F2			80		GIP_OPT1[7:0]								
1F3	SETGIP5	P2	81	1	NVALID	FLM_EQ	ETV_BLK_S0[10:8]			STV_BLK_S0[10:8]			
1F4			82		STV_BLK_S0[7:0]								
1F5			83		ETV_BLK_S0[7:0]								
1F6			84		STV_BLK_S2[3:0]				STV_BLK_S1[3:0]				
1F7			85		STV_OPT[3:0]				STV_BLK_S3[3:0]				
1F8			86		ETV_BLK_S2[3:0]				ETV_BLK_S1[3:0]				
1F9			87		ETV_OPT[3:0]				ETV_BLK_S3[3:0]				
1FA			88		FLM_ON_TU[7:0]								
1FB			89		FLM_OFF_TU[7:0]								
1FC	GAS_CTRL	P4	06	1	NVALID	GAS_DBS_CLR	GAS_IN_DBS_EN	GAS_OUT_DBS_EN	GAS_VCOM_EN	GAS_DBS_VEN	GAS_DBS_GEN	GAS_DBS_SEN	
1FD			07		GAS_DBS_LTH[7:0]								
1FE			08		GAS_SLPIN_EN	GAS_RE_SLPOUT	GAS_RE_SLPOUT_OTP_RELOAD	GAS_POR_OPT	GAS_POR_MASK	GAS_BLK_NUM[2:0]			
203	SETGIP3	P2	8E	1	NVALID	GIP_OPT3[4:0]					FLM_ON_LRN_EN	FLM_OFF_LRN_EN	
204			8F		AGON_EN	AGON_OPT	AGON_LINE0	AGON_LINE1	AGON_DLY[3:0]				
205			90		AGON_S[3:0]				AGON_W[3:0]				
206			91		AGON_ON0[7:0]								
207			92		AGON_ON1[7:0]								

20B	CE_CTRL0	P3	00	1	NVALID	-	-	-	-	-	-	CE_OTP_ROM_VLD	
20C	CE_CTRL1	P3	01	1	NVALID	-	-	-	CE_EDG_MODE[1:0]		CE_SAT_MODE[1:0]		
20D	CE_PRM(OTP*3)	P3	02	1	NVALID	-	-	CE_EDG_SP_PROT	CE_SAT_SP_PROT	CE_COL_EN	CE_HUE_EN	CE_VV_EN	
20E			03		-	CE_THREF[2:0]			-	CE_THSAT[2:0]			
20F			04		-	CE_THGREY[2:0]			-	CE_THCOLOR[2:0]			
210			05		CE_SAT_OFFS[7:0]								
211			06		CE_REF_OFFS[7:0]								
212			07		-	-	-	-	-	CE_THCOLOR2[2:0]			
213			08		CE_COL_OFFS[7:0]								
214			09		CE_SG016[3:0]				CE_SG000[3:0]				
215			0A		CE_SG048[3:0]				CE_SG032[3:0]				
216			0B		CE_SG080[3:0]				CE_SG064[3:0]				
217			0C		CE_SG112[3:0]				CE_SG096[3:0]				
218			0D		CE_SG144[3:0]				CE_SG128[3:0]				
219			0E		CE_SG176[3:0]				CE_SG160[3:0]				
21A			0F		CE_SG208[3:0]				CE_SG192[3:0]				
21B			10		CE_SG240[3:0]				CE_SG224[3:0]				
21C			11		-	-	-	-	CE_SG255[3:0]				
21D			12		-	-	CE_HUE_TBL00[5:0]						
21E			13		-	-	CE_HUE_TBL01[5:0]						
21F			14		-	-	CE_HUE_TBL02[5:0]						
220			15		-	-	CE_HUE_TBL03[5:0]						
221			16		-	-	CE_HUE_TBL04[5:0]						
222			17		-	-	CE_HUE_TBL05[5:0]						
223			18		-	-	CE_HUE_TBL06[5:0]						
224			19		-	-	CE_HUE_TBL07[5:0]						
225			1A		-	-	CE_HUE_TBL08[5:0]						
226			1B		-	-	CE_HUE_TBL09[5:0]						
227			1C		-	-	CE_HUE_TBL10[5:0]						
228			1D		-	-	CE_HUE_TBL11[5:0]						
229			1E		-	-	CE_HUE_TBL12[5:0]						
22A			1F		-	-	CE_HUE_TBL13[5:0]						
22B			20		-	-	CE_HUE_TBL14[5:0]						
22C			21		-	-	CE_HUE_TBL15[5:0]						
22D			22		-	-	CE_HUE_TBL16[5:0]						
22E			23		-	-	CE_HUE_TBL17[5:0]						
22F			24		-	-	CE_HUE_TBL18[5:0]						
230			25		-	-	CE_HUE_TBL19[5:0]						
231			26		-	-	CE_HUE_TBL20[5:0]						

232			27		-	-	CE_HUE_TBL21[5:0]						
233			28		-	-	CE_HUE_TBL22[5:0]						
234			29		-	-	CE_HUE_TBL23[5:0]						
235			2A		CE_EDG_FAC2[3:0]				CE_EDG_FAC1[3:0]				
236			02		NVALID	-	-	CE_EDG_SP_PROT	CE_SAT_SP_PROT	CE_COL_EN	CE_HUE_EN	CE_VV_EN	
237			03		-	CE_THREF[2:0]			-	CE_THSAT[2:0]			
238			04		-	CE_THGREY[2:0]			-	CE_THCOLOR[2:0]			
239			05		CE_SAT_OFFS[7:0]								
23A			06		CE_REF_OFFS[7:0]								
23B			07		-	-	-	-	-	CE_THCOLOR2[2:0]			
23C			08		CE_COL_OFFS[7:0]								
23D			09		CE_SG016[3:0]				CE_SG000[3:0]				
23E			0A		CE_SG048[3:0]				CE_SG032[3:0]				
23F			0B		CE_SG080[3:0]				CE_SG064[3:0]				
240			0C		CE_SG112[3:0]				CE_SG096[3:0]				
241			0D		CE_SG144[3:0]				CE_SG128[3:0]				
242			0E		CE_SG176[3:0]				CE_SG160[3:0]				
243			0F		CE_SG208[3:0]				CE_SG192[3:0]				
244			10		CE_SG240[3:0]				CE_SG224[3:0]				
245			11		-	-	-	-	CE_SG255[3:0]				
246			12		-	-	CE_HUE_TBL00[5:0]						
247			13	2	-	-	CE_HUE_TBL01[5:0]						
248			14		-	-	CE_HUE_TBL02[5:0]						
249			15		-	-	CE_HUE_TBL03[5:0]						
24A			16		-	-	CE_HUE_TBL04[5:0]						
24B			17		-	-	CE_HUE_TBL05[5:0]						
24C			18		-	-	CE_HUE_TBL06[5:0]						
24D			19		-	-	CE_HUE_TBL07[5:0]						
24E			1A		-	-	CE_HUE_TBL08[5:0]						
24F			1B		-	-	CE_HUE_TBL09[5:0]						
250			1C		-	-	CE_HUE_TBL10[5:0]						
251			1D		-	-	CE_HUE_TBL11[5:0]						
252			1E		-	-	CE_HUE_TBL12[5:0]						
253			1F		-	-	CE_HUE_TBL13[5:0]						
254			20		-	-	CE_HUE_TBL14[5:0]						
255			21		-	-	CE_HUE_TBL15[5:0]						
256			22		-	-	CE_HUE_TBL16[5:0]						
257			23		-	-	CE_HUE_TBL17[5:0]						
258			24		-	-	CE_HUE_TBL18[5:0]						
259			25		-	-	CE_HUE_TBL19[5:0]						

25A			26		-	-	CE_HUE_TBL20[5:0]						
25B			27		-	-	CE_HUE_TBL21[5:0]						
25C			28		-	-	CE_HUE_TBL22[5:0]						
25D			29		-	-	CE_HUE_TBL23[5:0]						
25E			2A		CE_EDG_FAC2[3:0]				CE_EDG_FAC1[3:0]				
25F			02		NVALID	-	-	CE_EDG_SP_PROT	CE_SAT_SP_PROT	CE_COL_EN	CE_HUE_EN	CE_VV_EN	
260			03		-	CE_THREF[2:0]			-	CE_THSAT[2:0]			
261			04		-	CE_THGREY[2:0]			-	CE_THCOLOR[2:0]			
262			05		CE_SAT_OFFS[7:0]								
263			06		CE_REF_OFFS[7:0]								
264			07		-	-	-	-	-	CE_THCOLOR2[2:0]			
265			08		CE_COL_OFFS[7:0]								
266			09		CE_SG016[3:0]				CE_SG000[3:0]				
267			0A		CE_SG048[3:0]				CE_SG032[3:0]				
268			0B		CE_SG080[3:0]				CE_SG064[3:0]				
269			0C		CE_SG112[3:0]				CE_SG096[3:0]				
26A			0D		CE_SG144[3:0]				CE_SG128[3:0]				
26B			0E		CE_SG176[3:0]				CE_SG160[3:0]				
26C			0F		CE_SG208[3:0]				CE_SG192[3:0]				
26D			10		CE_SG240[3:0]				CE_SG224[3:0]				
26E			11		-	-	-	-	CE_SG255[3:0]				
26F			12		-	-	CE_HUE_TBL00[5:0]						
270			13	3	-	-	CE_HUE_TBL01[5:0]						
271			14		-	-	CE_HUE_TBL02[5:0]						
272			15		-	-	CE_HUE_TBL03[5:0]						
273			16		-	-	CE_HUE_TBL04[5:0]						
274			17		-	-	CE_HUE_TBL05[5:0]						
275			18		-	-	CE_HUE_TBL06[5:0]						
276			19		-	-	CE_HUE_TBL07[5:0]						
277			1A		-	-	CE_HUE_TBL08[5:0]						
278			1B		-	-	CE_HUE_TBL09[5:0]						
279			1C		-	-	CE_HUE_TBL10[5:0]						
27A			1D		-	-	CE_HUE_TBL11[5:0]						
27B			1E		-	-	CE_HUE_TBL12[5:0]						
27C			1F		-	-	CE_HUE_TBL13[5:0]						
27D			20		-	-	CE_HUE_TBL14[5:0]						
27E			21		-	-	CE_HUE_TBL15[5:0]						
27F			22		-	-	CE_HUE_TBL16[5:0]						
280			23		-	-	CE_HUE_TBL17[5:0]						
281			24		-	-	CE_HUE_TBL18[5:0]						

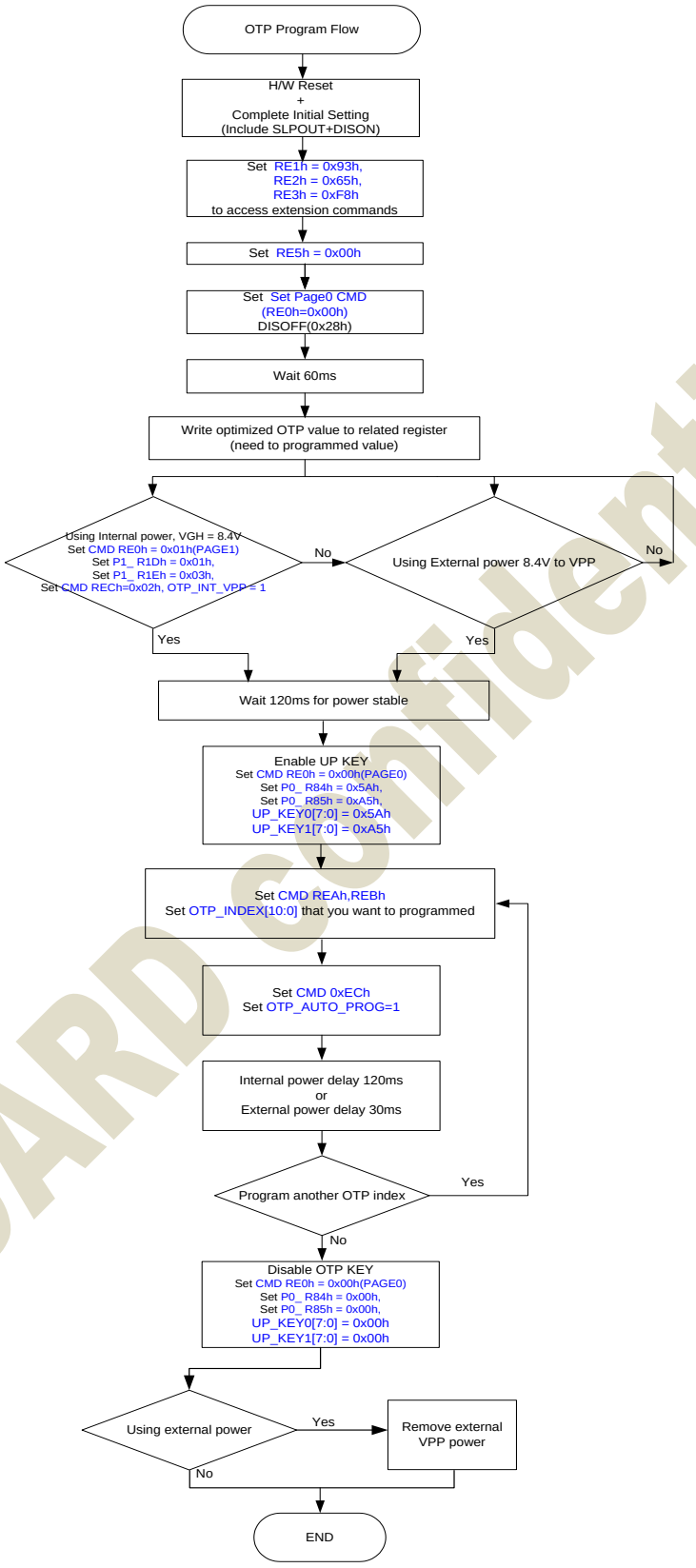
282			25		-	-	CE_HUE_TBL19[5:0]						
283			26		-	-	CE_HUE_TBL20[5:0]						
284			27		-	-	CE_HUE_TBL21[5:0]						
285			28		-	-	CE_HUE_TBL22[5:0]						
286			29		-	-	CE_HUE_TBL23[5:0]						
287			2A		CE_EDG_FAC2[3:0]				CE_EDG_FAC1[3:0]				
288	DGC_CTRL	P3	2B	1	NVALID	-	-	-	-	-	-	DGC_EN	
289			2C		-	-	-	-	-	-	DGC_SELECT[1:0]		
28A			2D		-	-	-	DTR_EN	DGC_CHKSUM_EN[2:0]			DGC_REG_SYNC_GT	
28B			2E		DGC_GT_BYTE0[7:0]								
28C			2F		DGC_GT_BYTE1[7:0]								
28D	SET_DIGITAL_GAMMA1	P3	30	1	NVALID	DGC_GAMMA1_GAIN[6:0]							
28E			31		DGC_GAMMA1_OFFSET[3:0]				DGC_GAMMA1_000[3:0]				
28F			32		DGC_GAMMA1_004[3:0]				DGC_GAMMA1_008[3:0]				
290			33		DGC_GAMMA1_012[3:0]				DGC_GAMMA1_016[3:0]				
291			34		DGC_GAMMA1_020[3:0]				DGC_GAMMA1_024[3:0]				
292			35		DGC_GAMMA1_028[3:0]				DGC_GAMMA1_032[3:0]				
293			36		DGC_GAMMA1_036[3:0]				DGC_GAMMA1_040[3:0]				
294			37		DGC_GAMMA1_044[3:0]				DGC_GAMMA1_048[3:0]				
295			38		DGC_GAMMA1_052[3:0]				DGC_GAMMA1_056[3:0]				
296			39		DGC_GAMMA1_060[3:0]				DGC_GAMMA1_064[3:0]				
297			3A		DGC_GAMMA1_068[3:0]				DGC_GAMMA1_072[3:0]				
298			3B		DGC_GAMMA1_076[3:0]				DGC_GAMMA1_080[3:0]				
299			3C		DGC_GAMMA1_084[3:0]				DGC_GAMMA1_088[3:0]				
29A			3D		DGC_GAMMA1_092[3:0]				DGC_GAMMA1_096[3:0]				
29B			3E		DGC_GAMMA1_100[3:0]				DGC_GAMMA1_104[3:0]				
29C			3F		DGC_GAMMA1_108[3:0]				DGC_GAMMA1_112[3:0]				
29D			40		DGC_GAMMA1_116[3:0]				DGC_GAMMA1_120[3:0]				
29E			41		DGC_GAMMA1_124[3:0]				DGC_GAMMA1_128[3:0]				
29F			42		DGC_GAMMA1_132[3:0]				DGC_GAMMA1_136[3:0]				
2A0			43		DGC_GAMMA1_140[3:0]				DGC_GAMMA1_144[3:0]				
2A1			44		DGC_GAMMA1_148[3:0]				DGC_GAMMA1_152[3:0]				
2A2			45		DGC_GAMMA1_156[3:0]				DGC_GAMMA1_160[3:0]				
2A3			46		DGC_GAMMA1_164[3:0]				DGC_GAMMA1_168[3:0]				
2A4			47		DGC_GAMMA1_172[3:0]				DGC_GAMMA1_176[3:0]				
2A5			48		DGC_GAMMA1_180[3:0]				DGC_GAMMA1_184[3:0]				
2A6			49		DGC_GAMMA1_188[3:0]				DGC_GAMMA1_192[3:0]				
2A7			4A		DGC_GAMMA1_196[3:0]				DGC_GAMMA1_200[3:0]				
2A8			4B		DGC_GAMMA1_204[3:0]				DGC_GAMMA1_208[3:0]				

2A9			4C		DGC_GAMMA1_212[3:0]	DGC_GAMMA1_216[3:0]
2AA			4D		DGC_GAMMA1_220[3:0]	DGC_GAMMA1_224[3:0]
2AB			4E		DGC_GAMMA1_228[3:0]	DGC_GAMMA1_232[3:0]
2AC			4F		DGC_GAMMA1_236[3:0]	DGC_GAMMA1_240[3:0]
2AD			50		DGC_GAMMA1_244[3:0]	DGC_GAMMA1_248[3:0]
2AE			51		DGC_GAMMA1_252[3:0]	DGC_GAMMA1_253[3:0]
2AF			52		DGC_GAMMA1_254[3:0]	DGC_GAMMA1_255[3:0]
2B0			53			DGC_GAMMA1_OFFSET_MAG[1:0] / DGC_GAMMA1_DELTA_MAG[1:0]
2B1	SET_DIGITAL_GAMMA2	P3	54	1	NVALID	DGC_GAMMA2_GAIN[6:0]
2B2			55		DGC_GAMMA2_OFFSET[3:0]	DGC_GAMMA2_000[3:0]
2B3			56		DGC_GAMMA2_004[3:0]	DGC_GAMMA2_008[3:0]
2B4			57		DGC_GAMMA2_012[3:0]	DGC_GAMMA2_016[3:0]
2B5			58		DGC_GAMMA2_020[3:0]	DGC_GAMMA2_024[3:0]
2B6			59		DGC_GAMMA2_028[3:0]	DGC_GAMMA2_032[3:0]
2B7			5A		DGC_GAMMA2_036[3:0]	DGC_GAMMA2_040[3:0]
2B8			5B		DGC_GAMMA2_044[3:0]	DGC_GAMMA2_048[3:0]
2B9			5C		DGC_GAMMA2_052[3:0]	DGC_GAMMA2_056[3:0]
2BA			5D		DGC_GAMMA2_060[3:0]	DGC_GAMMA2_064[3:0]
2BB			5E		DGC_GAMMA2_068[3:0]	DGC_GAMMA2_072[3:0]
2BC			5F		DGC_GAMMA2_076[3:0]	DGC_GAMMA2_080[3:0]
2BD			60		DGC_GAMMA2_084[3:0]	DGC_GAMMA2_088[3:0]
2BE			61		DGC_GAMMA2_092[3:0]	DGC_GAMMA2_096[3:0]
2BF			62		DGC_GAMMA2_100[3:0]	DGC_GAMMA2_104[3:0]
2C0			63		DGC_GAMMA2_108[3:0]	DGC_GAMMA2_112[3:0]
2C1			64		DGC_GAMMA2_116[3:0]	DGC_GAMMA2_120[3:0]
2C2			65		DGC_GAMMA2_124[3:0]	DGC_GAMMA2_128[3:0]
2C3			66		DGC_GAMMA2_132[3:0]	DGC_GAMMA2_136[3:0]
2C4			67		DGC_GAMMA2_140[3:0]	DGC_GAMMA2_144[3:0]
2C5			68		DGC_GAMMA2_148[3:0]	DGC_GAMMA2_152[3:0]
2C6			69		DGC_GAMMA2_156[3:0]	DGC_GAMMA2_160[3:0]
2C7			6A		DGC_GAMMA2_164[3:0]	DGC_GAMMA2_168[3:0]
2C8			6B		DGC_GAMMA2_172[3:0]	DGC_GAMMA2_176[3:0]
2C9			6C		DGC_GAMMA2_180[3:0]	DGC_GAMMA2_184[3:0]
2CA			6D		DGC_GAMMA2_188[3:0]	DGC_GAMMA2_192[3:0]
2CB			6E		DGC_GAMMA2_196[3:0]	DGC_GAMMA2_200[3:0]
2CC			6F		DGC_GAMMA2_204[3:0]	DGC_GAMMA2_208[3:0]
2CD			70		DGC_GAMMA2_212[3:0]	DGC_GAMMA2_216[3:0]
2CE			71		DGC_GAMMA2_220[3:0]	DGC_GAMMA2_224[3:0]
2CF			72		DGC_GAMMA2_228[3:0]	DGC_GAMMA2_232[3:0]
2D0			73		DGC_GAMMA2_236[3:0]	DGC_GAMMA2_240[3:0]

2D1			74		DGC_GAMMA2_244[3:0]				DGC_GAMMA2_248[3:0]			
2D2			75		DGC_GAMMA2_252[3:0]				DGC_GAMMA2_253[3:0]			
2D3			76		DGC_GAMMA2_254[3:0]				DGC_GAMMA2_255[3:0]			
2D4			77						DGC_GAMMA2_OFFSET_MAG[1:0]		DGC_GAMMA2_DELTA_MAG[1:0]	
2D5	PWM_CTRL	P3	98	1	NVALID	-	LEDON_OE	LEDON_EN	LEDON_POL	VCSW_VOL	LEDPWM_POL	LED_VOL
2D6			99		-	-	PWM_SYNC2VS	PWM_OFFSET[4:0]				
2D7			9A		SEL_CLK_DIV[7:0]							
2D8			9B		N_VAL[7:0]							
2D9			9C		PWM_FRAC[7:0]							
30E	POWER_OPT	P4	00	1	NVALID	PDS[30:24]						
30F			01		PDS[23:16]							
310			02		PDS[15:8]							
311			03		PDS[7:0]							
313	SETRGBCYC2	P4	09	1	NVALID	SDPRDUM	SDDUM[1:0]		SDSW[1:0]		SDPORCH[1:0]	
314			0A		RGB_SPAIF[3:0]				RGB_SPAIB[3:0]			
315			0B		RGB_SNAIF[3:0]				RGB_SNAIB[3:0]			
316	SETSTBA2	P4	0C	1	NVALID	-	VTEST[5:0]					
317			0D		-	SDS[22:16]						
318			0E		SDS[15:8]							
319			0F		SDS[7:0]							
328	SET_OSCD	P4	1E	1	NVALID	-	OSCD_EN	OSCD_BIAS_EN	-	OSCD_ADJ[2:0]		
329			1F		OSCD_OFFSET_SS	-	-	OSCD_SS_EN	OSCD_SS_F[2:0]		OSCD_SS_R	
333	SETMIPI1	P4	29	1	NVALID	TX_LDO_SEL[2:0]			PHY_VDC0_D3	RX_LDO_SEL[2:0]		
334	SETMIPI2	P4	2A	1	NVALID	PHY_VDC1_D6	RX_IBOOST_EN	VREF_DSI_EN	LP_CD_IB	HS_RX_PRE_IB	HS_RX_PST_IB	HS_RX_D2S_IB
335			2B		DSI_OPT0[7:0]							
336			2C		DSI_OPT1[7:0]							
337	SETMIPI3	P4	2D	1	NVALID	PHY_CTL0_D6	HS_RX_VCM[1:0]		LP_RX_VT[1:0]		LP_CD_VT[1:0]	
338			2E		DSI_CTL0[7:0]							
339			2F		DSI_CTL1[7:0]							
33A			30		DSI_CTL2[7:0]							
33B			31		DSI_CTL3[7:0]							
33C			32		DSI_CTL4[7:0]							
33D			33		DSI_CTL5[7:0]							
33E			34		DSI_CTL6[7:0]							
33F	SETMIPI4	P4	35	1	NVALID	DSI_CTL7[6:0]						
340	SETMIPI5	P4	36	1	NVALID	DSI_CTL8[6:0]						
341			37		DSI_CTL9[7:0]							
394	REG_CHKSUM	P4	97	1	NVALID	-	SLPIN_RST_EN	CHKSUM_OFF	-	CHKSUM_SEL[2:0]		
395	SET_INH_CHKSUM	P4	98	1	NVALID	-	-	SLPIN_RESET_EN	INH_CHKSUM_OFF	INH_CHKSUM_SEL[2:0]		

396	SET_GPO	P4	99	1	NVALID	GPO0_REV	GPO0_OE	GPO0_SEL[4:0]					
397			9A		-	GPO1_REV	GPO1_OE	GPO1_SEL[4:0]					
398			9B		-	GPO2_REV	GPO2_OE	GPO2_SEL[4:0]					
399			9C		-	GPO3_REV	GPO3_OE	GPO3_SEL[4:0]					
39A			9D		-	GPO4_REV	GPO4_OE	GPO4_SEL[4:0]					
39B			9E		VCSW1_OE	GPO5_REV	GPO5_OE	GPO5_SEL[4:0]					
39C			9F		VCSW2_OE	GPO6_REV	GPO6_OE	GPO6_SEL[4:0]					
39D			A0		-	INTERNAL_SEL2[2:0]			-	INTERNAL_SEL1[2:0]			
3A1	RX0A_OTP	P4	A4	1	NVALID	-	DSI_F8F9_EN	DISPON_SEL	-	-	-	RX0A_EN	
3A2			A5		RX0A[7:0]								
3A3	DSI_SMRP	P4	A6	1	NVALID	-	-	-	-	-	-	DSI_SMRP_TYPE	
3A4			A7		DSI_SMRP[15:8]								
3A5			A8		DSI_SMRP[7:0]								

3.2. OTP Programming Flow



3.3. Programming Sequence

Step	Operation
1	Power on and HWRST the module. Then do SLPOOUT.
2	Set 0xE1h = 0x93h, 0xE2h = 0x65h, 0xE3h = 0xF8h to access extension commands.
3	set RE5h = 0x00h.then DISOFF(delay 60ms)
4	Write optimized OTP value to related register.
5	Set page1 CMD(RE0h=0x01h) , then set Page1_R1Dh = 0x01h, Page1_R1Eh = 0x03h(VGH=8.4V) and CMD RECh, OTP_INT_VPP = 1 for using internal power mode. Or using the external power 8.4V to VPP.
6	Wait 120ms for VPP power stable.
7	Set Page0 CMD(RE0h=0x00h), then set Page0_0x84h = 0x5Ah,Page0_0x85h=0xA5h to enable UP KEY.
8	Set 0xEAh 0xEBh, UP_INDEX[10:0] that you want to programmed.
9	Set 0xECh, OTP_AUTO_PROG=1.
10	Delay 120ms for internal power to program OTP. Or delay 30ms for external power to program OTP.
11	One OTP block programming was completed. Return to step (7) for next OTP block programming. Or go next step if all OTP programming is finished.
12	Set Page0_0x84h = 0x00h,Page0_0x85h=0x00h to disable OTP KEY.
13	If you use external power, remove the external power 8.4V from VPP.

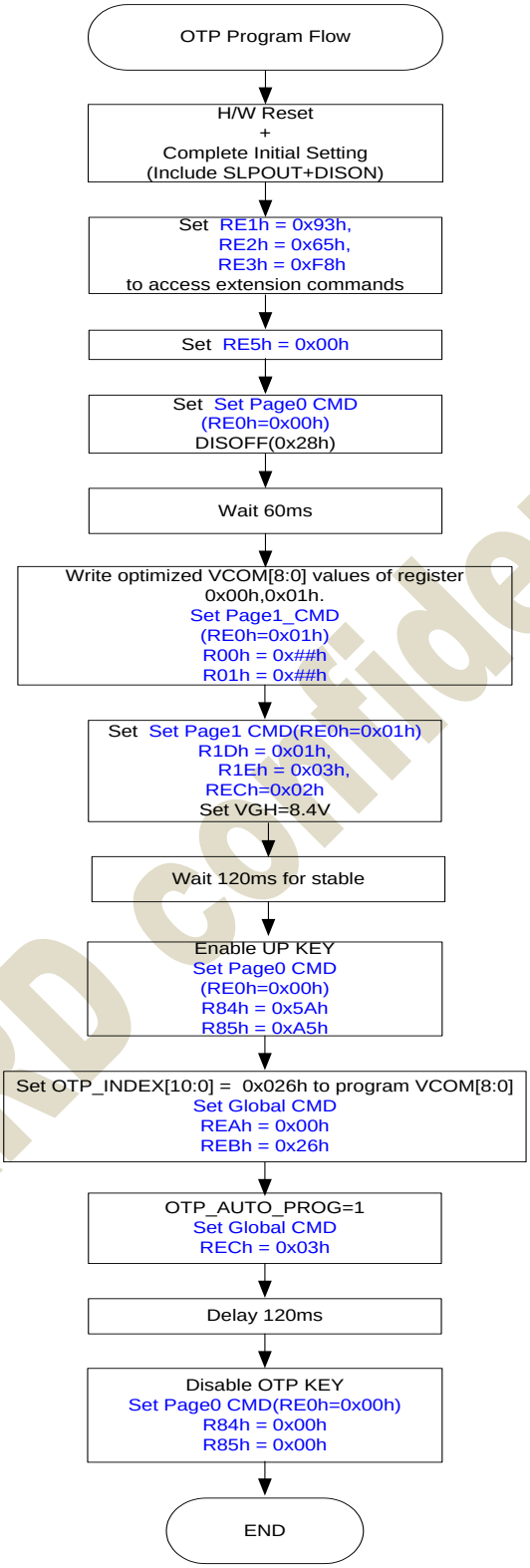
Note:

1. All OTP default value is 1.
2. OTP can be reloaded only NVALID bit is burned(value is 0).
3. Fifipower driver IC do auto OTP programming. User only set the start OTP_INDEX of the Ref. CMD block then all block is programmed by driver IC. This function also can be used for MTP Ref. CMD block.

   For example:

   a. To program VCOM_SET 1st time, user set OTP_INDEX=026h then from OTP_INDEX=026h to OTP_INDEX=027h(Ref. CMD block of 1st VCOM_SET) is programmed by driver IC.
   b. To program VCOM_SET 2nd time, user set OTP_INDEX=026h then from OTP_INDEX=028h to OTP_INDEX=029h(Ref. CMD block of 2nd VCOM_SET) is programmed by driver IC.

3.4. OTP Programming example of VCOM setting



3.6. OTP read example