

V0.00 Preliminary

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REVISION HISTORY

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	Original	Kevin	SW	Dennis	2010/11/3

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1 DESCRIPTION

1.1 Purpose of this Document

This document has been created to provide complete reference specifications for the NT35510. IC design engineers should refer to these specifications when designing ICs, test engineers when testing the compliance of manufactured ICs to guarantee their performance, and application engineers when helping customers to make sure they are using this IC properly.

1.2 General Description

The NT35510 device is a single-chip solution for a-Si TFT LCD that incorporates gate drivers and is capable of 480RGBx864, 480RGBx854, 480RGBx800, 480RGBx720, 480RGBx640 with internal CGRAM. It includes a 9,953,280 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The NT35510 supports MDDI interface, MIPI Interface, 16/18/24 bits RGB interface, 8/16/24-bit system interfaces, serial peripheral interfaces (SPI) and I2C interface. The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The NT35510 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 480-RGB x 864-dot 16.77M-color images. A deep standby mode is also supported for lower power consumption.

This LSI is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, including bi-directional pagers, digital audio players, cellular phones and handheld PDA..

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2 FEATURES

- Single chip WVGA a-Si TFT LCD Controller/driver with Display RAM.
- Display resolution option
 - 480RGB x 864 with 480x24-bitsx 864 GRAM
 - 480RGB x 854 with 480x24-bitsx 854 GRAM
 - 480RGB x 800 with 480x24-bitsx 800 GRAM
 - 480RGB x 720 with 480x24-bitsx 720 GRAM
 - 480RGB x 640 with 480x24-bitsx 640 GRAM
- Display data RAM (frame memory): 480 x 864 x 24-bits = 9,953,280 bits
- Display mode (Color mode)
 - Full color mode: 16.7M-colors
 - Reduce color mode: 262K colors
 - Reduce color mode: 65K colors
 - Idle mode: 8-colors
- Interface
 - 8-/16-/24-bits 80-series MPU interface
 - 16-bit serial peripheral interface
 - I2C interface
 - 16-/18-/24-bits RGB interface (DE mode and SYNC mode with polarity of HS/VS can be set by register)
 - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 or 2 data lane pairs)
 - Mobile Display Digital Interface (MDDI V1.2, 1 strobe and 1 or 2 data lane pairs)
- Display features
 - Window address functions for specifying a rectangular area on the internal RAM to write data
 - Individual gamma correction setting for RGB dots
 - Deep standby function
- ♦ On chip
 - VGHO/VGLO voltage generator for gate control signal and panel
 - Oscillator for display clock
 - Supports gate control signals to gate driver in the panel
 - On module color characteristics
 - On module checksums checking
 - Four GPO (General Purpose Output) pins for external control

♦ Supply voltage range

- I/O supply voltage range for VDDI to VSSI: 1.65V ~ 3.3V (VDDI) or 1.1 ~ 1.3V (VDDIL)
- Analog supply voltage range for VDDB/VDDA/VDDR to VSSB/VSSA/VSSR: 2.3V ~ 4.8V
- MIPI/MDDI regulator supply voltage range for VDDAM to VSSAM: 2.3V ~ 4.8V

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- Output voltage levels
 - Positive gate driver voltage range for VGH: AVDD+VDDB ~ 2xAVDD AVEE
 - Negative gate driver voltage range for VGLX: AVEE+VCL ~ 2xAVEE-AVDD
 - Step-up 1 output voltage range for AVDD: 4.5 $\sim 6.5 V$
 - Step-up 2 output voltage range for AVEE: -4.5 \sim -6.5V
 - Positive gamma high voltage range for VGMP: 3.0 \sim 6.3V (AVDD-0.3V)
 - Positive gamma low voltage range for VGSP: 0.0, 0.3 \sim 3.7V
 - Negative gamma high voltage range for VGMN: -3.0 ~ -6.3V (AVEE+0.3V)
 - Negative gamma low voltage range for VGSN: 0.0, -0.3 ~ -3.7V
 - Common electrode voltage range for VCOM: 0.0 ~ -3.5V (VCL+0.3V)
 - Panel voltage range for VRGH: 1.0V ~ 6.0V(AVDD-0.3V)

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4 PIN DESCRIPTION

4.1 Power Supply Pins

Symbol	Name	Description
VDDB	DC/DC Power	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level
VDDA	Analog Power	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level
VDDR	Regulator Power	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
VDD_DET	Detection Power	Connect to VDDB/VDDA/VDDR for detection.
VDDAM	MIPI Power	Power supply for MIPI/MDDI analog regulator system
VDDI	I/O Power	Power supply for interface system except MIPI/MDDI interface
DVDD	Digital Voltage	Regulator output for logic system power (1.55V typical) Connect a capacitor for stabilization.
DIOPWR	Dual I/O Voltage	Regulator output for dual I/O voltage system (1.2V/1.8V typical). Connect a capacitor for stabilization.
MVDDA	MIPI/MDDI Voltage	Regulator output for internal MIPI/MDDI analog system (1.5V typical) Connect a capacitor for stabilization. If not use MIPI/MDDI interface, please open this pin.
MVDDL	MIPI Voltage	Regulator output for internal MIPI low power system (1.2V typical) Connect a capacitor for stabilization. If not use MIPI interface, please open this pin
VSSB	DC/DC GND	System ground for DC/DC converter
VSSA	Analog GND	System ground for analog system
VSSR	Regulator GND	System ground for regulator system
VSSAM	MIPI GND	System ground for internal MIPI/MDDI analog system
VSSI	I/O GND	System ground for interface system except MIPI/MDDI interface
DVSS	Digital GND	System ground for internal digital system
AVSS	Source OP GND	System ground for source OP system.
MTP_PWR	MTP Power	MTP programming power supply pin (7.5 to 8.0V and 7.75V typical) Must be left open or connected to DVSS in normal condition.



4.2 80-System Interface Pins

Symbol	I/O	Description
CSX	I	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. This pin is not used for I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
WRX / SCL / I2C_SCL	I	WRX: Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C_SCL: Serial input clock in I2C I/F. This pin is not used for MIPI I/F, please connect to VSSI this pin.
RDX	Ι	Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface. This pin is not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
D/CX	Ι	Display data / command selection in 80-series MPU I/F. D/CX = "0" : Command D/CX = "1" : Display data or Parameter This pin is not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F. For 8080-series MPU I/F: 8-bit interface: D[7:0] are used, D[23:8] should be connected to VSSI 16-bit interface: D[15:0] are used, D[23:16] should be connected to VSSI 24-bit interface: D[23:0] are used These pins are not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI these pins.

NOTE: "1" = VDDI level, "0" = VSSI level.

4.3 SPI /I2C Interface Pins

NOTE: "1" = VDDI level, "0" = VSSI level.			
4.3 SPI /I2C Interface Pins			
Symbol	I/O	Description	
CSX	11	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. This pin is not used for I2C, MIPI or MDDI I/F, please connect to VSSI this pin.	
WRX / SCL / I2C_SCL	I	Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C_SCL: Serial input clock in I2C I/F. This pin is not used for MIPI I/F, please connect to VSSI this pin.	
SDI / I2C_SDA	I/O	 SCL: Serial input signal in SPI I/F. The data is input on the rising/falling edge of the SCL signal. I2C_SDA: Serial input/output signal in I2C I/F. The data is input/output on the rising edge of the I2C_SCL signal. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin. 	
SDO	0	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. This pin is not used for 80-series MPU, I2C, MIPI or MDDI I/F, please open this pin.	

NOTE: "1" = VDDI level, "0" = VSSI level.



4.4 RGB Interface Pins

Symbol	I/O	Description
PCLK	I	Pixel clock signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
VS	I	Vertical sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
HS	I	Horizontal sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
DE	I	Data enable signal in RGB I/F mode 1. This pin is not used for RGB mode 2, 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F. For RGB I/F: 16-bit/pixel: D[20:16]=R[4:0], D[13:8]=G[5:0] and D[4:0]=B[4:0], connect unused pins to VSSI 18-bit/pixel: D[21:16]=R[5:0], D[13:8]=G[5:0] and D[5:0]=B[5:0], connect unused pins to VSSI 24-bit/pixel: D[23:16]=R[7:0], D[15:8]=G[7:0] and D[7:0]=B[7:0] These pins are not used for MIPI or MDDI I/F, please connect to VSSI these pins.

NOTE: "1" = VDDI level, "0" = VSSI level.

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4.5 MIPI/MDDI Interface Pins

Symbol	I/O	Description
HSSI_CLK_P HSSI_CLK_N	I	 These pins are DSI-CLK+/- differential clock signals if MIPI interface is used. These pins are MDDI_STB_P/M differential strobe signals if MDDI interface is used. HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.
HSSI_D0_P HSSI_D0_N	I/O	-These pins are DSI-D0+/- differential data signals if MIPI interface is used. -These pins are MDDI_DATA0_P/M differential strobe signals if MDDI interface is used. -HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.
HSSI_D1_P HSSI_D1_N	I	-These pins are DSI-D1+/- differential data signals if MIPI interface is used. -These pins are MDDI_DATA1_P/M differential strobe signals if MDDI interface is used. -HSSI_D1_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.
ERR	0	CRC and ECC error output pin for MIPI interface. This pin is output low when it is not activated. When this pin is activated, it output high if CRC/ECC error found. If not used, please open this pin.
LANSEL	ı n M	Input pin to select 1 data lane or 2 data lanes in MIPI/MDDI interface. LANSEL Data Lane of MIPI/MDDI 0 1 data lane 1 2 data lanes If not used, please connect to VSSI.
		Input pin to select HSSI_D0/D1 data lane sequence and polarity in high speed interface only. For MIPI interface, both DSWAP and PSWAP function are available. For MDDI interface, only PSWAP function is available. Please connect DSWAP pin to VSSI. Pin Name HSSI_D0_P_HSSI_D0_N_HSSI_CLK_P_HSSI_CLK_N_HSSI_D1_P_HSSI_D1_N
		DSWAP=0 DSI-D0+ DSI-D0- DSI-CLK+ DSI-CLK- DSI-D1+ DSI-D1-
DSWAP PSWAP	I	Input PSWAP=0 DSI-D0- DSI-D0+ DSI-CLK- DSI-CLK+ DSI-D1- DSI-D1+
		Image: Nine I DSWAP=1 Signal DSI-D1+ PSWAP=0 DSI-D1+ DSI-D1- DSI-CLK+ DSI-CLK- DSI-D0+
		DSWAP=1 PSWAP=1 DSI-D1- DSI-D1+ DSI-CLK- DSI-CLK+ DSI-D0- DSI-D0+
		If not used, please connect to VSSI.



4.6 Interface Logic Pins

Symbol	I/O	Description													
RESX	I	This signal will reset the device and must be applied to properly initialize the chip.Signal is active low.The input voltage range for RESX pin is related to DSTB_SEL and VSEL pins.Input Voltage Level (DSTB_SEL="0")Min.Max.UnitVDDI=1.65~3.3VLogic High level input voltage0.7xVDDIVDDIVDDI=1.65~3.3VLogic High level input voltageVSSI0.3xVDDIVVDDI=1.65~3.3VVDDIL=1.1~1.3VUnitVDDI=1.65~3.3VVDDIL=1.1~1.3VUnitVDDI=1.65~3.3VVDDIL=1.1~1.3VUnitVDDI=1.65~3.3VVDDIL=1.1~1.3VUnitVDDI=1.65~3.3VVDDIL=1.1~1.3VUnitVDDI=1.65~3.3VVDDIL=1.1~1.3VUnitVSELLogic High level input voltageVSSI0.3xVDDIVDDIVSELLogic High level input voltage0.7xVDDIVDDI1.1651.95VVSELLogic High level input voltage0.7xVDDIVDDI1.1651.95VVSELLogic High level input voltage <th col<="" td=""></th>													
TE (TE_L)	0	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low. If not used, please open this pin.													
TE_R		Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. The same output signal as TE (TE_L) pin. If not used, please open this pin.													
IM[3:0]		Interface type selection. The connections of IM[3:0] which not shown in table are invalid.IM[3:0]Display DataCommand000080-series 8-bit MPU I/F, D[7:0]80-series 8-bit MPU I/F, D[7:0]000180-series 16-bit MPU I/F, D[15:0]80-series 16-bit MPU I/F, D[15:0]001080-series 24-bit MPU I/F, D[23:0]80-series 24-bit MPU I/F, D[23:0]0011RGB I/F, D[23:0]16-bit SPI (SCL rising edge trigger), SDI/SDO1011RGB I/F, D[23:0]16-bit SPI (SCL falling edge trigger), SDI/SDO1010RGB I/F, D[23:0]12C I/F, I2C_SDA0101MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/NMIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N0110MDDI, HSSI_D0_P/N, HSSI_D1_P/NMDDI, HSSI_D0_P/N, HSSI_D1_P/N1110MDDI, HSSI_D0_P/N, HSSI_D1_P/N16-bit SPI (SCL falling edge trigger), SDI/SDO0111MDDI, HSSI_D0_P/N, HSSI_D1_P/NMDDI, HSSI_D0_P/N, HSSI_D1_P/N0111MDDI, HSSI_D0_P/N, HSSI_D1_P/N16-bit SPI (SCL rising edge trigger), SDI/SDO0111MDDI, HSSI_D0_P/N, HSSI_D1_P/N16-bit SPI (SCL falling edge trigger), SDI/SDO0111MDDI, HSSI_D0_P/N, HSSI_D1_P/N16-bit SPI (SCL falling edge trigger), SDI/SDO0111MDDI, HSSI_D0_P/N, HSSI_D1_P/N12C I/F, 12C_SDA serial data													
RGBBP	I	Display data written path control in RGB interface. RGBBP="0", display data written to frame memory. RGBBP="1", display data written to line buffer (frame memory by pass mode) When not used in other interfaces, please connect to VSSI.													



		Select the I2C	interface ad	dress fro	om MPU. If r	not used, please cor	nect to VS	SI.							
		I2C_SA0	I2C_SA0 Slave Address												
I2C_SA0	I	0			10011 00										
		1			10011 01										
		Input pin to sv	vitch the I/O v	oltage.	DECY TE I		(BBC pipe								
		The VSEL du	al IO function	is valid	when DSTB	SFL="1"	CDDC pins.								
							ut Voltage L	evel							
		DSTB_SEL	VDDI	VSEL	DIOPWR	'		LEDON							
								LEDPWM							
			1.65~3.3V				VO								
		0	or	Х	Off	VOL=VSSI	vo	L=VSSI							
			1.1~1.3V												
				Low	1.2V	VOI=VSSI	VO	=1.2V							
VSEL	I	1	1.65~3.3V		25	VOH=VDDI or DIC	PWR VO	H=VDDI or VDDA							
				High	1.80	VOL=VSSI	VO	L=VSSI							
					1.21/	VOH=1.2V	VO	H=1.2V							
		1	1.1~1.3V	Low		VOL=VSSI	VO	L=VSSI							
				High	1.8V	VOH=1.8V	VO	H=1.8V							
		The input velt	ao rango for			VOL=VSSI	VO	L=VSSI							
			age lange lo	VOLL	Min Max										
		Logic High le	evel input volt	age	.88 1 VD E										
	JI IT	Logic Low le	vel input volt	age V	SSI 0.55	5 V									
	2	If not used, pl	ease connect	to VDD	l.										
GPO[3:0]		General purpo	se output pir	ns. The c	output voltag	ge swing is VDDI to	VSSI.								
	0	If not used, pl	ease open th	ese pins	•										
VGSW[3:0]	I	Input pin to se	elect the differ	rent app	lication.										
		Input pin to se	elect the exter	mal AVE	D DC/DC v	oltage.									
		EXB1T		A	VDD Voltag	e									
EXB1T	I	0	l	Jse inter	nal DC/DC f	or AVDD									
		1		se exter	nal DC/DC 1	for AVDD									
		ii not used, pi	ease connect	10 055											
		Input pin to se	elect the volta	ge sequ	ence of V0 ·	~ V255.									
NBWSEL	1	NBWSEL		/0 ~ V25	55 voltage se										
		0	$V_{(00h)} > V_{(0)}$)1h)>>\	/(FEh)>V(FFh)	(Normally White)									
			V (00h) <v< b=""> (0</v<>)1h)<<\	V(FEh) < V(FFh)	(NOTTIAILY BIACK)									
		Input pin to co	ontrol DIOPW	R regula	ator on/off.										
DSTB SEL	1	DSTB_SEL	DIOP	WR Ree	gulator	VSEL Func	tion								
			D					4							
			D	IOPWR	UN	Valid		J							

NOTE: "1" = VDDI level, "0" = VSSI level.

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4.7 Driver Output Pins

Symbol	I/O	Description
S1 ~ S1440	0	Pixel electrode driving output.
GOUT1 ~ GOUT32	0	Gate control signals for panel. The swing voltage level is VGHO to VGLO
SDUM0~3	0	Dummy Source, leave it Open if not used
VGHO	0	High voltage level for gate control signals and gate circuit of panel.
VGLO	0	Low voltage level for gate control signals and gate circuit of panel.
LVGL	0	Low voltage level for gate circuit of panel.
VCOM	0	Regulator output for common voltage of panel. Connect a capacitor for stabilization.
NONA		EK CONFISURE DISCLOSURE

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4.8 DC/DC Converter Pins

Symbol	I/O	Description
AVDD	0	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
AVEE	0	Output voltage from step-up circuit 2, generated from VDDB. Connect a capacitor for stabilization.
VCL	0	Output voltage from step-up circuit 3, generated from VDDB. Connect a capacitor for stabilization.
VGH	0	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGLX	0	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
VGL	I	Substrate voltage for driver IC. Please connect VGL to VGLX.
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	0	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	0	Capacitor connection pins for the step-up circuit which generate AVEE. Connect capacitor as requirement. When not in used, please open these pins.
C31P, C31N C32P, C32N	0	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
C41P, C41N	6	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	0	Capacitor connection pins for the step-up circuit which generate VGLX. Connect capacitor as requirement.
VRGH	0	Output voltage generated from AVDD. Connect a capacitor for stabilization. When not in use, please open this pin.
VGL_REG	0	Output voltage generated from VGLX. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
EXTP	0	PFM1 control output for DC/DC converter to generate AVDD. Connect to gate of external NMOS device. When not in use, please open this pin.
EXTN	0	PFM2 control output for DC/DC converter to generate AVEE. Connect to gate of external PMOS device. When not in use, please open this pin.
CSP	Ι	Current sensing input for PFM1 DC/DC converter (generate AVDD). When not in use, please connect to VSSB.
CSN	Ι	Current sensing input for PFM2 DC/DC converter (generate AVEE). When not in use, please connect to VSSB.
VREF_PWR	0	Regulator output for power voltage. Connect a capacitor for stabilization.
VREFCP	0	Reference voltage for internal voltage generating circuit. Connect capacitor for stabilization.

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Symbol	I/O	Description
VGMP	0	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP	0	Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VGMN	0	Output voltage generated from AVEE. LDO output for negative gamma high voltage generator.
VGSN	0	Output voltage generated from AVEE. LDO output for negative gamma low voltage generator.

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4.9 LABC and CABC Control Pins

Symbol	I/O	Description
LEDON	0	This pin is connect to the external LED driver. It is a LED driver control signal which is used for turning ON/OFF the LED backlight. If not used, please open this pin.
LEDPWM	0	This pin is connect to the external LED driver. It is a PWM type control signal for brightness of the LED backlight. The width of LEDPWM signal is set from 256 values between 0% (Low) and 100% (High) If not used, please open this pin.



4.10 Test Pins

Symbol	I/O	Description
PADA1 PADA2 PADA3 PADA4 PADB1 PADB2 PADB3 PADB4	I/O	 These test pins for chip attachment detection. PADA1 to PADA4 are output pins and PADB1 to PADB4 are input pins. For normal operation: Connect PADA1 and PADB1 together by ITO trace. Connect PADA2 and PADB2 together by ITO trace. Connect PADA3 and PADB3 together by ITO trace. Connect PADA4 and PADB4 together by ITO trace.
CONTACT1A, CONTACT1B, CONTACT2A, CONTACT2B	I/O	- Test pin, for test bonding quality, IC internal will connect CONTACT1A with CONTACT1B, CONTACT2A with CONTACT2B
AVSS_AVDD	-	Test pin, must be connected to AVSS
AVEE_AVSS	-	Test pin, must be connected to AVEE
VCL_VDDB	Ι	Test pin, must be connected to VCL
VCL_AVSS	Ι	Test pin, must be connected to VCL
VGMN_VGMP	Ι	Test pin, must be connected to VGMN
VGSN_VGSP	Ι	Test pin, must be connected to VGSN
KBBC	0	Test pin, not accessible to user. Must be left open.
TEST0-7	1/0	Test pin, not accessible to user. Must be left open.
OSC_TEST	1/0	Test pin, not accessible to user, Must left open
VDDI_OPT1~2	0	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VSSI_OPT1	0	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VSSIDUM0~106	0	-These pins are dummy with VSSI potential (not have any function inside). -Signal traces can't pass through on glass under these pads.



5 FUNCTIONAL DESCRIPTION

5.1 MPU Interface

NT35510 can interface with MPU at high speed. However, if the interface cycle time is faster than the limit, MPU needs to have dummy wait(s) to meet the cycle time limit.

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in Table 5.1.1

IM2	IM1	IMO	SRAM	Register
0	0	0	80-series 8-bit MPU interface, D[7:0]	80-series 8-bit MPU interface, D[7:0]
0	0	1	80-series 16-bit MPU interface, D[15:0]	80-series 16-bit MPU interface, D[15:0]
0	1	0	80-series 24-bit MPU interface, D[23:0]	80-series 24-bit MPU interface, D[23:0]
0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL rising trigger
0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL falling trigger
1	0	0	RGB interface, D[23:0]	I2C interface, I2C_SDA serial data
1	0	1	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N
1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO serial data, SCL rising trigger
1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO serial data, SCL falling trigger
1	1	1	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N I2C interface, I2C_SDA serial data
"X" =	Don't	care.	TER DISCI	
	IM2 0 0 0 0 1 1 1 1 1 *X" =	IM2 IM1 0 0 0 1 0 1 0 1 0 1 1 0 1 1 1 1 1 1 1 1	IM2 IM1 IM0 0 0 0 0 0 1 0 1 0 0 1 1 0 1 1 0 1 1 1 0 1 1 1 0 1 1 0 1 1 1 1 1 1 1 1 1 *X" = Don't care. It care.	IM2 IM1 IM0 SRAM 0 0 0 80-series 8-bit MPU interface, D[7:0] 0 0 1 80-series 16-bit MPU interface, D[15:0] 0 1 0 80-series 24-bit MPU interface, D[23:0] 0 1 1 RGB interface, D[23:0] 0 1 1 RGB interface, D[23:0] 1 0 0 RGB interface, D[23:0] 1 0 1 MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N 1 1 0 MDDI, HSSI_D0_P/N, HSSI_D1_P/N 1 1 0 MDDI, HSSI_D0_P/N, HSSI_D1_P/N 1 1 1 MDDI, HSSI_D0_P/N, HSSI_D1_P/N *X" = Don't care

Table 5.1.1 Interface Type Selection

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5.1.2 80-series MPU Interface

The MCU uses an 11-wires 8-data or 19-wires 16-data or 27-wires 24-data parallel interface.

The chip-select CSX (active low) enables and disables the parallel interface. WRX is the parallel data write, RDX is the parallel data read and D[23:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[23:0] bits are display RAM data or command parameters. When D/C='0', D[23:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. Interface bus width can be selected with IM3,IM2, IM1 and IM0.

The interface functions of 80-series parallel interface are given in *Table 5.1.2.*

Table 5.1.2 Parallel interface function (80-Series)

IM3	IM2	IM1	IMO	Interface	D/CX	RDX	WRX	Function
					0	1	↑	Write 16-bit command, D[7:0]
0	0	0	0	8-bit Parallol	1	1	1	Write 16/18/24-bit display data or 16-bit parameter, D[7:0]
0	0	0	0	o-Dil Farallei	1	↑	1	Read 16/18/24-bit display data, D[7:0]
					1	1	1	Read 16-bit parameter or status, D[7:0]
					0	1	↑	Write 16-bit command, D[7:0]
0	0	0	4	16 bit Dorallal	1	1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[15:0]
0	0	0		TO-DIL Farallel	1	↑	1	Read 16/18/24-bit display data, D[15:0]
					1	↑	\mathbf{b}	Read 16-bit parameter or status, D[15:0]
					0	1	↑	Write 16-bit command, D[23:0]
0	0	4		24 hit Parallal		1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[23:0]
0	0	\sim		24-Dit Farallerd	1	↑	1	Read 16/18/24-bit display data, D[23:0]
						↑		Read 16-bit parameter or status, D[23:0]
P		۲ ۱		NO	D	le		



5.1.2.1 WRITE CYCLE SEQUENCE

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[23:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').



Fig. 5.1.2 80-Series parallel bus protocol, write to register or display RAM

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5.1.2.2 READ CYCLE SEQUENCE

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.



Fig. 5.1.4 80-Series parallel bus protocol, read from register or display RAM

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5.1.2.3 8-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	0	0	1	0	1	1	0	0	2Ch
Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	0	0	0	0	0	0	0	0	00h
23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	R 4	R3	R2	R1	R0	G5	G4	G3	65K Color
х	Х	х	х	х	х	х	х	х	х	х	х	х	х	х	Х	G2	G1	G0	B4	B 3	B2	B1	B0	05K-C0101
Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	R5	R4	R3	R 2	R1	R0	Х	Х	
Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	G5	G4	G3	G2	G1	G0	Х	Х	262K-Color
Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	B 5	B4	B3	B 2	B1	B 0	Х	Х	
Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	R 7	R6	R5	R 4	R 3	R2	R1	R0	
х	Х	Х	х	Х	Х	х	Х	Х	Х	х	х	Х	Х	х	Х	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color
х	х	х	Х	Х	х	Х	х	х	х	х	х	х	х	х	Х	B 7	B6	B5	B4	B 3	B2	B1	B 0	2
	23 (23 (23 ((((((((((((((23 D22 K X K X Z3 D22 K X K X K X K X K X K X K X K X K X K X K X K X K X	23 D22 D21 x x x x x x x3 D22 D21 x x x	23 D22 D21 D20 x x x x x x x x x x x x x3 D22 D21 D20 x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x	23 D22 D21 D20 D19 x x x x x x x x x x x3 D22 D21 D20 D19 x x x x x x3 D22 D21 D20 D19 x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x	23 D22 D21 D20 D19 D18 x x x x x x x x x x x x x x x3 D22 D21 D20 D19 D18 x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x	23 D22 D21 D20 D19 D18 D17 x x x x x x x x x x x x x x x x 23 D22 D21 D20 D19 D18 D17 x x x x x x x x 23 D22 D21 D20 D19 D18 D17 x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x	23 D22 D21 D20 D19 D18 D17 D16 x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x	23 D22 D21 D20 D19 D18 D17 D16 D15 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 x C x <	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 x </th <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 x</th> <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 x</th> <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 x<th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 x</th><th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 x</th><th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 x</th><th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 < x</th><th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 x</th><th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 x</th><th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 x<th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 c x</th></th></th>	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 x <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 x</th> <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 x</th> <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 x</th> <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 < x</th> <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 x</th> <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 x</th> <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 x<th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 c x</th></th>	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 < x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 x	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 x <th>23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 c x</th>	23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 c x

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NOTES:

- 1. 2 times transfer is used to transmit 1 pixel data with the 16-bit color depth information.
- 2. The most significant bits are Rx4, Gx5 and Bx4.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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NOTES:

- 1. 3 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
- 2. The most significant bits are Rx5, Gx5 and Bx5.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 16M colors, RGB is 8-8-8-bit pixel data input



NOTES:

- 1. 3 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.
- 2. The most significant bits are Rx7, Gx7 and Bx7.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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5.1.2.4 16-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

																			-						
Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	Х	Х	Х	Х	Х	Х	Х	Х	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	2C00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	Х	Х	Х	Х	Х	Х	Х	Х	R 4	R3	R 2	R1	R0	G5	G4	G3	G2	G1	G0	B 4	B 3	B2	B1	B0	65K-Color
	Х	Х	Х	Х	Х	Х	Х	Х	R 5	R4	R3	R2	R1	R0	Х	Х	G5	G4	G3	G2	G1	G0	Х	Х	
0006h	Х	Х	Х	Х	Х	Х	Х	Х	B5	B4	B3	B2	B1	B 0	Х	Х	R5	R4	R3	R 2	R1	R0	Х	Х	262K-Color
	Х	Х	Х	Х	Х	Х	Х	Х	G5	G4	G3	G2	G1	G0	Х	Х	B5	B 4	B3	B2	B1	B 0	Х	Х	
	Х	Х	Х	Х	Х	Х	Х	Х	R 7	R6	R5	R4	R 3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	
0007h	х	х	х	х	х	х	х	х	B 7	B6	B5	B4	B 3	B2	B1	B0	R 7	R6	R5	R 4	R3	R2	R1	R0	16.7M-Color
	х	х	х	х	х	х	х	Х	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B 3	B2	B1	B 0	

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- 1. In one transfer (D15 to D0), 1 pixel data transmitted with the 16-bit color depth information.
- 2. The most significant bits are Rx4, Gx5 and Bx4.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 1. 3 times transfer is used to transmit 2 pixel data or 2 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
- 2. The most significant bits are Rx5, Gx5 and Bx5.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 1. 3 times transfer is used to transmit 2 pixel data or 2 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.
- 2. The most significant bits are Rx7, Gx7 and Bx7.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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5.1.2.5 24-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	х	X	X	X	Х	х	Х	Х	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	2C00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	Х	Х	Х	Х	Х	Х	Х	Х	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B 4	B 3	B 2	B 1	B0	65K-Color
0006h	Х	Х	Х	Х	Х	Х	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B 4	B3	B 2	B1	B0	262K-Color
0007h								R0	G7	G6	G5	G4	G3	G2	G1	G0	B 7	B6	B5	B4	B 3	B2	B1	B 0	16.7M-Color

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- 1. In one transfer (D15 to D0), 1 pixel data transmitted with the 16-bit color depth information.
- 2. The most significant bits are Rx4, Gx5 and Bx4.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 2. The most significant bits are Rx5, Gx5 and Bx5.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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- 16M colors, RGB is 8-8-8-bit pixel data input



- 1. In one transfer (D23 to D0), 1 pixel data transmitted with the 24-bit color depth information.
- 2. The most significant bits are Rx7, Gx7 and Bx7.
- 3. The least significant bits are Rx0, Gx0 and Bx0.

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5.1.2.6 8-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	0	0	1	0	1	1	1	0	2Eh
Command	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	0	0	0	0	0	0	0	0	00h
	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
Read	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	R 7	R6	R 5	R 4	R3	R 2	R1	R0	
Data	х	Х	Х	х	Х	Х	х	х	х	х	Х	Х	х	х	Х	х	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color
	х	Х	Х	х	Х	Х	х	х	х	х	Х	Х	х	х	Х	х	B 7	B6	B5	B4	B 3	B2	B1	B0	



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5.1.2.7 16-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

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Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	Х	Х	Х	Х	Х	Х	Х	Х	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	2E00h
Road	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
Data	Х	Х	Х	Х	Х	Х	Х	Х	R 7	R6	R5	R 4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16 7M-Color
Data	х	Х	х	х	х	х	х	х	B7	B6	B5	B4	B 3	B2	B1	B 0	х	х	х	х	х	х	х	Х	10.7 10-00101



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5.1.2.8 24-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

Register	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Command	х	Х	х	х	х	х	х	х	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	2E00h
Read	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
Data								R0	G7	G6	G5	G4	G3	G2	G1	G0	B 7	B6	B5	B 4	B3	B2	B1	B0	16.7M-Color



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5.1.3 Serial Interface

The selection of this interface is done by IM3, IM2, IM1 and IM0.

The serial interface can select IM3 = 0 or 1 to decide the trigger edge of serial clock (SCL) is rising edge or falling edge. The serial interface is used to communication between the micro controller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

5.1.3.1 WRITE MODE

The write mode of the interface means the micro controller writes commands and data to the NT35510. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low (see *Fig. 5.1.5*). SDI/SDO are sampled at the rising edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

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Fig. 5.1.5 Serial bus protocol for register write mode

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5.1.3.2 READ MODE

The read mode of the interface means that the micro controller reads register value from the NT35510. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send (see *Fig. 5.1.6*). The NT35510 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. For the memory data read, a dummy clock cycle is needed (16 SCL clocks) to wait the memory data send out in SPI interface. But it doesn't need any dummy clock when execute the command data read.

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Fig. 5.1.6 Serial bus protocol for register read mode

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5.1.3.3 SERIAL INTERFACE FOR DATA RAM WRITE

The serial interface is used with RGB interface (IM[2:0]="011") or MDDI interface (IM[2:0]="110"). In RGB+SPI interface, the data RAM write function for SPI is valid when bit ICM="1" (command B300h of page 0). In MDDI+SPI interface, the data RAM write function for SPI is valid when MDDI is not writing data to RAM. Different display data formats are available for three color depths supported by the LCM listed below:

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- 65K colors, RGB is 5-6-5-bit pixel data input (parameter of command 3A00h is 0x0005)

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- 262K colors, RGB is 6-6-6-bit pixel data input (parameter of command 3A00h is 0x0006) First Transmit s P Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) տուրուներուներ านน SCL (Host to Driver IC) (Falling Edge, IM3 = 1) lll SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z Command / Address and / Address Transmission d / Address High Byte Trans 8-bit 8-bit Second Transmit Transmission Byte Transmission Byte PS CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) տուրուներուներուներ ENIL SDI (Host to Driver IC) R/W D/CX H/L 0 SDO (Driver IC to Host) High-Z High-Z High-Z R/W = 0 for Writing 0 D/CX = 0 for Comma H/L = 0 for Comman and / Address Transmission nird Transmit (Red) PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z W = 0 for Writing HAM Data CX = 1 for RAM Data Transmission L = 0 for RAM Data Low Byte Transm Fourth Transmit (Green) PS smission Byte Trans CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) lll SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z ata Transmission ta Low Byte Trans 8-bit ifth Transmit (Blue) s PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) JIII (Rising Edge, IM3 = 0, SCL (Host to Driver IC) (Falling Edge, IM3 = 1) าบบา SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z R/W = 0 for Writing RAM Data D/CX = 1 for RAM Data Transmission H/L = 0 for RAM Data Low Byte Transmis 8-bit Transmission Byte Transmission Byte PS CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) าบบ $1 \Box \Box \Box$ SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z H/W = 0 for Writing HAM Data D/CX = 1 for RAM Data Transmission H/L = 0 for RAM Data Low Byte Transr

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First Transmit PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) տուրուներուներ านน SCL (Host to Driver IC) (Falling Edge, IM3 = 1) lll SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z Command / Address and / Address Transmission d / Address High Byte Trans 8-bit 8-bit Second Transmit Transmission Byte Transmission Byte PS CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) տուրուներուներուներ ENIL SDI (Host to Driver IC) R/W D/CX H/L 0 SDO (Driver IC to Host) High-Z High-Z High-Z R/W = 0 for Writing 0 D/CX = 0 for Comma H/L = 0 for Comman and / Address Transmission nd / Address Low Byte Trans nird Transmit (Red) PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z W = 0 for Writing RAM Data CX = 1 for RAM Data Transmission _ = 0 for RAM Data Low Byte Transm Fourth Transmit (Green) PS mission Byte Tran CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) TTTT. SCL (Host to Driver IC) (Falling Edge, IM3 = 1) lll SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z ata Transmission ta Low Byte Trans 8-bit ifth Transmit (Blue) s PS Transmission Byte Transmission Byte CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) JIII (Rising Edge, IM3 = 0, SCL (Host to Driver IC) (Falling Edge, IM3 = 1) าบบา SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z High-Z R/W = 0 for Writing RAM Data D/CX = 1 for RAM Data Transmission H/L = 0 for RAM Data Low Byte Transmi 8-bit Transmission Byte Transmission Byte PS CSX (Host to Driver IC) SCL (Host to Driver IC) (Rising Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM3 = 1) าบบ $1 \Box \Box \Box$ SDI (Host to Driver IC) SDO (Driver IC to Host) High-Z High-Z High-Z H/W = 0 for Writing HAM Data D/CX = 1 for RAM Data Transmission H/L = 0 for RAM Data Low Byte Transr

- 16.7M colors, RGB is 8-8-8-bit pixel data input (parameter of command 3A00h is 0x0007)

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5.1.3.4 SERIAL INTERFACE FOR DATA RAM READ

The read data RGB is 8-8-8-bit output as below.



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5.2 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I2C_SDA) and the Serial Clock Line (I2C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I2C-Bus Protocol:

Before any data is transmitted on the I2C-bus, the device, which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.



(b) Definitions:

- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



Fig. 5.2.2 System Configuration



5.2.1 Slave Address of I2C

NT35510 supports two slave addresses, 1001100, 1001101 after the START procedure via I2C bus for MCU usage .There are 1 hard pin, I2C_SA0 to determine the difference slave address. The slave address selection is described as the following table. The I2C interface address is selected from the external MPU.

I2C_SA0	Slave Address	Notes
0	1001100	0000xxx and 1111xxx: Reversed
1	1001101	

Table 5.2.1 Selection Table of Slave Address

5.2.2 Register Write Sequence of I2C Interface

NT35510 supports register write sequence via I2C-bus transfer. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in Fig.5.2.2.

- (2) After the START condition (S), a slave address is sent. R/W bit is setting to "zero" for WRITE.
- (3) The slave issues an ACK to master.
- (4) 16 bits register high byte address transfer first. Then transfer the register low byte address.
- (5) 16 bits register high byte data of parameter transfer first. Then transfer the register low byte data parameter.
- (6) A data transfer is always terminated by a STOP condition.



5.2.3 RAM Data Write Sequence of I2C Interface

NT35510 supports sequential RAM data writing via I2C-Bus. NT35510 will increase the RAM address automatic by window address when the Host MCU write the RAM data via this way. The transfer protocol of window address setting can refer to the 5.2.3 Register Write Sequence. Different display data formats are available for three color depths supported by the LCM.

The sequential RAM writing timing is shown in below.





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5.2.4 Register Read Sequence of I2C Interface

NT35510 supports register read sequence via I2C-bus transfer. Register data reading transfers follow the format and is shown in Fig.5.2.4.



Register Write Sequence. Then the master MCU need to send the BAM data read register "2E00h" to NT35510. And finally, the MCU can send the following RAM data reading timing to feedback single RAM data value by one complete I2C packet.

The RAM data reading timing is shown in below.





W: Write Bit, where W="0" R: Read Bit, where R="1" ACK: Acknowledge Bit, where ACK="0" NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address

ADD[15:0]: Register Address, where ADD[15:0]="0x2E00" R1[4:0], R2[4:0], ..., Rn[4:0]: The red color data of each pixel G1[5:0], G2[5:0], ..., Gn[5:0]: The green color data of each pixel B1[4:0], B2[4:0], ..., Bn[4:0]: The blue color data of each pixel

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W: Write Bit, where W="0" R: Read Bit, where R="1" ACK: Acknowledge Bit, where ACK="0" NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address

ADD[15:0]: Register Address, where ADD[15:0]="0x2E00" R1[5:0], R2[5:0], ..., Rn[5:0]: The red color data of each pixel G1[5:0], G2[5:0], ..., Gn[5:0]: The green color data of each pixel B1[5:0], B2[5:0], ..., Bn[5:0]: The blue color data of each pixel

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NACK: Non-acknowledge Bit, where NACK="1"

G1[7:0], G2[7:0], ..., Gn[7:0]: The green color data of each pixel B1[7:0], B2[7:0], ..., Bn[7:0]: The blue color data of each pixel

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5.3 Interface Pause

By using parallel interface, it is possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the CSX (Chip Select Line) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then NT35510 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the CSX (Chip Select Line) is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the CSX (Chip Select Line) is next enabled as shown below.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

Parallel Interface Pause



Serial Interface Pause

16-bit SPI interface does not support "Pause Mode"

MIPI Interface Pause

Pause can be done on DSI between Packets when they are sent to same or different receiver (Virtual Channel (VC)) e.g.

1) Same receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => ...

2) Different receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => ...

The means that "=>" symbol means a pause on DSI.

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5.4 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example (See *Fig. 5.4.1*)

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example (See *Fig. 5.4.2*)



Fig. 5.4.2 Serial bus protocol, write mode – interrupted by CSX



Display data transfer break is illustrated for reference purposes below. Without break



With break (See and check also exceptions*)



*) See also an exception on section "6.1 User Command Set" and Note 2.

The MCU can create a break condition when it is forcing DSI data lanes in the LP-11 mode

The NT35510 stops to control DSI data lanes (change from a transmitter mode to a received mode) if it was controlling DSI data lanes as a transmitter when the MCU is forcing DSI data lanes in the LP-11.

The break condition can be done any time when the MCU or the driver IC is controlling DSI data lanes e.g. the driver IC is sending data to the MCU.

Except MIPI interface, the data transfer break mechanism illustrated for reference purposes below.





5.5 Display Module Data Transfer Modes

The NT35510 has 3 kinds of color mode for transferring data to the frame Memory. There are 16-bit color per pixel, 18-bit color per pixel and 24-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

Start					Stop									
Start Frame Memory Write	Image Data Frame 1	Image Data Frame 2	Image Data Frame 3	•••••	Any Command	7								
	Fig. 5.5.1 Data Transfer Method 1													

Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



- 1) The Frame Memory can contain odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.
- 2) "Memory Write Continue (3Ch)" or "Memory Read Continue (3Eh)" commands are not stopping writing or reading to/from the frame memory. These commands can be used if there is wanted to continue the writing or reading to/from the frame memory when "Any Command" has stopped the memory writing or reading.

3) "Any Command" can be as same as "Start Frame Memory Write".





5.6 RGB Interface

5.6.1 General Description

For direct interface with both graphic controller and MPU, NT35510 offer RGB interface mode to display video signal. The parallel RGB interface includes: VS, HS, DE, PCLK, D[23:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[23:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative ("0", low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative ("0", low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a positive ("1", high) active and its state is read to the display module by a rising edge of the PCLK signal. D[23:0] (24-bit: R7-R0, G7-G0 and B7-B0;18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE= "1" and there is a rising edge of PCLK). D[23:0] can be "0" (low) or "1" (high). These lines are read by a rising edge of the PCLK signal.



Note: PCLK is an unsynchronized signal (It can be stopped)

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5.6.2 RGB Interface Timing Chart

The image information must be correct on the display, when the timings are in range on the interface.

However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.





5.6.3 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	D23-D0	VS	HS	Register VFP[7:0], VBP[7:0] HFP[7:0], HBP[7:0]
RGB Mode 1 (SYNC + DE)	Used	Used	Used	Used	Used	Not used
RGB Mode 2 (SYNC only)	Used	Not used	Used	Used	Used	Used

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D23 to D0), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to NT35510 DDI.

In RGB Mode 2, back porch of Vsync VBP is defined by VBP[7:0] of RGBCTR command. And back porch of Hsync HBP is defined by HBP[7:0] of RGRCTR command. Front porch of Vsync VFP is defined by VFP[7:0] of RGBCTR command. And front porch of Hsync HFP is defined by HFP[7:0] of RGBCTR command.

Note: VBP[7:0]=Vsync+VBP and HBP[7:0]=Hsync+HBP.

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Fig. 5.6.2 Video signal data writing method in RGB Mode 1 Interface

Notes:

1. Constraint:

V-Back Porch (Vsync+VBP) ≥ 5 HS lines, V-Front-Borch (VFP) ≥ 2 HS lines Vsync+VBP+VFP (porch of RGB signal) > VBPA/B/C[7:0] (internal display back porch) H-Back Porch (Hsync+HBP) ≥ 5 PCLK clocks, H-Front-Porch (HFP) ≥ 2 PCLK clocks 2. $t_{VHS} \ge 400$ ns

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Fig. 5.6.3 Video signal data writing method in RGB Mode 2 Interface

Notes:

1. Constraint:

V-Back Porch (VBP[7:0]) \geq 5 HS lines, V-Front Porch (VFP[7:0]) \geq 2 HS lines VBP[7:0]+VFP[7:0] (porch of RGB signal) > VBPA/B/C[7:0] (internal display back porch) H-Back Porch (HBP[7:0]) \geq 5 PCLK clocks, H-Back Porch (HFP[7:0]) \geq 2 PCLK clocks 2. $t_{VHS} \geq$ 400ns

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Fig. 5.6.5 RGB with SPI Timing Sequence (Exit Internal Clock Mode, ICM="0")

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5.6.4 RGB Interface Bus Width Set

All 3-kinds of bus width can be available during RGB interface mode (selected by the COLMOD command (3A00h): VIPF[3:0]).

3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus Width
50h	х	х	х	R 4	R3	R 2	R1	R0	х	х	G5	G4	G3	G2	G1	G0	х	х	х	B 4	B 3	B 2	B1	B 0	16-bit data
60h	х	х	R5	R4	R3	R2	R1	R0	х	х	G5	G4	G3	G2	G1	G0	х	х	B5	B 4	B 3	B2	B1	B0	18-bit data
70h	R 7	R6	R5	R 4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B 7	B6	B 5	B 4	B 3	B2	B1	B0	24-bit data
NOTEO																									

NOTES:

1. "x": Unused RGB data bus connected with VSSI.

2. R0 is the LSB for the red component; G0 is the LSB for the green component, etc.

3. For 16-bit pixels, R primary color MSB is R4, G primary color MSB is G5 and B primary color MSB is B4.

4. For 18-bit pixels, R primary color MSB is R5, G primary color MSB is G5 and B primary color MSB is B5

5. For 24-bit pixels, R primary color MSB is R7, G primary color MSB is G7 and B primary color MSB is B7

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Write data for 16-bit RGB interface bus width set is shown below.

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Write data for 18-bit RGB interface bus width set is shown below.

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VS	"1"
HS	"1"
DE	"1"
PCLK	
D23	R1 Rit 7 R2 Rit 7 R3 Rit 7 R0 Rit 7
D22	R1. Bit 6 R2. Bit 6 R3. Bit 6 R3. Bit 6
 D21	R1, Bit 5 R2, Bit 5 R3, Bit 5 R1, Bit 5
D20	R1, Bit 4 R2, Bit 4 R3, Bit 4 R1, Bit 4
D19	R1, Bit 3 R2, Bit 3 R3, Bit 3 Rn, Bit 3
D18	R1, Bit 2 R2, Bit 2 R3, Bit 2 R1, Bit 2
D17	R1, Bit 1 R2, Bit 1 R3, Bit 1 R1, Bit 1
D16	R1, Bit 0 R2, Bit 0 R3, Bit 0 Rn, Bit 0
D15	G1, Bit 7 G2, Bit 7 G3, Bit 7 Gn, Bit 7
D14	G1, Bit 6 G2, Bit 6 G3, Bit 6 G1, Bit 6 G1, Bit 6
D13	G1, Bit 5 G2, Bit 5 G3, Bit 5 Gn, Bit 5
D12	G1, Bit 4 G2, Bit 4 G3, Bit 4 Gn, Bit 4
D11	G1, Bit 3 G2, Bit 3 G3, Bit 3 G1, bit 3 G1, bit 3
D10	G1, Bit 2 G2, Bit 2 G3, Bit 2 G1, Bit 2 G1, Bit 2
	G1, Bit 1 G2, Bit 1 G3, Bit 1 G1, Bit 1 G1, Bit 1
D8	G1, Bit 0 G2, Bit 0 G3, Bit 0 Gn, Bit 0
D7	B1, Bit 7 B2, Bit 7 B3, Bit 7 Bn, Bit 7
D6	B1, Bit 6 B2, Bit 6 B3, Bit 6 Bn, Bit 6
DS	B1, Bit 5 B2, Bit 5 B3, Bit 5 Bn, Bit 5
	B1, Bit 4 B2, Bit 4 B3, Bit 4 Bn, Bit 4
	B1, Bit 3 B2, Bit 3 B3, Bit 3 Bn, Bit 3
	B1, Bit 2 B2, Bit 2 B3, Bit 2 Bn, Bit 2
D1	B1, Bit 1 B2, Bit 1 B3, Bit 1 Bn, Bit 1
D0	B1, Bit 0 B2, Bit 0 B3, Bit 0 Bn, Bit 0
-	Pixel 1 Pixel 2 Pixel 3 Pixel n
	Д

Write data for 24-bit RGB interface bus width set is shown below.

R1[7] R1[6] R1[5] R1[4] R1[3] R1[2] R1[1] R1[0] G1[7] G1[6] G1[5] G1[4] G1[3] G1[2] G1[1] G1[0] B1[7] B1[6] B1[5] B1[4] B1[3] B1[2] B1[1] B1[0]



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5.7 Frame Memory

5.7.1 Configuration

The NT35510 has an integrated 480 x 864 x 24-bit graphic type static RAM. This 9,953,280-bit memory allows to store on-chip a 480 x RGB x 864, 480 x RGB x 854, 480 x RGB x 800, 480 x RGB x 720 and 480 x RGB x 640 image with an 24-bit resolution (16.7M-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.





5.7.2 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 1-1-1-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The address pointers address the locations of RAM.

When CGM[7:0]="70h", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=863 (35Fh).

When CGM[7:0]="6Bh", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=853 (355h).

When CGM[7:0]="50h", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=799 (31Fh).

When CGM[7:0]="28h", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=719 (2CFh).

When CGM[7:0]="00h", the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=639 (27Fh).

Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example, the whole display contents will be written when CGM[7:0]="50h", if the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=479 (1DFh), YE=799 (31Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET" and "MADCTR" (see section 6 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 5.2.2 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

Condition **Column Counter Row Counter** Return to Return to When RAMWR/RAMRD command is accepted "Start Row (YS)" "Start Column (XS)" Twice Increment by 1 Complete Pixel Pair Read / Write action No change (First Pixel n then Pixel n+1) Return to The Column counter value is larger than "End Column (XE)" Increment by 1 "Start Column (XS)" The Column counter value is larger than "End Column (XE)" Return to Return to and the Row counter value is larger than "End Row (YE)" "Start Column (XS)" "Start Row (YS)" NOTE:

For each image condition, the controls for the column and row counters apply as below:

Data is always written to the Frame Memory in the order, regardless of the Memory Write Direction set by command MADCTL (36h) bit MY, MX and MV. The write order for each pixel unit is (R, G, B) transferred from (D2, D1, D0) = (R, G, B). One pixel unit represents 1 column and 1 page counter value on the Frame Memory



5.7.3 Interface to Memory Write Direction

The resultant image for each orientation setting is illustrated below.



NOTE: MV=D5 parameter of MADCTL command, MX=D6 parameter of MADCTL command, MY=D7 parameter of MADCTL command

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5.7.4 Frame Memory to Display Address Mapping

The frame memory to display address mapping for 480RGB x 864 resolution (RSMX=RSMY="0") is shown below figure. The maximum address of RA/SA/CA and used source outputs are decided by bit CGM[2:0] (see command 2Ah CASET, 2Bh PASET and section 7.2).



RA = Row Address,

CA = Column Address,

SA = Scan Address,

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

PTD = Source output voltage selection for 1-bit data "0" and "1", parameter of PWCTR5 command

* RA and CA is exchange when MV = "1"

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5.8 Tearing Effect Information

5.8.1 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.8.1.1 TEARING EFFECT LINE MODES

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh = The LCD display is not updated from the Frame Memory

tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.



thdh = The LCD display is not updated from the Frame Memory thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 3, this mode turn on the Tearing Effect Output signal when vertical scanning reaches line N.



N = The N-th scanning line which set by register N[15:0] of command STESL (44h)

The TE mode selection is described as below table

DOPCTR (B100h)	TEOFF (34h) TEON (35h)	STESL (44h)	TE Output
DSITE	M	N[15:0]	
0	X	Х	TE off (output low)
1	34h	Х	TE off (output low)
1	35h with M=0	N[15:0]=0	TE high in V-porch region (Mode 1)
1	35h with M=0	N[15:0]≠0	TE high at N-th line (Mode 3)
1	35h with M=1	Х	TE high in all V-porch and H-porch region (Mode 2)

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5.8.1.2 TEARING EFFECT LINE TIMING

The Tearing Effect signal is described below:



Table 5.8.1 AC characteristics of Tearing Effect Signal

Symbol	Parameter	min	max	unit	Description
tvdl	Vertical Timing Low Duration	TBD		ms	
tvdh	Vertical Timing High Duration	1000		μs	124
thdl	Horizontal Timing Low Duration	TBD		μs	
thdh	Horizontal Timing High Duration	TBD	500	μs	

Notes: 1. The timings in above table apply when MADCTL ML=0 and ML=1.

2. The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns when the maximum load is TBD Ω .

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

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5.8.1.3 EXAMPLE 1: MPU WRITE IS FASTER THAN PANEL READ.



Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



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5.8.1.4 EXAMPLE 2: MPU WRITE IS SLOWER THAN PANEL READ.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



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5.9 Checksum

The display module consists of two 8-bit checksum registers, which are used checksum calculations for "User Command Set" area registers (includes the frame memory), on the display module.

One of the checksum registers is "First Checksum" (FCS) and another is "Continue Checksum" (CCS).

These register values are set to 00h as an initial value when there is started to calculate a new checksum.

The display module is starting to calculate the new checksum after there is a write access on "User Command Set" area registers. This means that read commands are not used as a calculation starting trigger in this case.

The checksum calculation is always interrupted, when there is a new write access on Nokia area registers. The checksum calculation is also started from the beginning.

The result of the first finished checksum calculation is stored on the FCS register, which value is kept until there is the new write access on "User Command Set" area registers and the new checksum value is calculated in the first time again.

The maximum time, when the FCS is readable, is 150ms after there is the last write access on "User Command Set" area registers.

The checksum calculation is continuing after the finished first checksum calculation where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value is replaced a new one) after the last Nokia area register has been calculated to the checksum.

The maximum time, when the CCS is readable in the first time, is 300ms after there is the last write access on "User Command Set" area registers.

There is always updated a checksum comparison bit (See section: "Read Display Self-Diagnostic Result (0Fh)" and bit D0) when there is compared FCS and CCS checksums after a new checksum value is stored on CCS.

The maximum time, when the comparison has been done between FCS and CCS in the first time, is 300ms then the comparison has been done in every 150ms (this is maximum time).

User can read FCS, CCS and Comparison bit D0 values. See section: "Read First Checksum (AAh)", "Read Continue Checksum (AFh)" and "Read Display Self-Diagnostic Result (0Fh)".

There can be an overflow during a checksum calculation. These overflow bits are not needed to store anywhere. This means that these overflow bits can be ignored by the display module.

An example of the checksum calculation:

- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function is only running in "Sleep Out" mode and it is stopped in "Sleep In" mode.



Step Note1	Time Note2	Action	Temporary Register	First Checksum Register (FCS)	Continue Checksum Register (CCS)	Comment
1	0	Initialization	Set to 00h	Set to 00h	Set to 00h	The last write action on "User Command Set" area registers => FCS an CCS registers are initialized
2	0 150ms	Continue sum of "User Command Set" area registers	Counting	-	-	The first register counting is running
3	150ms	Stores sum of registers on FCS register	Set to 00h after value is moved to FCS register	Stores sum of "User Command Set" area registers on FCS register	-	The result of the first register counting is stored on FCS register. The result of the FCS is available to the MPU
4	150ms 300ms	Continue sum of "User Command Set" area registers	Counting			The second register counting is running
5	300ms	 Stores sum of registers on CCS register Compares stored FCS and CCS value 	Set to 00h after value is moved to CCS register		Stores sum of "User Command Set" area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
6	300ms 450ms	Continue sum of "User Command Set" area registers	Counting	SU		The third register counting is running
7	450ms	 Stores sum of registers on CCS register Compares stored FCS and CCS value 	Set to 00h after value is moved to CCS register		Stores sum of "User Command Set" area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
8	450 600ms	Continue sum of "User Command Set" area registers	Counting	-	_	The fourth register counting is running
9	600ms	 Stores sum of registers on CCS register Compares stored FCS and CCS value 	Set to 00h after value is moved to CCS register	-	Stores sum of "User Command Set" area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
10	etc	-	-	-	-	Same sequence continue e.g. step 4 and 5

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5.10 Power On/Off Sequence

VDDI and VDD (VDDA) can be applied in any order.

VDD (VDDA) and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD (VDDA) and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD (VDDA) can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. *Notes:*

- 1. There will be no damage to the display module if the power sequences are not met.
- 2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
- 3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
- 4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.10.1 and 5.10.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
- 5. There is not a limit for Rise/Fall time on VDDI and VDD (VDDA).
- The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 5ms after LP-11 (Clock and Data Channels), VDDI and VDD (VDDA) are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.



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5.10.1 Case 1 – RESX line is held High or Unstable by Host at Power On

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD (VDDA) and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.





5.10.2 Case 2 – RESX line is held Low by host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD (VDDA) and VDDI have been applied.



5.10.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.



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5.11 Power Level Modes

5.11.1 Definition

7 level modes are defined they are in order of maximum power consumption to minimum power consumption:

- 1. Normal Mode On (full display), Idle Mode Off, Sleep Out. In this mode, the display is able to show maximum 16.7M colors.
- Partial Mode On, Idle Mode Off, Sleep Out In this mode, part of the display is used with maximum 16.7M colors.
- 3. Normal Mode On (full display), Idle Mode On, Sleep Out. In this mode, the full display is used but with 8 colors.
- 4. Partial Mode On, Idle Mode On, Sleep Out In this mode, part of the display is used but with 8 colors.
- 5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.

6. Deep Standby Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory is random.

7. Power Off Mode

In this mode, VDDI and VDDA/VDDR/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

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5.11.2 Power Level Mode Flow Chart



NOTES:

There is not any abnormal visual effect when there is changing from one power mode to another power mode.
 There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode



The following table represents the SRAM and Registers its mode state. Control Mode SRAM Register Enter Exit Sleep in mode 1 (RAMKP = 1) Keep Keep Command Sleep in mode 2 (RAMKP = 0) Command Loss Keep Command Deep-standby mode Loss Reset pin Loss Keep Reset=L Reset (H/W) Loss (Default Value) The condition for irregular power off mode is shown below. VDDI VDD RESX **Power Off Mode** I/O Mode 1 ON OFF High or Low Low Mode 2 OFF ON High or Low Low Note: VDD means VDDA, VDDR, VDDB and VDDAM Power Off Condition VDD ON VDDOFF VDD ON VDDI ON VDDI OFF VDDION If VDD turned off If VDDI turned off Power-OFF Mode1 Power-OFF Mode2 Sleep-In Mode If VDDI turned on If VDD turned on

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5.12 Reset function

5.12.1 Register Default Value

Table 5.12.1 Default Values for User Command Set

	ltom	After	After	After	
	Item	Power On	Hardware Reset	Software Reset	
RDNUMPE (05h	ו)	00h	00h	00h	
RDDPM (0Ah)		08h	08h	08h	
RDDMADCTR (0Bh)	00h	00h	00h	
RDDCOLMOD ((0Ch)	07h	07h	07h	
RDDIM (0Dh)		00h	00h	00h	
RDDSM (0Eh)		00h	00h	Dooh	
RDDSDR (0Fh)		00h	00h	00h	
Sleep In/Out (10)h/11h)	In	In	In In	
Partial/Normal E	Display (12h/13h)	Normal	Normal	Normal	
Display Inversio	n On/Off (21h/20h)	Off	Off	Off	
All Pixel On/Off	(23h/22h)	Qff	Off	Off	
Gamma setting	(26h)	01h (GC0)	01h (GC0)	01h (GC0)	
Display On/Off ((29h/28h)	Off	Off	Off	
Column: Start A	ddress (XS, 2Ah)	0000h	0000h	0000h	
	CGM[7:0]="70h" (480x864)	01DFh (479d)	01DFh (479d)	01DFh (479d)	
Column:	CGM[7:0]="6Bh" (480x854)	01DFh (479d)	01DFh (479d)	01DFh (479d)	
End Address	CGM[7:0]="50h" (480x800)	01DFh (479d)	01DFh (479d)	01DFh (479d)	
(XE, 2Ah)	CGM[7:0]="28h" (480x720)	01DFh (479d)	01DFh (479d)	01DFh (479d)	
	CGM[7:0]="00h" (480x640)	01DFh (479d)	01DFh (479d)	01DFh (479d)	
Row: Start Addr	ess (YS, 2Bh)	0000h	0000h	0000h	
V	CGM[7:0]=*70h" (480x864)	035Fh (863d)	035Fh (863d)	035Fh (863d)	
Row:	CGM[7:0]="6Bh" (480x854)	0355h (853d)	0355h (853d)	0355h (853d)	
End Address	CGM[7:0]="50h" (480x800)	031Fh (799d)	031Fh (799d)	031Fh (799d)	
(YE, 2Bh)	CGM[7:0]="28h" (480x720)	02CFh (719d)	02CFh (719d)	02CFh (719d)	
	CGM[7:0]="00h" (480x640)	027Fh (639d)	027Fh (639d)	027Fh (639d)	
Frame memory	(2Ch, 2Eh, 3Ch, 3Eh)	Random	Random	Random	
Partial: Start Ad	dress (PSL, 30h)	0000h	0000h	0000h	
	CGM[7:0]="70h" (480x864)	035Fh (863d)	035Fh (863d)	035Fh (863d)	
Partial:	CGM[7:0]="6Bh" (480x854)	0355h (853d)	0355h (853d)	0355h (853d)	
End Address	CGM[7:0]="50h" (480x800)	031Fh (799d)	031Fh (799d)	031Fh (799d)	
(PEL, 30h)	CGM[7:0]="28h" (480x720)	02CFh (719d)	02CFh (719d)	02CFh (719d)	
	CGM[7:0]="00h" (480x640)	027Fh (639d)	027Fh (639d)	027Fh (639d)	
Tearing: On/Off	(35h/34h)	Off	Off	Off	



ltom		After	After	After
Item		Power On	Hardware Reset	Software Reset
Memory Data Access Contr	ol (36h)	00h	00h	00h
(MY/MX/MV/ML/RGB/MH/R	SMX/RSMY)	0011	0011	0011
Idle Mode On/Off (38h/39h)		Off	Off	Off
Interface Pixel Color Forma	t (3Ah)	77h	77h	77h
Set Tearing Effect Scan Lin	e (44h)	0000h	0000h	0000h
Get Scan Line (45h)		N/A	N/A	N/A
DSTB mode (4Fh)		00h	00h	00h
Profile Value for Display (50)h)	All values are FFh	All values are FFh	All values are FFh
Display Brightness (51h, 52	h)	00h	00h	00h
CTRL Display (53h, 54h)		00h	00h	00h
CABC Control (55h, 56h)		00h	00h	00h
Write Hysteresis (57h)		All values are FFh	All values are FFh	All values are FFh
Write Gamma Setting (58h)		All values are 11h	All values are 11h	All values are 11h
RDFSVM (5Ah)		00h	00h	00h
RDFSVL (5Bh)		00h	00h	00h
RDMFFSVM (5Ch)		00h	00h	00h
RDMFFSVL (5Dh)		00h	00h	00h
RDLSCCM (65h, 66h)		80h	80h	80h
RDLSCCL (65h, 67h)		00h	00h	00h
Black/White Color	After MTP	MTP Value	MTP Value	MTP Value
Characteristics (70h~74h)	Before MTP	00h	00h	00h
Red/Green Color	After MTP	MTP Value	MTP Value	MTP Value
Characteristics (75h~79h)	Before MTP	00h	00h	00h
Blue/AColor Color	After MTP	MTP Value	MTP Value	MTP Value
Characteristics (7Ah~7Eh)	Before MTP	00h	00h	00h
DDB Start/Continue (A1h)	After MTP	MTP Value	MTP Value	MTP Value
DDB Start/Continue (ATT)	Before MTP	00h	00h	00h
DDB Continue (A8h)	After MTP	MTP Value	MTP Value	MTP Value
DDB Continue (A81)	Before MTP	00h	00h	00h
First/Continue Checksum (A	Ah, AFh)	00h	00h	00h
	After MTP	MTP Value	MTP Value	MTP Value
		ID1 = "00h"	ID1 = "00h"	ID1 = "00h"
	Before MTP	ID2 = "80h"	ID2 = "80h"	ID2 = "80h"
		ID3 = "00h"	ID3 = "00h"	ID3 = "00h"

Table 5.12.1 Default Values for User Command Set (Continuous)



5.12.2 Output or Bi-directional (I/O) Pins

Output or	Bi-directional pins	After Power On	After Hardware Reset	After Software Reset	
HSS HSS	I_DATA0_P, I_DATA0_N	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)	
	TE	VSSI	VSSI	VSSI	
200	Using SPI	VDDI	VDDI	VDDI	
500	Not using SPI	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)	
Source	e Driver Output	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)	
GOU	T1~GOUT32	AVSS	AVSS	AVSS	

NOTE: There will be no output from TE, SDO, D23-D0, HSSI_DATA0_P/N and HSSI_DATA1_P/N during Power PRIFILA On/Off sequence, H/W Reset and S/W Reset

5.12.3 Input Pins

		During	After Dewer	After	After	During
	Input pins	Power On		Hardware	Software	Power Off
		Process		Reset	Reset	Process
	DECV	See Section	Input Valid	Input Valid	Input Volid	See Section
	neox	5.10	input valio	input wallu	inpar valio	5.10
	CSX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	D/CX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	WRX (SCL / I2C_SDA)	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	RDX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	D23 to D0	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	SDI (I2C_SCL)	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	HS	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
l	VS VS	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	PCLK	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	DE 🔰	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	HSSI_CLK_P,	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	HSSI_CLK_N	input invaliu	input valiu	input valiu	input valiu	input invaliu
	HSSI_DATA0_P,	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	HSSI_DATA0_N	input invalid			input valid	input invalid
	HSSI_DATA1_P,	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
	HSSI_DATA1_N	input invalid				input invalid

5.13 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

5.13.1 Register loading Detection

Sleep Out-command (See "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: Compares register and EEPROM values, 2nd step: Loads EEPROM value to register). If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of these commands is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1) and the used TE-line is set to low (Registers, what are set by "Tearing Effect Line On (35h)" command, are keeping their current values) when it can be reactivated by "Tearing Effect Line On (35h)" command.

The flow chart for this internal function is following:



NOTES:

- 1. There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DCh), by the display module.
- 2. This information is only used if TE line is used.

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5.13.2 Functionality Detection

Sleep Out-command (See "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of these commands is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1) and the used TE-line ie set to low (Registers, what are set by "Tearing Effect Line On (35h)" command, are keeping their current values) when it can be reactivated by "Tearing Effect Line On (35h)" command.

The flow chart for this internal function is following:



NOTES:

- 1. There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.
- 2. This information is only used if TE line is used.

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5.13.3 Chip Attachment Detection

Sleep Out-command (See "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit, which is defined in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= not increased by 1) and the used TE-line ie set to low (Registers, what are set by "Tearing Effect Line On (35h)" command, are keeping their current values) when it can be reactivated by "Tearing Effect Line On (35h)" command.

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



NOTE: This information is only used if TE line is used.

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5.14 Display Panel Color Characteristics

Color characteristics of the display panel are stored on the display module that they can be read via the used interface by the engine what is using this display panel color characteristics information to adjust a color information of the image frame, what is on the engine, to match a wanted color outlook of the image on the display panel.

Used color characteristics can share 2 categories: Mandatory and Optional. The mandatory color characteristics are Black, White, Red, Green and Blue. The optional color characteristics is used if it is needed and it is called as A color (e.g. Cyan). The bits of the A color are set to '0's they are not used on the display module.

A read color characteristic value is based on 10 bit floating value where the MSB is 9th bit and the LSB is 0th bit. All power values of the bits are listed below:

- Bit 9: 2-1 = 0.5,
- Bit 8: 2-2 = 0.25,
- Bit 7: 2-3 = 0.125,
- Bit 6: 2 4 = 0.0625,
- Bit 5: 2-5 = 0.03125,
- Bit 4: 2-6 = 0.015625,
- Bit 3: 2-7 = 0.007813,
- Bit 2: 2-8 = 0.003906,
- Bit 1: 2-9 = 0.001953,
- Bit 0: 2-10 = 0.000977.

The wanted value is an approximation in the most of the cases when there is used binary numbers. Therefore, there is used the nearest value what can get e.g. Rx can be:

- Actual value: 0.6400, Stored value Rx[9:0] = 10 1000 1111b = 0.6396,
- Actual value: 0.3300, Stored value Rx[9:0] = 01.0101 0010b = 0.3301,
- Actual value: 0.3000, Stored value Rx[9:0] = 01 0011 0011b = 0.2998,
- Actual value: 0.6000, Stored value Rx[9:0] = 10 0110 0101b = 0.5986,
- Actual value: 0.1500, Stored value Rx[9:0] = 00 1001 1010b = 0.1504,
- Actual value: 0.0600, Stored value Rx[9:0] = 00 0011 1101b = 0.0596,
- Actual value: 0.3127, Stored value Rx[9:0] = 01 0100 0000b = 0.3125,
- Actual value: 0.3290, Stored value Rx[9:0] = 01 0101 0001b = 0.3291.

The value 0.6396 has calculated as follows:

- Binary value: 10 1000 1111b
- Formula: Rx[9]x0.5+Rx[8]x0.25+Rx[7]x0.125+Rx[6]x0.0625+Rx[5]x0.03125+Rx[4]x0.015625+Rx[3]x0.007813+Rx[2]x0.003906+Rx[1]x0.001953+R[0]x0.000977
- Use: 1x0.5+0x0.25+1x0.125+0x0.0625+0x0.03125+0x0.015625+1x0.007813+1x0.003906+ 1x0.001953+1x0.000977

See also sections:

"Read Black/White Low Bits (70h)", "Read Bkx (71h)", "Read Bky (72h)", "Read Wx (73h)", "Read Wy (74h)", "Read Red/Green Low bits (75h)", "Read Rx (76h)", "Read Ry (77h)", "Read Gx (78h)", "Read Gy (79h)", "Read Blue/AColor Low Bits (7Ah)", "Read Bx (7Bh)", "Read By (7Ch)", "Read Ax (7Dh)", "Read Ay (7Eh)".

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5.15 Gamma Function

The structure of grayscale amplifier is shown as below. The 26 voltage levels between VGMP and VGSP are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register.



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5.16 Basic Display Mode

The NT35510 has some basic operation modes which are Normal Display Mode, Partial Display Mode, Idle Mode, All Pixel On and All pixel Off for panel display. User can change these display modes for each other is illustrated below.



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5.17 Instruction Setting Sequence

When setting instruction to the NT35510, the sequences shown in below figures must be followed to complete the instruction setting.

5.17.1 Sleep In/Out Sequence



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5.17.2 Deep Standby Mode Enter/Exit Sequence





5.18 Instruction Setup Flow

5.18.1 Initializing with the Built-in Power Supply Circuits



Fig. 5.18.1 Initializing with the built-in power supply circuit

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initializing.

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5.18.2 Power OFF Sequence



Fig. 5.18.2 Power off sequence



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5.19 MTP Write Sequence Start Power on and normal display RDMTP command Check related End MTP_STUS1 bit = 0 (EF00h) MTP_STUS2 bit = 0 (EF01h) MTP was programmed Yes Adjust the MTP registers to optimal value * Refer command EDxxh for the related MTP registers MTPEN command (ED00h, ED01h) Set related MTP_EN1 bit = 1 MTP Connect high voltage 7.75V to MTP_PWR pin Programming 7.75V is not connected to MTP_PWR pin MTPDET command (EC00h) Check MTP DET bit = 1 No Yes MTPWR command (EE00h) Wait for more than 500 msec Remove high voltage 7.75V from MTP_PWR pin MTPEN command (ED00h, ED01h) Set all MTP_EN1 bit = 0 Set hardware reset SLPOUT command (1100h) MTP Programming Verify Read MTP registers all correct ? Re-execute MTP Programming Sequence Yes End

Note: The multi-times MTP must be programmed from the 1st time. (ID1/2/3, VGMP/VGSP, VGMN/VGSN, VCOM, Gamma 2.2, VGMP/VGSP LUT)

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5.20 Column, 1-Dot, 2-Dot, 3-Dot and 4-Dot Inversion (VCOM DC Drive)

The NT35510, in addition to the frame-inversion liquid crystal drive, supports the column, 1–dot, 2-dot, 3-dot and 4-dot inversion driving methods to invert the polarity of liquid crystal. The column, 1–dot, 2-dot, 3-dot and 4-dot inversion can provide a solution for improving display quality.

In determining the inversion drive for the inversion cycle, check the quality of display on the liquid crystal panel. Note that setting 1-dot inversion will raise the frequency of the liquid crystal polarity inversion and increase the charging/discharging current on liquid crystal cells.

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6 COMMAND DESCRIPTIONS

6.1 User Command Set

	Address													
Instruction	АСТ	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function
NOP	Dir	w	00h	0000h		No Ar	qument	(0000h	in MDDI	I/F)				No Operation
SWRESET	Cnd1	w	01h	0100h	No Argument (0000h in MDDI I/F)								Software reset	
				0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read display ID
RDDID	Dir	R	04h	0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
				0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	•
RDNUMPE	Dir	R	05h	Х	х	P7	P6	P5	P4	P3	P2	P1	P0	Read No. of the Errors on DSI only
RDDPM	Dir	R	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Power Mode
RDDMADCTL	Dir	R	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display MADCTR
RDDCOLMOD	Dir	R	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Pixel Format
RDDIM	Dir	R	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Image Mode
RDDSM	Dir	R	0Eh	0E00h	00h	D7	D6	D5	D4	D3	D2	D1	DO	Read Display Signal Mode
RDDSDR	Dir	R	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Self-diagnostic result
SLPIN	DVS	w	10h	1000h		No Ar	gument	(0000h	in MDDI	I/F)			0	Sleep in & booster off
SLPOUT	Dir	w	11h	1100h	\sim	No Ar	gument	(0000h	in MDDI	l/F)		1		Sleep out & booster on
PTLON	DVS	w	12h	1200h		No Ar	gument	(0000h	in MDDI	l/F)	$\overline{\mathbf{a}}$	\mathbf{N}	11 15	Partial mode on
NORON	DVS	w	13h	1300h		No Ar	gument	(0000h	in MDDI	1/F)			<u>)) \</u>	Partial off (Normal)
INVOFF	DVS	w	20h	2000h		No Argument (0000h in MDDI I/F)								Display inversion off (normal)
INVON	DVS	w	21h	2100h	No Argument (0000h in MDDI I/F)								Display inversion on	
ALLPOFE	DVS	w	22h	2200h	No Argument (0000h in MDDI I/F)								All pixel off (black)	
ALLPON	DVS	w	23h	2300h	No Argument (0000h in MDDI I/F)								All pixel on (white)	
GAMSET	DVS	w	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	Gamma curve select
DISPOFF	DVS	w	28h	2800h		No Argument (0000h in MDDI I/F)							Display off	
DISPON	DVS	w	29h	2900h		No Ar	gument	(0000h	in MDDI	l/F)			•	Display on
				2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	Column address set XS[15:0]: column start address
CASET	Dir	\M/	24h	2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	XE[15:0]: column end address
CASET	DII	vv	240	2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
				2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
				2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	Row address set
DAGET	Dir	\M/	OPh	2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	YE[15:0]: row end address
RAGET	ווט	vv	2011	2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
				2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
RAMWR	Dir	w	2Ch	Х	х	D7	D6	D5	D4	D3	D2	D1	D0	Memory write
RAMRD	Dir	R	2Eh	2E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory read
				3000h	00h	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	Partial start/end address set
	DVC		00h	3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	PEL[15:0]: partial end address
PILAR	DV5	vv	3011	3002h	00h	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
				3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	
TEOFF	DVS	w	34h	3400h		No Ar	gument	(0000h	in MDDI	I/F)	-	-		Tearing effect line off
TEON	DVS	w	35h	3500h	00h	-	-	-	-	-	-	-	м	Tearing effect mode set & on
MADCTL	Cnd2	w	36h	3600h	00h	MY	МХ	MV	ML	RGB	МН	RSMX	RSMY	Memory data access control
IDMOFF	DVS	w	38h	3800h		No Ar	gument	(0000h	in MDDI	l/F)				Idle mode off
IDMON	DVS	w	39h	3900h	No Argument (0000h in MDDI I/F)								Idle mode on	

Table 6.1.1 User Command Set

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											_			
Instruction	АСТ	R/W	Ad	dress		1	Pa	ramete	er					Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
COLMOD	Dir	W	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0	Interface pixel format
RAMWRC	Dir	W	3Ch	3C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory write Continue
RAMRDC	Dir	R	3Eh	3C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory read Continue
STESI	DVS	w	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Set tearing effect scan line
OTEGE	540		4411	4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0	
CSI	Dir	D	45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Get scan line
GOL	Dii	n	4511	4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0	
DSTBON	DVS	w	4Fh	4F00h	00h	0	0	0	0	0	0	0	DSTB	Deep standby mode on
				5000h	00h	V017	V016	V015	V014	V013	V012	V011	V010	Write profile value for display
				5001h	00h	V027	V026	V025	V024	V023	V022	V021	V020	
WRPFD	DVS	w	50h	:	:	:	:	:	:	:	:		\sum	
				500Eh	00h	V157	V156	V155	V154	V153	V152	V151	V150	
				500Fh	00h	V167	V166	V165	V164	V163	V162	V161	V160	
WRDISBV	DVS	w	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Write display brightness
RDDISBV	Dir	R	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Read display brightness value
WRCTRLD	DVS	w	53h	5300h	00h	0	0	BCTRL	А	DD	BL	DB	G	Write control display
RDCTRLD	Dir	R	54h	5400h	.00h	0	0	BCTRL	A	DD	BL 📢	DB	G	Read control display value
WRCABC	DVS	w	55h	5500h	00h			0	0	0		C1	CO	Write CABC mode
RDCABC	Dir	R	56h	5600h	00h	0	0	0	0	0	0	C1	CO	Read CABC mode
			5	5700h	OOh	1017	1016	1015	1014	1013	1012	1011	1010	Write hysteresis
				5701h	00h	1027	1026	1025	1024	1023	1022	1021	1020	
6	\mathcal{N}		2			C		Л\	1		:	:		
	NN	111	$\left[\right]$	570Eh	00h	1157	1156	1155	1154	1153	1152	1151	1150	
$ \leq \leq $		A A		570Eb	00h	1167	1166	1165	1164	1163	1162	1161	1160	
WRHYSTE	DVS	w	57h	5710h	00h	D017	D016	D015	D014	D013	D012	D011	D010	
\mathcal{N}				5711h	00h	D027	D026	D025	D024	D023	D022	D021	D020	
				571Eb	00b	D157	D156	D155	D154	D153	D152	D151	D150	
				571Eh	00h	D167	D166	D165	D164	D162	D162	D161	D160	
				571111 5800b	00h	6022	C000	C021	C020	C012	C012	C011	C010	Write commo potting
				50001	00h	G023	G022	G021	G020	6013	G012	CODI	CODO	white gamma setting
	DVC	14/	EQh			G043	G042	G041	G040	G033	G032		G030	
WHOAIVIIVISET	003	vv	3011	50001					:					
				5806h	00h	G143	G142	G141	G140	G133	G132	G131	G130	
		-		5807h	UUh	G163	G162	G161	G160	G153	G152	G151	G150	
RDFSVM	Dir	R	5Ah	5A00h	00h	FSV15	FSV14	FSV13	FSV12	FSV11	FSV10	FSV9	FSV8	Read FS value MSBs
RDFSVL	Dir	R	5Bh	5B00h	00h	FSV7	FSV6	FSV5	FSV4	FSV3	FSV2	FSV1	FSV0	Head FS value LSBs
RDMFFSVM	Dir	R	5Ch	5C00h	00h	FFSV15	FFSV14	FFSV13	FFSV12	FFSV11	FFSV10	FFSV9	FFSV8	Read median filter FS value MSBs
RDMFFSVL	Dir	R	5Dh	5D00h	00h	FFSV7	FFSV6	FFSV5	FFSV4	FFSV3	FFSV2	FFSV1	FFSV0	Read median filter FS value LSBs
WRCABCMB	DVS	W	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Write CABC minimum brightness
RDCABCMB	Dir	R	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Read CABC minimum brightness

Table 6.1.1 User Command Set (Continued)

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PRELIMINARY

Instruction	АСТ	R/W	Ad	dress			Pa	ramete	er					Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRLSCC	DVS	w	65h	6500h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	Write light sensor compensation
				6501h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	coefficient
RDLSCCM	Dir	R	66h	6600h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	Read LSCC value MSBs
RDLSCCL	Dir	R	67h	6700h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Read LSCC value LSBs
RDBWLB	Dir	R	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	Read Black/White low bit
RDBkx	Dir	R	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	Read Bkx
RDBky	Dir	R	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	Read Bky
RDWx	Dir	R	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	Read Wx
RDWy	Dir	R	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	Read Wy
RDRGLB	Dir	R	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	Read Red/Green low bit
RDRx	Dir	R	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Read Rx
RDRy	Dir	R	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	Read Ry
RDGx	Dir	R	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	Read Gx
RDGy	Dir	R	79h	7900h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	Read Gy
RDBALB	Dir	R	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	Read Blue/AColor low bit
RDBx	Dir	R	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	Read Bx
RDBy	Dir	R	7Ch	7C00h	00h	By9	By8	By7	By6	By5	By4	Ву3	By2	Read By
RDAx	Dir	R	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	Read Ax
RDAy	Dir	R	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	АуЗ	Ay2	Read Ay
		- 6	5	A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Read DDB start
	2			A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
RDDDBS	Dir	R	A1h	A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
	N_{N}	NI 1		A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
\mathcal{I}	ノ			A104h	00h		1	1	1	1	1	1	1	
			0	A800h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Read DDB continue
U				A801h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
RDDDBC	Dir	R	A8h	A802h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
				A803h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
				A804h	00h	1	1	1	1	1	1	1	1	
RDFCS	Dir	R	AAh	AA00h	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	Read first checksum
RDCCS	Dir	R	AFh	AF00h	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	Read continue checksum
RDID1	Dir	R	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
RDID2	Dir	R	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
RDID3	Dir	R	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3

Table 6.1.1 User Command Set (Continued)

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Notes:

1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing Time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame
3	DHS (Display Horizontal Sync.)	Synchronized with the next line
4	Cnd1 (By Conditional 1)	StateExecuting timeWhen Sleep InDirOtherDHS
5	Cnd2 (By Conditional 2)	State Executing time B7, B6, B5 Dir B4, B3, B2, B1, B0 DVS

- 2. In MIPI interface, parameters of the command are stores onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. See more information on the section "5.4 DATA TRANSFER RECOVERY". This note is valid when a number of the parameters is equal or less than 32 (In case of other interfaces, parameters of command 2A00h~2A03h are stored on relative registers while command 2A00h~2A03h are executed completely and same for command 2B00h~2B03h, 3000h~3003h and 4000h~4001h).
- 3. When using the commands without parameter (No Argument) in MDDI interface, a dummy parameter must be followed after command address. For example, command SPLOUT can be executed as 0x11 only in MIPI, MPU and SPI interfaces but should be executed as 0x1100 + 0x0000 in MDDI interface.



NOP (0000h)

Inst / Para	R/W	Add	ress				Parame	ter					
IIISt / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	Write	00h	0000h		No A	Argume	nt (0000	h in MD	DI I/F)				
NOTE: "-" Don't car	'e												
Description	This c Howe data r (Mem	command ver it car ead cont ory Write	d is empty n be used tinue as d e Continu	y command. It does no d to terminate RAM da described in RAMWR ie) and RAMRDC (Me	ot have ta write (Memo mory F	e effect o e, RAM ory Write Read Co	on the d data rea e), RAMI ontinue)	isplay n ad, RAM RD (Me and par	nodule. I data w mory Re ameter	vrite con ead), RA write co	tinue or AMWRC ommand	RAM ; s.	
Restriction	-										_		
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes											
Default Flow Chart			Power S	Status On Sequence /W Reset /W Reset			3	Defa	N/A N/A N/A N/A	le			

Version 0.00



SWRESET: Software Reset (0100h)

		Add	ress					Paramet	er				
Inst / Para	R/W	MIPI	Others	D[15:8] (No	on-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SWRESET	Write	01h	0100h			No	Argume	nt (0000ł	n in MD	DI I/F)			
NOTE: "-" Don't car	e												
Description	When param The di <i>Note:</i>	the Soft leters to isplay is <i>The Fra</i> l	ware Re their S/W blank im me Mem	set commar / Reset defa mediately. ory content	nd is writt ault values <i>is kept or</i>	en, it c s. (See <i>not by</i>	auses a default <i>this con</i>	tables in <i>mand.</i>	e reset. each c	. It rese comman	ts the c d descr	comman ription)	ds and
Restriction	It will I The di If Soft Sleep Softwa	be neces isplay mo ware Re Out corr are Rese	sary to v odule loa set is app mand. et comma	vait 5msec k ds all displa plied during and cannot k	Defore ser ay supplier Sleep Ou De sent du	nding n r's fact it mode uring Si	ew com ory defa e, it will k eep Out	mand fol ult value be neces sequen	lowing s to the sary to ce.	softwar registe wait 12	e reset. rs durin Omsec	ng this 5n before s	msec. ending
Register Availability		Normal M Normal M Partial W Partial W	Aode On, Aode On, Iode On,	Status , Idle Mode , Idle Mode Idle Mode (Idle Mode (Sleep In	Off, Sleep On, Sleep Off, Sleep On, Sleep	Out Out Out Out			Av	ailability Yes Yes Yes Yes Yes			
Default			Power S H	Status On Sequen W Reset W Reset					Defa	ult Valu N/A N/A N/A	ie		
Flow Chart				SWRESET Display w blank scr V Set Comma to S/W De Value Sleep In N	reen and efault Mode			Host		Leger Comma Parame Displa Action Mode	nd und eter y hial er		

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RDDID: Read Display ID (0400h~0402h)

		ر ۸ ما ما		,											
Inst / Para	R/W	Aud	Others		50	De			DO	DO	D1	DO			
		MIPI	Others	ען ואסייאן (Non-MIPI)	D/	D6	D5	U4	D3	D2	וט				
			0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10			
RDDID	Read	04h	0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20			
	st / Para R/W - RDDID Read "-" Don't care scription This re The 1 st The 2 ^{nt} The 3 rd Note: 0 comma egister ailability F F Default Default w Chart		0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30			
NOTE: "-" Don't car	е														
Description	This re The 1 ⁵ The 2 ¹ The 3 ¹ <i>Note:</i> <i>comm</i>	ead byte st parame nd param rd parame <i>Comma</i> <i>comma</i>	returns eter (ID1 eter (ID2 eter (ID3 nds RDI , respect	24-bit display identifie): the module's manue 2): the module/driver 1): the module/driver 1): the module/driver 1): <i>D1/2/3 (DAh, DBh, dively.</i>	cation in Ifacture version ID. DCh) re	formatic ID. ID. ad data	on. corres _i	oond to	the pa	rameter	1, 2, 3	of the			
Restriction	-							210	<u> </u>	<u>Nn</u>					
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes													
Default			Power S	Status On Sequence S/W Reset I/W Reset	- ار	Afte MTP MTP MTP	er MTP Values Values Values	Defa ID ID ID	ault Valu Be I=00h, I I=00h, I I=00h, I	ue efore M⊺ D2=80h D2=80h D2=80h	D1 ID11 ID21 ID31	0h 0h 0h			
Flow Chart				RDDID(04h) M 1 st Parameter ID1[7:0] M 2 nd Parameter ID2[7:0] M 3 rd Parameter ID3[7:0]	7 7 7]	Host Driver		Legen ommar aramete Display Action Mode equent transfe						

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		bbΔ	1955	, ,			Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BDNUMED	Read	05h	X	X	P7	P6	P5	P4	P3	P2	 P1	P0
NOTE: "-" Don't car	e											
Description	The fi bits is P[60 P[7] is P[70 the firs See a This c	rst parar below.] bits are s set to "] bits are st param Iso sectio ommand	telling a telling a " if there set to "(eter info on "Ackn I is used	telling a number of the a number of the parity e is overflow with P[6 0"s (as well as RDDS rmation (= The read nowledge with Error F for MIPI DSI only. It	re parity / errors. 0] bits. SM(0Eh) function Report (/ is no fun	' errors 's D0 ai is comp AwER)" nction fo	on DSI. re set "C bleted). and cor or others	The mo " at the nmand I s interfa	same ti RDDSM	ailed des ime) afte 1 0Eh. ation.	scription er there	is sent
Restriction	-							20			V -	
Register Availability		Normal M Normal M Partial M Partial M	<i>l</i> ode On lode On lode On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			AV	ailability Yes Yes Yes Yes Yes			
Default			Power S	Status On Sequence W Reset	٦			Defa	ault Valu 00h 00h 00h	Je		
Flow Chart		la		RDNUMED(05h) Send 1 st Parameter P[7:0] = 00h DDSM(0Eh)'s D0='0	7		Hosi		Legel Comma Parame Displa Action Mode	nd and eter ay n itial eer		

RDNUMED: Read Number of Errors on DSI (0500h)

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		Ada					Darama	tor									
Inst / Para	R/W		Jress Othore	D[15:9] (Non MIDI)	D7	De	Parame		DЗ	D2		DO					
	Road		Others			De	DS		03	D2							
NOTE: "-" Don't ca	reau	UAII	UAUUII	0011	זט	00	D3	D4	03	DZ		DU					
	This c	omman	d indicate	es the current status (of the c	lisplav a	s descri	bed in th	ne table	below:							
	E	Bit	<u></u>	Description		liopiaj a		Val	ue								
		07	Booster \	/oltage Status	"1"	=Booste	r On, "0	"=Boost	er Off								
		06	Idle Mode	e On/Off	"1"	=Idle Mo	de On,	"0"=ldle	Mode (Off							
		05	Partial Mo	ode On/Off	"1"	= Partia	I Mode	On, "0" -	= Partia	I Mode (⊃ff						
Description	[04	Sleep In/	Out	"1"	= Sleep	Out Mo	de, "0" =	= Sleep	In Mode	÷						
	0)3	Display N	Jormal Mode On/Off	"1"	= Displa	ıy Norm	al On, "()" = Dis	play No	rmal Off	1					
)2	Display C)n/Off	"1"	= Displa	ıy is On	, "0" = D	isplay is	s Off	11						
	Γ	D1	Not Defin	led	Se	t to "0" (r	not usec	l)									
	Γ	00	Not Defin	ied	Se	t to "0" (r	not usec	l)									
Restriction	-				11			Availability									
					<u>, 117</u>					~							
				Status	$\overline{\mathcal{U}}$	U	4	Av	ailability								
		Normal	Mode On	. Idle Mode Off. Slee	p Out		\approx		Yes								
Register		Normal	Mode On	, Idle Mode On, Slee	p Out		Ś		Yes								
Availability		Partial	Mode On	Ndle Mode Off, Sleer	Parameter D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0 s of the display as described in the table below:												
		Partial	Mode On	, Idle Mode On, Sleer	o Out				Yes								
		<u> </u>		Sleep In	コヒ				Yes								
_ { 		V								D3 D2 D1 D3 D2 D1 itable below: Off ode Off Partial Mode Off Partial Mode Off Display Normal Off Day is Off ability es res rend rend rend rend rential rential rential <t< td=""><td></td></t<>							
	Υ	~ (1											
	f.	\mathbb{R}^{HH}		Status				Defa	ault Valu	he							
Default		\overline{W}	Power	On Sequence					08h								
		$\frac{\eta}{2}$	<u> </u>	W Reset					08h								
			F	I/W Reset					08n								
								,									
								į Lo	egend								
			1						_								
			ļ				Host		nmand	li							
				••••••		 г	Tivor		mana	<u> </u>							
			Γ		7			/ Par	ameter								
			/ ^s	Send 1 ^{er} Parameter	/					$\overline{}$							
Flow Chart			-					¦ 🕒	isplay								
									ction	$\mathbf{\mathbf{z}}$							
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RDDPM: Read Display Power Mode (0A00h)

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1		-17		_ (• _ • • • •)			_					
Inst / Para	R/W	Add	dress				Parame	ter				
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDMADCTL	Read	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0
NOTE: "-" Don't car	e											
	This c	comman	d indicate	es the current status of	of the di	splay as	s descril	oed in th	ne table	below:		
		Bit		Description					Valu	е		
		07	Row Add	ress Order (MY)			"0" = In	cremen	t,"1"=	Decrem	nent	
		D6	Column A	Address Order (MX)			"0" = In	cremen	t, "1" =	Decrem	nent	
		D5	Row/Colu	Imn Exchange (MV)			"0"= No	ormal , "	1"= Rov	//columr	n exchar	nge
Description)4	vertical re	etresh Order (ML)			"0" = In	cremen	t,"1"=	Decrem	nent	
		03	RGB-BGI	R Order			"0" = R "1" = B	GB colo GR colo	r seque r seque	nce nce		2
	[02	Horizonta	l refresh Order (MH)			"0" = In	cremen	t , "1" =	Decrem	nent	
	[D1	Flip horiz	ontal (RSMX)		25	"0" = N	ormal ,	'1" → Ho	rizontal	flip	
		D0	Flip vertic	al (RSMY)	~	2 \	"0" = N	ormal,	'1" = Ve	rtical flip	р	
Bestriction	-					≥₩						
						<u> </u>		15	זור			
			1	Status				Δν	ailability			
		Normat	Mode On	Idle Mode Off Slee	n Out		\mathbb{C}		Yes			
Register		Normal	Mode On	Idle Mode On, Slee					Yes			
Availability		Partial	Mode On.	Idle Mode Off. Sleer	o Out	\bigcirc	$\mathbf{\Theta}$		Yes			
\mathcal{P}		Partial I	Mode On,	Idle Mode On, Sleep	Out				Yes			
		0.0	5	Steep In	リー				Yes			
		n ((
		<u> </u>		Status				Defa	ault Valu	le		
Default		<u> / </u>	Power	On Sequence					00h			
Delault		11 2	S	W Reset					00h			
			H	I/W Reset					00h			
								r	 agand			
			_					ļ	sychu			
			F	RDDMADCTL(0Bh)				¦		7:		
							Host		nmand	_i _		
			_		7		Driver	i Par	ameter	7		
			/s	Send 1 st Parameter	/				ameter	_ ¦ _		
Elow Chart				/					isplay	<u>}</u> !		
TIOW Chart										Ji		
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RDDMADCTL: Read Display MADCTL (0B00h)

11/8/2010

Version 0.00



				()								
linet / Devie		Ad	dress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
	Deed		00001		D7		50		D0	D0		D0
RDDCOLMOD	Read	UCh	0000h	0011	D7	D6	D5	D4	D3	D2	DI	DU
NOTE: "-" Don't car	e											
	This c	ommar	nd indicate	es the current status of	of the di	splay a	s descril	oed in th	ne table	below:		
	E	3it		Description					Valu	е		
	Г)7	Not Defin	ed			Set to '	'0" (not i	ised)			
							"101"	10 hit /	nivel			
			DCP Into	rfaga Calar Format			101 =	10-DIL/	pixel			
Description	00	~ D4	ngp inte				110 = "~~~"		pixei		Π	
Description								24-DIL /	pixei			
	E)3	Not Defin	ed			Set to '	'0" (not i	used)			
							"101" =	16-bit /	pixel		UL	
	D2	~ D0	Control Ir	nterface Color Forma	t		"110" =	18-bit /	pixel	/ Nn		
						-	"111" =	24-bit /	pixel	U I		
						2111						
Restriction	-				11		、ノ			3		
									215			
				Charles				7		2		
				Status				AV	anabing			
Deviator		Normal	Mode On	, Idle Mode Off, Slee	p Out		$\bigcirc \Downarrow$		Yes			
Register		Normal	Mode On	, Idle Mode On, Slee	p Out			\bigcup	Yes			
Availability	20	Partial	Mode On	Ndle Mode Off, Sleep	Out				Yes			
		Partial	Mode On	, Idle Mode On, Sleer	o Out				Yes			
RDDCOLMOD Read Och Occool On D7 D6 D5 D4 D3 t NOTE: "-" Don't care This command indicates the current status of the display as described in the table bed Water Value Value D7 Not Defined Set to "0" (not used) '101" = 16-bit / pixel '101" = 16-bit / pixel Description D6 D4 RGB Interface Color Format '101" = 16-bit / pixel '101" = 16-bit / pixel D8 Not Defined Set to "0" (not used) '101" = 16-bit / pixel '111" = 24-bit / pixel D8 Not Defined Set to "0" (not used) '101" = 16-bit / pixel '111" = 24-bit / pixel D2 D0 Control Interface Color Format '101" = 16-bit / pixel '111" = 24-bit / pixel D2 D0 Control Interface Color Format '101" = 16-bit / pixel '111" = 24-bit / pixel Normal Mode On, Idle Mode On, Sleep Out '101" = 16-bit / pixel '111" = 24-bit / pixel Normal Mode On, Idle Mode On, Sleep Out Yes Yes Yes Normal Mode On, Idle Mode On, Sleep Out Yes Yes												
		V P	5		<u> </u>							
		<u> </u>		Ctatula		1		Dofe	ult Vol	10		
		\times		Status				Dela		Je		
Default		$\overline{\mathcal{M}}$	Power	On Sequence		_			07n			
		\overline{n}	5	S/W Reset		_			07h			
			ŀ	I/W Reset					07h			
								I				
					1			L L	egend	ļ		
			L L					i				
			Ľ		J		Host		mmand	11		
			••••	•••••••					IIIIaiiu	_J¦		
			7		7	L	Jriver	Par	ameter	7 i		
			/ 9	Send 1 st Parameter	/				ameter	_ ¦ _		
				/					icolov	_ i ر		
Flow Chart									ispiay	ノ		
								!	ction			
								¦ <u>~</u>		<u> </u>		
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									ansfer_			
								i				

RDDCOLMOD: Read Display Pixel Format (0C00h)

11/8/2010

Version 0.00



		٥	droop				Deremo	tor				
Inst / Para	R/W		Othore	D[15:9] (Non MIDI)		De			D2	D2		DO
	Dood		Others			Do	D5		D3	D2		
	neau	UDI	UDUUII	0011	Di	Do	D5	D4	D3	DZ	DI	DU
NOTE Dont Ca	e This c	ommai	ad indicat	as the current status	of the	display as	doscril	ood in th	no tablo	bolow:		
		Johnna Rit	iu muicate	Description		uispiay as	S UESCIII	V	alue	DEIOW.		
		77	Vertical S	Scrolling On/Off		Set to "0"	" (not us	ed)				
		D6	Horizonta	al Scrolling On/Off		Set to "0"	" (not us	ed)				
		D5	Inversion	On/Off		"1" = Inve	ersion C)n. "0" =	Inversi	on Off	~	
Description		04	All Pixel	On		"1" = Wh	ite displ	av. "0" =	= Norma	al displa	v	
		03	All Pixel	Off		"1" = Bla	ck displa	ay, "0" =	Norma	l display		1
	D2	~ D0	Gamma	Curve Selection		"000" = 0 "010" = 0 "100" to "	GC0, " GC2, " 1111" =	001" = 0 011" = 0 not defin	GC1 GC3 ned			
Restriction	-			^	11					3		
						IT U			216			
				Status	17	<u>j</u> ü	5	Av	ailability			
		Normal	Mode Or	, Idle Mode Off, Slee	p Out			Ì I I	Yes			
Register		Norma	Mode Or	, Idle Mode On, Slee	p Out		51	\bigcirc	Yes			
Availability	~ ~	Partial	Mode On	, Idle Mode Off, Slee	Out	(1)	Parameter D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0 s described in the table below: Value "(not used) ersion On, "0" = Inversion Off itte display, "0" = Normal display ick display, "0" = Normal display ick display, "0" = Normal display GC0, "001" = GC1 GC2: "011" = GC3 "T11" = not defined Availability Yes Yes Yes Yes Yes Yes Ves Ves Ves Ves Ves Ves Ves V					
		M Mill Others D[15:8] (Non-MIP) D7 D6 D5 D4 D3 D2 D1 ead 0Dh 0D00h 00h 07 D6 D5 D4 D3 D2 D1 his command indicates the current status of the display as described in the table below: Bit Description Value D7 Vertical Scrolling On/Off Set to "0" (not used) D6 Horizontal Scrolling On/Off Set to "0" (not used) D6 Horizontal Scrolling On/Off Set to "0" (not used) 00 D3 Inversion Off D1 D1 Walue D5 Inversion On/Off "1" = Ninversion On, "0" = Inversion Off D4 All Pixel Off "1" = Black display, "0" = Normal display D3 All Pixel Off "1" = Black display, "0" = Normal display D3 D2 D1 D2 D0 Gamma Curve Selection "00" = GC2, "011" = GC2 "100" (e "11)" = Addition Moreal Mode On, Idle Mode Off, Sleep Out Yes Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Yes Sleep In Yes Sleep In Yes										
				Sleep In	Л				Yes			
	H U	~	- {		2							
	ľ —											
				Status				Defa	ault Valu	Je		
Default			Powe	r On Sequence					00h			
		$\frac{1}{\sqrt{2}}$		S/W Reset					00h			
			F	H/W Reset					00n			
Flow Chart				RDDIM(0Dh)] 7	Ε	Host Driver		egend mmand rameter isplay cction Aode quentia			

RDDIM: Read Display Image Mode (0D00h)

11/8/2010

Version 0.00



	Ispidy											
Inst / Para	R/W	Add	oress		D7	Da	Parame	ter	Da			Do
DDDOM	Deed		Others		D7	D6	D5	D4	D3	D2		DU
	Read	UEN	UEUUN	000	D7	D6	D5	D4	D3	D2	DI	DU
NOTE: "-" Don't car	This a		al in alia a ta		ملاطات مازم		- de e evil	الجمع أبعا		halauu		
		comman Dit	a indicate	Description	or the dis	splay as	s descri	bed in tr		below:		
			Tooring	Effect Line On/Off		"1"	On "0'	0#	value			
			Tearing E	Effect Line Mode		"1"	• On, 0	= OII	Modo 1			
		26				"1"		(2, 0) = 1		hit ic "O'	,	
Description		20	Vertical S	ar Sync. (IIS, NOD I/I		"1"	. VS hit	is i, (ic "1" "()" – VS	bit is 6		
Description		24	Pixel Clo	ck (PCLK BGB I/F)C	n/Off	"1" –		line is O	n = 0.0		ine is Of	f
		20	Data Ena	ble (DE BGB I/F)On		"1" –	DF hit	is "1" "(1, 0 –)' – DE	hit is "0"	, ,	
		5 <u>2</u> D1	Not Defin	ied		Set	to "0" (n	nt used)				
		0	Error on				- Error	0" – No	Error			
	Note	Bit D5 t	o D2 indi	cate current status of	the line	s when	this cor	nmand	has bee	n sent		
Restriction	-	Dit Do t	o be mar					hana		i oont.		
						<u> </u>		1	לור	>		
			1	Status				Δν	ailahilitu			
		Normal	Mode On	Idle Mode Off Slee	n Out				Yes			
Register		Normal	Mode On	, Idle Mode On, Slee	p Out				Yes			
Availability	R	Partial	Mode On	Idle Mode Off. Slee	o Out		e		Yes			
1		Partial I	Mode On	, Idle Mode On, Sleep	o Out				Yes			
		00	5	Sleep In	ノー				Yes			
{ <u>}</u>		-	\approx						14 D3 D2 D1 D in the table below: Value Value Off " = Mode 1 ", "0" = HS bit is "0" is On, "0" = PCLK line is Off ", "0" = DE bit is "0" sed) No Error Ind has been sent. Availability Yes Display Action			
						1						
n –				Status				Defa	ault Valu	le		
Default		\overline{n}	Power	r On Sequence					00h			
		U	5	S/W Reset					00h			
			F	I/W Reset					00h			
								r — — — ·				
					1			į Lo	egend			
				BDDSM(0Eb)				 		-1		
					J		Host		mmand	li		
			••••	••••••		 Г	Driver		IIIIaila	<u> </u>		
			Γ		7	-		/ Par	ameter			
				Send 1 ^{er} Parameter	/					_		
Flow Chart								¦ 🕒	isplay)i		
									ction	>!		
									lode	\mathcal{I}_{I}		
								Sec	quentia			
									ansfer_	<u> </u>		
								<u> </u>]		
1	1											

RDDSM: Read Display Signal Mode (0E00h)

11/8/2010

Version 0.00



		μΔ	dress		,		Parame	tor				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6			БЗ	D2	D1	DO
BUDSUB	Road	0Eb	0E00h	00h		DG	D5		D3	D2		
	neau	0111	01 0011	0011	Di	D0	D5	D4	D3	DZ		DU
NOTE Dont car	e Thia a		al in aliante		مطغله مطأنا		- de e e uil	+ h		halaur		
		onnai Sit				spiay as	sueschi			Delow.		
			Degister			-			value			
		57	Register	Loading Detection		_						
		06	Functiona	ality Detection		See	section	5.13				
		5	Chip Atta	chment Detection		_				~	Π	
Description)4	Display G	lass Break Detection	1		"O" (<u>a IN</u>		
		03	Not Defin	ed		Set	to "0" (n	ot used)				
)2	Not Defin	ed		Set	to "0" (n	ot used)				
		D1	Not Defin	ed		Set t	to "0" (n	ot used)	·			
		00	Checksur	ns Comparison		"0": (Checks	ims are	the san	ne		
					415	1.1.1	Checks	ims are	not the	same		
Restriction	-											
					1/4/1			nir	<u>)) \?</u>			
			. 1	Status	U T			Av	ailability			
		Normal	Mode On	, Idle Mode Off, Slee	p Out 🏒				Yes			
Register	st/ Para RW Address ratialities MMP Others D(15:3) (Non-MP) D7 D6 D4 D3 D2 D1 DDSDR Read 0Fh 0F00h 00h D7 D6 D5 D4 D3 D2 D1 DDSDR Read 0Fh 0F00h 00h D7 D6 D5 D4 D3 D2 D1 :** Don't care This command indicates the current status of the display as described in the table below: Bit Description Value Value D7 Register Loading Detection See section 5.13 See section 5.13 See section 5.13 D3 Not Defined Set to '0' (not used) Set to '0' (not used) D1 Not Defined Set to '0' (not used) D2 Not Defined Set to '0' (not used) To checksums are the same To Checksums are the same To Checksums are the table below: Normal Mode On, Idle Mode On, Steep Out Yes Yes Partial Mode On, Idle Mode On, Steep Out Yes Yes Partial Mode On, Idle Mode On, Steep Out Yes Yes Status Default Value Doh Doh Normal Mode O											
Availability	R	Partial	Mode On,	Idle Mode Off, Sleep	o Out	\bigcirc			Yes			
\mathbb{P}		Partial	Mode On,	Idle Mode On, Sleep	o Out				Yes			
		0.0	1	Sleep In	ノー				Yes			
			\sim									
		<u> </u>										
l ~		M/M		Status				Defa	ault Valu	le		
Default			Power	On Sequence					00h			
		V	S	/W Reset					00h			
			F	/W Reset					00h			
								r		!		
					1			i L	egenu	ł		
			Γ	RDDSDR(0Fh)				i		7!		
					-		Host	Coi	mmand	į		
			_	▼	_	D	Driver					
			/ 5	Send 1 st Parameter	/			Z Par	ameter	_/ ¦		
									icolov	٦İ		
Flow Chart									ispiay	ノ		
								< A	ction	>!		
									lode	ノ		
								Sec	quentia			
									ansfer_	<u> </u>		
										 /		

RDDSDR: Read Display Self-Diagnostic Result (0F00h)

11/8/2010

Version 0.00



SLPIN: Sleep In (1000h)

Inst / Dara		Add	ress				Parame	ter				
inst / Para	R/VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SLPIN	Write	10h	1000h		No	Argumer	nt (0000	h in MC	DI I/F)			
NOTE: "-" Don't car	re											
Description	This c In this stopp	command mode th ed. Sou Memo In	d causes ne DC/DC nrce / Ga ory Scar ternal O C / DC C	the TFT LCD module C converter is stopped ate Output B n Operation IIII scillator	e to entr d, Interr lank Dis	er the minal displa	ay oscilla STO STC	power of ator is s P DP	consum topped,	ption ma and pa TOP	ode. nel scar	nning is
	Contro or lose User of this in Sleep Dimm	ol Interfa es (RAM can senc nformatio Out-mo ing funct is used	ice as wi IKP="0") I PCLK, I In is valid de. tion does an intern	II as memory and rec its contents. HS and VS information d during 2 frames af not work when there hal oscillator for blank	Parameter D7 D6 D5 D4 D3 D2 D1 D No Argument (0000h in MDDI I/F) e to enter the minimum power consumption mode. d, Internal display oscillator is stopped, and panel scanning Iank Display STOP STOP Image: Stop OFF gisters are still working and the memory keeps (RAMKP=" on on RGB I/F for blank display after Sleep In command a fter Sleep In command if there is used Normal Mode On a is changing mode from Sleep Out to Sleep In. s display. s already in sleep in mode. Sleep In Mode can only be exit Sending next command, this is to allow time for the sup sending Sleep Out command (when in Sleep In Mode) before Availability is pout Yes p Out Sleep In Mode <td< td=""><td>(P="1") nd and 9 On in</td></td<>	(P="1") nd and 9 On in						
Restriction	This c the SI It will voltag It will Sleep	command eep Out be nece les and c be neces In comm	t has no Comman essary to clock circ ssary to nand can	effect when module is nd (11h). wait 5msec before a uits to stabilize. wait 120msec after so be sent.	s alreac sending ending	ly in slee 1 next co Sleep O	p in mo ommanc ut comn	de. Slee d, this is nand (w	ep In Mo s to allo vhen in s	ode can ow time Sleep Ir	only be for the n Mode)	exit by supply before
		-		Status				Av	ailability	/		
		Normal N	Mode On	, Idle Mode Off, Slee	p Out				Yes			
Register		Normal N	Mode On	, Idle Mode On, Slee	p Out	_			Yes			
Availability		Partial N	<i>lode</i> On,	Idle Mode Off, Sleep	o Out				Yes			
		Partial N	lode On,	Idle Mode On, Sleep	o Out				Yes			
				Sleep In					Yes			
				Status				Defa	ault Valu	le		
Default			Power	On Sequence				Slee	p In Mo	de		
Default			S	W Reset		1		Slee	p In Mo	de		
			H	I/W Reset				Slee	p In Mo	de		
						•						





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Version 0.00



SLPOUT: Sleep Out (1100h)

		bbΔ	ress					Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (No	n-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
	Write	11h	1100h	<u>D[10.0](110</u>	,	No	Argumer	nt (0000	h in MD			51	
NOTE: "-" Don't car			110011			110	rugamoi	11 (0000		, 81 1/1 /			
NOTE: "-" Don't car	e This c In this started	ommanc mode th d. Sourc Memory Inte DC / can start	turns of ne DC/DC se / Gate y Scan (rnal Osc DC Con to send valid at lo	f sleep mode C converter is Output Operation cillator nverter PCLK, HS a east 2 frame	e. s enabled STOP STOP STOP	d, Inter	ART	ay oscil (II GB I/F mand, i	Iator is a	started, Blank X N 29h is Sleep (Sleep (is left S	and par CDP of Memory set)	nel scar or Frame (Contents)	ining is
Restriction	Out-m There NT355 Sleep reset. It will voltag NT355 there same NT355 It will Sleep	ode in N is used 510 will c Out Mor be nece and c 510 load cannot b when thi 510 is do be neces Out com	lormal Me an intern do seque de can o ssary to clock circo s all defa be any ab is load is bing self-o ssary to mand ca	ode On. al oscillator f nce control a nly be exit b wait 5msec uits to stabili ault values of normal visua done and wi diagnostic fur wait 120mset an be sent.	or blank about gat by the Sk before s ze. i extende al effect o hen the N nctions d c after se	display e contre eep In aending d and on the NT355 ⁻ uring t ending	y. Comma Comma next cor display i 10 is alre his 5mse Sleep In	ommand to mage if ady Sle comma	sleep o), S/W d, this is o the re those c ep Out also see and (wh	reset co s to allo gisters default a -mode. ction 5. ction 5.	ommanc ow time during t and regis 13. leep Ou	for the his 5ms ster valu t mode)	or H/W supply ec and ues are before
Register Availability		Normal M Normal M Partial M Partial M	Mode On Mode On Node On, Node On,	Status , Idle Mode C , Idle Mode C Idle Mode C Idle Mode C Sleep In	Dff, Sleep Dn, Sleep Dff, Sleep Dn, Sleep	Out Out Out Out			Av	ailability Yes Yes Yes Yes Yes	<i>y</i>		
Default			Power S H	Status On Sequence /W Reset /W Reset	ce				Defa Slee Slee Slee	ault Valı p In Mo p In Mo p In Mo	ue de de de		

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Version 0.00



Inot / Poro		Add	ress				Parame	ter				
inst / Para	H/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
PTLON	Write	12h	1200h		No /	Argume	nt (0000	h in MD	DI I/F)			
NOTE: "-" Don't car	re											
Description	This comm To lea There	comman and (30I ave Partia is no ab	d turns H) al mode, normal v	on Partial mode. Th the Normal Display N risual effect during mo	ie parti Node O ode cha	al mode n comm nge bet	e windo and (13 ween N	w is de H) shou ormal m	escribec Ild be wi 10de On	d by the ritten. to Part	e Partia ial mode	I Area
Restriction	This c	ommano	d has no	effect when Partial Di	isplay n	node is a	active.				_	
Register Availability		Normal M Normal M Partial M Partial M	Mode On Mode On Node On, Node On,	Status , Idle Mode Off, Sleep , Idle Mode On, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	o Out o Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			
Default Flow Chart	See F	Partial Art	Power S H ea (30h)	Status On Sequence /W Reset /W Reset			3	Defa Norma Norma	ault Valu al Mode al Mode al Mode	ie On On On		

PTLON: Partial Display Mode On (1200h)

11/8/2010

Version 0.00



NORON: Normal Display Mode On (1300h)

Inst / Para		Add	ress				Parame	ter				
ilist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
NORON	Write	13h	1300h		No	Argume	nt (0000	h in MD	DI I/F)			
NOTE: "-" Don't car	e											
Description	This c Norma Exit fr There	ommano al display om NOF is no ab	d returns y mode o ON by th normal v	the display to normal on means Partial mod- ne Partial mode On co risual effect during mo	mode. e off. omman ode cha	d (12h) Inge froi	m Partia	l mode	On to N	lormal n	node Or	I.
Restriction	This c	ommano	d has no	effect when Normal D	Display	mode is	active.					
Register Availability		Normal N Normal N Partial N Partial N	Mode On Mode On Node On, Node On,	Status , Idle Mode Off, Sleep , Idle Mode On, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	o Out o Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			
Default Flow Chart	See P	Partial Ar	Power S H ea Defini	Status On Sequence /W Reset I/W Reset	details o	of when	to use t	Defa Norma Norma his com	ault Valu al Mode al Mode al Mode mand	Je On On On		

Version 0.00



INVOFF: Display Inversion Off (2000h)

Inst. / Para RW MiPT Others D[15:8] (Mon-MIPI) D7 D6 D5 D4 D3 D2 D1 D0 INVOFF Wite 20h 200h No Argument (0000h in MDDI I/F) No Argument (0000h in MDDI I/F) NOTE: ** Don't care This command is used to recover from display inversion mode. This command does not change of contents of frame memory. This command does not change of contents of frame memory. This command does not change of contents of frame memory. Description Maximum does not change of contents of frame memory. Register This command has no effect when module lealinged, in Inversion Off-mode. Register Normal Mode On, Idle Mode Off. Sleep Out Vres Availability Normal Mode On, Idle Mode Off. Sleep Out Vres Partial Mode On, Idle Mode Off. Sleep Out Vres Partial Mode On, Idle Mode Off. Sleep Out Vres Partial Mode On, Idle Mode Off. Sleep Out Vres Partial Mode On, Idle Mode Off. Sleep Out Partial Mode On, Idle Mode Off. Sleep Out Vres Partial Mode On, Idle Mode Off. Sleep Out Vres Partial Mode On, Idle Mode Off. Sleep Out Vres Vres Inversion off Inversion off Inversion off Inversion off			٨dd	rocc	-				Paramo	tor				
INVOFF Mint of United Eq. (15) (United in (17) Ext = Dot = D	Inst / Para	R/W	MIDI	Othore	D[15:9]		D7	De			D2	D2	D1	DO
Intervent Twing Lot 1/20001 NOTE: ** Don't care This command is used to recover from display inversion mode. This command does not change of contents of frame memory. This command does not change any other status. (Example) Description Restriction This command has no effect when module is already in triversion Off-mode. Normal Mode Op, Idle Mode Off, Sleep Out Ves Partial Mode On, Idle Mode Off, Sleep Out Ves Partial Mode On, Idle Mode Off, Sleep Out Ves Partial Mode On, Idle Mode Off, Sleep Out Ves Partial Mode On, Idle Mode Off, Sleep Out Ves Default Object Off Sequence Display Inversion off HW Reset Display Inversion off HW Reset Display Inversion off HW Reset Display Inversion off Mode Off Mode		\\/rito	20h	2000h	D[13.0]		No	Argumo	D3	bin MD		DZ		DU
NOTE: - Don't table This command is used to recover from display inversion mode. This command does not change of contents of frame memory. This command does not change any other status. (Example) Description Restriction This command has no effect when module istalfeady in triversion Off-mode. Restriction Restriction Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode Off, Sleep Out Ves Parinal Mode On, Idle Mode Off, Sleep Out Ves Parinal Mode On, Idle Mode Off, Sleep Out Ves Parinal Mode On, Idle Mode Off, Sleep Out Ves Parinal Mode On, Idle Mode Off, Sleep Out Ves Parinal Mode On, Idle Mode Off, Sleep Out Ves Parinal Mode On, Idle Mode Off, Sleep Out Ves Parinal Mode On, Idle Mode Off, Sleep Out Ves Sleep Inf Ves Default Default Power Off Sequence Display Inversion off HW Reset Display Inversion off HW Reset Display Inversion off Off Mode Ves Sequential Inversion		white	2011	200011			INU A	Argume	iii (0000		(רווטי			
This command makes to change of contents of frame memory. This command makes no change of contents of frame memory. Description Restriction This command has no effect when module is already in Inversion Off mode. Register Availability Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode Off, Sleep Out Ves Perinal Mode On, Idle Mode Off, Sleep Out Ves Partial Mode On, Idle Mode Off, Sleep Out Ves Partial Mode On, Idle Mode On, Sleep Out Ves Default Default Object of Sequence Display Inversion off HW Reset Display Inversion off Mode Off Mode	NOTE Dontcar	e Thia a				u fuene aliene								
This command dates no change any other status. Description Minor Period Pestriction This command dues no change any other status. Restriction This command has no effect when module is already in Inversion Off-mode. Register Availability Normal Mode On, table Model On, Sleep Out Normal Mode On, table Model On, Sleep Out Ves Partial Mode On, table Model On, Sleep Out Ves Partial Mode On, table Model On, Sleep Out Ves Partial Mode On, table Model On, Sleep Out Ves Partial Mode On, table Model On, Sleep Out Ves Partial Mode On, table Model On, Sleep Out Ves Partial Mode On, table Model On, Sleep Out Ves Default Default On Mode Image On Sequence Display Inversion off HW Reset Display Inversion Image On Mode		This C	ommand	i is used I makacu		er irom aisp	tay inve	rsion m	ode.					
Ins command uses not used and use and used. Description Image: Command has no effect when module is already in intension Off mode. Register Availability Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Default Default Value Display Inversion off HW Reset Display Inversion off Display Inversion off HW Reset Display Inversion off Display UNOFF(20h) Under Mode Off Mode Mode Status		This C	ommand	doos no	t change	any other	is ur ira status	ne mei	nory.					
Description Memory During Restriction This command has no effect when module is already in Inversion Off mode. Register Availability Availability Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Power On Sequence Display Inversion off UNOFF(20h) Usplay Inversion off HW Reset Display Inversion off UNOFF(20h) Usplay On Mode Mode Off Mode Sequential Invortion Mode		(Exam	nole)		t change	any other a	status.							
Description Image: Construction of the state of th		(Exam	1010)		Memory	T				Display				
Restriction This command has no effect when module is already in Inversion Off-mode. Register Availability Availability Normal Mode On, Idle Mode Off, Sleep Out Ves Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Status Default Yes Ves Status Default Value Power On Sequence Display Inversion off Status Default Value Display Inversion off HW Reset Display Inversion off Parameter INVOFF(20h) Invorf (20h) Parameter INVOFF(20h) Display Inversion Mode Off Mode Sequential Sequential	Description											~	Π	
Restriction This command has no effect when module is already in Inversion Off mode. Register Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Parinal Mode On, Idle Mode Off, Sleep Out Yes Parinal Mode On, Idle Mode Off, Sleep Out Yes Parinal Mode On, Idle Mode Off, Sleep Out Yes Parinal Mode On, Idle Mode Off, Sleep Out Yes Parinal Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Default Status Default Display Inversion off HW Reset Display Inversion off Display Inversion Command Parameter Display UNOFF(20h) Vetic Display Inversion Mode Flow Chart Display Inversion Off Mode Sequential Tarsfer Sequential							N					$A \mid R$		
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Restriction This command has no effect when module is already in Inversion Off mode. Register Availability Status Availability Normat Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Status Default Period Kase Display Inversion off SW Reset Display Inversion off HW Reset Display Inversion off INVOFF(20h) Image: Command Mode Off Mode INVOFF(20h) Display Inversion Off Off Mode Mode Off Mode Mode Off Mode Mode							$\neg \gamma$					<u>\\</u> U		
Restriction This command has no effect when module is already in Inversion Off-mode. Register Availability Status Availability Perial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Default Status Default Off Sequence Display Inversion off Display Inversion off HW Reset Display Inversion off UNCOFF(20h) Display Inversion On Mode On Mode Off Mode Sequential								6		╶┼╾┟╴	╺╬═╬═╡╲	7 -		
Restriction This command has no effect when module is already in Inversion Off-mode. Register Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Status Default Ves Sleep In Yes Display Inversion off S/W Reset Display Inversion off UNVOFF(20h) Image: Sequential Intersion On Mode Image: Sequential Intersion Off Mode Sequential Intersion Off Mode Sequential Intersion								<u>]] [] c</u>						
Register Availability Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Panial Mode On, Idle Mode On, Sleep Out Yes Panial Mode On, Idle Mode On, Sleep Out Yes Panial Mode On, Idle Mode On, Sleep Out Yes Panial Mode On, Idle Mode On, Sleep Out Yes Panial Mode On, Idle Mode On, Sleep Out Yes Panial Mode On, Idle Mode On, Sleep Out Yes Panial Mode On, Idle Mode On, Sleep Out Yes Panial Mode On, Idle Mode On, Sleep Out Yes Panial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display Inversion off SW Reset Display Inversion off HW Reset Display Inversion off INVOFF(20h) Inversion Verset Display INVOFF(20h) Display Display Inversion Mode Off Mode Sequential transfer Sequential	Restriction	This c	ommanc	has no	effect wh	en module i	is alread	dy in In∖	ersion C)ff mode	Э.	1		
Register Availability Normal Mode On, Idle Mode Ott, Sleep Out Yes Normat Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Status Default Value Power On Sequence Display Inversion off Befault SW Reset Display Inversion off HW Reset Display Inversion off INVOFF(20h) Image of the second off INVOFF(20h) Image of the second off Display Inversion Mode Off Mode Mode Status Display Inversion Off Mode Mode Off Mode Sequential transfer Sequential														
Register Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display Inversion off SW Reset Display Inversion off HW Reset Display Inversion off On Mode Parameter INVOFF(20h) Display Inversion Oisplay Inversion Mode Off Mode Mode					Status	<u> </u>		2		Av	ailability			
Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Default Status Default Default Value Power On Sequence Display Inversion off HW Reset Display Inversion off Under Chart Display Inversion INVOFF(20h) Display Inversion Off Mode Mode Sequential transfer Inversion	Register		Normal N	Node On	Idle Mod	le Off, Slee	p Out	- (\gg		Yes			
Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Default Endet Value Power On Sequence Display Inversion off SW Reset Display Inversion off HW Reset Display Inversion off On Mode Image: Command Inversion off Image: Command Inversion Image: Command Inversion Image: Command Inversion Image: Command Inversion <td>Availability</td> <td></td> <td>Normal N</td> <td>Node On</td> <td>Idle Moo</td> <td>le On, Slee</td> <td>p Out</td> <td></td> <td></td> <td>U'</td> <td>Yes</td> <td></td> <td></td> <td></td>	Availability		Normal N	Node On	Idle Moo	le On, Slee	p Out			U'	Yes			
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Steep int Tes Default Status Default Value Power On Sequence Display Inversion off S/W Reset Display Inversion off H/W Reset Display Inversion off Unitsplay Inversion Image: Command off Image: Command off Image: Command off Imag		I IN A.	Partial W	iode On,		e On, Siee	p Qui				Yes			
Default Staus Default Value Power On Sequence Display Inversion off S/W Reset Display Inversion off H/W Reset Display Inversion off H/W Reset Display Inversion off Image: Signal provision of the second			71.		Sleep III		ルビ				162			
Default Staus Default Value Power On Sequence Display Inversion off S/W Reset Display Inversion off H/W Reset Display Inversion off	$\mathbb{Z} = \mathbb{Z} = \mathbb{Z}$	U U												
Default Power On Sequence Display Inversion off S/W Reset Display Inversion off H/W Reset Display Inversion off					Status					Defa	ault Valu	le		
S/W Reset Display Inversion off H/W Reset Display Inversion off Display Inversion Image: Command off the second se	Default		MMZ	Power	On Sequ	ience				Display	Inversio	on off		
H/W Reset Display Inversion off Display Inversion Legend On Mode Command Parameter Display INVOFF(20h) Display Display Inversion Mode Off Mode Sequential transfer Inversion			171.	S S	W Rese	t				Display	Inversion	on off		
Flow Chart			U	Н	/W Rese	t				Display	Inversion	on off		
Flow Chart														
Flow Chart Display Inversion On Mode Display Inversion On Mode Display Inversion Display Inversion Off Mode Sequential transfer											egen			
Flow Chart Flow Flow Flow Flow Flow Flow Flow Flow					solav In	version	\backslash							
Flow Chart Flow Chart				(On Mo	ode)							
Flow Chart				\sim			/				ommar			
Flow Chart INVOFF(20h) Display Inversion Off Mode Sequential transfer					Ļ						aramet	er Z		
Flow Chart Display Inversion Off Mode Sequential transfer				_										
Display Inversion Off Mode Sequential transfer	Flow Chart					(20h)					Display			
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Off Mode Sequential transfer				(D	splay In	version					Mode			
Sequentia transfer				\sim	Off Mo	ode	/					<u> </u>		
										i s	equent	ia		
											transfe	r		
										L		i		

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INVON: Display Inversion On (2100h)

		۸dd	rooo				Poromot	or				
Inst / Para	R/W	Auu	Othoro		7	De			D0	D 2		
	\\//vite		Others			Do	U5 + (0000k	D4		D2	DI	DU
	write	210	2100h		NO A	rgumen			DLI/F)			
NOTE: "-" Don't car	re Tri i											
Description	This c This c This c To exi (Exam	ommanc ommanc ommanc t from D ıple)	d is used d makes d does no isplay Inv	to enter display inversion no change of contents of ot change any other state version On, the Display	n mod f fram us. Invers	de. ne mem sion Off	ory. commai	nd (20h Display) shoul	d be wr	itten.	7
Restriction	This c	ommanc	has no	effect when module is a	ready	/ in Inve	rsion O	1 mode		3		
Register Availability		Normal N Normal N Partial M Partial M	Mode On Mode On, Iode On, Iode On,	Status I, Idle Mode Off, Sleep O I, Idle Mode On, Sleep O I, Idle Mode Off, Sleep O Idle Mode On, Sleep O Sleep In Status r On Sequence	ut ut ut			Ava Defa	vilability Yes Yes Yes Yes Yes ult Valu	Je Don off		
Delauit		la.	S H	S/W Reset			 [])isplay)isplay	Inversio Inversio	on off on off		
Flow Chart				Display Inversion Off Mode INVON(21h) Display Inversion On Mode					egend ommar rramete Display Action Mode equenti			

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ALLPOFF: All Pixel Off (2200h)

Г	Inct / Para		Add	ress				Parame	ter				
	ilist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
	ALLPOFF	Write	22h	2200h		No	Argume	nt (0000	h in MD	DDI I/F)			
٨	IOTE: "-" Don't car	е											
	Description	This c registe This c This c "All Pi The d	command or can be ommand ommand ommand nand ommand ommand ommand ommand ommand ommand ommand ommand ommand ommand	d turns ti e on or of d makes no d does no Mer Mer , "Norma anel is si	he display panel bla if. no change of content ot change any other s mory I Display Mode On" of howing the content of	ck in \$ s of fra tatus.	Sleep Or me men ial Mode rame me	on" comory a	e and a Display	status (E s are us	of the xample sed to les splay C	Display) eave this Dn" and f	On/Off mode. 'Partial
	Restriction	This c	ommand	has no	effect when module is	alrea	dy in All	Pixel Of	f mode.	3			
	Register Availability		Vormal N Vormal N Partial M Partial M	Mode On Mode On Mode On, Mode On,	Status , Idle Mode Off, Sleep , Idle Mode On, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	o Out o Out o Out o Out		5	Av	railability Yes Yes Yes Yes Yes	<i>y</i>		
	Default			Power S H	Status On Sequence /W Reset /W Reset				Defa All All All	ault Valu pixel of pixel of pixel of	ue f f f		





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ALLPON: All Pixel On (2300h)

Inst / Pore		Add	ress				Parame	ter				
ilist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
ALLPON	Write	23h	2300h		No	Argume	nt (0000	h in MD	DDI I/F)			
NOTE: "-" Don't car	e											
Description	This c registe This c This c (Exam "All Pi The d Mode	xels Off On con	d turns t e on or of d makes d does no d es no does no d does no d does no d does no d	he display panel whi ff. no change of contents ot change any other st Memory I Display Mode On" of howing the content of	te in S s of fra tatus.	ial Mode	ut mode nory.	p D D D D D D D D D D D D D D D D D D D	status	of the lesplay O	Display	On/Off mode. "Partial
Restriction	This c	ommano	has no	effect when module is	s alrea	dy in all	Pixel Or	n mode.	10.			
Register Availability		Normal I Normal I Partial M Partial M	Mode On Mode On Mode On, Mode On,	Status , Idle Mode Off, Sleep , Idle Mode On, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	Out Out Out Out),	Av	vailability Yes Yes Yes Yes Yes	/		
Default			Power S H	Status On Sequence /W Reset /W Reset				Defa All All All	ault Valu pixel of pixel of pixel of	ue f f f		





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GAMSET: Gamma Set (2600h)

		Add	ress				Parame	ter						
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
GAMSET	Write	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0		
NOTE: "-" Don't car	e													
	This c curves descri	comman s can b bed in th	d is use e selecte ne Table.	d to select the desir ed. The curve is se	ed Gan lected	nma cur by setti	rve for t ng the	he curr appropi	ent disp iate bit	in the	maximu parame	m of 4 eter as		
		GC[7:0	D]	Parameter			Curve	e Select	ed					
Description		01h		GC0		Ga	amma C	urve 1 (G=2.2)		-			
		02h		GC1			Re	served		A n				
		04h		GC2			Re	served				2		
		08h		GC3			Re	eserved	H					
	Note:	All other	r values a	are undefined.						100				
Restriction	Value: curve	s of GC until vali	[7:0] not id is rece	shown in table above ived.	e are in	valid an	d will no	tchang	e the cu	irrent se	elected g	jamma		
				0						3				
				Status		U V		Av	ailability					
Deviaten		Normal I	Mode On	, Idle Mode Off, Slee	p Out		1		Yes					
Register		Normal I	Mode On	, Idle Mode On, Slee	p Out		\sim		Yes					
Availability		Partial Mode On, Idle Mode Off, Sleep Out Yes												
	N	Partial Mode On, Idle Mode On, Sleep Out Yes												
				Sleep In					Yes					
				alde	クレ	т —								
		- ~ ((Status				Defa	ault Valu	le				
Default	-fi	$\frac{111}{111}$	Power	On Sequence					01h					
		<u>191</u>							01h					
		₩ Ŭ	Г	I/W Resel					UTH					
Flow Chart			G	AMSET(26h) GC[7:0] New Gamma Jurve Loaded				Cor Par Di A Sec	egend nmand ameter splay ction Aode quentia					

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DISPOFF: Display Off (2800h)

	1						-					
Inst / Para	R/W	Add	ress				Paramet	er				
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DISPOFF	Write	28h	2800h		No	Argume	nt (0000ł	n in MD	DI I/F)			
NOTE: "-" Don't car	re											
Description	This c disabl This c other (Exan	ommanc es and b commanc status. T iple)	l is used lank pag d makes here will	to enter into DISPLA e inserted. no change of conter be no abnormal visit Vemory	Y OFF I	node. Ir rame m t on the	n this moo	de, the 'his cor	output f	from Fra does n	ame Mer ot chang	nory is ge any
Restriction	This c	ommanc	has no	effect when module is	s alread	ly in Dis	play Off	mode.		1		
Register Availability Default		Normal M Normal M Partial M Partial M	Aode On Aode On, Iode On, Iode On, Node	Status , Idle Mode Off, Sleep Idle Mode On, Sleep Idle Mode On, Sleep Idle Mode On, Sleep Sleep In Status On Sequence /W Reset /W Reset	Out Out Out Out		5	Defa Dis Dis	ailability Yes Yes Yes Yes Yes ult Valu splay off splay off	Je f f		
Flow Chart				isplay On Mode)				egen ommar aramete Display Action Mode equent transfe			

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DISPON: Display On (2900h)

		۸dd	rocc				Paramot	or				
Inst / Para	R/W		Othora		דם			ים. עם	ςΩ	50		DO
DIODONI	VA ((ושוואו-ווטאו) נס.כיוןם	U/					υz	וט	00
DISPON	Write	29h	2900h		NO P	Argumer	nt (00001	n in MD	DLI/F)			
NOTE: "-" Don't car	re 											
Description	This c This c (Exam	ommanc ommanc ommanc iple)	I is used makes I does no Me	to recover from DISP no change of contents of change any other s	PLAY OF s of fran tatus.	F mode ne mem				Aemory	is enabl	ed.
Restriction	This c	ommanc	nas no	effect when module is	s airead	y in Disj	olay On	mode.		4		
Register Availability Default		Normal M Normal M Partial M Partial M	Aode On Aode On, Iode On, Iode On,	Status , Idle Mode Off, Sleep , Idle Mode Off, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In Status On Sequence	o Out o Out Out Out		3	Ava Defa Dis	Yes Yes Yes Yes Yes ult Valu play off	Je f		
U			у s н	/W Reset /W Reset				Dis Dis	play off play off	f		
Flow Chart				isplay Off Mode DISPON(29h) isplay On Mode)				Display Action Mode			

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CASET: Column Address Set (2A00h~2A03h)

			Add	ress				Parame	ter						
	Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
				2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		
				2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
	CASET	Write	2Ah	2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		
				2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
N	DTE: "-" Don't car	e						I	I						
	Description	This c This c Each (Exan	ommanc ommanc value rep nple)	I is used I makes presents	to define area of fram no change on the oth one column line in th XS[15:0]	me mem ner drive ne Fram XE[15:0]	er status e Memo	ere MPL	J can ac	cess.			n		
	Restriction	XS[15 When ignore For C MV = For C MV = For C MV = For C MV = For C MV = For C MV =	XS[15:0] always must be equal to or less than XE[15:0] When XS[15:0] or XE[15:0] is greater than maximum address like below, data of out of range will be gnored. For CGM[7:0] = "70h" (480 x 864 resolution) MV = "0": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 863 (035Fh) For CGM[7:0] = "6Bh" (480 x 854 resolution) MV = "0": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "0": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "0": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 799 (031Fh) For CGM[7:0] = "28h" (480 x 720 resolution) MV = "0": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "0": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "0": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "0": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh) MV = "1": Parameter range 0 \leq XS[15:0] \leq XE[15:0] \leq 479 (01DFh)												
	Register Availability		Normal M Normal M Partial M Partial M	<i>l</i> lode On lode On lode On lode On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes	,				

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RASET: Row Address Set (2B00h~2B03h)

last / Dere		Add	ress				Parame	ter						
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
			2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		
DAOFT	\A/ ··		2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
RASET	vvrite	2BN	2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		
			2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
NOTE: "-" Don't car	e													
Description	This c This c Each (Exan	ommanc ommanc value rep iple)	d is used d makes presents	to define area of fram no change on the oth one column line in th YS[15:0]	me mem ner drive ne Fram	ory whe r status e Memo	ere MPL	J can ac	cess.			7		
Restriction	YS[15 When ignore For C MV = For C	$\begin{aligned} \begin{array}{c} (110.0) & (110.0) & (110.0) \\ \hline \\ YS[15:0] always must be equal to or less than YE[15:0] \\ When YS[15:0] or YE[15:0] is greater than maximum address like below, data of out of range will be ignored. \\ For CGM[7:0] = "70h" (480 × 864 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 863 (035Fh) \\ MV = "1": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "6Bh" (480 × 854 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 853 (0355h) \\ MV = "1": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "50h" (480 × 800 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "50h" (480 × 720 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "28h" (480 × 720 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "28h" (480 × 720 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "00h" (480 × 640 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "00h" (480 × 640 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "00h" (480 × 640 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "00h" (480 × 640 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "00h" (480 × 640 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "00h" (480 × 640 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "00h" (480 × 640 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For CGM[7:0] = "00h" (480 × 640 resolution) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 639 (027Fh) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 639 (027Fh) \\ MV = "0": Parameter range 0 & XS[15:0] & XE[15:0] & 479 (01DFh) \\ For $												
Register Availability		Normal N Normal N Partial M Partial M	Mode On Mode On Node On Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes	,				

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RAMWR: Memory Write (2C00h)

	, .												
Inst / Para	B/W	Add	ress	Parameter									
mot / r ara		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	
RAMWR	Write	2Ch	2C00h	D[15:8]	:	:	•	:	:	:	:	:	
				D[15:8]		De	D5	D4		D2	D1		
NOTE: " " Don't oor												00	
NOTE Dont car	This command is used to transfer data from MPU interface to frame memory												
	This command is used to transfer data from MPU Interface to frame memory.												
	When this command is accepted, the column register and the row register are resetuto the Start												
Description	Colum	nn/Start I	Row pos	itions.		giotor t		1011 10	giotor			oluit	
	The S	tart Colu	ımn/Star	t Row positions are d	ifferent	in accor	dance v	vith MAI	DCTLS	etting			
	Then	D[23:0] i	s stored	in frame memory and	d the co	lumn reg	gister ar	nd the ro	w regis	ter incre	emented	1.	
	Sendi	ng any o	ther com	mand can stop Fram	ne Write			212	$N \overline{N}$	<u>\</u> U			
Restriction	There	here is no restriction on length of parameters. No access in the frame memory in Sleep In mode											
						2////							
				Status	TIL	<i>۵\</i> (۱		Av	ailabilit	2			
		Normal Mode On Idle Mode Off Sleep Out											
Register		Normal Mode On, Idle Mode On, Sleep Out											
Availability		Partial Mode On, Idle Mode Off, Sleep Out											
		Partial Mode On, Idle Mode On, Sleep Out											
	Sleep In Yes												
1													
		Status Default Value											
	- 1	Power On Sequence Contents of memory is set randomly									lv.		
Default	5		SM	Reset	Contents of memory is set randomly								
1 -		$\frac{111}{111}$	HW	Reset	Contents of memory is set randomly								
	Contents of memory is set randomly												
		U											
								[]					
									egeno				
			F	RAMWB(2Ch)									
								l l					
				Image Data				i/ Pa	ramete	r /¦			
			(D1	[23:0], D2[23:0],									
Flow Chart				, Dn[23:0]	Display								
					Action								
				and Commonal									
				iny Command									
								<u>'</u> _ '	NOUE	\mathcal{I}_{L}			
								Se	quentia				
							transfer						
								`		' 			
										!			

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RAMRD: Memory Read (2E00h)

	, 											
Inst / Para	R/W	Add	ress									
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
RAMRD	Read	2Eh	2E00h	D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
NOTE: "-" Don't car	e											
	This c	ommand	d is used	to transfer data from	frame i	nemorv	to MPU	interfa	ce.			
Description	This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTR setting.											
	incren	incremented										
	Frame	e Read c	an be ca	inceled by sending an	ny other	comma	ind.				<u> </u>	
Restriction	Ihere	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode										
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On Idle Mode Off, Sleep Out Yes										
	~ ~	Partial Mode On, Idle Mode On, Sleep Out Yes										
		Sleep In Yes										
Default		Status Default Value Power On Sequence Contents of memory is set randomly S/W Reset Contents of memory is set randomly H/W Reset Contents of memory is set randomly										
Flow Chart				RAMRD(2Eh) Image Data 23:0], D2[23:0], , Dn[23:0]					egend mmano ramete risplay Action Mode quentia ansfer			

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PTLAR: Partial Area (3000h~3003h)

Inst / Dara		Address		Parameter									
mst / Lara	Fi/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
PTLAR			3000h	00h	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
	Write	30h	3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
	vvnie	5011	3002h	00h	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
			3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	
NOTE: "-" Don't car	TE: "-" Don't care												
Description	This c comm figures If End	command and, the s below. Row > S Start PSL End PEL Start Row < S End PEL Start Row = S	d defines first def PSL and Start Rov (15:0]	s the partial mode's ines the Start Row (F d PEL refer to the Fra v when MADCTL ML v when MADCTL ML v when MADCTL ML	display PSL) and ame Mer =0: Non-d Non-d F1: Non-d =0: Non-d a will be	area. T d the se mory row isplay Ar isplay Ar isplay Ar splay Ar splay Are	rhere ar cond the waddress ea ea ea ea ea ea ea ea ea ea ea ea ea	re 4 part e End R ss coun	rameter: ow (PE ter.	s assoc L), as ill rtial Disp	iated w ustratec olay Area lay Area	ith this I in the	

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	PSL[15:0] and PEL[15:0] should have below range									
Restriction	CGM[7:0] = "70h" (480 x 864): 0 ≦ PSL[15:0], PEL[15:0] ≦ 863 (035Fh), PEL–PSL ≦ 863 (035F									
	$CGM[7:0] = "6Bh" (480 \times 854): 0 \leq PSL[15:0], PE$	$L[15:0] \leq 853 (0355h), PEL-PSL \leq 853 (0355h)$								
	$GM[7:0] = "50h" (480 \times 800): 0 \le PSL[15:0], PEL[15:0] \le 799 (031Fh), PEL-PSL \le 799 (031Fh)$									
	$CGM[7:0] = "28h" (480 \times 720): 0 \le PSL[15:0], PEL[15:0] \le 719 (02CFh), PEL-PSL \le 719 (02CFh)$									
	$CGM[7:0] = "00h" (480 \times 640): 0 \leq PSL[15:0], PEI$	$[15:0] \leq 639 (027Fh), PEL-PSL \leq 639 (027Fh)$								
	Status	Availability								
	Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes 🕥								
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes								
	Partial Mode On, Idle Mode On, Sleep Out	Yes								
	Sleep In	Yes								
	Dabulk Value									
	Status									
		035Eb (863d) if CCM[7:0] = "70b"								
		0355h (853d) if CGM[7:0] = "6Bh"								
		031Fh (799d) if CGM[7:0] = "50h"								
	Power On Sequence	0000h 02CFh (719d) if CGM[7:0] = "28h"								
		027Fh (639d) if CGM[7:0] = "00h"								
		0167h (359d) if CGM[7:0] = "FEh"								
		035Fh (863d) if CGM[7:0] = "70h"								
Default	FUI ALSUF	0355h (853d) if CGM[7:0] = "6Bh"								
Delaun	SAM Depart	031Fh (799d) if CGM[7:0] = "50h"								
	Sivi nesei	02CFh (719d) if CGM[7:0] = "28h"								
		027Fh (639d) if CGM[7:0] = "00h"								
U		0167h (359d) if CGM[7:0] = "FEh"								
		035Fh (863d) if CGM[7:0] = "70h"								
	V	0355h (853d) if CGM[7:0] = "6Bh"								
	LIAM Depart	031Fh (799d) if CGM[7:0] = "50h"								
	H/W Reset	02CFh (719d) if CGM[7:0] = "28h"								
		027Fh (639d) if CGM[7:0] = "00h"								
		0167h (359d) if CGM[7:0] = "FEh"								

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5		Add	ress	Parameter											
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
TEOFF	Write	34h	3400h		No	Argume	rgument (0000h in MDDI I/F)								
NOTE: "-" Don't car	е					0			,						
Description	This c	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.													
Restriction	This c	nis command has no effect when Tearing Effect output is already OFF.													
			Availability												
		Normal N	Mode On	, Idle Mode Off, Sleep	o Out				Yes		Π				
Register		Normal N	Mode On	, Idle Mode On, Sleep	o Out				Yes	n R					
Availability		Partial N	lode On,	Idle Mode Off, Sleep	o Out				Yes		211	2			
		Partial N	lode On,	Idle Mode On, Sleep	o Out	Yes									
				Sleep In			216		Yes						
					/	2111									
				<u>.</u>	11					2					
				Status											
Default			Power	Learing Effect off											
				learing Effect off											
		H/W Reset													
						()	\sim								
		<u>' </u>	_		Legend										
		0		Line Output ON	Y			į		—1					
		- 6	1, 1		/				ommar						
	5	M						jĽ	ommai						
U -		N M						¦/Pa	aramet	er /					
	`		<u> </u>	TEOFE(24b)						<u> </u>					
Flow Chart		U		TEOFF(34n)					Display	/)¦					
Flow Ghart									. ,						
			_	•				i <	Action	>					
			(те						Mode	<u> </u>					
					/			j 🖵	woue	\square_{+}					
								1/s	equent	ial					
								1	transfe	r_l					
								-		i					
										'					

TEOFF: Tearing Effect Line OFF (3400h)

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TEON: Tearing Effect Line ON (3500h)

		Add	ress	-			Parame	ter						
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
TEON	Write	35h	3500h	00h	-	-	-	-	-	-	-	M		
NOTE: "-" Don't car	е Э	0011	000011											
Description	This c not afi The T Line. (When When	fected by earing E ("-" = Don M = "0": Ver Sca M = "1": Ver Sca During S	d is used / changir ffect Line n't Care) The Tea tival Time lle The Tea tival Time lle Sleep In I	to turn ON the Tearing og MADCTL bit ML. e On has one parame aring Effect Output lir aring Effect Output lir aring Effect Output lir Mode with Tearing Effect	ng Effec eter, whi he consis t _{vc}	t output ch desc sts of V d sts of bo	signal f ribes th Blankin oth V-Bl earing E	rom the e mode g inform t _{vdh}	e TE sig of the T nation o and H-B	nal line. Fearing nly. Hinking i	This ou Effect O nformat	tput is utput		
Restriction	This c	ommand	has no	effect when Tearing	Effect or	utput is	already	ON.	シア					
Register Availability Default		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Tearing Effect off S/W Reset Tearing Effect off H/W Reset Tearing Effect off												
Flow Chart	TE Line Output OFF TEON(35h) TE Mode Parameter (M) TE Line Output ON TE Line Output ON Legend Command Parameter Display Action Mode Sequential transfer													

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	-			. ,									
last / Dara		Ado	dress				I	Parame	ter				
inst / Para	Π/ ٧٧	MIPI	Others	D[15:8] (Non-N	/IPI)	D7	D6	D5	D4	D3	D2	D1	D0
MADCTL	Write	36h	3600h	00h		MY	MX	MV	ML	RGB	MH	RSMX	RSMY
NOTE: "-" Don't care	Э											-	
	This c	omman	d defines	read/write scar	nning	directio	n of fran	ne mem	ory.				
	This c	omman	d makes	no change on th	ne oth	ner drive	er status						
	Bi	t	N	AME				DES	SCRIPT	ION			
	N	IY R	low Addre	ess Order	The	se 3 bit	s contro	ls interfa	ace to n	hemory	write/re	ad direc	tion.
	N	IX C	olumn Ac	dress Order	The	behavi	or on dis	splay aft	er patte	ern chan	ged.	1	
	N	IV R	low/Colur	nn Exchange									
	Ν	1L V	ertical Re	efresh Order	TFT Imm	LCD V	ertical re / behavi	efresh d or on di	irection splay.	control.			2
				Ordor	Colo	or selec	tor switc	h contro	ol "+" D				
		ח סג	IGD-DGN	Order	Imm	ediatel	/ behavi	or on di	splay		r seque	ence	
	N	IH H	lorizontal)rder	Refresh	TFT	· LCD H	orizonta / behavi	l refresi or on di	n directi splay.	on contr	rol		
	RS	MX F	lip Horizo	Intal	Flip: Imm	s the dia rediately	play im / behavi	age left or on di	to right. splay.	21			
	RS	MY F	lip Vertica		Flips	s the dis rediate	splay im / behavi	age top or on di	to dowr splay.	1.			
Description	M				VIL: V	ertical	Refresh	Order					
		V IL	Top-Le	eft (0,0) Memor	у	ノビ	3	Top-Le	ft (0,0)	Displa	у		
MO /	[]] [ML	_"0" 				Send Send Send Send Send	1st 2nd 3rd					
			Top-Le	eft (0,0) Memor	у		0	Top-Le	eft (0,0)	Displa			
		ML	="1"				Send I Send 3 Send 2 Send 2	<u>ast</u> > 3rd 2nd 1st					

MADCTL: Memory Data Access Control (3600h)

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IDMOFF: Idle Mode Off (3800h)

		Address Parameter										
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
IDMOFF	Write	38h	3800h	· · · · · · · · · · · · · · · · · · ·	No	Argumer	nt (0000	h in MC	DI I/F)		•	
NOTE: "-" Don't cai	'e					0	,		,			
Description	This c In the	ommand idle off r	l is used node, dis	to recover from Idle r splay panel can displa	node o ıy maxi	n mum 16	.7M colo	ors.				
Restriction	This c	ommanc	has no	effect when module is	s alread	ly in Idle	Off mod	de.				
Register Availability		Normal M Normal M Partial M Partial M	Mode On Mode On, Iode On, Iode On,	Status , Idle Mode Off, Sleep , Idle Mode On, Sleep Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	o Out o Out o Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			1
Default			Power S	Status On Sequence /W Reset				Defa Idle Idle Idle	ault Valu Mode o Mode o Mode o	Je off off		
Flow Chart				Idle On Mode)				ommar aramete Display Action Mode equent transfe			

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IDMON: Idle Mode On (3900h)

	D 444	Add	ress				F	Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (N	lon-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
IDMON	Write	39h	3900h		· •	No /	Argumen	t (0000	h in MD	DI I/F)			
NOTE: "-" Don't car	е						0	,		,			
	This c In the each I	ommanc idle on n R, G, and	l is used node, co d B in Fra	to enter int lor express ame Memo	o Idle moc ion is redu ry, 8 color	le on. Iced. Th depth o	ne primai data is di	ry and t splayed	he seco 1.	ndary o	colors u	sing MS	B of
Description			Me	Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important Important									7
NON	Memory Contents vs. Display Colors R7R6R5R4R3R2R1R0 R7G6G5G4G3G2G1G0 B7B6B5B4B3B2B1B0 Black 0XXXXXXX 0XXXXXXX 0XXXXXXX Blue 0XXXXXXX 0XXXXXXX 0XXXXXXX Green 0XXXXXX 1XXXXXXX 0XXXXXXX Cyan 0XXXXXX 1XXXXXXX 0XXXXXXX Yellow 1XXXXXXX 1XXXXXXX 0XXXXXXX White 1XXXXXXX 1XXXXXXX 1XXXXXXX												
Restriction	This c	ommanc	has no	effect wher	n module is	s alread	ly in Idle	On mo	de				
Register Availability		Normal M Normal M Partial M Partial M	<i>l</i> ode On <i>l</i> ode On, lode On,	Status , Idle Mode , Idle Mode Idle Mode Idle Mode Sleep In	o Out o Out o Out o Out o Out			Ava	ailability Yes Yes Yes Yes Yes	/			
Default		Status Power On Sequence S/W Reset H/W Reset							Defa Idle Idle Idle	ult Valu Mode c Mode c Mode c	ue off off		





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Inst / Para R/W MIPI Others D[15:8] (Non-MIPI) D7 D6 D5 D4 D3 D2 COLMOD Write 3Ah 3A00h 00h VIPF3 VIPF2 VIPF1 VIPF0 IFPF3 IFPF2 NOTE: "-" Don't care This command is used to define the format of RGB picture data, which is to be transferred interface. The formats are shown in the table: DESCRIPTION Bit NAME DESCRIPTION "0101" = 16-bit/pixel "0110" = 18-bit/pixel VIPF3 VIPF2 Pixel Format for RGB Interface "0110" = 18-bit/pixel "0111" = 24-bit/pixel Description VIPF0 Pixel Format for RGB Interface "0111" = 24-bit/pixel The others = not defined	D1 IFPF1	D0 IFPF0 RGB											
COLMOD Write 3Ah 3A00h 00h VIPF3 VIPF2 VIPF1 VIPF0 IFPF3 IFPF2 NOTE: "-" Don't care This command is used to define the format of RGB picture data, which is to be transferred interface. The formats are shown in the table: Bit NAME DESCRIPTION VIPF3 VIPF2 Pixel Format for RGB Interface "0101" = 16-bit/pixel "0110" = 18-bit/pixel Description VIPF1 VIPF0 Pixel Format for RGB Interface "0111" = 24-bit/pixel	IFPF1	IFPF0 RGB											
NOTE: "-" Don't care This command is used to define the format of RGB picture data, which is to be transferred interface. The formats are shown in the table: Bit NAME DESCRIPTION VIPF3 VIPF2 Pixel Format for RGB Interface "0101" = 16-bit/pixel UIPF1 VIPF0 Pixel Format for RGB Interface "0111" = 24-bit/pixel	d via the	RGB											
Description This command is used to define the format of RGB picture data, which is to be transferred interface. The formats are shown in the table: Bit NAME DESCRIPTION VIPF3 VIPF2 VIPF1 Pixel Format for RGB Interface "0101" = 16-bit/pixel "0111" = 24-bit/pixel "0111" = 24-bit/pixel The others = not defined "0101"	d via the	RGB											
Bit NAME DESCRIPTION VIPF3 VIPF2 Pixel Format for RGB Interface "0101" = 16-bit/pixel VIPF1 VIPF0 Pixel Format for RGB Interface "0111" = 24-bit/pixel													
Bit NAME DESCRIPTION VIPF3 VIPF2 "0101" = 16-bit/pixel VIPF1 Pixel Format for RGB Interface "0101" = 18-bit/pixel VIPF0 Pixel Format for RGB Interface "0111" = 24-bit/pixel													
VIPF3 VIPF2 VIPF1 Pixel Format for RGB Interface "0101" = 16-bit/pixel '0110" = 18-bit/pixel "0111" = 24-bit/pixel '0111" = 24-bit/pixel The others = not defined													
Description VIPF2 VIPF1 VIPF0 Pixel Format for RGB Interface "0110" = 18-bit/pixel "0111" = 24-bit/pixel "0111" = 24-bit/pixel The others = not defined "0110"													
Description VIPF1 "0111" = 24-bit/pixel VIPF0 The others = not defined	n												
VIPF0 The others = not defined													
		2											
"0101" = 16-bit/pixel	UL-												
IFPF2 Pixel Format for Control Interface 0110 = 10-Dupixel IFPF1 Pixel Format for Control Interface "0111" = 24-bit pixel													
The others = not defined													
	There is no visible effect until the Frame Memory is written to.												
Restriction I here is no visible effect until the Frame Memory is written to:													
Cterro	Status												
Normal Mode On Idla Mode Off Sloop Out													
Register Normal Mode On, Idle Mode On, Sleep Out Ves													
Availability Partial Mode On, Idle Mode Off, Sleep Out Yes													
Partial Mode On, Idle Mode On, Sleep Out Yes													
Steep In Yes													
Status Default Value													
Default Power On Sequence 77h													
S/W Reset 77h													
H/W Reset 77h													
(24-bit/pixel Mode)													
Parameter													
COLMOD(3Ah)													
Flow Chart Display													
Raramotor /													
/ IFPF[3:0] = "0110" /													
(18-bit/pixel Mode)													

COLMOD: Interface Pixel Format (3A00h)

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RAMWRC: Memory Write Continue (3C00h)

		Add	ress				Parame	ter					
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	
RAMWRC	Write	3Ch	3C00h	D[15:8]	:	:	:	:	:	:	:	:	
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	
NOTE: "-" Don't car	e			_[::::0]									
	This o	comman	d is use	d to transfer data fr	om MP	U interfa	ace to	frame m	nemory,	if there	e is war	nted to	
	contin	ue mem	ory write	after "RAMWR Mem	ory Wri	te (2Ch)	" comm	and.					
	This c	ommano	d makes	no change to the oth	er drive	r status.					Π		
Description	When	this cor	mmand i	s accepted, the colu	mn reg	ister an	d the ro	ow regis	ter are	not res	et to th	e Start	
	Colum	nn/Start	Row pos	itions. t Row positions are d	ifforont	in accor	danco v			otting	シート	2	
	The S	D[23:0] i	s stored	in frame memory and	the co	lumn rei	nister ar	nd the ro		etting ter incre	ementer	4	
	Sendi	ng anv g	ther con	mand can stop Fram	ne Write		gister a		, wiegis				
Restriction	There	is no re	striction	on length of parameter	ers. No	access	in the fr	ame me	mory in	Sleep I	n mode		
				<u> </u>	NIC		じ		- 1	3			
				Status	1112			Av	ailability				
		Normal N	Mode Or	, Idle Mode Off, Slee	n Out		4	TIC	Yes				
Register	Normal Mode On, Idle Mode On, Sleep Out Yes												
Availability		Partial N	lode On	, Idle Mode Off, Sleep	o Out 🥖		51		Yes				
		Partial N	lode On	, Idle Mode On, Sleep	Out		$\overline{\mathcal{A}}$	9	Yes				
		11 11		Sleep In					Yes				
		<u>, </u>											
		~	5		2								
	ľ 느	(Sta	atus			[Default \	Value				
Default	\mathcal{L}	P	ower On	Sequence		Con	tents of	memory	y is set	random	ly		
0			S/W	Reset		Con	tents of	memory	y is set i	random	ly		
		\overline{n}	H/W	Reset		Con	tents of	memor	y is set i	random	ly		
							ſ						
							ļ	LC	yenu				
			Γ	RAMWRC(3Ch)				\sim		1:			
				•				Corr	nmand	Jį			
				Image Data			İ	Para	meter	7			
			([1[23:0], D2[23:0],									
Flow Chart				, Dn[23:0]				Dis	splay)			
r iow chart				•				\geq					
			Г	Any Command					tion	> ¦			
			L	, any command			ļ	M	ode)			
								000	uentia				
								(tra	nsfer) I			
								\sim		⊐i			
										-1			

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RAMRDC: Memory Read Continue (3E00h)

		Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
RAMRDC	Read	3Eh	3E00h	D[15:8]	:		:	:	÷	:	:	:
		-		D[15:8]	D7	De	D5	D4	50	י. רם	D1	
NOTE: "-" Don't car	<u>م</u>			D[10.0]		DU	00	7	00	02		00
	This d	comman	d is use	d to transfer data fr	om fran	ne mer	norv to	MPII in	terface	if there	- is war	nted to
	contin	ue mem	ory write	after "RAMRD Memo	ory Rea	d (2Eh)'	" comma	and.	torrado,			
	This c	ommano	d makes	no change to the oth	er drive	r status.					n	
	When	this cor	mmand i	s accepted, the colu	mn reg	ister an	d the ro	w regis	ter are	not res	et to th	e Start
Description	Colum	nn/Start	Row pos	itions.							シル	2
	The S	tart Colu	ımn/Star	t Row positions are d	ifferent	in accor	dance v	vith MAI	OCTR s	etting.	11C	
	Then	D[23:0]	is read	back from the fram	ne mem	iory and	d the c	olumn r	egister	and th	e row r	egister
	Erame	nented Boad o	an he ca	uncoled by sending a	av other	commo	and	2				
Bestriction	Thoro	is no re	arriction	on length of parameter	Ty Uner	200000	in the fr	omo mo	morv in	Sloon I	n mode	
Trestriction	THEFE	13 110 16	Striction			access					minoue	
				Status				1	oilchilit			
		Normal	Inda On	Status			R	AV	Anability			
Register		Normal		I, Idle Mode On, Slee	p Out			. 111 .	Vee			
Availability		Partial A	Inde On	, Idle Mode Off, Slee			\sum		Voc			
1	R	Partial N		Idle Mode On, Sleep					Vac			
\mathcal{P}		1 annai 1		Sleen In					Yes			
		00	1									
	<u> </u>	6										
	~		Sta	atus			[Default V	Value			
Default		<u>P</u>	owe <mark>r</mark> On	Sequence		Con	tents of	memory	y is set i	random	ly	
201001		12	S/W	Reset		Con	tents of	memory	y is set i	random	ly	
		U	H/W	Reset		Con	tents of	memor	y is set i	random	ly	
							Ī					
								Le	gend			
			Г	RAMRDC(3Eh)				_		1!		
			L				į	Com	mand			
				Imaga Data			i			- 7		
			(r	01[23:0], D2[23:0],			ľ	/ Para	Imeter	/i		
Flow Chart				, Dn[23:0]				Dis	nlav	١		
Flow Chart							į		piay			
			r				i		tion	> ¦		
			L	Any Command					ode			
							!		oue			
							į	Seq	uential	\sum		
								tra	nster	≤¦		
							<u> </u>			_i		

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Inct / Para		Add	lress				Parame	ter					
illst / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
OTEOI	\\/rito	14b	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8	
SIESL	vvnie	440	4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0	
NOTE: "-" Don't car	е												
	This c	command	d turns o	n the display module ³	s Tearii	ng Effec	t output	signal c	on the T	E signa	l line wh	en the	
	displa	y modul	e reache	s line N. The TE sign	al is no	affecte	d by cha	anging N	MADCT	L bit ML			
	The T	earing E	ffect Line	e On has one parame	eter, wh	ich desc	ribes th	e mode	of the 7	Fearing	Effect C	output	
	Line r	node. Th	ne Tearin	g Effect Output line c	onsists	of V-Bla	anking ir	nformati	on only.		Π		
		Ve	rtival Time		L.	/dl	•	L _{vdh}		n A			
Description		Sca	ale	/ \					1 Au			2	
	Note	that STE	SL with I	N[15:0]="000h" is equ	uivalent	to TEOI	N with N	1∋"0"	N N		UL		
	The T	earing E	ffect Out	put line shall be activ	ve low w	hen the	display	module	is in Sl	eep in n	node.		
	This o	comman	d takes	affect on the frame	followir	ig the c	urrent f	rame. T	Therefor	e, if the	e TE ou	utput is	
	already on, the TE output shall continue to operate as programmed by the previous "TEON (35h)" o "STESL (44h) command" until the end of the frame.												
	"STES	STESL (44h) command" until the end of the frame.											
	When	When N[15:0] is greater than maximum scanning line like below, data of out of range will be ignored. For CGM[7:0] = "70h" (480 x 864 resolution)											
	For C Para	GIVI[7:0]	= 700		260b)	6	$\gg \parallel$						
	For C	GM[7:0]	= "6Bh"	480 x 854 resolution)		5		1				
	Para	meter ra	inge 0	$N[15:0] \leq 854 (03)$, 356h)	())	\sim						
Restriction	For C	GM[7:0]	= "50h" (480 x 800 resolution		\bigcirc							
	Para	meter ra	inge 0 ≦	≦ N[15:0 <mark>]</mark> ≦ 800 (03	320h)								
	For C	GM[7:0]	= "28h"	480 x 720 resolution									
	Para	meter ra	inge 0 🛓	≦ N[15:0] ≦ 720 (02	2D0h)								
	For C	GIM[7:0]	= "000" (480 X 640 resolution) 2006)								
ų -	Fala			$ \mathbf{H}[13.0] \ge 040 (02)$	20011)								
				Status				Δν	ailability	,			
		Normal I	Mode On	Idle Mode Off Slee	n Out			7.0	Yes	/			
Register		Normal I	Mode On	, Idle Mode On, Slee	p Out				Yes				
Availability		Partial N	/lode On	, Idle Mode Off, Sleep	o Out				Yes				
		Partial N	/lode On	, Idle Mode On, Slee	o Out				Yes				
				Sleep In					Yes				
				Status				Defa	ault Valu	le			
Default			Power	r On Sequence				(0000h				
			S	S/W Reset				(0000h				
			ŀ	I/W Reset				(0000h				
1												_	

STESL: Set Tearing Effect Scan Line (4400h~4401h)

11/8/2010





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GSL: Get Scan Line (4500h~4501h)

hast (Dava		Add	ress				Parame	ter						
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
	Dood	45b	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8		
GSL	Reau	4011	4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0		
NOTE: "-" Don't care	е													
Description	This c scan I first lir When	command lines on ne of V S in Sleep	d returns display is sync and o in mode	the current scan line s defined as VSYNC is denoted as Line 0 e, the returned value	e, N, use + VBP is unde	ed to up + VADF fined.	date the R + VFF	e display P. The fi	/ modul rst scar	e. The t I line is	otal nur defined	nber of as the		
Restriction	-													
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes												
Default Flow Chart	Status Default Value Power On Sequence XXXXh S/W Reset XXXXh HW Reset XXXXh HW Reset XXXXh GSL(45h) Host GSL(45h) Legend V Driver Send Parameter Display N[15:8] Action Mode Sequential													

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		Adu	drace	–	,		·	Daram	ator				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-	MIPI)	D7	D6			D3	D2	D1	00
	W/rito	X	4400h	00h	10111 17	0	0	0		0	0	0	ICM
	vvine	^	47000	0011		U	U	U	0	U	U	U	ICIVI
	e This c	omman	d ie ueod	to select SRAI	M data	innut n	oth and	dienlay	<u>, clock ir</u>		ntarfaca		
			10 13 0300	Data Writ	te to S	RAM	atriana	uispiay	SRAM	Data B	ead to D	Nisnlav	٦
Description	10	CM -	SBAM	Write Clock	SRA	M Data	Input P	Path	Inte	rnal Dis	eau to D	nopiay	-
Description	┃ ├──	0	F	CLK	0	D[2	3:01	4	V	S. HS a	nd PCLI	K	-
		1		SCL		SI		\rightarrow	lr	iternal C	Oscillato	r 🚬	1
Restriction	┠╧═										- ÎN		
Heathouth	_									-77		シア	3
				Status					Av	ailabilit			
	⊢	Normal	Mode Or	Idle Mode Off	f Slee	n Out		-15		Yes	5 11		
Register	⊢	Normal	Mode On	, Idle Mode On	ı, Slee	p Out	177	Mr		Yes			
Availability		Partial	Mode On	, Idle Mode Off	, Sleep	o Out				Yes	3		
		Partial I	Mode On	, Idle Mode On	, Sleep	Out				Yes			
				Sleep In			3		1/1	Yes			
	 				Ľ			\gg		<u>A</u> i			
			<u> 2 WL</u>			(<u>"</u>		$\underline{()}$	7			
	25	<u>11 </u>		Status				$\underline{\bigcirc}$	Defa	ault Valu	Je		
Default	A		Power	r On Sequence	<u>)((``</u>					M = "0"			
		$\mathcal{P}n$		3/W Reset	\mathcal{H}	ノビ				M = "0"			
$\otimes \mathbb{N}(\mathbb{N}) \otimes \mathbb{N}$	<u> </u>			I/W Reset)				IU	M = "0			
					_					L L	Lec	aend	-
-		Displa	av Clock	bv PCLK	(Display	/ Clock	by \	١				
					$\overline{\ }$	Interna	Oscilla	tor	1	1	Com	mand	!
										į		manu	<u> </u>
		DF	CKRGB	(4Ah)	Г	DPCKE	RGB (4A	h)		ļ,	/ Para	meter	7¦
		<u> </u>			L	Di cia		,		1-			
Flow Chart		<i></i>	<u> </u>		_		▼		7			play) i
		/ Par	ameter I	CM = 1	/ F	Parame	ter ICM	= 0 /	/		< Ac	tion	
	-									ļ			
		Di	∎ isplav Clo	ock by	\subset		V	$\overline{}$	۱	i		bde	1
			ernal Os	cillator	(Dis	splay C	lock by	PCLK)	ļ	Sequ	uential	7
		\sim			\sim						trar	nsfer	
										<u> </u>			_i

DPCKRGB: Display Clock in RGB Interface (4A00h)

11/8/2010

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	<u> </u>	Add	lress				Parame	ter					
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
DSTBON	Write	Х	4F00h	00h	0	0	0	0	0	0	0	DSTB	
NOTE: "-" Don't ca	re	<u>I</u>				_		-	-	-	_		
Description	This c DSTB Notes 1. Bel Us 2. It c 3. To	command S="1", en S: fore setti er can no an not e exit Dee	d is used ter deep ng this cr ot write th xit Deep ep Standk	to enter deep standb standby mode. ommand, enter Sleep his register in Sleep-C Standby Mode while by Mode, input low pu	o In Mod Out and Setting b Ilse mor	Display Dit DSTE e than 3	h) and I -On moo 3 from " 3 msec t	Display de. 1" to "0" o pin RI	Off (280 ESX.	00h) first		1	
Restriction	<u> -</u>							<u> </u>		<u> </u>			
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
Default	Status Default Value Power On Sequence DSTB = "0" S/W Reset DSTB = "0" H/W Reset DSTB = "0"												
Flow Chart		la.	((Sleep In and Display Off Mode DSTBM (4Fh) Parameter DSTB Deep Standby Mc	e = 1 ode			Le Com Dis Ac M. Seq tra	gend mand meter play tion ode uential nsfer				

DSTBON: Deep Standby Mode On (4F00h)

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WRPFD: Write Profile Value for Display (5000h~500Fh)

		bbΔ	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			5000h	00h	V017	V016	V015	V014	V013	V012	V011	V010
			5001h	00h	V027	V026	V025	V024	V023	V022	V021	V020
			5002h	00h	V037	V036	V035	V034	V033	V032	V031	V030
WRPFD	Write	50h	:	00h	:	:	:	:	:	:	:	:
			500Dh	00h	V147	V146	V145	V144	V143	V142	V141	V140
			500Eh	00h	V157	V156	V155	V154	V153	V152	V151	V150
			500Fh	00h	V167	V166	V165	V164	V163	V162	V161	V160
NOTE: "-" Don't car	re									11 1	<u> </u>	
Description	This c	ommanc	l is used	to define profile valu	es for d	isplay.		!			J.F	
Restriction	-							2 10				
						af	<u> 11/2</u>					
				Status	1			Av	ailability	/		
D		Normal N	Node On	, Idle Mode Off, Slee	p Out	2 // 2			Yes			
Register		Normal N	Node On	, Idle Mode On, Slee	p Out				Yes	2		
Availability		Partial N	lode On.	, Idle Mode Off, Sleep	Out		$ \mathbb{A} $		Yes			
		Partial N	lode On	, Idle Mode On, Sleep					Yes			
				Sleep II	π		$\overline{\mathbf{C}}$		165			
	ÎN	11 11										
		. U .		Status				Defa	ault Vali	Ie		Ĩ
	╽╟─	~	Power	On Sequence				2010	FFh			
Detault	╏┝─	n ((S	W Reset					FFh			
	\overline{C}	1111/2)) F	I/W Reset					FFh			
6		A	S									
		l -						· — 1			-	
					1			į	Lege	end	1	
			r								l I	
			l	WRPFD(50h)	J			- ۲	Comm	and	į	
				•		_		ίL	Comm	lanu		
			15	st Doromotor V01[7	01	7		- ¦ [Param	neter /	'	
			$\binom{1}{2^n}$	^d Parameter V02[7	.0] ·0] /	/					į	
Flow Chart			/ -	:				- i (Disp	lay)		
			/ 16	th Parameter V16[7	':0]							
		L						<	Actio	on >	ļ	
								İ	Мос	de)	1	
									trans	sfer)	
											Pj	
								<u> </u>			1	

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WRDISBV: Write Display Brightness (5100h)

	-	اداد ۸					D	4 a				
Inst / Para	R/W	Add	ress		D -	Da	Parame	ler			D (
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	DO
WRDISBV	Write	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
NOTE: "-" Don't cai	re											
	This c In prir bright	command nciple rel ness.	l is used ationship	to adjust brightness is that 00h value m	value. eans the	e lowest	brightn	ess and	FFh va	lue mea	ans the I	nighest
	D	BV[7:0]		Brightness (Ratio)			Brightn	ess (%))		
Description		00h		0/256				0	%			
Description		01h		2/256				0.78	125%	<u> </u>		
		:		:					://			1
		FEh		255/256				99.60	9375%	11		
		FFh		256/256				10	0%			
Restriction	The d	isplay su	pplier ca	annot use this comma	and for t	uning (e	e.g. facto	ory tunir	ig, etc.)			
					nr		Ĵ			3		
				Status				Av	ailability	6		
		Normal N	Node On	, Idle Mode Off, Slee	p Out	3	0	11	Yes			
Register		Normal Mode On, Idle Mode On, Sleep Out Yes										
Availability		Partial Mode On, Idle Mode Off, Sleep Out Yes										
		Partial M	lode On	Idle Mode On, Slee	o Out	(-)	$\overline{\mathcal{A}}$		Yes			
	/ IN	 		Sleep In					Yes			
		96.	5	alse	严							
			\mathcal{I}	Status				Defa	ault Valı	le		
Default	2		Power	r On Sequence					00h			
U _ oracan				S/W Reset					00h			
		$\frac{1}{2}$	ŀ	I/W Reset					00h			
Flow Chart			Pa	WRDISBV(51h)	7				Leger Comma Parame Displa Action Mode Sequen transfe			

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		<i>,</i> ,											
Inst / Para	R/W	Add	ress				Parame	ter				-	
	10,00	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDISBV	Read	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	
NOTE: "-" Don't car	e												
Description	This c In prin	ommano nciple rel	d returns ationship	brightness value. b is that 00h value me	eans the	e lowest	brightne	ess and	FFh va	lue mea	ans the	highest	
	bright	ness.											
Restriction	-												
				Status				Av	ailability				
Deviator		Normal I	Mode On	, Idle Mode Off, Slee	p Out				Yes			2	
Availability		Normal I	Mode On	, Idle Mode On, Slee	p Out			2	Yes		0-		
Availability		Partial N	lode On	, Idle Mode Off, Slee	o Out				Yes				
		Partial Mode On, Idle Mode On, Sleep Out Sleep In Yes											
		Sleep In Yes											
					1/2/1		~						
			n f		U	6	\approx	Deta		le			
Default		16	Fower		- (00h				
	~~			IW Reset	R		$ \mathbf{r} $		00h				
		<u></u>				Ş			0011				
NO «				RDDISBV(52h)			Host		egend	 1!			
Flow Chart				Send Parameter DBV[7:0]	7	C	Driver		ameter				
								A Sec tra	ction Node quential ansfer				

RDDISBV: Read Display Brightness (5200h)

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WRCTRLD: Write CTRL Display (5300h)

		۸d	droop				Doromot	or							
Inst / Para	R/W	Au			D7	Do			Do	DO	D4	Do			
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
WRCTRLD	Write	53h	5300h	00h	0	0	BCTRL	Α	DD	BL	DB	G			
NOTE: "-" Don't car	e														
	This c	ommar	nd is used	to control ambient lig	ght, bri	ightness a	and gam	ma sett	ing.						
	BCTF	L: Brigh	ntness Co	ntrol Block On/Off											
	The B		pit is alwa	ys used to switch brig	ghtnes	s for disp	lay with	dimmin	g effect	(accord	ing to D	D bit).			
	BC	TRL		DESCRIPTION				LEDP	WM Pir	ו					
		0	Off,			LEDPW	POL="0"	: keep l	ow (0%	, high le	vel is du	uty)			
		-	DBV[7:0]	and KBV[7:0] are 00	n.	LEDPW	POL="1"	: keep	high (0%	6, low le	vel is du	uty)			
		1	On,			LEDPW	POL="0"	: PWM	output	high lev	rel is du	ty)			
				and KBV[7:0] are act	ive	LEDPW	POL="1"	: PWM	output		er is duty	1)			
	A: LA The B		oit is used	to control LABC bloc	k			11	JI 12	1 ND					
		A		DESCRIPTION		101	PWM	l duty fo	or LEDP	WM Pir	1				
		0	Off		71 17	By DB	/[7:0] of	comma	nd "WB	DISBV	(5100h) [;]	"			
		1	On			By LAE	C block				()				
	DD: D	isplav [Dimmina (Control On/Off	<u>M</u>			nr	うた	2					
			g	DESCRIPTION	$P \sim$	1	1		\ll						
		0	Display di	mming is off			$\bigcirc \mathbb{N}$		120						
		125	Display di	mmina is on	~	()		<u>ک</u>							
	BL: B	acklight	Control C	splay dimming is on											
	When	BL bit	change fr	om "On" to "Off", disp	play br	ightness	is turned	d off wit	hout gra	adual dii	nming,	even if			
	dimm	ing on (DD="1") i	s selected.	リピ										
		BL		DESCRIPTION				LED	ON Pin						
Description		01	Off			LEDON	NPOL="0	": outpu	ut low (fe	or high a	active)				
						LEDON	NPOL="1	": outpu	ut high (for low a	active)				
			On			LEDON	NPOL="0	": outpu ". outpu	ut high (ut low (fr	for high	active)				
			Prightnoss	Manual/Automatia		LEDON	NFUL= I	. outpt		or iow a	clive)				
		NB ISPIAY L	Sirgininess	Manual/Automatic	r										
			Janual th	e user has to use thi	is setti	ng for ma	nual adi	ustmer	t of the	brightne	es to h	ave			
		0	an effect.		5 5011	ing for fine	andar adj	ustinoi		brightin	555 10 11	ave			
		1 /	Automatic	, information about th	e use	d brightne	ess is inc	luded i	n the ac	tive pro	file.				
	Note:	All rea	d and wri	te commands are va	lid, bu	t there is	no effe	ct (exce	ept regis	sters ca	n be ch	anged)			
	when	write co	ommands	are used.				,	, 0			0 /			
	G: Ga	ımma C	urve Man	ual/Automatic											
		G	DESCRIPTION												
		0	Manual, b	y GAMSET-command	d										
		1 /	Automatic	, information about th	ie use	d gamma	is includ	led in th	ne active	e profile					
	The d	limming	function	is adapted to the brig	ghtnes	ss registe	rs for dis	splay w	hen bit	BCTRL	is chan	ged at			
	DD="	1", e.g.	BCTRL: 0	\rightarrow 1 or 1 \rightarrow 0.											
	When	the ar	nbient lig	ht sensing off-mode	(A="0)"), displa	iy brighti	ness a	nd gam	ma sett	ing sho	uld be			
	manu	al settin	ig (DB="0	" and G="0"). Setting	values	s are the	ast one	written	with "W	rite Disp	lay Brig	htness			
	(5100	h)" com	imand and	d GAMSET-command	d or th	e default	one.								
	When	the an	nbient lig	nt control on, light se	ensor	control b	lock is a	always	working	, even	it backli	ght off			
	(BL="	0") and	display bi	rightness manual (DE	s="0")	are selec	ted.								

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PRELIMINARY

NT35510

Restriction	-	
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes Yes Yes
Default	Status Power On Sequence S/W Reset H/W Reset	Default Value 00h 00h 00h
Flow Chart	WRCTRLD(53h) Parameter: BCTRL, A, DD, BL, DB New Control Value Loaded	Legend Command Parameter Display Action Mode Sequentia transfer

11/8/2010

Version 0.00



RDCTRLD: Read CTRL Display Value (5400h)

	-	Ado	dress				Paramet	ter						
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
RDCTRLD	Read	54h	5400h	00h	0	0	BCTRL	А	DD	BL	DB	G		
NOTE: "-" Don't car	е													
	This c	omman	d returns	ambient light, brightr	ness co	ontrol and	d gamma	a settino	value.					
	BCTR	L: Brigh	ntness Co	ntrol Block On/Off			0		,					
	The B	CTRLb	oit is alwa	ys used to switch brig	ghtness	s for disp	lay with	dimmin	g effect	(accord	ing to D	D bit).		
	BC	TRL		DESCRIPTION				LEDF	PWM Pi	n				
		0	Off,			LEDPV	VPOL="0)": PWN	l keep l	ow (for h	nigh acti	ve)		
		0	DBV[7:0]	and KBV[7:0] are 00I	h.	LEDPV	VPOL="1	": PWN	l keep h	igh (for	low acti	ve)		
		1	On,			LEDPV	VPOL="0)": PWN	1 output	(high le	vel is dı	uty)		
			DBV[7:0]	and KBV[7:0] are act	ive	LEDPV	VPOL="1	": PWN	1 output	(low lev	el is du	ty)		
	A: LA	BC Bloc	k On/Off					2 <i> V</i>	N N	/ //u				
	The B		nt is used	to control LABC bloc	CK.	- ale								
		A	0 #	DESCRIPTION	15			auty fo			(E100b)	"		
			On On					comma	IIU VVA		(51001)			
) Jimming (by LAL	DIOCK	1	<u> </u>	>				
	<u>рр. р</u>	יואטיין נייטעריי חר			15	U I	7		火ミ					
		0	Display di	imming is off		\sim	\sim		120					
			Display di	mming is on		\bigcirc		<u>ا</u>						
	BN B	acklight	Control On/Off without Diaming Effect											
	When	BL bit	change fr	om "On" to "Off", disr	olav bri	ahtness	is turned	d off wit	hout ara	adual dir	nming,	even if		
	dimmi	ing on (l	DD="1") i	s selected.	ノビ						3,			
	E	3L		DESCRIPTION				LED	ON Pin					
Description		01	Off			LEDON	VPOL="0)": PWN	l keep lo	ow (for h	nigh acti	ve)		
	- C					LEDPV	VPOL="1	": PWN	/ keep h	igh (for	low acti	ve)		
			On				VPOL="()": PWN	1 output	(high le	vel is du	uty)		
) rightpage	Manual/Automatia		LEDPV	VPOL= I			(low lev	ei is du	ty)		
	ив. и	ispiay E	singnitness	a manual/Automatic										
			lanual th	ne user has to use thi	is settir	a for m	anual adi	iustmer	nt of the	brightne	es to h	ave		
		0 7	in effect.		5 50111	ig ioi ini	andar adj	Justinei		brightin	55 10 11	ave		
		1 A	Automatic	, information about th	ie usec	brightne	ess is inc	luded i	n the ac	tive pro	file.			
	Note:	All read	d and wri	te commands are va	lid, but	t there is	s no effe	ct (exce	ept regis	sters cal	n be ch	anged)		
	when	write co	ommands	are used.								• •		
	G: Ga	mma C	urve Man	ual/Automatic										
	(G DESCRIPTION												
		0 N	/lanual, b	y GAMSET-comman	d									
		1 A	Automatic	, information about th	ie usec	l gamma	is incluc	ded in th	ne active	e profile.				
	The d	imming	function	is adapted to the bri	ghtnes	s registe	ers for dis	splay w	hen bit	BCTRL	is chan	ged at		
	DD="1	1", e.g. I	BCTRL: 0	$\rightarrow 1 \text{ or } 1 \rightarrow 0.$	(
	when	the an	noient lig	ni sensing off-mode	(A=″Ŭ), aispla	ay pright	ness a	na gam	rita Sett	ing sho	uid De		
	(5100	ai sellin h)" com	y (DD= 0 mand and	and $G = 0$). Setting	values		one	willen	VVILII VV	nie Disp	ay Dig	niness		
	When	the an	nbient lin	nt control on. light s	ensor (control h	lock is a	alwavs	working	. even	if backli	aht off		
	(BL="	0") and	display bi	rightness manual (DE	3="0") a	are selec	ted.			,		3 0.1		

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PRELIMINARY

NT35510

Restriction	-	
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In	Availability Yes Yes Yes Yes Yes
Default	Status Power On Sequence S/W Reset H/W Reset	Default Value 00h 00h 00h
Flow Chart	RDCTRLD(54h) Send Parameter BCTRL, A, DD, BL, DB	Host Driver Display Action Mode Sequential transfer

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		Ado	dress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCABC	Write	55h	5500h	00h	0	0	0	0	0	0	C1	C0
NOTE: "-" Don't cal	re		1									
Description	This function are de C C C C C C C C C C C C C C C C C C C	commar onality. ⁻ efined or 1 0 0	nd is us There is p n a table C0 0 1 0 1	ed to set paramete cossible to use 4 diff below. Fur Off User Interface Imae Still Picture Image Moving Picture Ima	ers for ferent m nction ge (UI-N (Still-Ma age (Mo	image nodes fo Mode) ode) ving-Mo	content or conter	based nt adapt	adapti ive ima	ve brigi ge funct	ntness tionality,	control which
Restriction	i nis r	egister i	s synchro	onized with V-sync by	/ Interna	u circuit.			$\frac{\partial h}{\partial t}$			
Register Availability		Normal Normal Partial Partial	Mode On Mode On Mode On, Mode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Slee Idle Mode On, Slee Sleep In	p Out p Out o Out o Out		S	Av	ailability Yes Yes Yes Yes Yes			
Default			Power S	Status On Sequence W Reset				Defa	ault Valu 00h 00h 00h	Je		
Flow Chart			F Pi	WRCABC(55h) Parameter: C[1:0] xel Compensation and Gating Function ON/OFF	7				Leger Comma Carame Displa Action Mode Gequen transfe	nd ter y hia		

WRCABC: Write Content Adaptive Brightness Control (5500h)

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				0	•	,								
Inct / Para		Ado	dress				Parame	ter						
illst / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
RDCABC	Read	56h	5600h	00h	0	0	0	0	0	0	C1	C0		
NOTE: "-" Don't car	е													
	This of function	commar onality.	nd is use There is p	ed to read the setti cossible to use 4 diff	ngs for ferent m	image nodes fo	conten	t basec nt adapt	l adapti ive ima	ive brig ge func	htness tionality	control , which		
	are de	efined or	n a table l	pelow.										
	С	1	C0	Fur	nction									
Description	C)	0	Off							n			
	C)	1	User Interface Image	ge (UI-N	/lode)				- A				
	1		0	Still Picture Image	(Still-Mo	ode)			\sim	·\\ IC		2		
	1		1	Moving Picture Ima	age (Mo	ving-Mo	de)	2		\\ ī	-DE			
Restriction	-							11	<u> III</u>	100				
						105			a .					
				Status	nF			Av	ailability	4				
		Normal	Mode On	, Idle Mode Off, Slee	p Out		P		Yes					
Register		Normal	Mode On	, Idle Mode On, Slee	p Out			nK	Yes					
Availability		Partial I	Mode On,	Idle Mode Off, Sleep	o Out			111	Yes					
		Partial Mode On, Idle Mode On, Sleep Out Yes												
	Sleep In Yes													
	A	<u> </u>			<u> </u>		U							
		0-		Status	<u>ل</u>			Defa	ault Valu	Je				
Default	- 1	- (Power	On Sequence		_			00h					
		<u>((</u>	S	W Reset					00h					
U				W Reset					00h					
	, · · · ·	\overline{n}												
Flow Chart				RDCABC(56h)	7		Host Driver		Leger comma arame Displa Action Mode	nd nd ter y have the second se				
								<u> </u>		J				

RDCABC: Read Content Adaptive Brightness Control (5600h)

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WRHYSTE: Write Hysteresis (5700h~573Fh)

		Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			5700h	00h	10115	l0114	10113	10112	10111	10110	1019	1018
			5701h	00h	1017	1016	1015	1014	1013	1012	1011	1010
			5702h	00h	10215	10214	10213	10212	10211	10210	1029	1028
			5703h	00h	1027	1026	1025	1024	1023	1022	1021	1020
			:	00h	ln15	In14	In13	In12	ln11	In10	In9	In8
			:	00h	ln7	In6	In5	In4	ln3	In2	In1	In0
			571Ch	00h	l1515	l1514	11513	11512	11511	11510	1159	1158
			571Dh	00h	l157	l156	l155	l154	1153	1152	1151	1150
			571Eh	00h	l1615	l1614	l1613	J1612	11611	11610	1169	l168
	\\/wite	57h	571Fh	00h	l167	l166	1165	1164	1163	1162	l161	l160
WRHYSTE	vvrite	57N	5720h	00h	D0115	D0114	D0113	D0112	D0111	D0110	D019	D018
			5721h	00h	D017	D016	D015	D014	D013	D012	D011	D010
			5722h	00b	D0215	D0214	D0213	D0212	D0211	D0210	D029	D028
			5723h	00h	D027	D026	D025	D024	D023	D022	D021	D020
			. n: []	00h	Dn15	Dn14	Dn13	Dn12	Dn11	Dn10	Dn9	Dn8
			2 V.S	00h	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0
		5730h 00h D1515 D1514 D1513 D1512 D1511 D1510 D159 I 5730h 00h D1515 D1514 D1513 D1512 D1511 D1510 D159 I										
			573Dh	00h	D157	D156	D155	D154	D153	D152	D151	D010
		20	573Eh	00h	D1615	D1614	D1613	D1612	D1611	D1610	D169	D168
		5/3En 00n 01615 01614 01613 01612 01611 01610 0169 0 573Fh 00h 0167 0166 0165 0164 0163 0162 0161 0										D160
NOTE: "-" Don't car	e											
0	This c	command	t is used	to define Hysteresis	filter fur	nction.						
Description	In[15: Don't	0] define	s increm	ent values and Dn[1	5:0] deti	nes dec	rement	values.				
Description	116[15	5:01 bits	and D1	6[15 : 0] bits are alv	vavs set	to "655	י) . 535 (FFI	FFh)" in	ternallv.	. if 15[1	5 : 01 b	its and
	D15[1	5 : 0] bit	are still	valid and less than "6	65535 (F	FFFh)"		,	,	,] -	
Restriction	-											
						-						
				Status				Av	ailability	/		
D		Normal N	Node On	, Idle Mode Off, Slee	p Out				Yes			
Register		Normal N	Node On	, Idle Mode On, Slee	p Out				Yes			
Availability		Partial Mode On, Idle Mode Off, Sleep Out Yes										
		Partial Mode On, Idle Mode On, Sleep Out										
		Sleep In Yes										
				Status		1		Def	ault Vali	le		
			Power	On Sequence				0010	FFh	~~		
Default			S	S/W Reset					FFh			
		H/W Reset FFh										

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WRGAMMSET: Write Gamma Setting (5800h~5807h)

last / Dere		Add	ress				Parame	ter							
inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
			5800h	00h	G023	G022	G021	G020	G013	G012	G011	G010			
			5801h	00h	G043	G042	G041	G040	G033	G032	G031	G030			
			5802h	00h	G063	G062	G061	G060	G053	G052	G051	G050			
	W/rito	EOP	5803h	00h	G083	G082	G081	G080	G073	G072	G071	G070			
	vvnie	5011	5804h	00h	G103	G102	G101	G100	G093	G092	G091	G090			
			5805h	00h	G123	G122	G121	G120	G113	G112	G111	G110			
			5806h	00h	G143	G142	G141	G140	G133	G132	G1 31	G130			
			5807h	00h	G163	G162	G161	G160	G153	G152	G151	G150			
NOTE: "-" Don't car	е							- 0		ŇĪ	J				
	This c	ommano	d is used	to define gamma set	tting val	ues for e	each lur	ninance	level.	UV					
	Gamn	nma value is defined on command "Gamma Set (2600h)".													
		Gn[3:0] Parameter Curve Selected													
Description		01h GC0 Gamma Curve 1 (G=2.2)													
		02h		GC1		<u>v</u>	Re	eserved	シデ	2					
		04h GC2 Reserved							_						
		08h	>{\ 	GC3		Reserved									
Restriction	-	21	3 V ??		n (()			-						
1		1/ //	JU			\bigcirc									
				Status				Av	ailability	/					
		Normal I	Mode On	, Idle Mode Off, Slee	p Out				Yes						
Register		Normal	Mode On	, Idle Mode On, Slee	p Out				Yes						
Availability	0	Partial N	lode On	, Idle Mode Off, Sleep	o Out				Yes						
U		Partial N	lode On	, Idle Mode On, Slee	o Out				Yes						
	Sleep In Yes														
						1									
				Status		<u> </u>		Defa	ault Valu	le					
Default			Power	On Sequence		<u> </u>			01h						
									016						
			F	IV W RESEL					UIII						

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RDFSVM: Read FS Value MSBs (5A00h)

hast / Davis		Add	ress				Parame	ter					
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDFSVM	Read	5Ah	5A00h	00h	FSV15	FSV14	FSV13	FSV12	FSV11	FSV10	FSV9	FSV8	
NOTE: "-" Don't car	e												
Description	This c has be Anoth When to the should read v If any registe FSV[1 <i>Note:</i> other	ommand een remo using re same va d be rele vill also u other c ers for M 5:8] sho <i>Although</i> words, u	d returns poved from and for 1 ead LSBs alue whe ased. Ar update M ommand SBs and SBs and uld be 00 h FSV[15 ser don't	MSBs (FSV[15:8]) o n ambient light readii LSBs (FSV[7:0]). See s/MSBs command, co en LSBs/MSBs are re- nd that if e.g. LSBs a ISBs. If MSBs are re- ds are received betw LSBs should be rele 0h when bit 'A' of the 5:0] is 16-bit length re- t care about the para	f the "Fr ng. e the con prrespor ead. Afte re read ad at firs veen LS eased. "Write (gister, to meter ve	ont Side mmand nding M er readir and the st, the m BBs reading CTRL D he valid alues ov	Ambier "Read F SBs/LSI ng both re is no ext MSE d comm isplay (5 value ra ver than	nt Light TS Value Bs shou values, MSBs r Bs read hand an 5300h)" <i>ange is (</i> "65535	Sensor e LSBs ld be loo register ead cor will upd d MSB d MSB comma 0 ~ 6555 (FFFFr	Value" ((5B00h) cked so rs for MS nmand, ate LSB s read nd is "0' 35 (0000 n)".	after the ". that the SBs and the nex s. commar '. Dh ~ FFF	y refer LSBs LSBs C, the	
Restriction	-			- 0			と						
Register Availability Default		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Status Yes Status Default Value Power On Sequence 00h S/W Reset 00h H/W Reset 00h											
Flow Chart				RDFSVM(5Ah)	7		Host Driver		egend mmanc rameter Display Action Mode				

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RDFSVL: Read FS Value LSBs (5B00h)

last / Dava		Add	ress				Parame	ter					
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDFSVL	Read	5Bh	5B00h	00h	FSV7	FSV6	FSV5	FSV4	FSV3	FSV2	FSV1	FSV0	
NOTE: "-" Don't car	re												
Description	This c has be Anoth When to the should read v If any registe FSV[7 <i>Note:</i> other	command een reme using re same va d be rele vill also u other c ers for M 7:0] shou <i>Although</i> words, u	d returns poved from and for l ead LSBs alue whe ased. Ar update M ommand SBs and SBs and Id be 001 h FSV[15 ser don't	LSBs (FSV[7:0]) of n ambient light readii MSBs (FSV[15:8]). S s/MSBs command, co en LSBs/MSBs are re- nd that if e.g. LSBs a ISBs. If MSBs are re- ds are received betw LSBs should be rele- h when bit 'A' of the " 5:0] is 16-bit length re- t care about the para	the "Fro ng. ee the o prrespon ead. After re read ad at first veen LS eased. Write C gister, t meter v	ont Side comman nding M er readir and the st, the no SBs readir SBs readir TRL Dis he valid alues ov	Ambien d "Reac SBs/LSI ng both re is no ext MSE d comm splay (53 value ra ver than	I FS Val 3s shou values, MSBs r 3s read and an 300h)" c ange is ("65535	Sensor lue MSE ld be lo register ead cor will upd d MSB omman 0 ~ 6553 (FFFFf	Value" (3s (5A00 cked so rs for M: nmand, ate LSB s read d is "0". 35 (0000 n)".	after the Dh)". that the SBs and the nex s. commar	flicker y refer LSBs LSBs LSBs d, the	
Restriction	-			- 0									
Register Availability Default		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Status Yes Status Default Value Power On Sequence 00h S/W Reset 00h H/W Reset 00h											
Flow Chart				RDFSVL(5Bh) Send Parameter FSV[7:0]	7		Host Driver		egend mmanc ramete Display Action Mode				

11/8/2010

Version 0.00



Address Parameter Inst / Para R/W MIPI Others D[15:8] (Non-MIPI) D7 D5 D0 D6 D4 D3 D2 D1 **RDMFFSVM** Read 5Ch 5C00h 00h FFSV8 FFSV15FFSV14FFSV13FFSV12FFSV11 FFSV10 FFSV9 NOTE: "-" Don't care This command returns MSBs (FFSV[15:8]) of the "Front Side Ambient Light Sensor Value" after the median filter. Another command for LSBs (FFSV[7:0]). See the command "Read Median Filter FS Value LSBs (5D00h)". When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs Description should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs. If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released. FFSV[15:8] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0". Note: Although FFSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)". Restriction Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Register Normal Mode On, Idle Mode On, Sleep Out Yes Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes **Default Value** Status Default Power On Sequence 00h S/W Reset 00h 00h H/W Reset Legend RDMFFSVM(5Ch) Host Command Driver Parameter Send Parameter FFSV[15:8] Display Flow Chart Action Mode Sequentia transfer

RDMFFSVM: Read Median Filter FS Value MSBs (5C00h)

11/8/2010

Version 0.00



Address Parameter Inst / Para R/W MIPI Others D[15:8] (Non-MIPI) D7 D5 D0 D6 D4 D3 D2 D1 RDMFFSVL Read 5Dh 5D00h 00h FFSV7 FFSV5 FFSV2 FFSV0 FFSV6 FFSV4 FFSV3 FFSV1 NOTE: "-" Don't care This command returns LSBs (FDSV[7:0]) of the "Front Side Ambient Light Sensor Value" after the median filter. Another command for MSBs (FFSV[15:8]). See the command "Read Median Filter FS Value MSBs (5C00h)". When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs Description should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs. If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released. FFSV[7:0] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0". Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)". Restriction Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Register Normal Mode On, Idle Mode On, Sleep Out Yes Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes **Default Value** Status Default Power On Sequence 00h S/W Reset 00h 00h H/W Reset Legend RDMFFSVL(5Dh) Host Command Driver Parameter Send Parameter FFSV[7:0] Display Flow Chart Action Mode Sequentia transfer

RDMFFSVL: Read Median Filter FS Value LSBs (5D00h)

11/8/2010

Version 0.00



Inst / Para		Address Parameter											
inst / i aia	11/11	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRCABCMB	Write	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	
NOTE: "-" Don't care													
Description	This c In prir the hiç	This command is used to set the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.											
Restriction	-												
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes											
Default		Status Default Value Power On Sequence 00h S/W Reset 00h H/W Reset 00h											
Flow Chart			Pa L	Arameter CMB[7:0					Lege Comma Parame Displa Actio	nd and eter			
									Sequer transf				

WRCABCMB: Write CABC minimum brightness (5E00h)

11/8/2010

Version 0.00



	R/W	Address												
Inst / Para		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5		DЗ	D2	D1	DO		
BDCABCMB	Read	5Eb	5E00h	00h	CMB7	CMB6	CMB5		CMB3	CMB2	CMB1	CMBO		
NOTE: "-" Don't care														
Description	This c In prir the hig CMB[(5Eh)'	This command return the minimum brightness value of CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. CMB[7:0] is minimum brightness forCABC specified with "WRCABCMB Write CABC minimum brightness (5Eh)" command.												
Restriction	-													
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes											2		
Default	u Al		Power S	Status On Sequence S/W Reset			3	Defa	ault Valu 00h 00h 00h	ıe				
Vie.	<u> </u>		R 	DCABCMB(5Fh)	7		Host Driver		Legeno	d nd er				
Flow Chart			/	/					Action Mode equent transfe					

RDCABCMB: Read CABC minimum brightness (5F00h)

11/8/2010

Version 0.00



-													
Inst / Para	R/W	/W Address					Parame	ter		1			
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WBI SCC	Write	65h	6500h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	
		00.1	6501h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	
NOTE: "-" Don't car	NOTE: "-" Don't care												
Description	This c Defau	This command is used to send the compensation coefficient value (CC[15 : 0]). Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary).											
Restriction	The d	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).											
Register Availability		Normal N Normal N Partial M Partial M	Mode On Mode On Node On	Status I, Idle Mode Off, Slee I, Idle Mode On, Slee I, Idle Mode Off, Slee I, Idle Mode On, Slee Sleep In	Availability Yes Yes Yes Yes Yes Yes								
Default	Status Default Value Power On Sequence 8000h S/W Reset 8000h H/W Reset 8000h												
Flow Chart				WRLSCC(65h) Parameter CC[15: Parameter CC[7:0 New CC Value Loaded	8] 7) 7) 7)				Lege Comma Parame Displa Action Mode	nd and eter ay n entia			

WRLSCC: Write Light Sensor Compensation Coefficient Value (6500h~6501h)

11/8/2010

Version 0.00



Inst / Para	R/W	Add	ress	Parameter									
liist / T ala	11/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDLSCCM	Write	66h	6600h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	
NOTE: "-" Don't care													
Description	This c Light It can Defau	This command returns MSBs of the compensation coefficient value (CC[15:8]) which is stored by "Write Light Sensor Compensation Coefficient Value (6500h)" command. It can read MSBs/LSBs of "Light Sensor Compensation Coefficient value" with any order. Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary). MSBs are "1000 000".											
Restriction	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).												
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
Default	Status Default Value Power On Sequence 80h S/W Reset 80h H/W Reset 80h												
Flow Chart				RDLSCCM(66h)	7		Host Driver		Legen comma aramet Display Action Mode				

RDLSCCM: Read Light Sensor Compensation Coefficient Value MSBs (6600h)

11/8/2010

Version 0.00


	1		-	Address												
Inst / Para	R/W	Add	ress				Parame	ter								
	10,00	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0				
RDLSCCL	Write	67h	6700h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0				
NOTE: "-" Don't car	re															
Description	This c Light It can Defau	ommand Sensor (read MS It value	d returns Compens SBs/LSBs for comp	LSBs of the compen sation Coefficient Values of "Light Sensor Co ensation coefficient is	sation c ue (650 mpensa s 1.0 (10	oefficier 1h)" con ttion Co 000 000	nt value nmand. efficient 0 0000 ((CC[7:0 value" 0000 in l)]) which with any binary).	n is store / order. MSBs a	ed by "V are "000	Vrite 0 000".				
Restriction	The d	isplay sι	upplier ca	annot use this comma	and for t	uning (e	.g. facto	ory tunin	ig, etc.).		-					
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes														
Default		Status Default Value Power On Sequence 00h S/W Reset 00h H/W Reset 00h														
Flow Chart				RDLSCCL(67h)	7		Host Driver		Leger Comma Parame Displa Action Mode Sequen transfe	nd nd ter						

RDLSCCL: Read Light Sensor Compensation Coefficient Value LSBs (6700h)

11/8/2010

Version 0.00



				e (! ••••!)									
Inct / Para		Add	ress				Parame	ter					
llist / Fala		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDBWLB	Read	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	
NOTE: "-" Don't car	e												
Description	This o Black White	command : Bkx and : Wx and	d returns d Bky d Wy	the lowest bits of bla	ick and	white co	lor char	acterist	ic.				
Restriction	-												
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On, Node On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out p Out p Out			Av	ailability Yes Yes Yes Yes Yes				
Default	4	Status Default Value Power On Sequence MTP Value 00h S/W Reset MTP Value 00h H/W Reset MTP Value 00h											
Flow Chart				RDBWLB(70h)	7	[Host Driver		Legen ommar aramet Display Action Mode equent transfe				

RDBWLB: Read Black/White Low Bits (7000h)

11/8/2010

Version 0.00



RDBkx: Read Bkx (7100h)

		Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBkx	Read	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2
NOTE: "-" Don't car	re		-									
Description	This o	command	d returns	the Bkx bit (Bkx[9:2]) of blac	k color (characte	eristic.				
Restriction	-											
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			2
Default		Status Default Value After MTP Before MTP Power On Sequence MTP Value 00h S/W Reset MTP Value 00h H/W Reset MTP Value 00h										
Flow Chart				RDBkx(71h) Send Parameter Bkx[9:2]	7		Host Driver		Display Action Mode			

11/8/2010

Version 0.00



RDBky: Read Bky (7200h)

Inst / Para	R/W	Add	ress				Parame	ter				
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBky	Read	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2
NOTE: "-" Don't car	e											
Description	This c	command	d returns	the Bky bit (Bky[9:2]) of blac	k color (characte	eristic.				
Restriction	-											
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On Node On Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			2
Default			Power	Status On Sequence S/W Reset			After M MTP Va MTP Va	Defa TP Ilue Ilue	ault Valu	Before	e MTP Dh Dh Dh	
Flow Chart					Display Action Mode							

11/8/2010

Version 0.00



RDWx: Read Wx (7300h)

		Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWx	Read	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2
NOTE: "-" Don't car	е	,	J							<u> </u>	<u></u>	
Description	This c	command	d <u>returns</u>	the Wx bit (Wx[9:2])	of white	color c	haracte	ristic.				
Restriction	-											
Register Availability		Normal N Normal N Partial N Partial N	Vlode On Vlode On Node On Node On	Status I, Idle Mode Off, Slee I, Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			2
Default		T	Power	Status r On Sequence 3/W Reset			After M MTP Va MTP Va	Defa TP Ilue Ilue	ault Valu	Je Before 00 00 00	MTP)h)h)h	
Flow Chart				RDWx(73h) Send Parameter Wx[9:2]	7		Host Driver		egend ommar aramete Display Action Mode equent transfe			



RDWy: Read Wy (7400h)

		-										
Inct / Para		Add	ress				Parame	ter				
inst / Para	rt/ VV	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWy	Read	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2
NOTE: "-" Don't car	е										-	
Description	This o	command	d returns	the Wy bit (Wy[9:2])	of white	color c	haracte	ristic.				
Restriction	-											
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			1
Default		T	Power	Status On Sequence S/W Reset			After M MTP Va MTP Va	Defa TP Ilue Ilue	ault Valu	Je Before 00 00	e MTP Dh Dh Dh	
Flow Chart				RDWy(74h) Send Parameter Wy[9:2]	<u>بار</u>		Host Driver		Legen ommar aramet Display Action Mode equent transfe			



Inst / Para	R/W	Add	ress				Parame	ter	1	1	1		
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDRGLB	Read	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	
NOTE: "-" Don't care	е												
Description	This c Red: I Greer	command Rx and F n: Gx and	d returns Ry d Gy	the lowest bits of rec	l and gre	een colo	or chara	cteristic					
Restriction	-												
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On Node On, Node On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			7	
Default	4	Status Default Value After MTP Before MTP Power On Sequence MTP Value 00h S/W Reset MTP Value 00h H/W Reset MTP Value 00h											
Flow Chart				RDRGLB(75h)	7]	Host Driver		Legen ommar arameta Display Action Mode equent transfe				

RDRGLB: Read Red/Green Low Bits (7500h)

11/8/2010

Version 0.00



RDRx: Read Rx (7600h)

		Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRx	Read	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2
NOTE: "-" Don't cai	re	8									8	
Description	This c	command	d returns	the Rx bit (Rx[9:2]) c	of red co	lor char	acteristi	с.				
Restriction	-											
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			2
Default			Power	Status On Sequence S/W Reset	After M MTP Va MTP Va	Defa TP Ilue Ilue	ult Valu	Before 00 00 00	e MTP Dh Dh Dh			
Flow Chart				RDRx(76h)	7		Host Driver		egend aramete Display Action Mode equent transfe			

Version 0.00



RDRy: Read Ry (7700h)

		Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRy	Read	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2
NOTE: "-" Don't car	е											<u> </u>
Description	This c	command	d returns	the Ry bit (Ry[9:2]) c	of red co	lor char	acteristi	ic.				
Restriction	-											
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			1
Default			Power	Status On Sequence G/W Reset			After M MTP Va MTP Va MTP Va	Defa TP alue alue	ault Valu	Je Before 00 00 00	e MTP Dh Dh Dh	
Flow Chart				RDRy(77h)	7		Host Driver		Display Action Mode			



RDGx: Read Gx (7800h)

	D 444	Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGx	Read	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2
NOTE: "-" Don't car	e	8										<u> </u>
Description	This o	command	d returns	the Gx bit (Gx[9:2]) of	of green	color cl	naracter	istic.				
Restriction	-											
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			1
Default			ault Valu	Before	e MTP Dh Dh Dh							
Flow Chart				RDGx(78h) Send Parameter Gx[9:2]	7		Host Driver		Display Action Mode			



RDGy: Read Gy (7900h)

		bhA	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGv	Read	79h	7900h	00h	Gv9	Gv8	Gv7	Gv6	Gv5	Gv4	Gv3	Gv2
NOTE: "-" Don't car	e.				<i>.,</i> ,,		y .		<i></i>	<i></i> ,		<u>j</u> _
Description	This c	omman	d returns	the Gy bit (Gy[9:2]) of	of areen	color c	naracter	istic				
Bestriction	-	, on main			, gioon	00101 01	alaotoi	101101				
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out	- A 5E		Av	ailability Yes Yes Yes Yes Yes			1
Default			Je Before 00 00 00	e MTP Dh Dh Dh								
Flow Chart				RDGy(79h) Send Parameter Gy[9:2]	7		Host Driver		Display Action Mode			



				()								
Inst / Para	R/W	Add	lress				Parame	ter				
inst / i aia	11/11	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBALB	Read	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0
NOTE: "-" Don't car	e											
Description	This c Blue: A: Ax	command Bx and I and Ay	d returns By	the lowest bits of blu	e and A	color c	haracte	ristic.				
Restriction	-											
Register Availability		Normal I Normal I Partial M Partial M	Mode On Mode On Mode On, Mode On,	Status , Idle Mode Off, Slee , Idle Mode On, Slee Idle Mode Off, Sleep Idle Mode On, Sleep Sleep In	p Out p Out o Out o Out			Av	railability Yes Yes Yes Yes Yes			
Default	4		Power S	Status On Sequence /W Reset //W Reset			After M MTP Va MTP Va MTP Va	Defa ITP alue alue		Before 00 00	e MTP Dh Dh Dh	
Flow Chart				RDBALB(7Ah)	7		Host Driver		Legen ommar aramet Display			
									Mode equent transfe			

RDBALB: Read Blue/AColor Low Bits (7A00h)

11/8/2010

Version 0.00



RDBx: Read Bx (7B00h)

	D 444	Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBx	Read	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2
NOTE: "-" Don't car	e	8										<u> </u>
Description	This o	command	d returns	the Bx bit (Bx[9:2]) o	f blue co	olor cha	racterist	tic.				
Restriction	-											
Register Availability		Normal I Normal I Partial N Partial N	Mode On Mode On Aode On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			2
Default	Default Value Status After MTP Before MTP Power On Sequence MTP Value 00h S/W Reset MTP Value 00h H/W Reset MTP Value 00h											
Flow Chart				RDBx(7Bh) Send Parameter Bx[9:2]	7		Host Driver		Display Action Mode equent transfe			

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RDBy: Read By (7C00h)

		Add	ress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBv	Read	7Ch	7C00h	00h	Bv9	Bv8	Bv7	Bv6	Bv5	Bv4	Bv3	Bv2
NOTE: "-" Don't car	e.					-,-	_,		-)-	-,		-)-
Description	This c	omman	d returns	the By bit (By[9:2]) o	f blue co	olor cha	racteris	tic.				
Restriction	-											
Register Availability		Normal I Normal I Partial M Partial M	Mode On Mode On Jode On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out			Av	ailability Yes Yes Yes Yes Yes			1
Default		Status Default Value After MTP Before MTP Power On Sequence MTP Value 00h S/W Reset MTP Value 00h H/W Reset MTP Value 00h										
Flow Chart				RDBy(7Ch) Send Parameter By[9:2]	7		Host Driver		Display Action Mode			



RDAx: Read Ax (7D00h)

		Add	ress				Parame	ter					
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDAx	Read	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	
NOTE: "-" Don't car	e												
Description	This c	omman	d returns	the Ax bit (Ax[9:2]) o	f A colo	r charac	cteristic.						
Restriction	-												
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes											
Default	Status Default Value After MTP Before MTP Power On Sequence MTP Value 00h S/W Reset MTP Value 00h H/W Reset MTP Value 00h												
Flow Chart				RDAx(7Dh) Send Parameter Ax[9:2]	7		Host Driver		Display Action Mode				

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RDAy: Read Ay (7E00h)

		Add	ress				Parame	ter					
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDAy	Read	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	
NOTE: "-" Don't car	e				,	,	,	,	,	,	,	,	
Description	This c	ommano	d returns	the Av bit (Av[9:2]) o	f A colo	r charac	cteristic.						
Restriction	-												
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes											
Default	Status Default Value After MTP Before MTP Power On Sequence MTP Value 00h S/W Reset MTP Value 00h H/W Reset MTP Value 00h												
Flow Chart	P F			RDAy(7Eh)	7		Host Driver		Display Action Mode				



RDDDBS: Read DDB Start (A100h~A104h)

Inst / Dara		Add	ress				Parame	ter				
inst / Fala	U/ 1	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
			A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
RDDDBS	Read	A1h	A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
			A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
			A104h	00h	1	1	1	1	1	1	1	1
NOTE: "-" Don't car	e				0							
Description	Note: This information is not the same what "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands are returning. Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block. This read sequence can be interrupted by any command and it can be continued by "Read DDB Continue (A8h)" command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1 st parameter has been sent => 2 nd parameter has been sent=> interrupt => RDDDBC => 3 rd parameter of the RDDDBS has been sent. SID[15:0]: Supplier identification MID[15:0]: Module ID											
Restriction	-		~ 1		U	6						
Register Availability		Normal I Normal I Partial M Partial M	Mode On Mode On Node On Node On	Status , Idle Mode Off, Slee , Idle Mode On, Slee , Idle Mode Off, Slee , Idle Mode On, Slee Sleep In	p Out p Out o Out o Out		5	Av	ailability Yes Yes Yes Yes Yes	/		
				Status				Defa	ault Valu	le		
				Olaldo			After M	TP		Before	e MTP	
Default			Power	r On Sequence			MTP Va	alue		00)h	
			S	S/W Reset			MTP Va	alue		00)h	
			ŀ	I/W Reset			MTP Va	alue		00)h	



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RDDDBC: Read DDB Continue (A800h~A804h)

last / Dara		Add	ress				Parame	ter				
inst / Fara		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			A800h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
			A801h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
RDDDBC	Read	A8h	A802h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
			A803h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
			A804h	00h	1	1	1	1	1	1	1	1
NOTE: "-" Don't car	е	•										
Description	This c point v Note: Note:	command where R Parame For use 1. Set m 2. Read 3 Read	d returns DDDBS ter 0xFF example aximum 0xA1, re 0xA8 re	the supplier identific command was interru is an "Exit Code", thi , return packet size=3 turn 3 bytes SID[7:0] turn 2 bytes MID[15;	ation an upted by is mean , SID[15 8] and 0	d displa an other s that th 5:8], MIL xFF	y modu er comm ere is no p[7:0]	le mode nand. o more	e/revisio data in t	n inform	hation fro	om the
	A Roc		Start con	mand (RDDDRS) ch	ould be		d at loa	st onco	boforo	Boad		ntinuo
Restriction	command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue											
	comm	nand is u	ndefined				n		2 \			
			<u>an []</u>		V		\gg		120			
				Status		\bigcirc	5	Av	ailability	/		
	R	Normal N	Node On	, Idle Mode Off, Slee	p Out				Yes			
Register		Normal N	Mode On	, Idle Mode On, Slee	p Out				Yes			
Availability		Partial N	lode On	, Idle Mode Off, Sleep	oOut				Yes			
	Р Ч <u> </u>	Partial	lode On	, Idle Mode On, Sleep	o Out				Yes			
				Sleepin					165			
U		ŇŴ	\mathcal{I}									
		11 2		_				Defa	ault Valu	le		Ĭ
				Status			After M	TP		Before	MTP	
Default			Power	r On Sequence			MTP Va	lue		00	h	
			5	S/W Reset			MTP Va	lue		00	h	
			H	I/W Reset			MTP Va	lue		00	h	

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RDFCS: Read First Checksum (AA00h)

last / Deve		Add	ress				Parame	ter						
inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
RDFCS	Read	AAh	AA00h	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0		
NOTE: "-" Don't car	re													
Description	This of register register	command ers (not i ers and/d	d returns nclude "I or frame	the first checksum Manufacture Comma memory has been do	what h nd Set) one.	as been and the	calcula frame n	ated from nemory	m "User after the	r Comm e write a	and Se access to	t" area o those		
Restriction	It will regist	be nece ers befor	essary to	wait 150ms after th can read this checksu	nere is um value	the last e.	write a	ccess o	n "User	Comm	and Se	t" area		
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes												
Default		Status Default Value Power On Sequence 00h SW Reset 00h H/W Reset 00h												
NO /	<i>F</i>	H/W Reset 00h RDFCS(AAh) Host Command												
Flow Chart				Send Parameter FCS[7:0]	/				Display Action Mode equent transfe					

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RDCCS: Read Continue Checksum (AF00h)

Inst / Dara		Add	ress				Parame	ter						
inst / Para	F7/ V V	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
RDCCS	Read	AFh	AF00h	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0		
NOTE: "-" Don't car	e													
Description	This of check acces	comman sum has s to thos	d returns calculat e registe	s the continue check ed from "User Comm ers and/or frame men	ksum w nand Se nory has	hat has t" area r s been d	been o egisters one.	alculate and the	ed conti e frame	nuously memory	v after t v after th	he first ie write		
Restriction	It will regist	be nece ers befor	essary to re there o	wait 300ms after th can read this checks	nere is um value	the last e in the	write a	ccess o e.	n "User	r Comm	and Se	t" area		
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes												
Default	1	Status Default Value Power On Sequence 00h S/W Reset 00h H/W Reset 00h												
MO,	<u> </u>	H/W Reset 00h Legend RDCCS(AFh) Host Command												
Flow Chart				Send Parameter CCS[7:0]	/				Display Action Mode equent transfe					

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RDID1: Read ID1 Value (DA00h)

la st / Dava		Add	iress				Parame	ter					
inst / Para	K/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDID1	Read	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
NOTE: "-" Don't car	re				<u> </u>					·			
Description	This r	read byte	identifie	s the TFT LCD modu	ıle's ma	nufactu	re ID.						
Restriction	-												
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes											
Default		Status Default Value After MTP Before MTP Power On Sequence MTP Value 00h S/W Reset MTP Value 00h H/W Reset MTP Value 00h											
Flow Chart				RDID1(DAh) Send Parameter ID1[7:0]	7		Host Driver		Legend ommar aramete Display Action Mode equent transfe				

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RDID2: Read ID2 Value (DB00h)

last / Dava		Add	ress				Parame	ter						
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
RDID2	Read	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
NOTE: "-" Don't car	е													
Description	This r made Paran	ead byte to the di neter Ra	e is used isplay, m nge: ID2	to track the TFT LCI aterial or construction = 80h to FFh	D modul n specifi	e/driver cations.	versior	n. It is cł	nanged	each tin	ne a ver	rsion is		
Restriction	-													
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes												
Default	Y AL	Status Default Value Status After MTP Power On Sequence MTP Value S/W Reset MTP Value H/W Reset MTP Value												
Flow Chart	R			RDID2(DBh)	7		Host Driver		ommar aramete Display Action Mode equent transfe					

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RDID3: Read ID3 Value (DC00h)

Inst / Para		Add	lress				Parame	ter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID3	Read	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
NOTE: "-" Don't car	e											
Description	This p	paramete	er read by	yte identifies the TFT	LCD m	odule/dı	river.					
Restriction	-											
Register Availability		StatusAvailabilityNormal Mode On, Idle Mode Off, Sleep OutYesNormal Mode On, Idle Mode On, Sleep OutYesPartial Mode On, Idle Mode Off, Sleep OutYesPartial Mode On, Idle Mode On, Sleep OutYesSleep InYes										
Default		Status Default Value After MTP Before MTP Power On Sequence MTP Value 00h S/W Reset MTP Value 00h H/W Reset MTP Value 00h										
Flow Chart				RDID3(DCh) Send Parameter ID3[7:0]	7		Host Driver		Display Action Mode			

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7 REFERENCE APPLICATIONS

7.1 Microprocessor Interface

The display, which is using 80-series MPU interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.2 Interfacing for 80-series 16-bit MPU by Connecting IM[3:0]="0001"

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Note: Left MVDDL and MVDDA open (not used) when using 80-series MPU interface.

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The display, which is using RGB with 16-bit SPI interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.4 Interfacing for RGB with SPI by Connecting IM[3:0]="X011"

The display, which is using RGB with I2C interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.5 Interfacing for RGB with I2C by Connecting IM[3:0]="0100"

Note 1. Connecting D23, D22, D15, D14, D7 and D6 to VSSI when using 18-bit/pixel (VIPF[3:0]="0110"). Connecting D23~D21, D15, D14 and D7~ D5 to VSSI when using 16-bit/pixel (VIPF[3:0]="0101"). Note 2. Left MVDDL and MVDDA open (not used) when using RGB with SPI interface. Note 3. IM3 is used to select SCL rising or falling edge trigger for 16-bit SPI interface.

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The display, which is using MIPI DSI and the TE line, is connected to the MPU as it is illustrated below.



Fig. 7.1.6 Interfacing for MIPLOSI with TE Line by Connecting IM[3:0]="0101"

The display, which is using MIPI DSI without the TE line, is connected to the MPU as it is illustrated below.



Fig. 7.1.7 Interfacing for MIPI DSI without TE Line by Connecting IM[3:0]="0101"

Note1. Bit DSITE should be "1", the TE line is enabled, when using MIPI with TE line.

Note2. Bit DSITE should be "0", the TE line is disabled, when using MIPI without TE line. The command 35h TEON cannot active the separated TE line.

Note3. Connecting HSSI_DATA1_P/N to VSSAM when using 1 data lane application.

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The display, which is using MDDI with 16-bit SPI interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.8 Interfacing for MDDI with 16-bit SPI by Connecting IM[3:0]="X110"

The display, which is using MDDI with I2C interface, is connected to the MPU as it is illustrated below.



Fig. 7.1.9 Interfacing for MDDI with I2CI by Connecting IM[3:0]="0111"

Notes:

1. Connecting HSSI_DATA1_P/N to VSSAM when using MDDI Type-I (1 data lane).

2. IM3 is used to select SCL rising or falling edge trigger when using 16-bit SPI interface.

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7.2 Connections with Panel



NOTES:

1. The scan direction from top to bottom indicated in above figure means (CTB XOR ML = "0"). 2. The relationship between Sn output sequence and CRL/CGM[7:0] is shown below.

CGM[7:0]	Display Resolution	Sn Output Sequence	Note
70h	480RGB x 864		
6Bh	480RGB x 854		
50h	480RGB x 800	$5(R) \rightarrow 52(G) \rightarrow 53(B) \rightarrow \rightarrow 51438(R) \rightarrow 51439(G) \rightarrow 51440(B)$	All 51 (0 51440
28h	480RGB x 720	$S1440 \rightarrow S1439 \rightarrow S1438 \rightarrow \rightarrow S3 \rightarrow S2 \rightarrow S1 \rightarrow S1 \rightarrow S1 \rightarrow S1 \rightarrow S1 \rightarrow S1 \rightarrow S1$	are used
⁰ 00h	480RGB x 640		
		2	