NV3041A Datasheet

720x544 System-On-Chip Driver
For 480 RGB x 272 TFT LCD

Version 1.2
October 10, 2022

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1. General Description

NV3041A is a single-chip SOC driver for 262,144-color, a-TFT liquid crystal display with maximum resolution of 480RGBx272 dots. It contains 720-channel source driver, a 544-channel Gate driver which used for dual-gate control, 293760 bytes GRAM for graphic display data, internal precise power supply circuit which supports full color, 6-color display mode and sleep mode.

NV3041A provides parallel 8/9/16-bit data bus MCU interface with 8080-I/8080-II, 3/4 Wire serial peripheral interface (SPI), 2 data line SPI interface, Q-SPI interface and 6/18bit data bus RGB interface. The display area can be specified in internal GRAM by window address function.

NV3041A is suitable for medium or Industrial products which low power characteristics is major concern. And it can make a display system with fewest components.

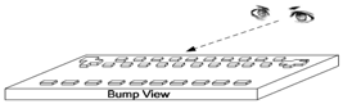
2. Features

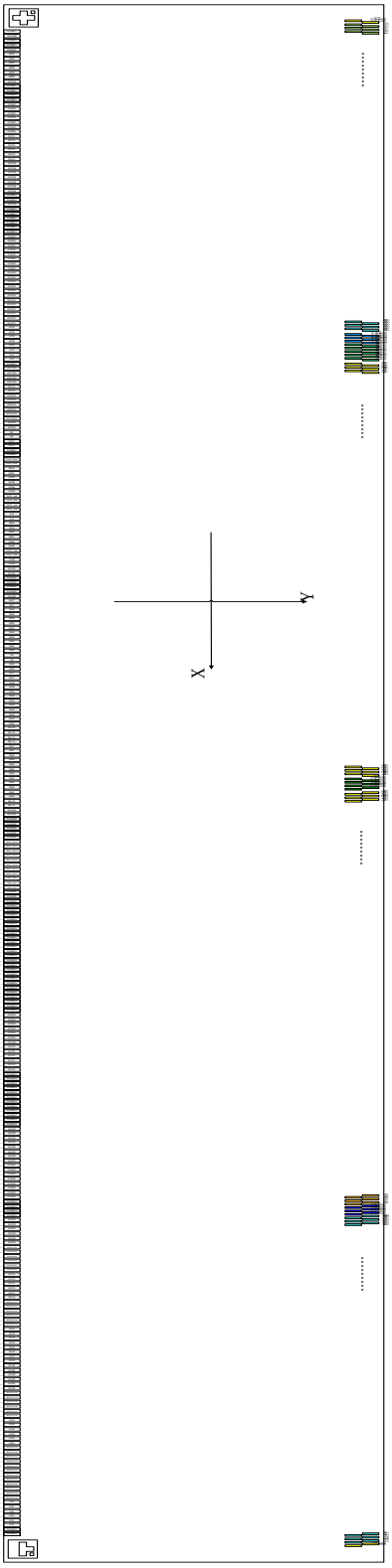
- Display resolution options:
  - 480(RGB) (H) X 272 (V)
  - 320(RGB) (H) X 240 (V)
- LCD Driver Output Circuits
  - Source Outputs: 720 Channels
  - Gate Outputs: 544 Channels
  - Common Electrode Output
- 64 gray scale with true 6 bit DAC
- Interface
  - 8-bits/16-bits interface with 8080-I/8080-II series MCU
  - 6/18-bit RGB interface
  - 3-wire/4-wire Serial Peripheral Interface (SPI)
  - 2 data lane SPI
  - Q-SPI
- On Chip Build-In Circuits
  - DC/DC Converter
  - Timing Controller
  - Graphic RAM: 293760 bytes
  - Non-Volatile (NV) Memory to store initial Register setting and factory default value
- Wide Supply Voltage Range
  - I/O Voltage (IOVCC to DGND): 1.65V ~ VCI
  - Analog Voltage (VCI to AGND): 3.0V ~ 3.6V
  - Charge pump Voltage (VCIP to PGND): 3.0V ~ 3.6V
- On-Chip Power System
  - GVDD: +5.968V ~ +4.96V
  - GVCL: -4.48V ~ -2.96V
  - Gate driver HIGH level (VGH to AGND): +13.36V ~ +16.197V
  - Gate driver LOW level (VGL to AGND): -10.83V~ -7.995V
- Optimized layout for COG Assembly

3. Pad arrangement

3.1. Output Bump Dimension

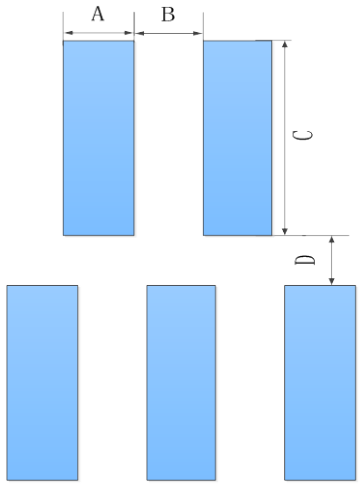
Chip size: 20190μm x720μm
Chip thickness: 280μm
Pad Location: Pad center
Coordinate Origin: Chip center





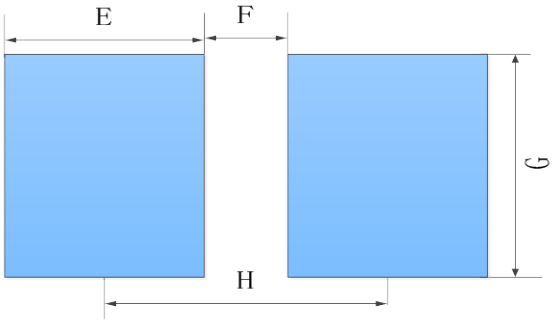
3.2. Bump Dimension

Output Pin: S1~S720、G1~G544、VCOM、DUMMY (Pin 332-1628)



Symbol	Item	Size
A	Bump Width	15um
B	Bump Gap 1 (Horizontal)	15um, 30um, 75um
C	Bump Height	100um
D	Bump Gap 2 (Vertical)	30um

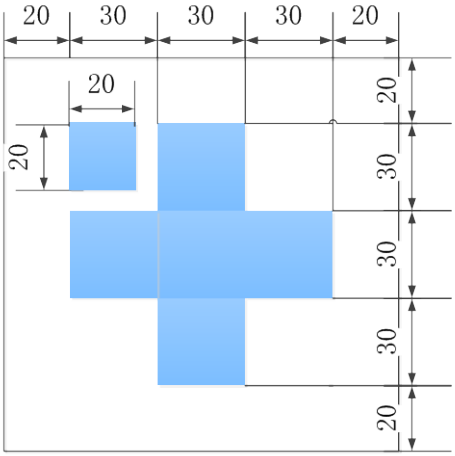
Input Pin: Pin 1-331



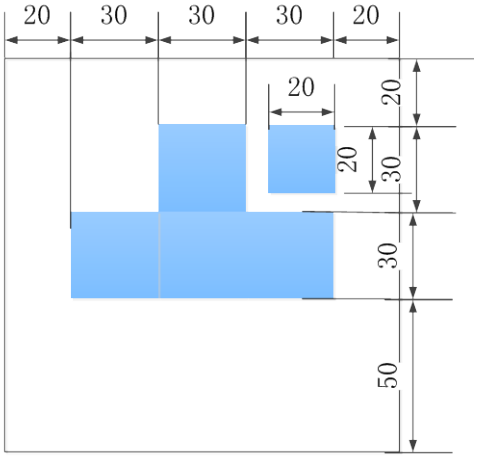
Symbol	Item	Size
E	Bump Width	35um
F	Bump Gap	24um
G	Bump Height	100um
H	Bump Pitch	59um

3.3. Alignment Mark Dimension

Alignment Mark: A1(X,Y)=(-9963,-235)



Alignment Mark: A2(X,Y)=(+9963,+235)



3.4. Pad Coordinates

NO.	Pin Name	X	Y
1	DUMMY	-9735	-257
2	VCOM	-9676	-257
3	DUMMY	-9617	-257
4	DUMMY	-9558	-257
5	DGND	-9499	-257
6	VPP	-9440	-257
7	VPP	-9381	-257
8	VPP	-9322	-257
9	VPP	-9263	-257
10	VPP	-9204	-257
11	VPP	-9145	-257
12	VCOM	-9086	-257
13	DUMMY	-9027	-257
14	DUMMY	-8968	-257
15	DUMMY	-8909	-257
16	DUMMY	-8850	-257
17	DGND	-8791	-257
18	GVDD	-8732	-257
19	GVDD	-8673	-257
20	GVDD	-8614	-257
21	GVDD	-8555	-257
22	GVDD	-8496	-257
23	GVDD	-8437	-257
24	GVCL	-8378	-257
25	GVCL	-8319	-257
26	GVCL	-8260	-257
27	GVCL	-8201	-257
28	GVCL	-8142	-257
29	GVCL	-8083	-257
30	VCOM	-8024	-257
31	VCOM	-7965	-257
32	VCOM	-7906	-257
33	VCOM	-7847	-257
34	VCOM	-7788	-257
35	VCOM	-7729	-257
36	VCOM	-7670	-257
37	DUMMY	-7611	-257
38	DUMMY	-7552	-257
39	VCOM	-7493	-257
40	DUMMY	-7434	-257
41	DUMMY	-7375	-257
42	DUMMY	-7316	-257
43	DUMMY	-7257	-257
44	DUMMY	-7198	-257
45	DUMMY	-7139	-257
46	DGND	-7080	-257
47	DGND	-7021	-257
48	DGND	-6962	-257
49	PGND	-6903	-257
50	PGND	-6844	-257
51	PGND	-6785	-257
52	PGND	-6726	-257
53	PGND	-6667	-257

NO.	Pin Name	X	Y
54	DVDD	-6608	-257
55	DVDD	-6549	-257
56	DVDD	-6490	-257
57	DVDD	-6431	-257
58	DVDD	-6372	-257
59	DVDD	-6313	-257
60	IOVCC	-6254	-257
61	IOVCC	-6195	-257
62	IOVCC	-6136	-257
63	IOVCC	-6077	-257
64	IOVCC	-6018	-257
65	IOVCC	-5959	-257
66	VCIP	-5900	-257
67	VCIP	-5841	-257
68	VCIP	-5782	-257
69	VCIP	-5723	-257
70	VCIP	-5664	-257
71	VCI	-5605	-257
72	VCI	-5546	-257
73	VCI	-5487	-257
74	DUMMY	-5428	-257
75	VSYNC	-5369	-257
76	VSYNC	-5310	-257
77	HSYNC	-5251	-257
78	HSYNC	-5192	-257
79	DCLK	-5133	-257
80	DCLK	-5074	-257
81	VDPOL	-5015	-257
82	VDPOL	-4956	-257
83	HDPOL	-4897	-257
84	HDPOL	-4838	-257
85	DCLKPOL	-4779	-257
86	DCLKPOL	-4720	-257
87	SBGR	-4661	-257
88	SBGR	-4602	-257
89	DE	-4543	-257
90	DE	-4484	-257
91	DCX	-4425	-257
92	DCX	-4366	-257
93	DUMMY	-4307	-257
94	DUMMY	-4248	-257
95	PARA_SERI	-4189	-257
96	PARA_SERI	-4130	-257
97	RDX	-4071	-257
98	RDX	-4012	-257
99	HDIR	-3953	-257
100	HDIR	-3894	-257
101	VDIR	-3835	-257
102	VDIR	-3776	-257
103	TEST_IN3	-3717	-257
104	TEST_IN3	-3658	-257
105	TEST_IN4	-3599	-257
106	TEST_IN4	-3540	-257

NO.	Pin Name	X	Y
107	CS	-3481	-257
108	CS	-3422	-257
109	SDA	-3363	-257
110	SDA	-3304	-257
111	WRX	-3245	-257
112	WRX	-3186	-257
113	DISP	-3127	-257
114	DISP	-3068	-257
115	TEST_IN5	-3009	-257
116	TEST_IN5	-2950	-257
117	GRB	-2891	-257
118	GRB	-2832	-257
119	SYNC	-2773	-257
120	SYNC	-2714	-257
121	DUMMY	-2655	-257
122	DUMMY	-2596	-257
123	DUMMY	-2537	-257
124	DUMMY	-2478	-257
125	DGND	-2419	-257
126	DR7	-2360	-257
127	DR7	-2301	-257
128	DR6	-2242	-257
129	DR6	-2183	-257
130	DR5	-2124	-257
131	DR5	-2065	-257
132	DR4	-2006	-257
133	DR4	-1947	-257
134	DR3	-1888	-257
135	DR3	-1829	-257
136	DR2	-1770	-257
137	DR2	-1711	-257
138	TE	-1652	-257
139	TE	-1593	-257
140	DR0	-1534	-257
141	DR0	-1475	-257
142	DG7	-1416	-257
143	DG7	-1357	-257
144	DG6	-1298	-257
145	DG6	-1239	-257
146	DG5	-1180	-257
147	DG5	-1121	-257
148	DG4	-1062	-257
149	DG4	-1003	-257
150	DG3	-944	-257
151	DG3	-885	-257
152	DG2	-826	-257
153	DG2	-767	-257
154	IM<0>	-708	-257
155	IM<0>	-649	-257
156	IM<1>	-590	-257
157	IM<1>	-531	-257
158	DB7	-472	-257
159	DB7	-413	-257

NO.	Pin Name	X	Y
160	DB6	-354	-257
161	DB6	-295	-257
162	DB5	-236	-257
163	DB5	-177	-257
164	DB4	-118	-257
165	DB4	-59	-257
166	DB3	0	-257
167	DB3	59	-257
168	DB2	118	-257
169	DB2	177	-257
170	IM<2>	236	-257
171	IM<2>	295	-257
172	SPI4W	354	-257
173	SPI4W	413	-257
174	DUMMY	472	-257
175	DUMMY	531	-257
176	DUMMY	590	-257
177	DUMMY	649	-257
178	DUMMY	708	-257
179	TESTOUT0	767	-257
180	TESTOUT1	826	-257
181	TESTOUT2	885	-257
182	TESTOUT3	944	-257
183	TESTOUT4	1003	-257
184	TESTOUT5	1062	-257
185	TESTOUT6	1121	-257
186	TESTOUT7	1180	-257
187	TEST_IN0	1239	-257
188	TEST_IN1	1298	-257
189	TEST_IN2	1357	-257
190	DUMMY	1416	-257
191	DUMMY	1475	-257
192	DUMMY	1534	-257
193	DUMMY	1593	-257
194	DUMMY	1652	-257
195	DUMMY	1711	-257
196	DUMMY	1770	-257
197	DUMMY	1829	-257
198	DUMMY	1888	-257
199	DUMMY	1947	-257
200	DUMMY	2006	-257
201	DUMMY	2065	-257
202	DUMMY	2124	-257
203	DUMMY	2183	-257
204	DUMMY	2242	-257
205	DUMMY	2301	-257
206	DUMMY	2360	-257
207	DUMMY	2419	-257
208	DUMMY	2478	-257
209	DUMMY	2537	-257
210	DUMMY	2596	-257
211	DUMMY	2655	-257
212	DUMMY	2714	-257
213	DUMMY	2773	-257
214	DUMMY	2832	-257
215	DUMMY	2891	-257

NO.	Pin Name	X	Y
216	DUMMY	2950	-257
217	AGND	3009	-257
218	AGND	3068	-257
219	AGND	3127	-257
220	AGND	3186	-257
221	AGND	3245	-257
222	AGND	3304	-257
223	DGND	3363	-257
224	AVCL	3422	-257
225	AVCL	3481	-257
226	AVCL	3540	-257
227	AVCL	3599	-257
228	AVCL	3658	-257
229	AVCL	3717	-257
230	DUMMY	3776	-257
231	DUMMY	3835	-257
232	DUMMY	3894	-257
233	DUMMY	3953	-257
234	DUMMY	4012	-257
235	DUMMY	4071	-257
236	DUMMY	4130	-257
237	DUMMY	4189	-257
238	DUMMY	4248	-257
239	DUMMY	4307	-257
240	DUMMY	4366	-257
241	DUMMY	4425	-257
242	AVDD	4484	-257
243	AVDD	4543	-257
244	AVDD	4602	-257
245	AVDD	4661	-257
246	AVDD	4720	-257
247	AVDD	4779	-257
248	AVDD	4838	-257
249	AVDD	4897	-257
250	PGND	4956	-257
251	PGND	5015	-257
252	PGND	5074	-257
253	PGND	5133	-257
254	PGND	5192	-257
255	PGND	5251	-257
256	PGND	5310	-257
257	PGND	5369	-257
258	DUMMY	5428	-257
259	DUMMY	5487	-257
260	DUMMY	5546	-257
261	DUMMY	5605	-257
262	AVDD	5664	-257
263	AVDD	5723	-257
264	AVDD	5782	-257
265	AVDD	5841	-257
266	AVDD	5900	-257
267	AVDD	5959	-257
268	TESTOUT9	6018	-257
269	TESTOUT9	6077	-257
270	TESTOUT9	6136	-257
271	TESTOUT9	6195	-257

NO.	Pin Name	X	Y
272	TESTOUT9	6254	-257
273	TESTOUT9	6313	-257
274	AVCL	6372	-257
275	AVCL	6431	-257
276	AVCL	6490	-257
277	AVCL	6549	-257
278	AVCL	6608	-257
279	AVCL	6667	-257
280	TESTOUT11	6726	-257
281	TESTOUT11	6785	-257
282	TESTOUT11	6844	-257
283	TESTOUT11	6903	-257
284	TESTOUT11	6962	-257
285	TESTOUT11	7021	-257
286	VCIP	7080	-257
287	VCIP	7139	-257
288	VCIP	7198	-257
289	VCIP	7257	-257
290	VCIP	7316	-257
291	VCIP	7375	-257
292	VCIP	7434	-257
293	VCIP	7493	-257
294	VGSP	7552	-257
295	VGSP	7611	-257
296	VGSP	7670	-257
297	VGSP	7729	-257
298	VGSP	7788	-257
299	VGSP	7847	-257
300	TESTOUT13	7906	-257
301	TESTOUT13	7965	-257
302	TESTOUT13	8024	-257
303	TESTOUT13	8083	-257
304	TESTOUT13	8142	-257
305	TESTOUT13	8201	-257
306	VGH	8260	-257
307	VGH	8319	-257
308	VGH	8378	-257
309	VGH	8437	-257
310	VGH	8496	-257
311	VGH	8555	-257
312	TESTOUT14	8614	-257
313	TESTOUT14	8673	-257
314	TESTOUT14	8732	-257
315	TESTOUT14	8791	-257
316	TESTOUT14	8850	-257
317	TESTOUT14	8909	-257
318	TESTOUT15	8968	-257
319	TESTOUT15	9027	-257
320	TESTOUT15	9086	-257
321	TESTOUT15	9145	-257
322	TESTOUT15	9204	-257
323	TESTOUT15	9263	-257
324	VGL	9322	-257
325	VGL	9381	-257
326	VGL	9440	-257
327	VGL	9499	-257

NO.	Pin Name	X	Y
328	VGL	9558	-257
329	VGL	9617	-257
330	DUMMY	9676	-257
331	DUMMY	9735	-257
332	DUMMY	9945	127
333	DUMMY	9930	257
334	G2	9900	127
335	G4	9885	257
336	G6	9870	127
337	G8	9855	257
338	G10	9840	127
339	G12	9825	257
340	G14	9810	127
341	G16	9795	257
342	G18	9780	127
343	G20	9765	257
344	G22	9750	127
345	G24	9735	257
346	G26	9720	127
347	G28	9705	257
348	G30	9690	127
349	G32	9675	257
350	G34	9660	127
351	G36	9645	257
352	G38	9630	127
353	G40	9615	257
354	G42	9600	127
355	G44	9585	257
356	G46	9570	127
357	G48	9555	257
358	G50	9540	127
359	G52	9525	257
360	G54	9510	127
361	G56	9495	257
362	G58	9480	127
363	G60	9465	257
364	G62	9450	127
365	G64	9435	257
366	G66	9420	127
367	G68	9405	257
368	G70	9390	127
369	G72	9375	257
370	G74	9360	127
371	G76	9345	257
372	G78	9330	127
373	G80	9315	257
374	G82	9300	127
375	G84	9285	257
376	G86	9270	127
377	G88	9255	257
378	G90	9240	127
379	G92	9225	257
380	G94	9210	127
381	G96	9195	257
382	G98	9180	127

NO.	Pin Name	X	Y
383	G100	9165	257
384	G102	9150	127
385	G104	9135	257
386	G106	9120	127
387	G108	9105	257
388	G110	9090	127
389	G112	9075	257
390	G114	9060	127
391	G116	9045	257
392	G118	9030	127
393	G120	9015	257
394	G122	9000	127
395	G124	8985	257
396	G126	8970	127
397	G128	8955	257
398	G130	8940	127
399	G132	8925	257
400	G134	8910	127
401	G136	8895	257
402	G138	8880	127
403	G140	8865	257
404	G142	8850	127
405	G144	8835	257
406	G146	8820	127
407	G148	8805	257
408	G150	8790	127
409	G152	8775	257
410	G154	8760	127
411	G156	8745	257
412	G158	8730	127
413	G160	8715	257
414	G162	8700	127
415	G164	8685	257
416	G166	8670	127
417	G168	8655	257
418	G170	8640	127
419	G172	8625	257
420	G174	8610	127
421	G176	8595	257
422	G178	8580	127
423	G180	8565	257
424	G182	8550	127
425	G184	8535	257
426	G186	8520	127
427	G188	8505	257
428	G190	8490	127
429	G192	8475	257
430	G194	8460	127
431	G196	8445	257
432	G198	8430	127
433	G200	8415	257
434	G202	8400	127
435	G204	8385	257
436	G206	8370	127
437	G208	8355	257
438	G210	8340	127

NO.	Pin Name	X	Y
439	G212	8325	257
440	G214	8310	127
441	G216	8295	257
442	G218	8280	127
443	G220	8265	257
444	G222	8250	127
445	G224	8235	257
446	G226	8220	127
447	G228	8205	257
448	G230	8190	127
449	G232	8175	257
450	G234	8160	127
451	G236	8145	257
452	G238	8130	127
453	G240	8115	257
454	G242	8100	127
455	G244	8085	257
456	G246	8070	127
457	G248	8055	257
458	G250	8040	127
459	G252	8025	257
460	G254	8010	127
461	G256	7995	257
462	G258	7980	127
463	G260	7965	257
464	G262	7950	127
465	G264	7935	257
466	G266	7920	127
467	G268	7905	257
468	G270	7890	127
469	G272	7875	257
470	G274	7860	127
471	G276	7845	257
472	G278	7830	127
473	G280	7815	257
474	G282	7800	127
475	G284	7785	257
476	G286	7770	127
477	G288	7755	257
478	G290	7740	127
479	G292	7725	257
480	G294	7710	127
481	G296	7695	257
482	G298	7680	127
483	G300	7665	257
484	G302	7650	127
485	G304	7635	257
486	G306	7620	127
487	G308	7605	257
488	G310	7590	127
489	G312	7575	257
490	G314	7560	127
491	G316	7545	257
492	G318	7530	127
493	G320	7515	257
494	G322	7500	127

NO.	Pin Name	X	Y
495	G324	7485	257
496	G326	7470	127
497	G328	7455	257
498	G330	7440	127
499	G332	7425	257
500	G334	7410	127
501	G336	7395	257
502	G338	7380	127
503	G340	7365	257
504	G342	7350	127
505	G344	7335	257
506	G346	7320	127
507	G348	7305	257
508	G350	7290	127
509	G352	7275	257
510	G354	7260	127
511	G356	7245	257
512	G358	7230	127
513	G360	7215	257
514	G362	7200	127
515	G364	7185	257
516	G366	7170	127
517	G368	7155	257
518	G370	7140	127
519	G372	7125	257
520	G374	7110	127
521	G376	7095	257
522	G378	7080	127
523	G380	7065	257
524	G382	7050	127
525	G384	7035	257
526	G386	7020	127
527	G388	7005	257
528	G390	6990	127
529	G392	6975	257
530	G394	6960	127
531	G396	6945	257
532	G398	6930	127
533	G400	6915	257
534	G402	6900	127
535	G404	6885	257
536	G406	6870	127
537	G408	6855	257
538	G410	6840	127
539	G412	6825	257
540	G414	6810	127
541	G416	6795	257
542	G418	6780	127
543	G420	6765	257
544	G422	6750	127
545	G424	6735	257
546	G426	6720	127
547	G428	6705	257
548	G430	6690	127
549	G432	6675	257
550	G434	6660	127

NO.	Pin Name	X	Y
551	G436	6645	257
552	G438	6630	127
553	G440	6615	257
554	G442	6600	127
555	G444	6585	257
556	G446	6570	127
557	G448	6555	257
558	G450	6540	127
559	G452	6525	257
560	G454	6510	127
561	G456	6495	257
562	G458	6480	127
563	G460	6465	257
564	G462	6450	127
565	G464	6435	257
566	G466	6420	127
567	G468	6405	257
568	G470	6390	127
569	G472	6375	257
570	G474	6360	127
571	G476	6345	257
572	G478	6330	127
573	G480	6315	257
574	G482	6300	127
575	G484	6285	257
576	G486	6270	127
577	G488	6255	257
578	G490	6240	127
579	G492	6225	257
580	G494	6210	127
581	G496	6195	257
582	G498	6180	127
583	G500	6165	257
584	G502	6150	127
585	G504	6135	257
586	G506	6120	127
587	G508	6105	257
588	G510	6090	127
589	G512	6075	257
590	G514	6060	127
591	G516	6045	257
592	G518	6030	127
593	G520	6015	257
594	G522	6000	127
595	G524	5985	257
596	G526	5970	127
597	G528	5955	257
598	G530	5940	127
599	G532	5925	257
600	G534	5910	127
601	G536	5895	257
602	G538	5880	127
603	G540	5865	257
604	G542	5850	127
605	G544	5835	257
606	DUMMY	5760	127

NO.	Pin Name	X	Y
607	DUMMY	5745	257
608	DUMMY	5730	127
609	DUMMY	5715	257
610	DUMMY	5700	127
611	DUMMY	5685	257
612	S1	5610	127
613	S2	5595	257
614	S3	5580	127
615	S4	5565	257
616	S5	5550	127
617	S6	5535	257
618	S7	5520	127
619	S8	5505	257
620	S9	5490	127
621	S10	5475	257
622	S11	5460	127
623	S12	5445	257
624	S13	5430	127
625	S14	5415	257
626	S15	5400	127
627	S16	5385	257
628	S17	5370	127
629	S18	5355	257
630	S19	5340	127
631	S20	5325	257
632	S21	5310	127
633	S22	5295	257
634	S23	5280	127
635	S24	5265	257
636	S25	5250	127
637	S26	5235	257
638	S27	5220	127
639	S28	5205	257
640	S29	5190	127
641	S30	5175	257
642	S31	5160	127
643	S32	5145	257
644	S33	5130	127
645	S34	5115	257
646	S35	5100	127
647	S36	5085	257
648	S37	5070	127
649	S38	5055	257
650	S39	5040	127
651	S40	5025	257
652	S41	5010	127
653	S42	4995	257
654	S43	4980	127
655	S44	4965	257
656	S45	4950	127
657	S46	4935	257
658	S47	4920	127
659	S48	4905	257
660	S49	4890	127
661	S50	4875	257
662	S51	4860	127

NO.	Pin Name	X	Y
663	S52	4845	257
664	S53	4830	127
665	S54	4815	257
666	S55	4800	127
667	S56	4785	257
668	S57	4770	127
669	S58	4755	257
670	S59	4740	127
671	S60	4725	257
672	S61	4710	127
673	S62	4695	257
674	S63	4680	127
675	S64	4665	257
676	S65	4650	127
677	S66	4635	257
678	S67	4620	127
679	S68	4605	257
680	S69	4590	127
681	S70	4575	257
682	S71	4560	127
683	S72	4545	257
684	S73	4530	127
685	S74	4515	257
686	S75	4500	127
687	S76	4485	257
688	S77	4470	127
689	S78	4455	257
690	S79	4440	127
691	S80	4425	257
692	S81	4410	127
693	S82	4395	257
694	S83	4380	127
695	S84	4365	257
696	S85	4350	127
697	S86	4335	257
698	S87	4320	127
699	S88	4305	257
700	S89	4290	127
701	S90	4275	257
702	S91	4260	127
703	S92	4245	257
704	S93	4230	127
705	S94	4215	257
706	S95	4200	127
707	S96	4185	257
708	S97	4170	127
709	S98	4155	257
710	S99	4140	127
711	S100	4125	257
712	S101	4110	127
713	S102	4095	257
714	S103	4080	127
715	S104	4065	257
716	S105	4050	127
717	S106	4035	257
718	S107	4020	127

NO.	Pin Name	X	Y
719	S108	4005	257
720	S109	3990	127
721	S110	3975	257
722	S111	3960	127
723	S112	3945	257
724	S113	3930	127
725	S114	3915	257
726	S115	3900	127
727	S116	3885	257
728	S117	3870	127
729	S118	3855	257
730	S119	3840	127
731	S120	3825	257
732	S121	3810	127
733	S122	3795	257
734	S123	3780	127
735	S124	3765	257
736	S125	3750	127
737	S126	3735	257
738	S127	3720	127
739	S128	3705	257
740	S129	3690	127
741	S130	3675	257
742	S131	3660	127
743	S132	3645	257
744	S133	3630	127
745	S134	3615	257
746	S135	3600	127
747	S136	3585	257
748	S137	3570	127
749	S138	3555	257
750	S139	3540	127
751	S140	3525	257
752	S141	3510	127
753	S142	3495	257
754	S143	3480	127
755	S144	3465	257
756	S145	3450	127
757	S146	3435	257
758	S147	3420	127
759	S148	3405	257
760	S149	3390	127
761	S150	3375	257
762	S151	3360	127
763	S152	3345	257
764	S153	3330	127
765	S154	3315	257
766	S155	3300	127
767	S156	3285	257
768	S157	3270	127
769	S158	3255	257
770	S159	3240	127
771	S160	3225	257
772	S161	3210	127
773	S162	3195	257
774	S163	3180	127

NO.	Pin Name	X	Y
775	S164	3165	257
776	S165	3150	127
777	S166	3135	257
778	S167	3120	127
779	S168	3105	257
780	S169	3090	127
781	S170	3075	257
782	S171	3060	127
783	S172	3045	257
784	S173	3030	127
785	S174	3015	257
786	S175	3000	127
787	S176	2985	257
788	S177	2970	127
789	S178	2955	257
790	S179	2940	127
791	S180	2925	257
792	S181	2910	127
793	S182	2895	257
794	S183	2880	127
795	S184	2865	257
796	S185	2850	127
797	S186	2835	257
798	S187	2820	127
799	S188	2805	257
800	S189	2790	127
801	S190	2775	257
802	S191	2760	127
803	S192	2745	257
804	S193	2730	127
805	S194	2715	257
806	S195	2700	127
807	S196	2685	257
808	S197	2670	127
809	S198	2655	257
810	S199	2640	127
811	S200	2625	257
812	S201	2610	127
813	S202	2595	257
814	S203	2580	127
815	S204	2565	257
816	S205	2550	127
817	S206	2535	257
818	S207	2520	127
819	S208	2505	257
820	S209	2490	127
821	S210	2475	257
822	S211	2460	127
823	S212	2445	257
824	S213	2430	127
825	S214	2415	257
826	S215	2400	127
827	S216	2385	257
828	S217	2370	127
829	S218	2355	257
830	S219	2340	127

NO.	Pin Name	X	Y
831	S220	2325	257
832	S221	2310	127
833	S222	2295	257
834	S223	2280	127
835	S224	2265	257
836	S225	2250	127
837	S226	2235	257
838	S227	2220	127
839	S228	2205	257
840	S229	2190	127
841	S230	2175	257
842	S231	2160	127
843	S232	2145	257
844	S233	2130	127
845	S234	2115	257
846	S235	2100	127
847	S236	2085	257
848	S237	2070	127
849	S238	2055	257
850	S239	2040	127
851	S240	2025	257
852	S241	2010	127
853	S242	1995	257
854	S243	1980	127
855	S244	1965	257
856	S245	1950	127
857	S246	1935	257
858	S247	1920	127
859	S248	1905	257
860	S249	1890	127
861	S250	1875	257
862	S251	1860	127
863	S252	1845	257
864	S253	1830	127
865	S254	1815	257
866	S255	1800	127
867	S256	1785	257
868	S257	1770	127
869	S258	1755	257
870	S259	1740	127
871	S260	1725	257
872	S261	1710	127
873	S262	1695	257
874	S263	1680	127
875	S264	1665	257
876	S265	1650	127
877	S266	1635	257
878	S267	1620	127
879	S268	1605	257
880	S269	1590	127
881	S270	1575	257
882	S271	1560	127
883	S272	1545	257
884	S273	1530	127
885	S274	1515	257
886	S275	1500	127

NO.	Pin Name	X	Y
887	S276	1485	257
888	S277	1470	127
889	S278	1455	257
890	S279	1440	127
891	S280	1425	257
892	S281	1410	127
893	S282	1395	257
894	S283	1380	127
895	S284	1365	257
896	S285	1350	127
897	S286	1335	257
898	S287	1320	127
899	S288	1305	257
900	S289	1290	127
901	S290	1275	257
902	S291	1260	127
903	S292	1245	257
904	S293	1230	127
905	S294	1215	257
906	S295	1200	127
907	S296	1185	257
908	S297	1170	127
909	S298	1155	257
910	S299	1140	127
911	S300	1125	257
912	S301	1110	127
913	S302	1095	257
914	S303	1080	127
915	S304	1065	257
916	S305	1050	127
917	S306	1035	257
918	S307	1020	127
919	S308	1005	257
920	S309	990	127
921	S310	975	257
922	S311	960	127
923	S312	945	257
924	S313	930	127
925	S314	915	257
926	S315	900	127
927	S316	885	257
928	S317	870	127
929	S318	855	257
930	S319	840	127
931	S320	825	257
932	S321	810	127
933	S322	795	257
934	S323	780	127
935	S324	765	257
936	S325	750	127
937	S326	735	257
938	S327	720	127
939	S328	705	257
940	S329	690	127
941	S330	675	257
942	S331	660	127

NO.	Pin Name	X	Y
943	S332	645	257
944	S333	630	127
945	S334	615	257
946	S335	600	127
947	S336	585	257
948	S337	570	127
949	S338	555	257
950	S339	540	127
951	S340	525	257
952	S341	510	127
953	S342	495	257
954	S343	480	127
955	S344	465	257
956	S345	450	127
957	S346	435	257
958	S347	420	127
959	S348	405	257
960	S349	390	127
961	S350	375	257
962	S351	360	127
963	S352	345	257
964	S353	330	127
965	S354	315	257
966	S355	300	127
967	S356	285	257
968	S357	270	127
969	S358	255	257
970	S359	240	127
971	S360	225	257
972	DUMMY	150	127
973	DUMMY	135	257
974	DUMMY	120	127
975	DUMMY	105	257
976	DUMMY	90	127
977	DUMMY	75	257
978	DUMMY	60	127
979	S361	-15	257
980	S362	-30	127
981	S363	-45	257
982	S364	-60	127
983	S365	-75	257
984	S366	-90	127
985	S367	-105	257
986	S368	-120	127
987	S369	-135	257
988	S370	-150	127
989	S371	-165	257
990	S372	-180	127
991	S373	-195	257
992	S374	-210	127
993	S375	-225	257
994	S376	-240	127
995	S377	-255	257
996	S378	-270	127
997	S379	-285	257
998	S380	-300	127

NO.	Pin Name	X	Y
999	S381	-315	257
1000	S382	-330	127
1001	S383	-345	257
1002	S384	-360	127
1003	S385	-375	257
1004	S386	-390	127
1005	S387	-405	257
1006	S388	-420	127
1007	S389	-435	257
1008	S390	-450	127
1009	S391	-465	257
1010	S392	-480	127
1011	S393	-495	257
1012	S394	-510	127
1013	S395	-525	257
1014	S396	-540	127
1015	S397	-555	257
1016	S398	-570	127
1017	S399	-585	257
1018	S400	-600	127
1019	S401	-615	257
1020	S402	-630	127
1021	S403	-645	257
1022	S404	-660	127
1023	S405	-675	257
1024	S406	-690	127
1025	S407	-705	257
1026	S408	-720	127
1027	S409	-735	257
1028	S410	-750	127
1029	S411	-765	257
1030	S412	-780	127
1031	S413	-795	257
1032	S414	-810	127
1033	S415	-825	257
1034	S416	-840	127
1035	S417	-855	257
1036	S418	-870	127
1037	S419	-885	257
1038	S420	-900	127
1039	S421	-915	257
1040	S422	-930	127
1041	S423	-945	257
1042	S424	-960	127
1043	S425	-975	257
1044	S426	-990	127
1045	S427	-1005	257
1046	S428	-1020	127
1047	S429	-1035	257
1048	S430	-1050	127
1049	S431	-1065	257
1050	S432	-1080	127
1051	S433	-1095	257
1052	S434	-1110	127
1053	S435	-1125	257
1054	S436	-1140	127

NO.	Pin Name	X	Y
1055	S437	-1155	257
1056	S438	-1170	127
1057	S439	-1185	257
1058	S440	-1200	127
1059	S441	-1215	257
1060	S442	-1230	127
1061	S443	-1245	257
1062	S444	-1260	127
1063	S445	-1275	257
1064	S446	-1290	127
1065	S447	-1305	257
1066	S448	-1320	127
1067	S449	-1335	257
1068	S450	-1350	127
1069	S451	-1365	257
1070	S452	-1380	127
1071	S453	-1395	257
1072	S454	-1410	127
1073	S455	-1425	257
1074	S456	-1440	127
1075	S457	-1455	257
1076	S458	-1470	127
1077	S459	-1485	257
1078	S460	-1500	127
1079	S461	-1515	257
1080	S462	-1530	127
1081	S463	-1545	257
1082	S464	-1560	127
1083	S465	-1575	257
1084	S466	-1590	127
1085	S467	-1605	257
1086	S468	-1620	127
1087	S469	-1635	257
1088	S470	-1650	127
1089	S471	-1665	257
1090	S472	-1680	127
1091	S473	-1695	257
1092	S474	-1710	127
1093	S475	-1725	257
1094	S476	-1740	127
1095	S477	-1755	257
1096	S478	-1770	127
1097	S479	-1785	257
1098	S480	-1800	127
1099	S481	-1815	257
1100	S482	-1830	127
1101	S483	-1845	257
1102	S484	-1860	127
1103	S485	-1875	257
1104	S486	-1890	127
1105	S487	-1905	257
1106	S488	-1920	127
1107	S489	-1935	257
1108	S490	-1950	127
1109	S491	-1965	257
1110	S492	-1980	127

NO.	Pin Name	X	Y
1111	S493	-1995	257
1112	S494	-2010	127
1113	S495	-2025	257
1114	S496	-2040	127
1115	S497	-2055	257
1116	S498	-2070	127
1117	S499	-2085	257
1118	S500	-2100	127
1119	S501	-2115	257
1120	S502	-2130	127
1121	S503	-2145	257
1122	S504	-2160	127
1123	S505	-2175	257
1124	S506	-2190	127
1125	S507	-2205	257
1126	S508	-2220	127
1127	S509	-2235	257
1128	S510	-2250	127
1129	S511	-2265	257
1130	S512	-2280	127
1131	S513	-2295	257
1132	S514	-2310	127
1133	S515	-2325	257
1134	S516	-2340	127
1135	S517	-2355	257
1136	S518	-2370	127
1137	S519	-2385	257
1138	S520	-2400	127
1139	S521	-2415	257
1140	S522	-2430	127
1141	S523	-2445	257
1142	S524	-2460	127
1143	S525	-2475	257
1144	S526	-2490	127
1145	S527	-2505	257
1146	S528	-2520	127
1147	S529	-2535	257
1148	S530	-2550	127
1149	S531	-2565	257
1150	S532	-2580	127
1151	S533	-2595	257
1152	S534	-2610	127
1153	S535	-2625	257
1154	S536	-2640	127
1155	S537	-2655	257
1156	S538	-2670	127
1157	S539	-2685	257
1158	S540	-2700	127
1159	S541	-2715	257
1160	S542	-2730	127
1161	S543	-2745	257
1162	S544	-2760	127
1163	S545	-2775	257
1164	S546	-2790	127
1165	S547	-2805	257
1166	S548	-2820	127

NO.	Pin Name	X	Y
1167	S549	-2835	257
1168	S550	-2850	127
1169	S551	-2865	257
1170	S552	-2880	127
1171	S553	-2895	257
1172	S554	-2910	127
1173	S555	-2925	257
1174	S556	-2940	127
1175	S557	-2955	257
1176	S558	-2970	127
1177	S559	-2985	257
1178	S560	-3000	127
1179	S561	-3015	257
1180	S562	-3030	127
1181	S563	-3045	257
1182	S564	-3060	127
1183	S565	-3075	257
1184	S566	-3090	127
1185	S567	-3105	257
1186	S568	-3120	127
1187	S569	-3135	257
1188	S570	-3150	127
1189	S571	-3165	257
1190	S572	-3180	127
1191	S573	-3195	257
1192	S574	-3210	127
1193	S575	-3225	257
1194	S576	-3240	127
1195	S577	-3255	257
1196	S578	-3270	127
1197	S579	-3285	257
1198	S580	-3300	127
1199	S581	-3315	257
1200	S582	-3330	127
1201	S583	-3345	257
1202	S584	-3360	127
1203	S585	-3375	257
1204	S586	-3390	127
1205	S587	-3405	257
1206	S588	-3420	127
1207	S589	-3435	257
1208	S590	-3450	127
1209	S591	-3465	257
1210	S592	-3480	127
1211	S593	-3495	257
1212	S594	-3510	127
1213	S595	-3525	257
1214	S596	-3540	127
1215	S597	-3555	257
1216	S598	-3570	127
1217	S599	-3585	257
1218	S600	-3600	127
1219	S601	-3615	257
1220	S602	-3630	127
1221	S603	-3645	257
1222	S604	-3660	127

NO.	Pin Name	X	Y
1223	S605	-3675	257
1224	S606	-3690	127
1225	S607	-3705	257
1226	S608	-3720	127
1227	S609	-3735	257
1228	S610	-3750	127
1229	S611	-3765	257
1230	S612	-3780	127
1231	S613	-3795	257
1232	S614	-3810	127
1233	S615	-3825	257
1234	S616	-3840	127
1235	S617	-3855	257
1236	S618	-3870	127
1237	S619	-3885	257
1238	S620	-3900	127
1239	S621	-3915	257
1240	S622	-3930	127
1241	S623	-3945	257
1242	S624	-3960	127
1243	S625	-3975	257
1244	S626	-3990	127
1245	S627	-4005	257
1246	S628	-4020	127
1247	S629	-4035	257
1248	S630	-4050	127
1249	S631	-4065	257
1250	S632	-4080	127
1251	S633	-4095	257
1252	S634	-4110	127
1253	S635	-4125	257
1254	S636	-4140	127
1255	S637	-4155	257
1256	S638	-4170	127
1257	S639	-4185	257
1258	S640	-4200	127
1259	S641	-4215	257
1260	S642	-4230	127
1261	S643	-4245	257
1262	S644	-4260	127
1263	S645	-4275	257
1264	S646	-4290	127
1265	S647	-4305	257
1266	S648	-4320	127
1267	S649	-4335	257
1268	S650	-4350	127
1269	S651	-4365	257
1270	S652	-4380	127
1271	S653	-4395	257
1272	S654	-4410	127
1273	S655	-4425	257
1274	S656	-4440	127
1275	S657	-4455	257
1276	S658	-4470	127
1277	S659	-4485	257
1278	S660	-4500	127

NO.	Pin Name	X	Y
1279	S661	-4515	257
1280	S662	-4530	127
1281	S663	-4545	257
1282	S664	-4560	127
1283	S665	-4575	257
1284	S666	-4590	127
1285	S667	-4605	257
1286	S668	-4620	127
1287	S669	-4635	257
1288	S670	-4650	127
1289	S671	-4665	257
1290	S672	-4680	127
1291	S673	-4695	257
1292	S674	-4710	127
1293	S675	-4725	257
1294	S676	-4740	127
1295	S677	-4755	257
1296	S678	-4770	127
1297	S679	-4785	257
1298	S680	-4800	127
1299	S681	-4815	257
1300	S682	-4830	127
1301	S683	-4845	257
1302	S684	-4860	127
1303	S685	-4875	257
1304	S686	-4890	127
1305	S687	-4905	257
1306	S688	-4920	127
1307	S689	-4935	257
1308	S690	-4950	127
1309	S691	-4965	257
1310	S692	-4980	127
1311	S693	-4995	257
1312	S694	-5010	127
1313	S695	-5025	257
1314	S696	-5040	127
1315	S697	-5055	257
1316	S698	-5070	127
1317	S699	-5085	257
1318	S700	-5100	127
1319	S701	-5115	257
1320	S702	-5130	127
1321	S703	-5145	257
1322	S704	-5160	127
1323	S705	-5175	257
1324	S706	-5190	127
1325	S707	-5205	257
1326	S708	-5220	127
1327	S709	-5235	257
1328	S710	-5250	127
1329	S711	-5265	257
1330	S712	-5280	127
1331	S713	-5295	257
1332	S714	-5310	127
1333	S715	-5325	257
1334	S716	-5340	127

NO.	Pin Name	X	Y
1335	S717	-5355	257
1336	S718	-5370	127
1337	S719	-5385	257
1338	S720	-5400	127
1339	VCOM	-5475	257
1340	VCOM	-5490	127
1341	VCOM	-5505	257
1342	VCOM	-5520	127
1343	VCOM	-5535	257
1344	VCOM	-5550	127
1345	VCOM	-5565	257
1346	VCOM	-5580	127
1347	VCOM	-5595	257
1348	VCOM	-5610	127
1349	DUMMY	-5685	257
1350	DUMMY	-5700	127
1351	DUMMY	-5715	257
1352	DUMMY	-5730	127
1353	DUMMY	-5745	257
1354	DUMMY	-5760	127
1355	G543	-5835	257
1356	G541	-5850	127
1357	G539	-5865	257
1358	G537	-5880	127
1359	G535	-5895	257
1360	G533	-5910	127
1361	G531	-5925	257
1362	G529	-5940	127
1363	G527	-5955	257
1364	G525	-5970	127
1365	G523	-5985	257
1366	G521	-6000	127
1367	G519	-6015	257
1368	G517	-6030	127
1369	G515	-6045	257
1370	G513	-6060	127
1371	G511	-6075	257
1372	G509	-6090	127
1373	G507	-6105	257
1374	G505	-6120	127
1375	G503	-6135	257
1376	G501	-6150	127
1377	G499	-6165	257
1378	G497	-6180	127
1379	G495	-6195	257
1380	G493	-6210	127
1381	G491	-6225	257
1382	G489	-6240	127
1383	G487	-6255	257
1384	G485	-6270	127
1385	G483	-6285	257
1386	G481	-6300	127
1387	G479	-6315	257
1388	G477	-6330	127
1389	G475	-6345	257
1390	G473	-6360	127

NO.	Pin Name	X	Y
1391	G471	-6375	257
1392	G469	-6390	127
1393	G467	-6405	257
1394	G465	-6420	127
1395	G463	-6435	257
1396	G461	-6450	127
1397	G459	-6465	257
1398	G457	-6480	127
1399	G455	-6495	257
1400	G453	-6510	127
1401	G451	-6525	257
1402	G449	-6540	127
1403	G447	-6555	257
1404	G445	-6570	127
1405	G443	-6585	257
1406	G441	-6600	127
1407	G439	-6615	257
1408	G437	-6630	127
1409	G435	-6645	257
1410	G433	-6660	127
1411	G431	-6675	257
1412	G429	-6690	127
1413	G427	-6705	257
1414	G425	-6720	127
1415	G423	-6735	257
1416	G421	-6750	127
1417	G419	-6765	257
1418	G417	-6780	127
1419	G415	-6795	257
1420	G413	-6810	127
1421	G411	-6825	257
1422	G409	-6840	127
1423	G407	-6855	257
1424	G405	-6870	127
1425	G403	-6885	257
1426	G401	-6900	127
1427	G399	-6915	257
1428	G397	-6930	127
1429	G395	-6945	257
1430	G393	-6960	127
1431	G391	-6975	257
1432	G389	-6990	127
1433	G387	-7005	257
1434	G385	-7020	127
1435	G383	-7035	257
1436	G381	-7050	127
1437	G379	-7065	257
1438	G377	-7080	127
1439	G375	-7095	257
1440	G373	-7110	127
1441	G371	-7125	257
1442	G369	-7140	127
1443	G367	-7155	257
1444	G365	-7170	127
1445	G363	-7185	257
1446	G361	-7200	127

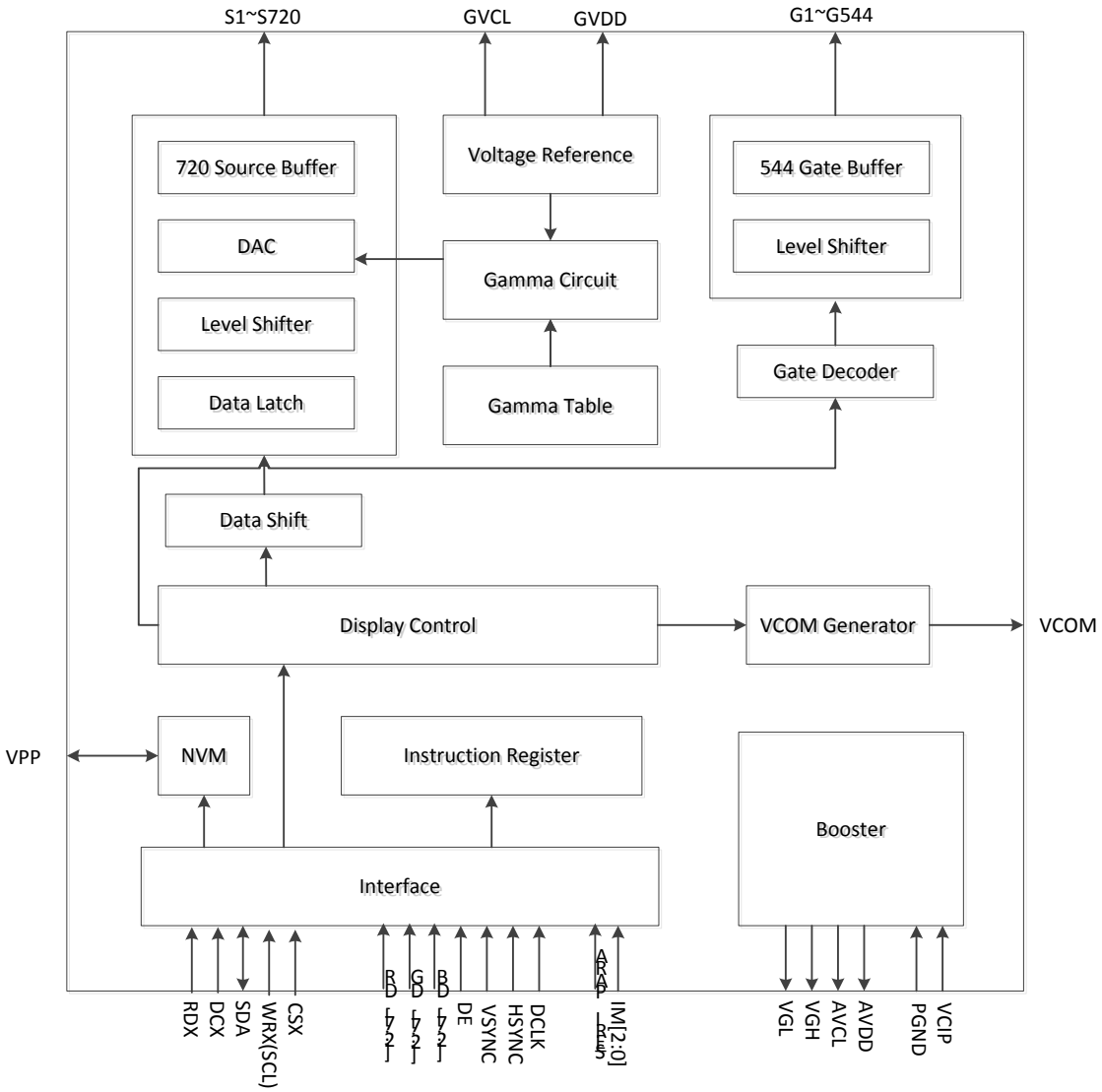
NO.	Pin Name	X	Y
1447	G359	-7215	257
1448	G357	-7230	127
1449	G355	-7245	257
1450	G353	-7260	127
1451	G351	-7275	257
1452	G349	-7290	127
1453	G347	-7305	257
1454	G345	-7320	127
1455	G343	-7335	257
1456	G341	-7350	127
1457	G339	-7365	257
1458	G337	-7380	127
1459	G335	-7395	257
1460	G333	-7410	127
1461	G331	-7425	257
1462	G329	-7440	127
1463	G327	-7455	257
1464	G325	-7470	127
1465	G323	-7485	257
1466	G321	-7500	127
1467	G319	-7515	257
1468	G317	-7530	127
1469	G315	-7545	257
1470	G313	-7560	127
1471	G311	-7575	257
1472	G309	-7590	127
1473	G307	-7605	257
1474	G305	-7620	127
1475	G303	-7635	257
1476	G301	-7650	127
1477	G299	-7665	257
1478	G297	-7680	127
1479	G295	-7695	257
1480	G293	-7710	127
1481	G291	-7725	257
1482	G289	-7740	127
1483	G287	-7755	257
1484	G285	-7770	127
1485	G283	-7785	257
1486	G281	-7800	127
1487	G279	-7815	257
1488	G277	-7830	127
1489	G275	-7845	257
1490	G273	-7860	127
1491	G271	-7875	257
1492	G269	-7890	127
1493	G267	-7905	257
1494	G265	-7920	127
1495	G263	-7935	257
1496	G261	-7950	127
1497	G259	-7965	257
1498	G257	-7980	127
1499	G255	-7995	257
1500	G253	-8010	127
1501	G251	-8025	257
1502	G249	-8040	127

NO.	Pin Name	X	Y
1503	G247	-8055	257
1504	G245	-8070	127
1505	G243	-8085	257
1506	G241	-8100	127
1507	G239	-8115	257
1508	G237	-8130	127
1509	G235	-8145	257
1510	G233	-8160	127
1511	G231	-8175	257
1512	G229	-8190	127
1513	G227	-8205	257
1514	G225	-8220	127
1515	G223	-8235	257
1516	G221	-8250	127
1517	G219	-8265	257
1518	G217	-8280	127
1519	G215	-8295	257
1520	G213	-8310	127
1521	G211	-8325	257
1522	G209	-8340	127
1523	G207	-8355	257
1524	G205	-8370	127
1525	G203	-8385	257
1526	G201	-8400	127
1527	G199	-8415	257
1528	G197	-8430	127
1529	G195	-8445	257
1530	G193	-8460	127
1531	G191	-8475	257
1532	G189	-8490	127
1533	G187	-8505	257
1534	G185	-8520	127
1535	G183	-8535	257
1536	G181	-8550	127
1537	G179	-8565	257
1538	G177	-8580	127
1539	G175	-8595	257
1540	G173	-8610	127
1541	G171	-8625	257
1542	G169	-8640	127
1543	G167	-8655	257
1544	G165	-8670	127
1545	G163	-8685	257
1546	G161	-8700	127
1547	G159	-8715	257
1548	G157	-8730	127
1549	G155	-8745	257
1550	G153	-8760	127
1551	G151	-8775	257
1552	G149	-8790	127
1553	G147	-8805	257
1554	G145	-8820	127
1555	G143	-8835	257
1556	G141	-8850	127
1557	G139	-8865	257
1558	G137	-8880	127

NO.	Pin Name	X	Y
1559	G135	-8895	257
1560	G133	-8910	127
1561	G131	-8925	257
1562	G129	-8940	127
1563	G127	-8955	257
1564	G125	-8970	127
1565	G123	-8985	257
1566	G121	-9000	127
1567	G119	-9015	257
1568	G117	-9030	127
1569	G115	-9045	257
1570	G113	-9060	127
1571	G111	-9075	257
1572	G109	-9090	127
1573	G107	-9105	257
1574	G105	-9120	127
1575	G103	-9135	257
1576	G101	-9150	127
1577	G99	-9165	257
1578	G97	-9180	127
1579	G95	-9195	257
1580	G93	-9210	127
1581	G91	-9225	257
1582	G89	-9240	127
1583	G87	-9255	257
1584	G85	-9270	127
1585	G83	-9285	257
1586	G81	-9300	127
1587	G79	-9315	257
1588	G77	-9330	127
1589	G75	-9345	257
1590	G73	-9360	127
1591	G71	-9375	257
1592	G69	-9390	127
1593	G67	-9405	257
1594	G65	-9420	127
1595	G63	-9435	257
1596	G61	-9450	127
1597	G59	-9465	257
1598	G57	-9480	127
1599	G55	-9495	257
1600	G53	-9510	127
1601	G51	-9525	257
1602	G49	-9540	127
1603	G47	-9555	257
1604	G45	-9570	127
1605	G43	-9585	257
1606	G41	-9600	127
1607	G39	-9615	257
1608	G37	-9630	127
1609	G35	-9645	257
1610	G33	-9660	127
1611	G31	-9675	257
1612	G29	-9690	127
1613	G27	-9705	257
1614	G25	-9720	127

NO.	Pin Name	X	Y
1615	G23	-9735	257
1616	G21	-9750	127
1617	G19	-9765	257
1618	G17	-9780	127
1619	G15	-9795	257
1620	G13	-9810	127
1621	G11	-9825	257
1622	G9	-9840	127
1623	G7	-9855	257
1624	G5	-9870	127
1625	G3	-9885	257
1626	G1	-9900	127
1627	DUMMY	-9930	257
1628	DUMMY	-9945	127

4. Block Diagram



5. Pin Description

Pin Name	I/O	Description
CS	I	Chip select, internal pull high.
SDA	I	Serial communication data input and output, internal pull low.
WRX	I	Clock input, internal pull high.
RDX	I	MCU interface read enable input, internal pull high.
DCX	I	Data or Command flag DCX = “H” is data DCX = “L” is command Internal pull high.
SPI4W	I	Std SPI 3/4 wire selection. SPI4W=“H”, 4 wire SPI; SPI4W=“L”, 3wire SPI.
PARA_SERI	I	PARA_SERI=“H”, Parallel 18-bit RGB input through DR2~7, DB2~DB7, DG2~DG7. PARA_SERI=“L”, Serial 6-bit RGB input through DG2~DG7. Internal pull high.
DR2~DR7	I	6-bit digital Red data input, internal pull low.
DG2~DG7	I	6-bit digital Green data input, internal pull low.
DB2~DB7	I	6-bit digital Blue data input, internal pull low.
DCLK	I	Clock signal; latching data at the falling edge, internal pull low.
HSYNC	I	Horizontal sync signal; negative polarity, internal pull high.
VSYNC	I	Vertical sync signal; negative polarity, internal pull high.
DE	I	Data input enable. Active High to enable the data input, internal pull low.
SYNC	I	No Function. User should connect it to “Low”, internal pull low.
HDIR	I	Horizontal scan direction control (Please refer to the register setting : HDIR) HDIR (pin) = “Low”: The definition of HDIR register setting is inversion from original. HDIR (register) = “0”: Shift from left to right; HDIR (register) = “1”: Shift from right to left. (Default) HDIR (pin) = “High”: The definition of HDIR register setting is invariant.

Pin Name	I/O	Description
		HDIR (register) = “0”: Shift from right to left; HDIR (register) = “1”: Shift from left to right. (Default) Internal pull high.
VDIR	I	Vertical scan direction control (Please refer to the register setting: VDIR) VDIR (pin) = “Low”: The definition of VDIR register setting is inversion from original. VDIR (register) = “0”: Shift from up to down; VDIR (register) = “1”: Shift from down to up. (Default) VDIR (pin) = “High”: The definition of VDIR register setting is invariant. VDIR (register) = “0”: Shift from down to up; VDIR (register) = “1”: Shift from up to down. (Default) Internal pull high.
VDPOL	I	VSYNC polarity control. VDPOL=“1”, negative polarity VDPOL=0, positive polarity When not used, user should connect it to “High” (Please refer to the register setting : VDPOL) Internal pull high.
HDPOL	I	HSYNC polarity control. HDPOL=“1”, negative polarity HDPOL=“0”, positive polarity When not used, user should connect it to “High” (Please refer to the register setting : HDPOL) Internal pull high.
DCLKPOL	I	DCLK polarity control. DCLKPOL=“1”, negative polarity DCLKPOL=“0”, positive polarity (Please refer to the register setting : DCLKPOL) Internal pull high.
SBGR	I	Data R[7:2] & B[7:2] exchanged internally SBGR=“1” R[7:2]→B[7:2] B[7:2]→R[7:2] SBGR=“0” R[7:2]→R[7:2] B[7:2]→B[7:2] Internal pull low.
GRB	I	Global reset. Active low, Internal pull high
DISP	I	User should connect it to “Low”, Internal pull high.
IM[2:0]	I	IM = 3’b000, Intel-8080 interface enable; IM = 3’b001, Standard SPI interface enable; IM = 3’b010, Dual SPI interface enable;

Pin Name	I/O	Description
		IM = 3'b011, Quard SPI interface enable; IM = 3'b100, RGB interface enable. Internal pull low.
TE	O	Tearing effect output pin is used to synchronize MCU frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is GND level.
Power Supply		
VCI	P	Power supply for analog circuit
IOVCC	P	Power supply for digital interface I/O pins
VCIP	P	Power supply for charge pump circuit
AGND	G	Ground pin for analog circuit
DGND	G	Ground pin for digital circuit
PGND	G	Ground pin for charge pump circuit
DVDD	P	Internal digital power
VPP	P	Power input pin for NVM. When writing NVM, it needs external power supply voltage (7.5V). If not used, let this pin open.
AVCL	P	Power pad for analog circuit.
AVDD	P	Power pad for analog circuit.
VGH	P	Positive power supply for gate driver output.
VGL	P	Negative power supply for gate driver output.
GVDD	P	A reference voltage (Positive) of grayscale voltage generator.
GVCL	P	A reference voltage (Negative) of grayscale voltage generator.
VGSP	P	Internal Virtual Ground monitor pin
Test Pin		
TEST_IN3	I	Test pins for internal testing only. Internal pull low.
TEST_IN4	I	Dummy pin
TEST_IN5	I	Test pins for internal testing only. Internal pull high.
TESTIN0~3	I	Dummy pins

Pin Name	I/O	Description
TESTOUT9	O	Analog test pins for internal testing only.
TESTOUT11		
TESTOUT13		
TESTOUT14		
TESTOUT15		
TESTOUT[0:7]	O	Digital test pins for internal testing only.

Note:
I: input, O: output, I/O: input/output, P: power input, G: GND
If unused pin don’t floating, the pin fix to IOVCC or DGND.

6. Interface Description

6.1. Interface and Bus Mapping

The interface of NV3041A supports 8/9/16 bit parallel data bus for 8080 series, Std SPI, D-SPI, Q-SPI and RGB interface.

Selection of these interface are set by IM<2:0> pins as shown below Table 6-1-1.

IM2	IM1	IM0	Interface	Read Back Data Bus Selection
0	0	0	8080 series 8bit	DG3-2, DB7-2
			8080 series 9bit	DG4-2, DB7-2
			8080 series 16bit	DR5-2, DG7-2, DB7-2
0	0	1	3/4-wire Std SPI	SDA: In/Out
0	1	0	Dual SPI	SDA:In/Out DCX:In
0	1	1	Quad SPI	SDA:In/Out DCX:In DB[2]:In DB[3]:In
1	0	0	Parallel 18-bit RGB	DR7-2, DG7-2, DB7-2
			Serial 6-bit RGB	DG7-2(Default) Use register E1H bit[1:0] to select from DR7-2, DG7-2 or DB7-2

Table 6-1-1

6.2. Inter-8080 Parallel Interface

The MCU 8080 interface has different bus width application as 8/9/16bit. The chip-select CSX (active low) enables and disables the parallel interface. GRB (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and DR[7:2], DG[7:2], DB[7:2] is parallel data.

NV3041A latches the input data at the rising edge of WRX signal. The DCX is the data or command flag. When DCX='1', DR[7:2], DG[7:2], DB[7:2] bits are display RAM data or command parameters. When DC='0', DR[7:2], DG[7:2], DB[7:2] bits are commands.

The 8080-series bi-direction interface can be used for communication between the micro- controller and LCD driver chip. The interface functions of 8080-series parallel interface are given in Table 6-2-1.

IM2	IM1	IM0	41H bus_width[1:0]	Interface
0	0	0	2'b01	8-bit parallel
0	0	0	2'b10	9-bit parallel
0	0	0	2'b11	16-bit parallel

Table 6-2-1

6.2.1. Write Cycle/Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, WRX) and data signals (DR[7:2], DG[7:2], DB[7:2]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (= '0') and vice versa it is data (= '1'). The write cycle is described in the following figure.

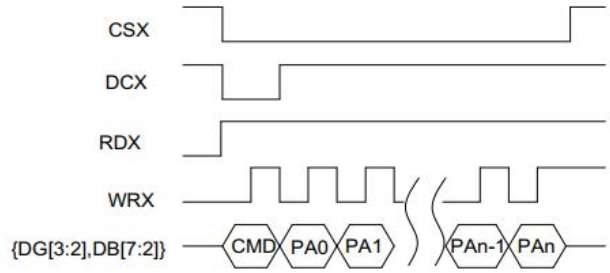


Figure 6-2-1-1 8080 MCU Write sequence (8-bit parallel)

6.2.2. Read Cycle/Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from the display via interface. The display sends data (DR[7:2], DG[7:2], DB[7:2]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

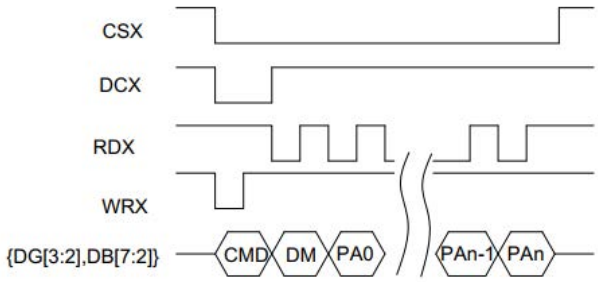


Figure 6-2-2-1 8080 Read sequence (8-bit parallel)

Note:
1. Reading operation applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, etc.;
2. Read operation need one dummy cycle.

6.3. SPI interface (Std-SPI, Dual-SPI, Quard-SPI)

6.3.1. Introduction

Pad Name	Serial Interface Pin Name	Description
CS	CSX	A chip select signal.Signal is active low.
WRX	SCL	This pin is used serial interface clock.
SDA	SDA/ SDO1	SPI bi-direction data pin
DCX	DCX/SDO2	Std-SPI(4 wire): command or parameter select. Dual-SPI: the second data lane. Quard-SPI: the second data pin
DB2	SDO3	the third pin of Quard-SPI
DB3	SDO4	the fourth pin of Quard-SPI

Table 6-3-1-1

The selection of interface is done by IM<2:0> bits. Please refer to below Table 6-3-1-2

IM2	IM1	IM0	41H bus_width[1:0]	OPCODE	SPI4W	Interface
0	0	1			0	3-wire 9bit SPI
					1	4-wire 8bit SPI
0	1	0	2’b 00			6bit Dual-SPI
			2’b 01			8bit Dual-SPI
			2’b 10			9bit Dual-SPI
0	1	1		8'h02		1 line data or cmd Quard-SPI
				8'h32/8'h12		4 line data Quard-SPI

Table 6-3-1-2

6.3.2. Std SPI Interface

NV3041A supplies 3-wire/ 9-bit and 4-wire/8-bit bi-directional serial interfaces for communication between MCU and NV3041A Driver.

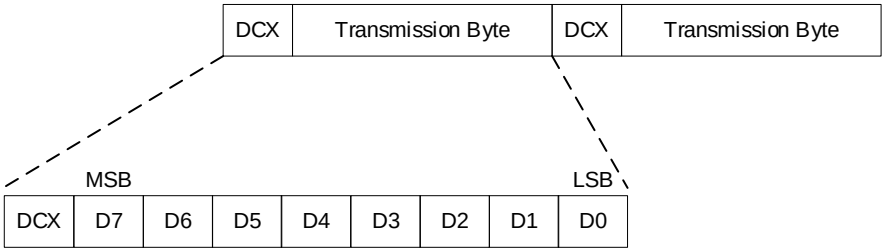
The 3-wire serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDA/SDO).

The 4-wire serial mode consists of the Data/Command selection input (DCX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDA/SDO) for data transmission. The data bus (DR[7:2], DG[7:2], DB[7:2]), which are not used, must be connected to GND.

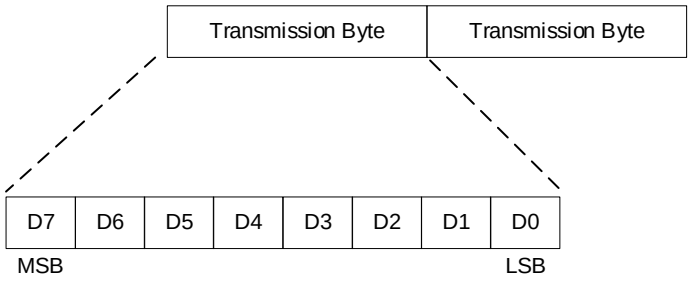
6.3.2.1. Write Cycle Sequence

The write mode of the interface means that MCU writes commands or data to NV3041A. The 3-wire serial data packet contains a data/command select bit (DCX) and a transmission byte. If the DCX bit is “low”, the transmission byte is interpreted as a command byte. If the DCX bit is “high”, the transmission byte is captured as RAM data or parameter of specified register.

Any instruction can be sent in any order to NV3041A and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4- wire serial interface.

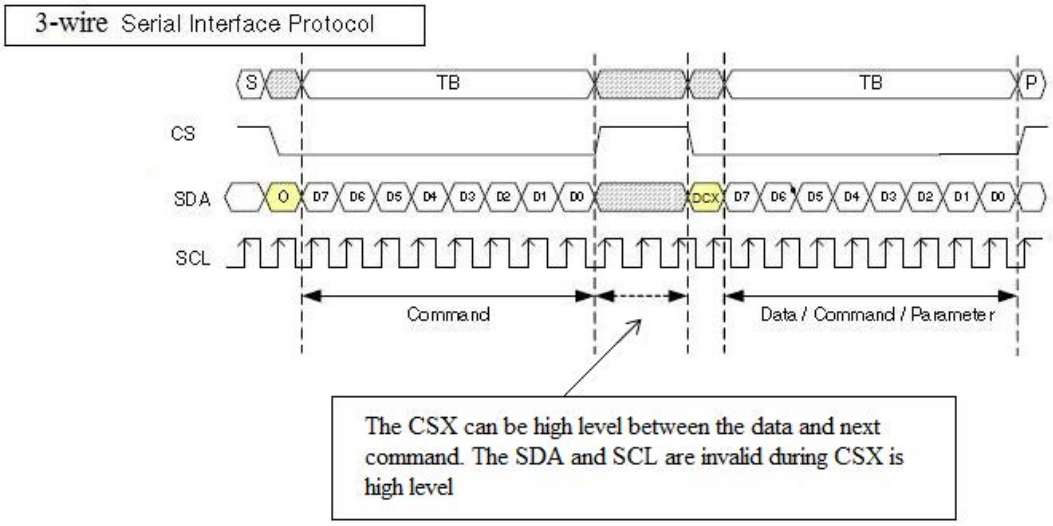


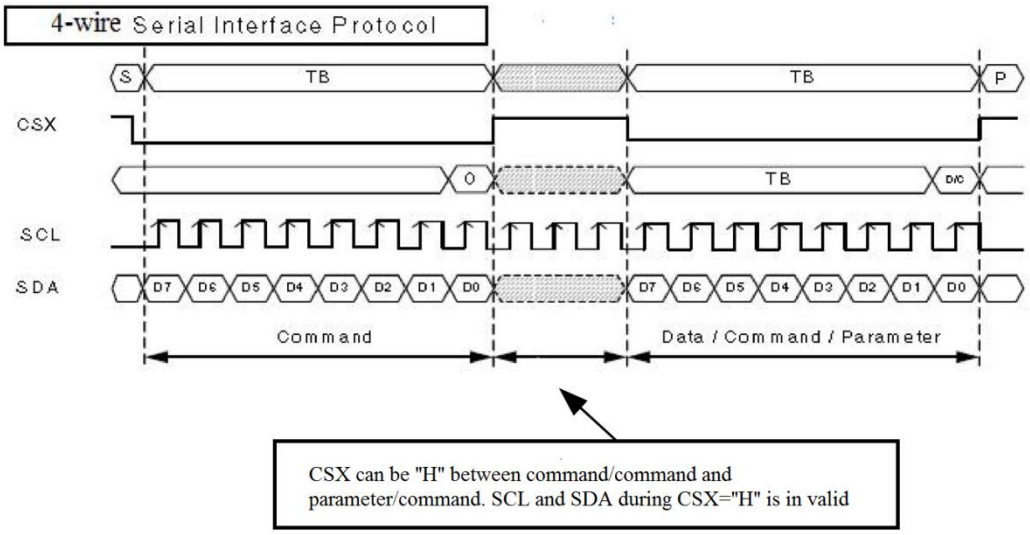
Std-SPI 3-Wire Data flow



Std-SPI 4-Wire Data flow

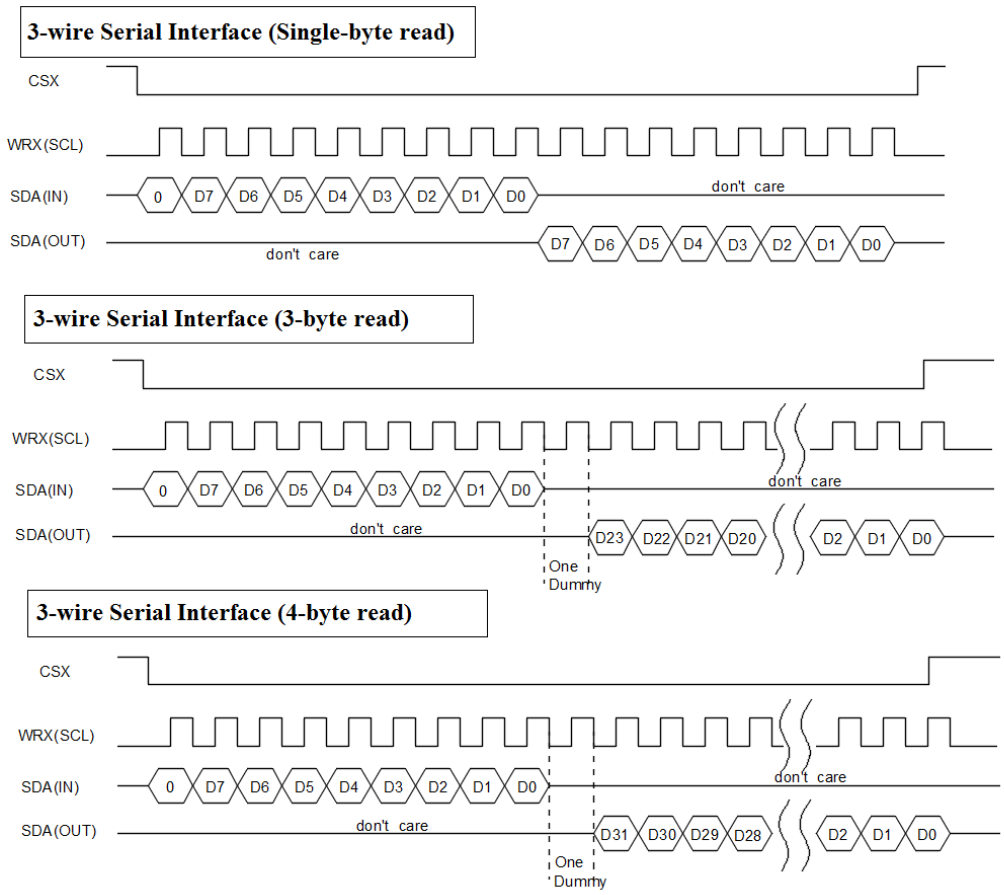
MCU drives the CSX pin to low and starts by setting the DCX bit on SDA. The bit is read by NV3041A on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the MCU. On the next falling edge of SCL, the next bit (D6) is set on SDA. The 3/4-wire serial interface writes sequence described in the figure as below.

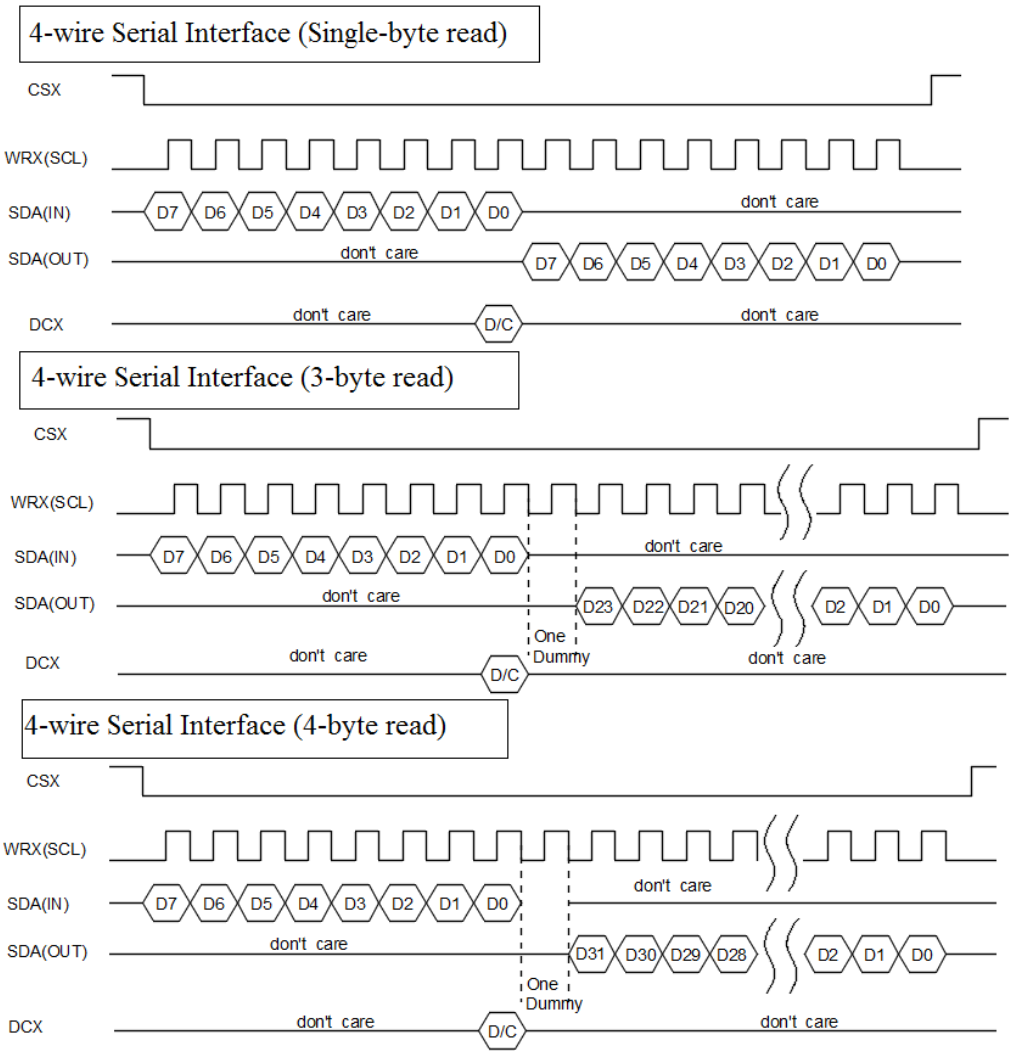




6.3.2.2. Read Cycle Sequence

The read mode of interface means that the MCU reads register's parameter from NV3041A. The MCU has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. NV3041A latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri- state and no later than at the falling edge of SCL of the last bit. The read mode has two types of transmitted command data (single/multi-byte) according to command code.




4-wire Serial Interface (Single-byte read)
CSX
WRX(SCL)
SDA(IN)
D7 D6 D5 D4 D3 D2 D1 D0
don't care
SDA(OUT)
don't care
D7 D6 D5 D4 D3 D2 D1 D0
DCX
don't care
D/C
don't care
4-wire Serial Interface (3-byte read)
CSX
WRX(SCL)
SDA(IN)
D7 D6 D5 D4 D3 D2 D1 D0
don't care
SDA(OUT)
don't care
D23 D22 D21 D20
D2 D1 D0
One Dummy
DCX
don't care
D/C
don't care
4-wire Serial Interface (4-byte read)
CSX
WRX(SCL)
SDA(IN)
D7 D6 D5 D4 D3 D2 D1 D0
don't care
SDA(OUT)
don't care
D31 D30 D29 D28
D2 D1 D0
One Dummy
DCX
don't care
D/C
don't care

6.3.3. Dual-SPI Interface

NV3041A supplies 6-bit, 8-bit and 9-bit Dual SPI interfaces for communication between MCU and NV3041A.

Two data lane serial interface use: CSX (chip enable), DCX(serial clock) and SDA (serial data input/output 1), and WRX (serial data input 2).

Set IM<2:0> as 3'b010 to enable Dual-SPI interface.

6.3.3.1. Write Cycle Sequence

The command write protocol of 2 data lane serial interface is the same with the 3-wire serial interface. RAM write sequences are illustrated in section 6.4.14 and 6.4.15.

6.3.3.2. Read Cycle Sequence

The read mode of 2 data lane serial interface is the same with the 3-wire serial interface. No RAM Reading supported.

6.3.4. Quad-SPI Interface

NV3041A supports Quad SPI interfaces for communication between MCU and NV3041A.

Four data lane serial interface use: CSX (chip enable), WRX (serial clock) and SDA (serial data input/output 1), DCX (serial data input 2), DB2 (serial data input 3) and DB3 (serial data input 4).

Set IM<2:0> as 3'b011 to enable QSPI Interface.

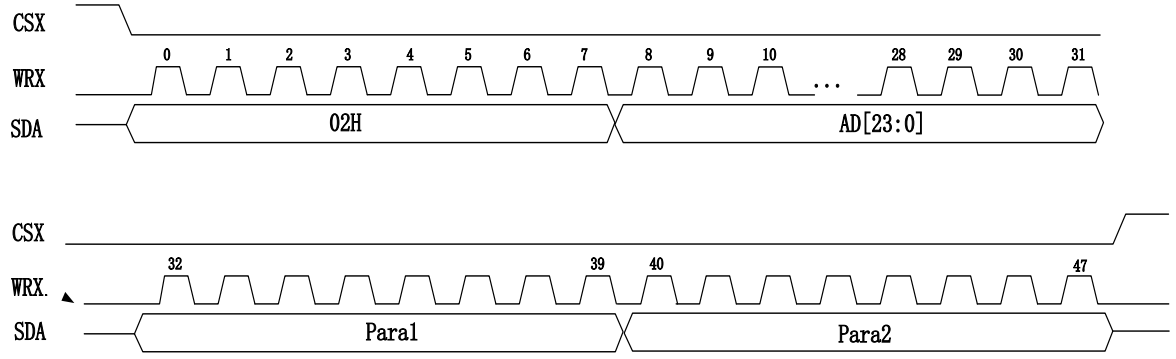
Each transmission has three part: op-code (first byte after CSX falling edge), Address and Data. op-code used to distinguish different operations between MCU and NV3041A, as below table shows.

OP code	Operation	Description
02H	Write Command	In general, this operation used to write registers. When the address is "2C", the following data is identified as RAM data. It's not a good choice because of its slowly accessing rate.
03H	Read Command	Read register content from NV3041A
12H	Write RAM data	The address must be "2C" and the timing takes 24 cycles, see the section 6.4.12 and 6.4.13 for details
32H	Write RAM data	The address must be "2C" and the timing takes 6 cycles, see the section 6.4.12 and 6.4.13 for details

Note: Each transmission must end with CSX rising edge.

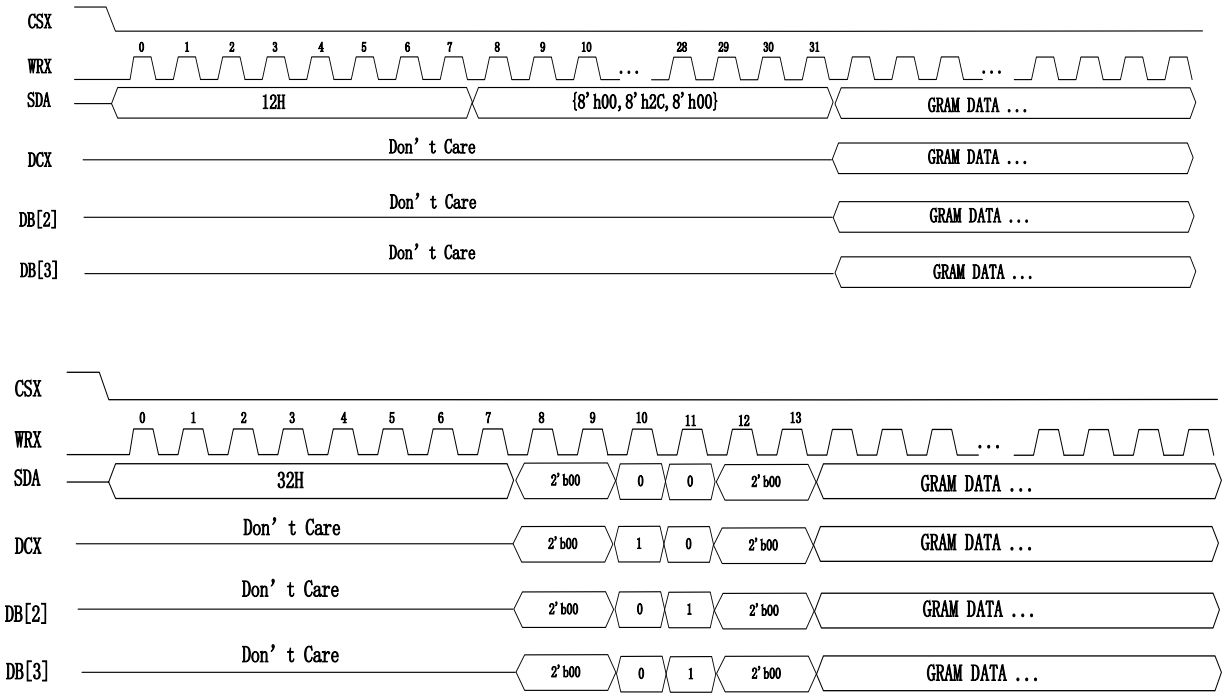
6.3.4.1. Write Cycle Sequence(op code = “02H”)

The function of command writing is driven by CSX, WRX, SDA, as shown below. op code “02H” is sent after CSX falling edge. AD[23:0] format is {8’h00,CMD[7:0],8’h00}. If the address includes “2CH” command, Para# is captured as GRAM data.



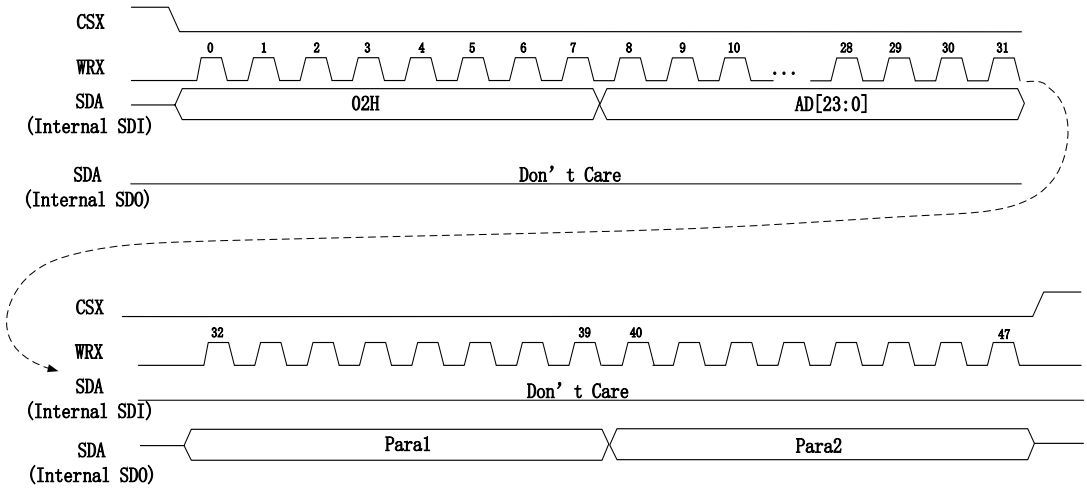
6.3.4.2. Write GRAM (op code = “12H” or “32H”)

GRAM writing operation must be terminated with CSX rising edge. The GRAM DATA format is illustrated in section 6.4.10~6.4.13



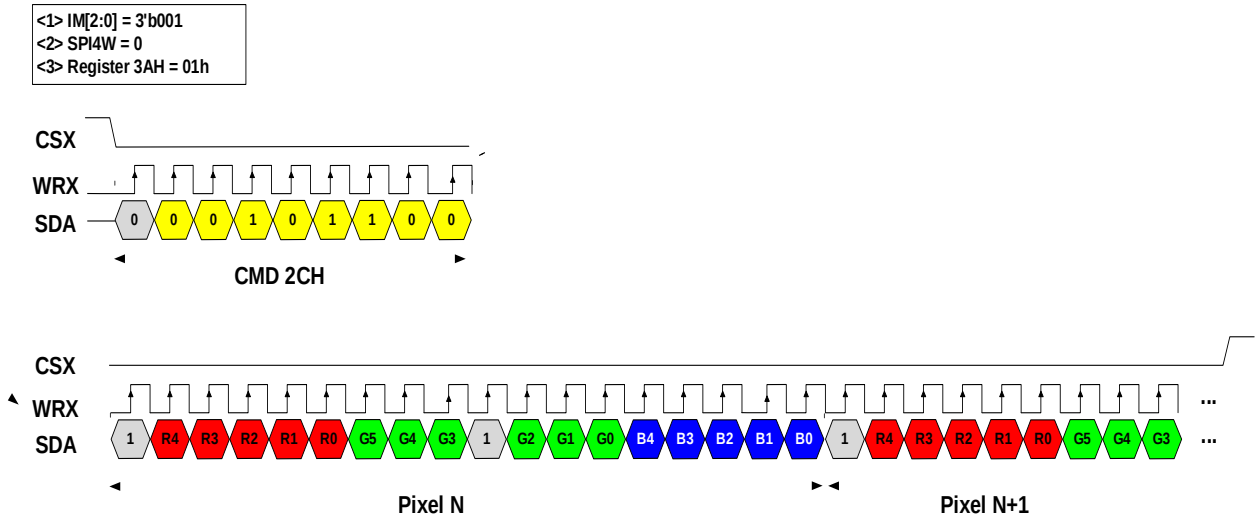
6.3.4.3. Read Cycle Sequence (op code = “03H”)

The function of command reading is also driven by CSX, WRX, SDA, as shown below. op code “03H” is sent after CSX falling edge. AD[23:0] format is {8’h00,CMD[7:0],8’h00}. SDA direction is switched to output driven by NV3041A, when WRX falling edge of last cycle of AD is arrived. As shown below.

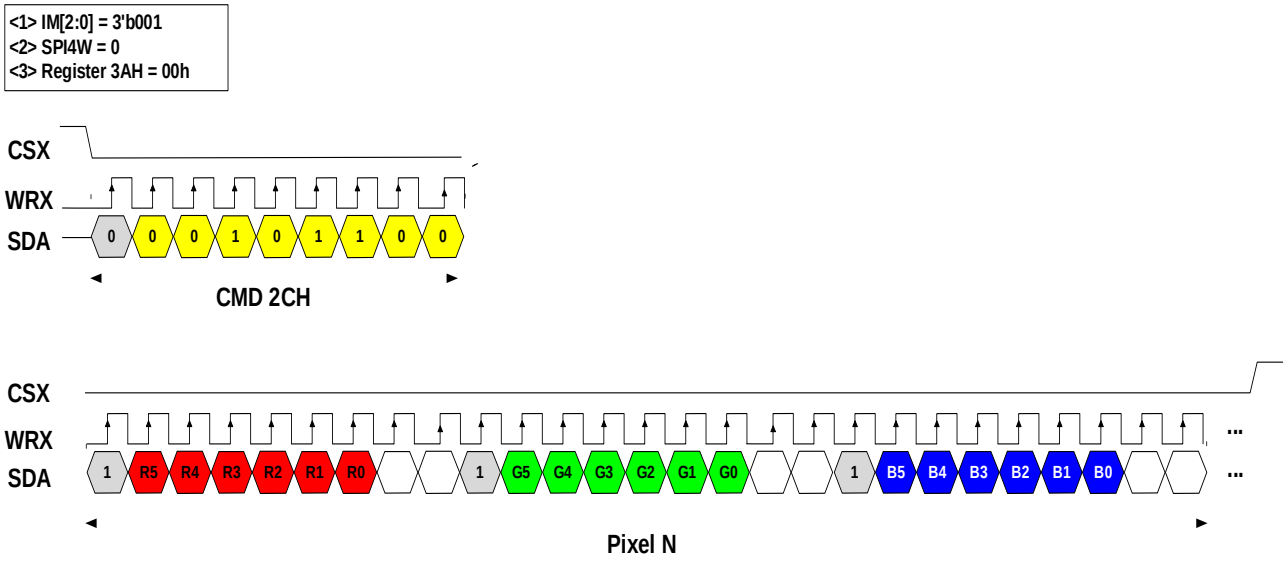


6.4. Display Date Writing Format

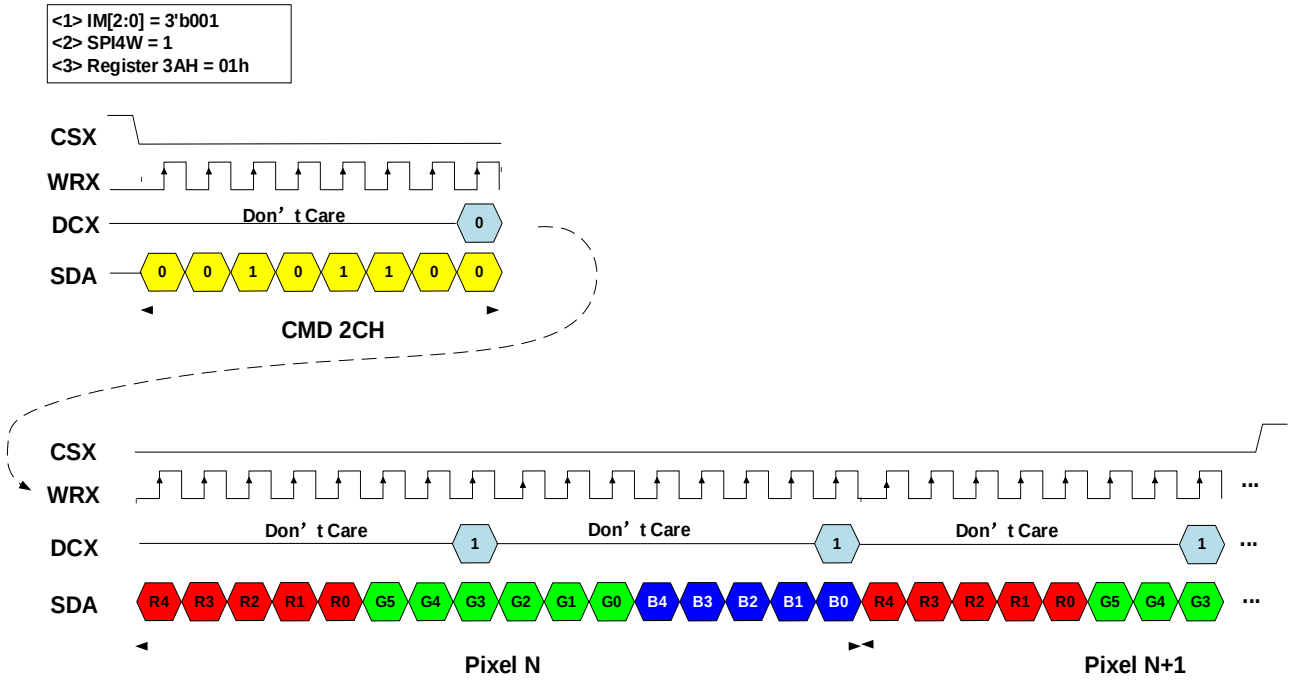
6.4.1. Std SPI 3Wire RGB Format (5-6-5)



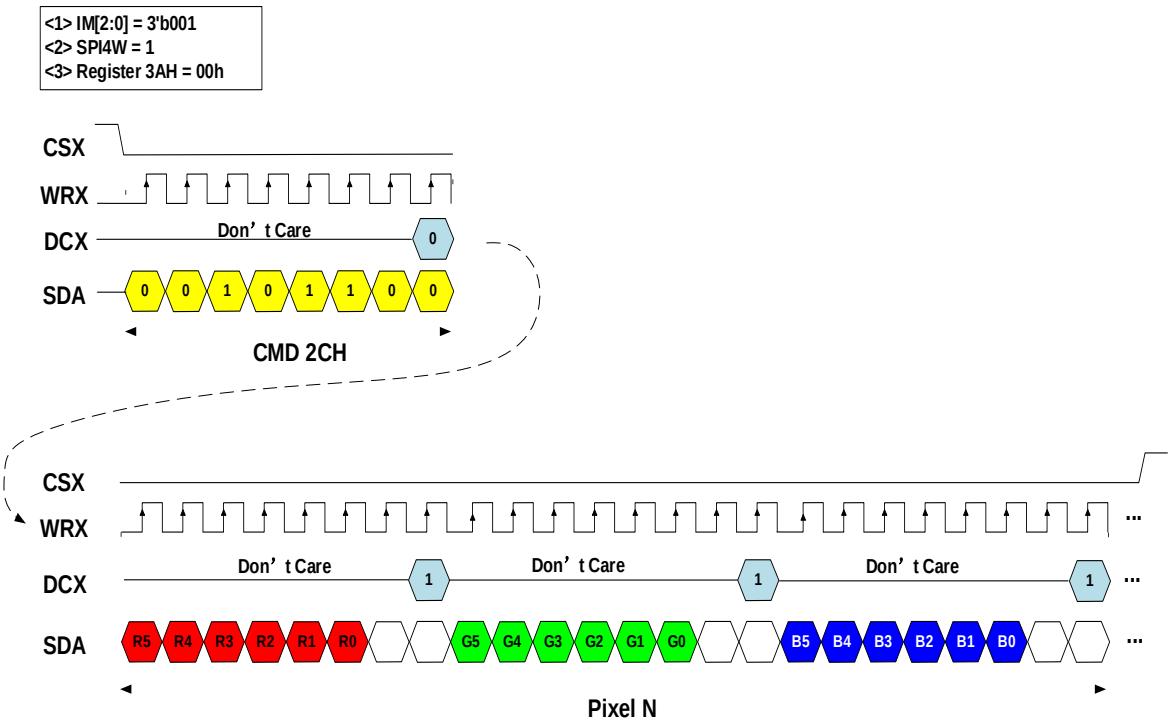
6.4.2. Standard SPI 3Wire RGB Format (6-6-6)



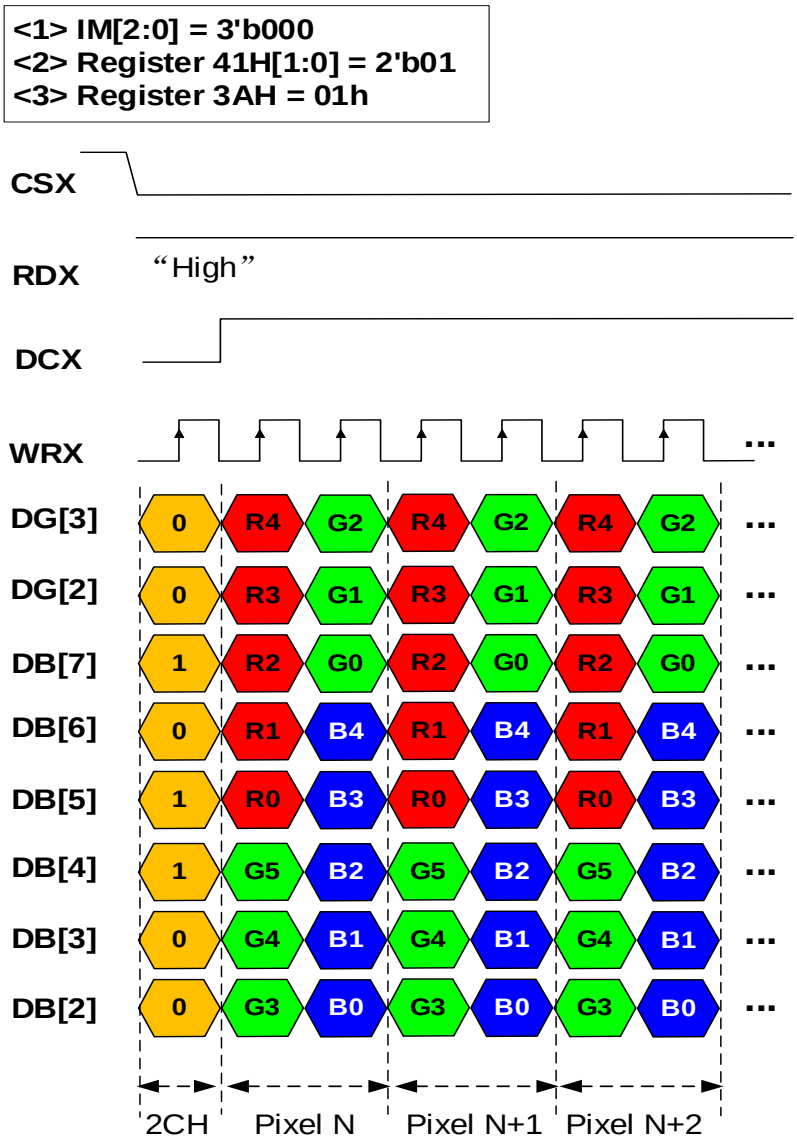
6.4.3. Standard SPI 4Wire RGB Format (5-6-5)



6.4.4. Standard SPI 4Wire RGB Format (6-6-6)

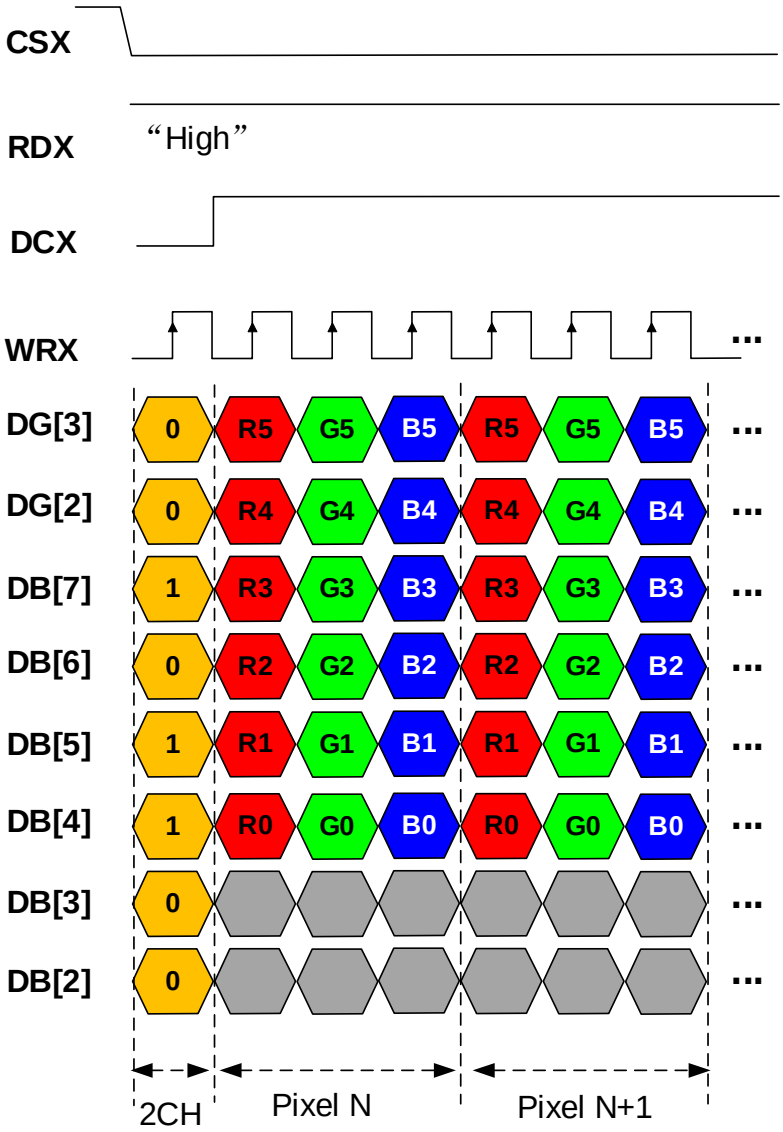


6.4.5. MCU 8 Bit RGB Format (5-6-5)



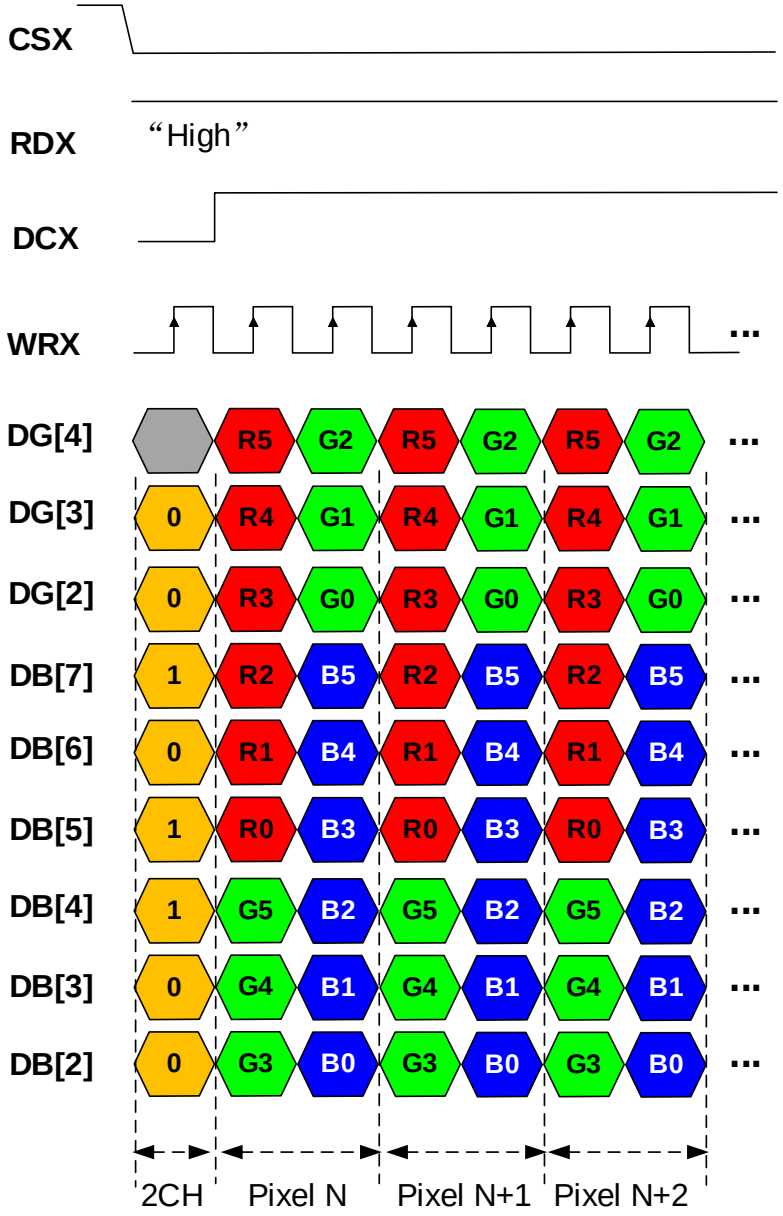
6.4.6. MCU 8 Bit RGB Format (6-6-6)

<1> IM[2:0] = 3'b000
<2> Register 41H[1:0] = 2'b01
<3> Register 3AH = 00h



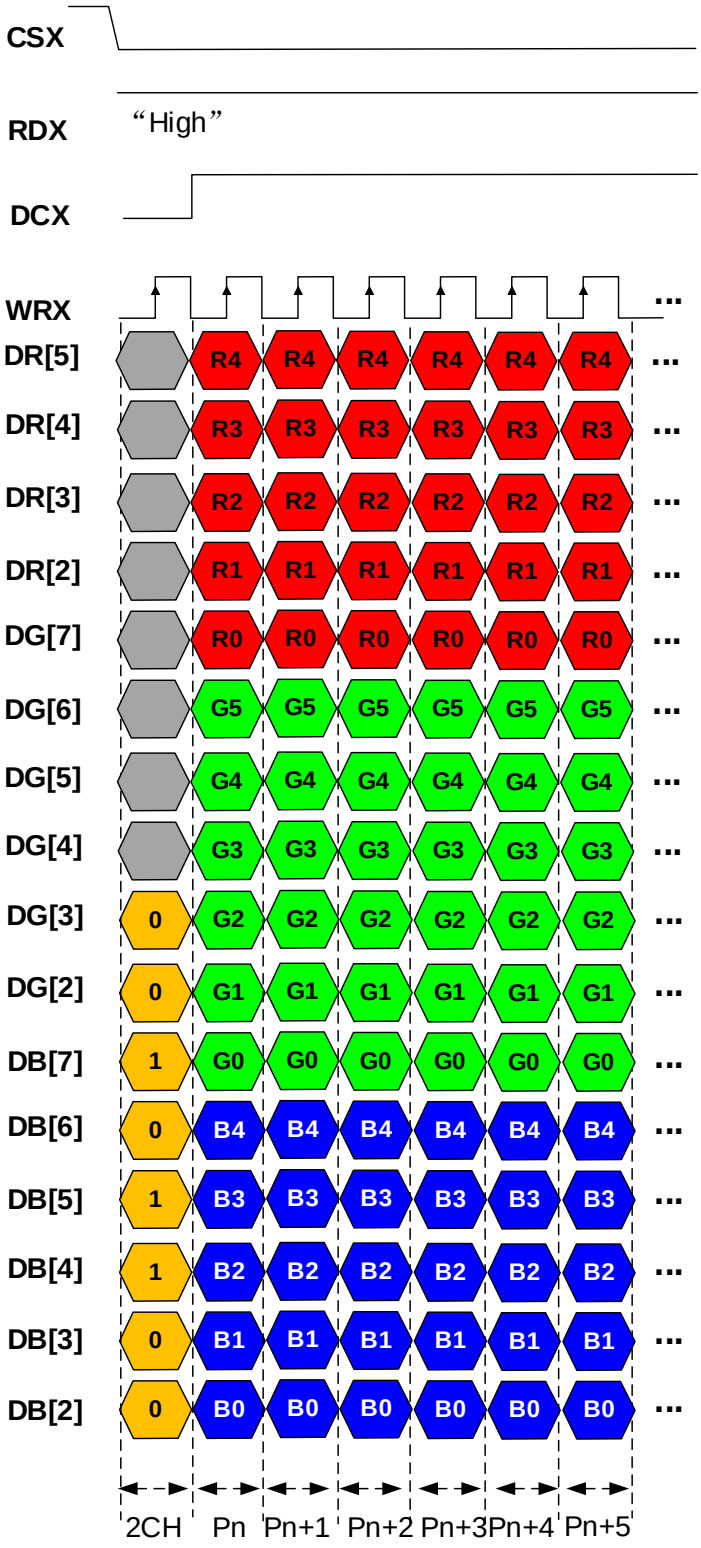
6.4.7. MCU 9 Bit RGB Format (6-6-6)

<1> IM[2:0] = 3'b000
<2> Register 41H[1:0] = 2'b10
<3> Register 3AH = 00h



6.4.8. MCU 16 Bit RGB Format (5-6-5)

<1> IM[2:0] = 3'b000
<2> Register 41H[1:0] = 2'b11
<3> Register 3AH = 01h



6.4.9. MCU 16 Bit RGB Format (6-6-6)

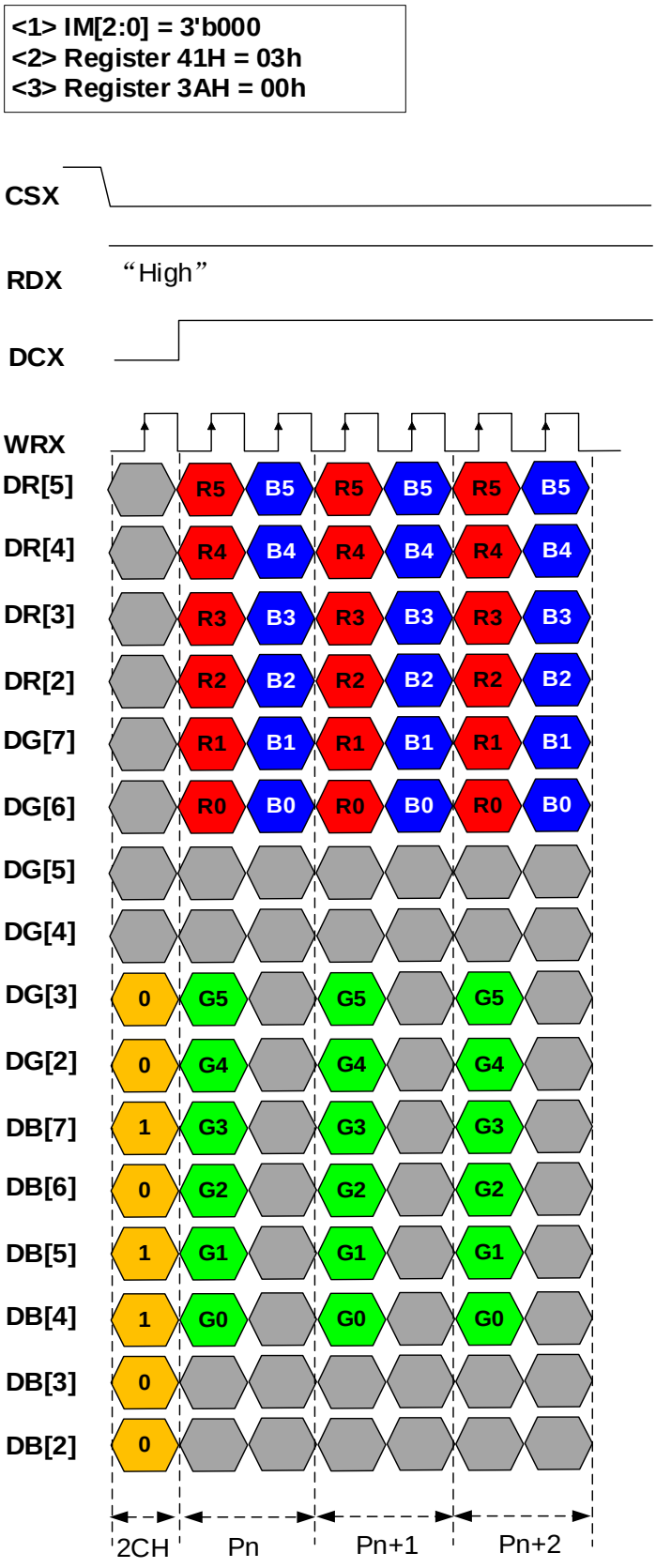


Figure 6.4.9.1

<1> IM[2:0] = 3'b000
<2> Register 41H = 13h
<3> Register 3AH = 00h

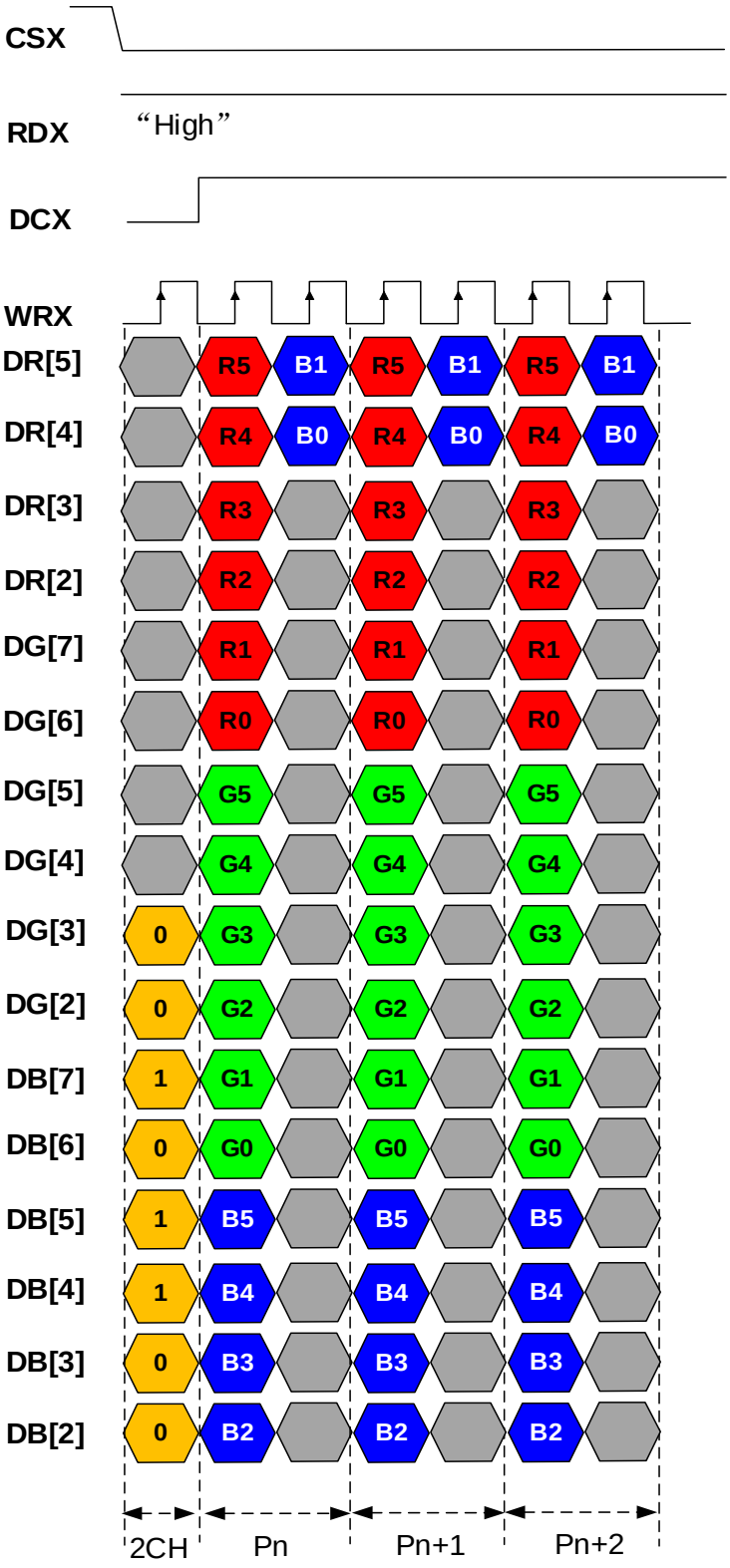


Figure 6.4.9.2

<1> IM[2:0] = 3'b000
<2> Register 41H = 23h
<3> Register 3AH = 00h

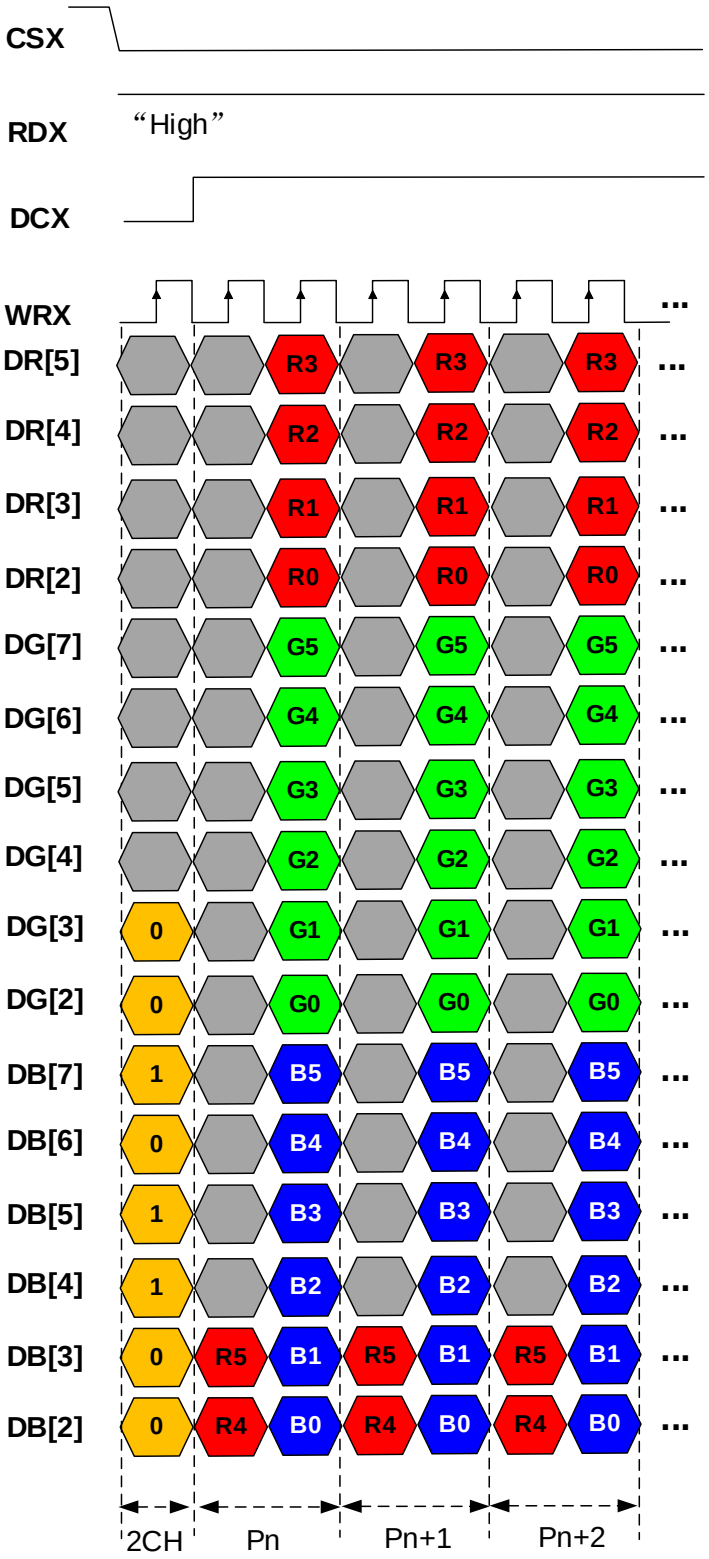


Figure 6.4.9.3

<1> IM[2:0] = 3'b000
<2> Register 41H = 33h
<3> Register 3AH = 00h

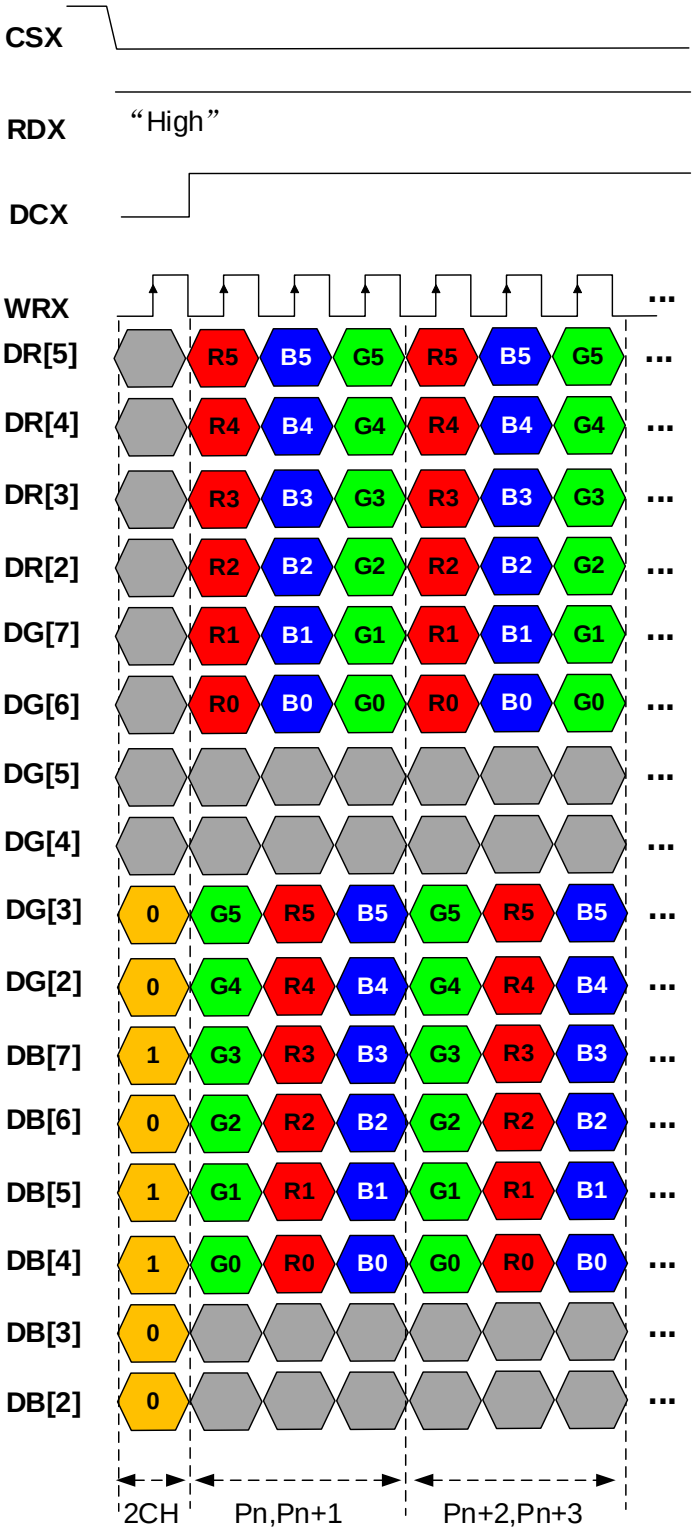
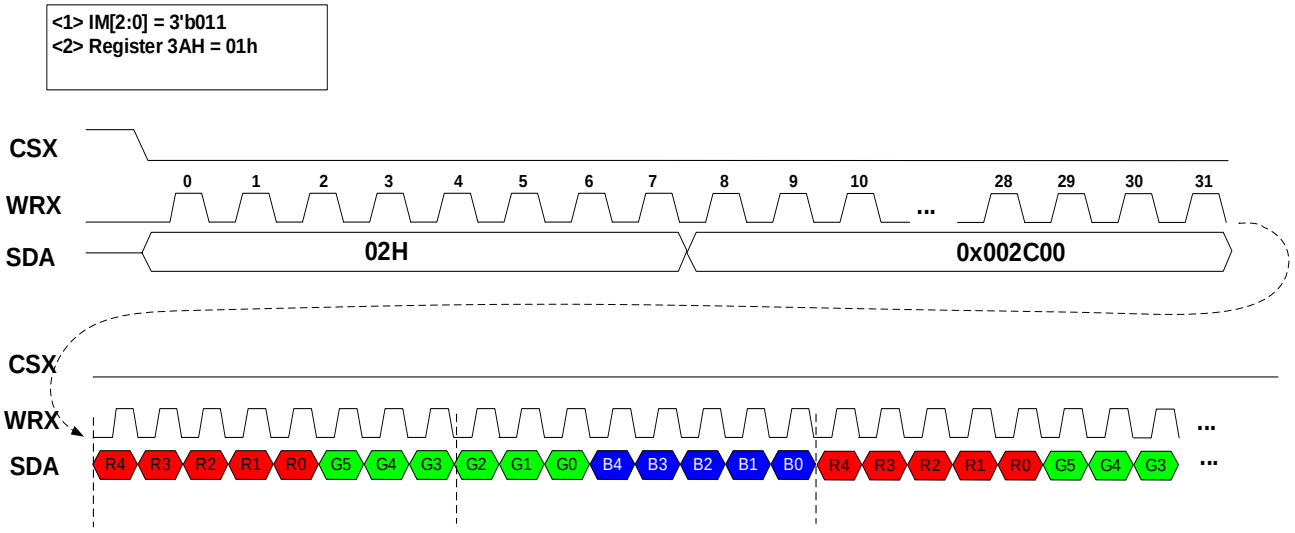
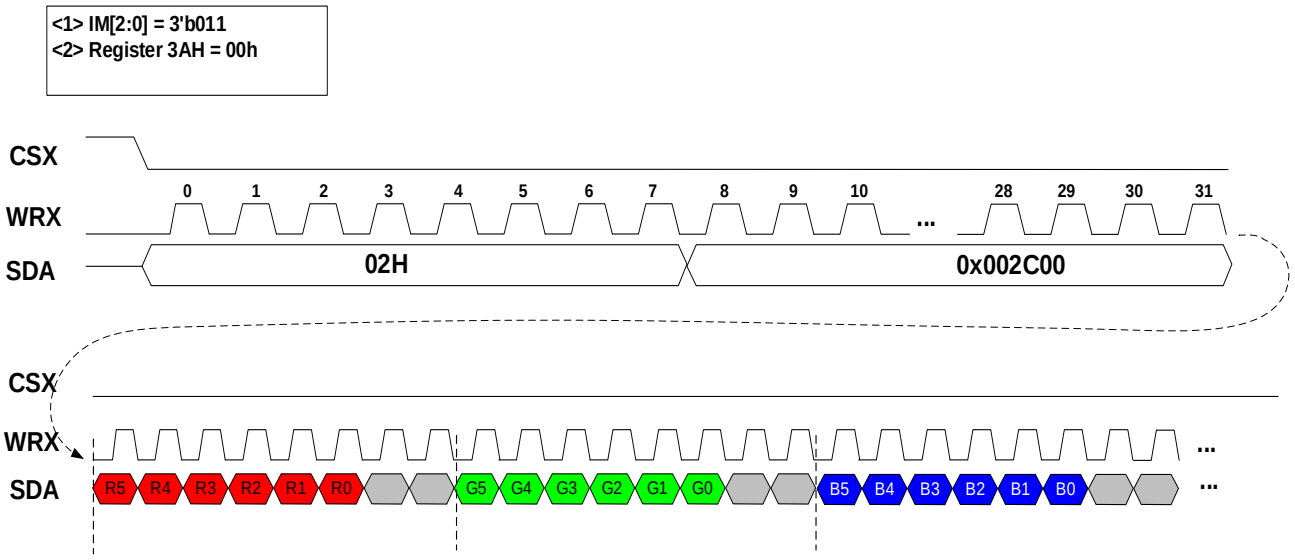


Figure 6.4.9.4

6.4.10. QSPI 1 lane RGB Format (5-6-5)



6.4.11. QSPI 1 lane RGB format(6-6-6)



6.4.12. QSPI 4 lane RGB format(5-6-5)

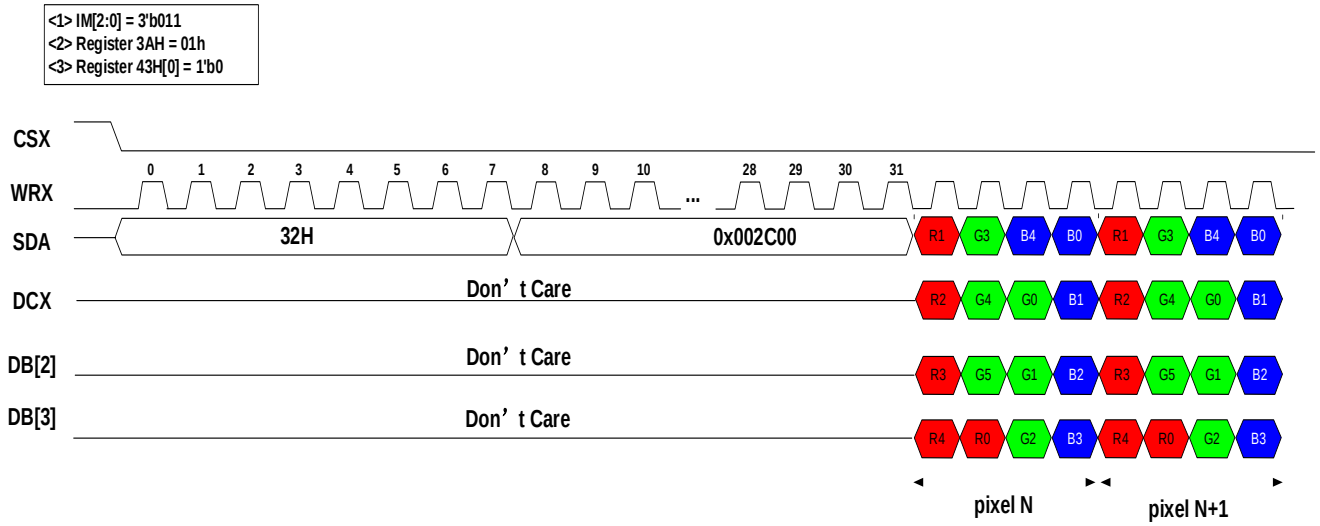


Figure 6.4.12.1

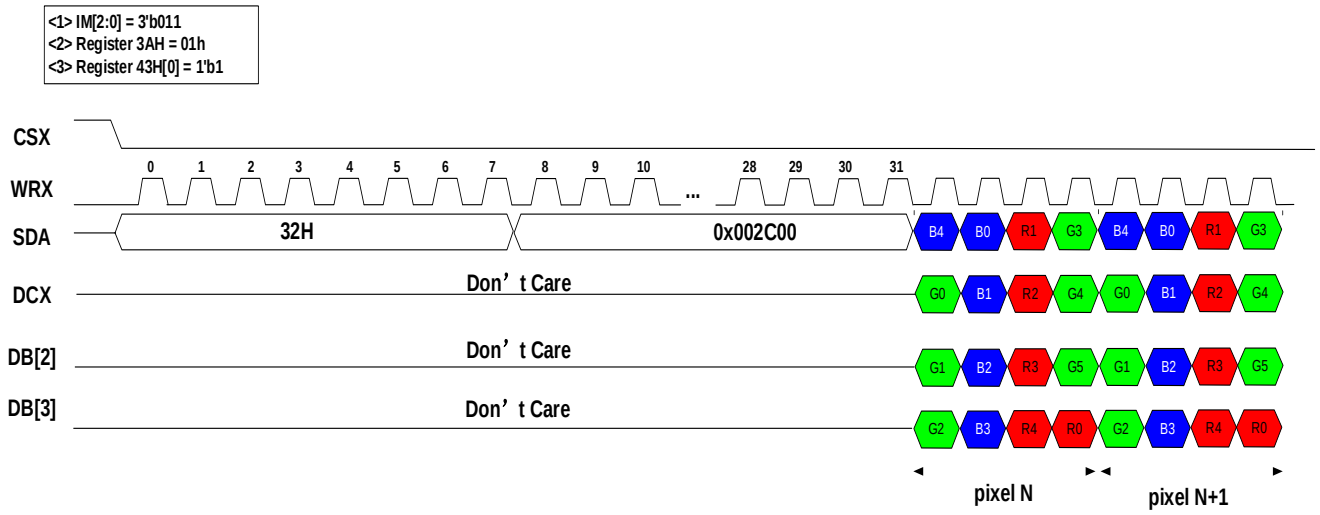


Figure 6.4.12.2

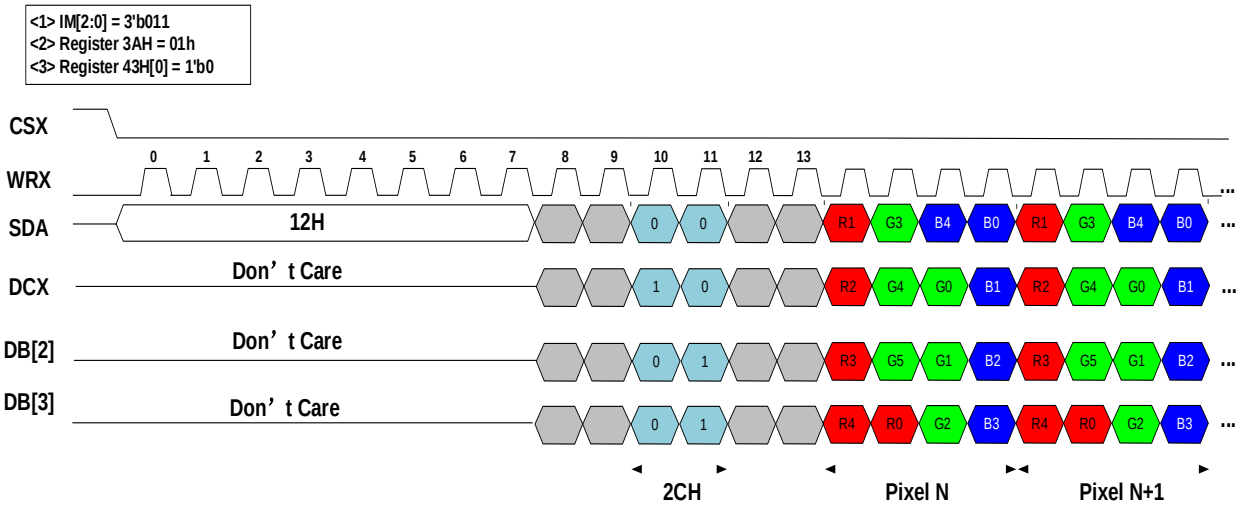


Figure 6.4.12.3

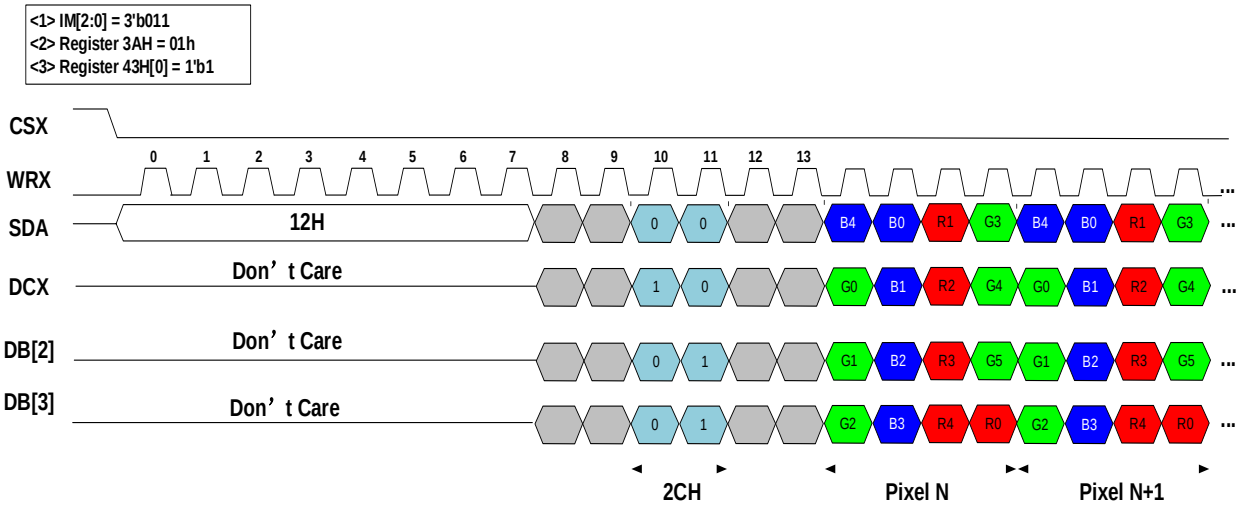


Figure 6.4.12.4

6.4.13. QSPI 4 lane RGB format(6-6-6)

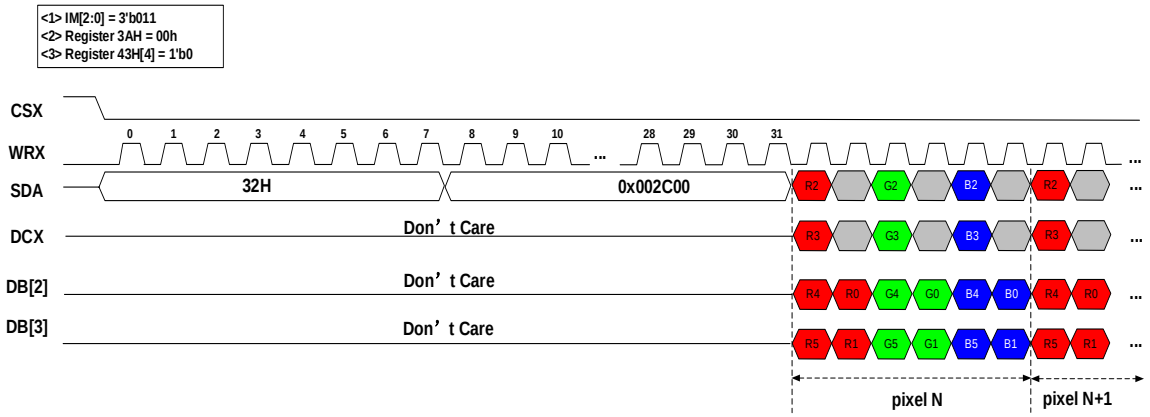


Figure 6.4.13.1

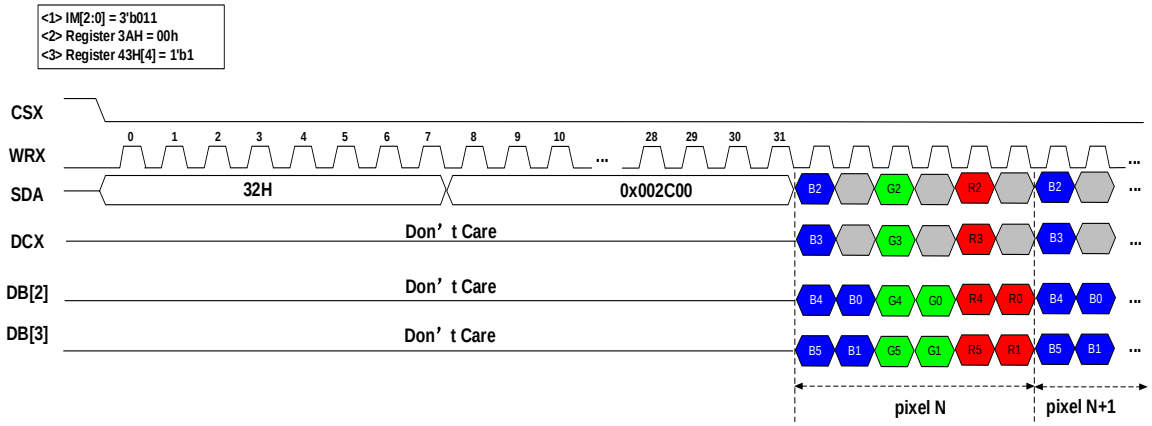


Figure 6.4.13.2

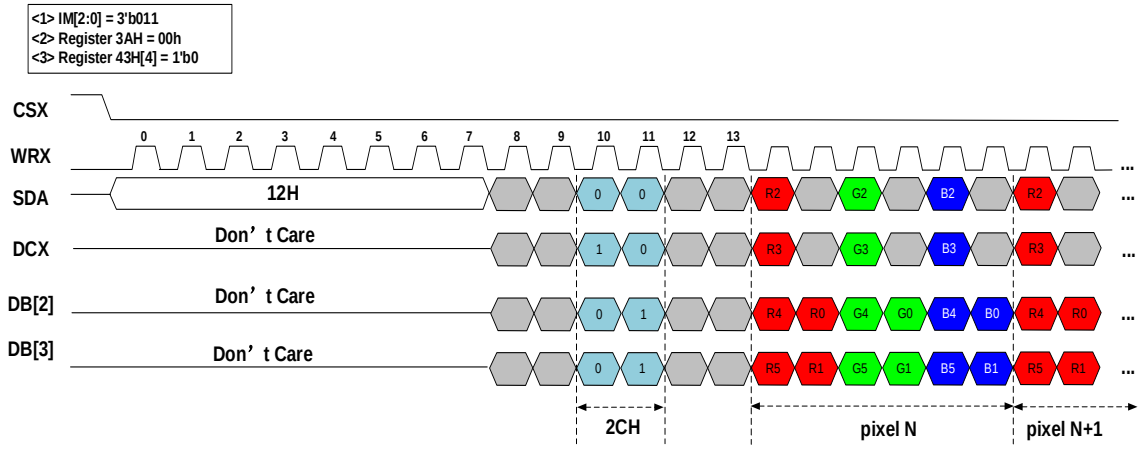


Figure 6.4.13.3

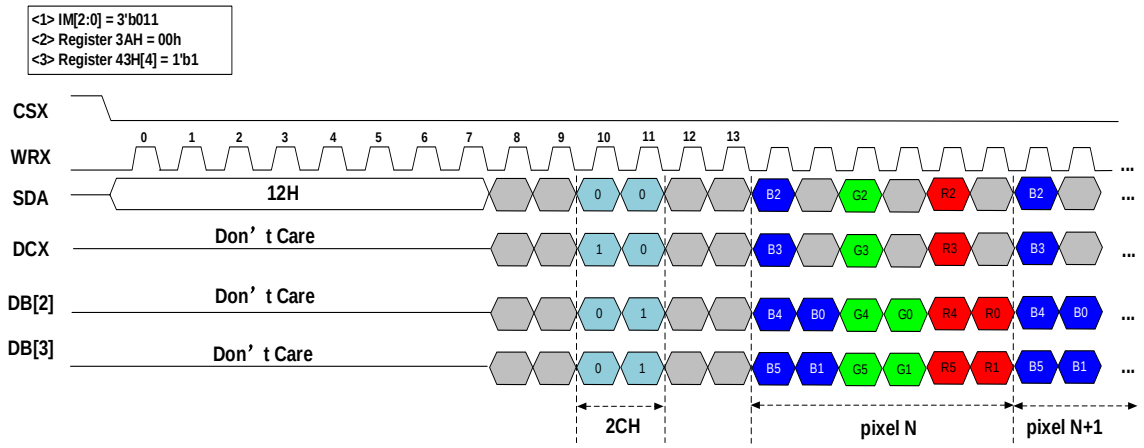
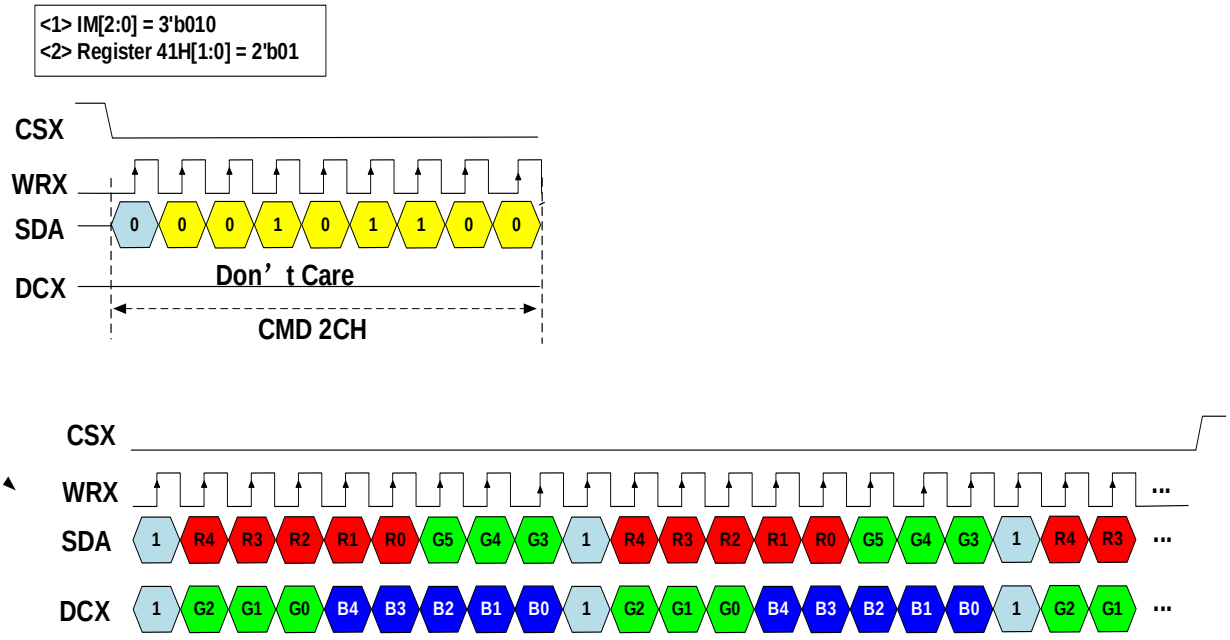


Figure 6.4.13.4

6.4.14. Dual SPI RGB format(5-6-5)



6.4.15. Dual SPI RGB format(6-6-6)

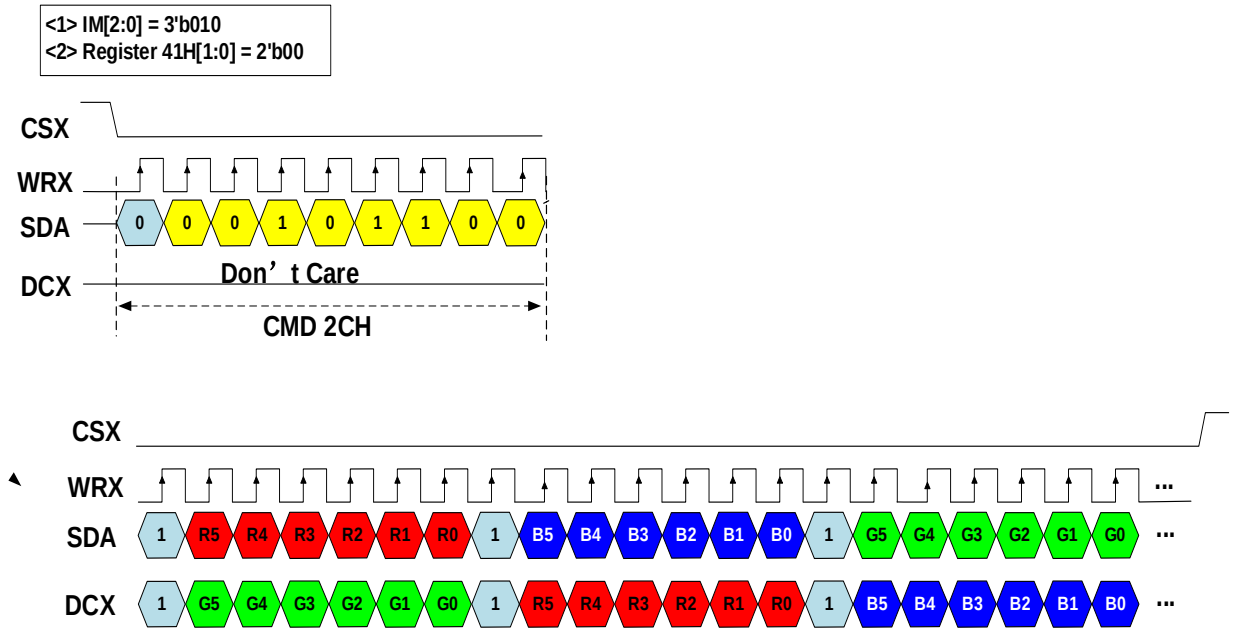


Figure 6.4.15.1

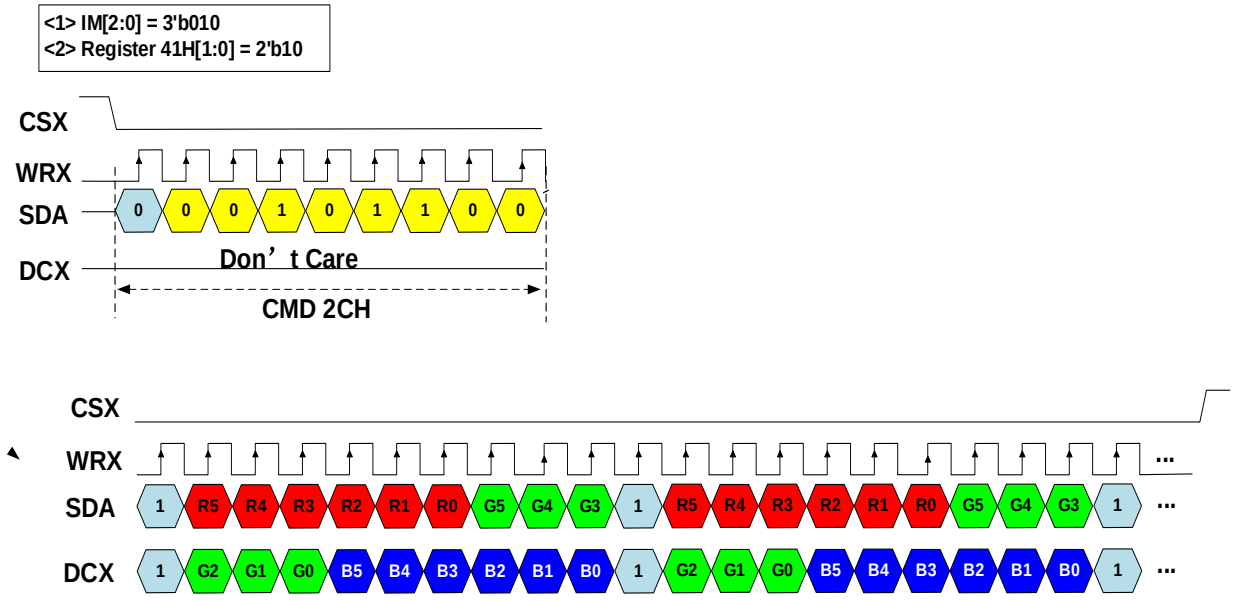


Figure 6.4.15.2

6.5. RGB Interface

6.5.1. RGB Interface

NV3041A supplies 6-bit, 18-bit RGB interfaces for communication between MCU and NV3041A. In this case, user can send command and parameter through Std-SPI interface.

The video stream is synchronized with the VSYNC, HSYNC, and DCLK signals. The display data can be captured by NV3041A only within the active area which indicated by DE signal (de mode) or configurable area (sync mode).

The pad definition is shown below:

Pad Name	Description
DR[7:2]	Data signal
DG[7:2]	
DB[7:2]	
HSYNC	Horizontal synchronizing signal
VSYNC	Vertical-sync signal
DE	Valid data selection communication signal
DCLK	Pixel synchronizing clock

Table 6-5-1-1

The selection of interface is done by IM<2:0> bits. Please refer to below Table 6-5-1-2

IM2	IM1	IM0	PARA_SERI	BUS Selection
1	0	0	0	6-bit input, Register E1[1:0] = 2'b00 DG[7:2], Register E1[1:0] = 2'b01 DR[7:2] Register E1[1:0] = 2'b10 DB[7:2]
			1	18bit input , DR[7:2],DG[7:2],DB[7:2]

Table 6-5-1-2

6.5.2. Parallel 18-bit RGB Timing Table

Item		Min	Typ	Max	Unit
DCLK		——	9	12	MHz
Horizontal Area	Period Time	——	500	——	DCLK
	Display Area	——	480	——	
	HBP	8	10	——	
	HFP	——	10	——	
	HS Width	2	4	——	
Veritcal Area	Period Time	——	292	——	H Period Time
	Display Area	——	272	——	
	HBP	2	10	——	
	HFP	2	10	——	
	VS Width	2	4	——	

Note: It is necessary to keep VBP=10 and HBP =10 in SYNC Mode. DE Mode is unnecessary to keep it.

6.5.3. Serial 6-bit RGB Timing Table

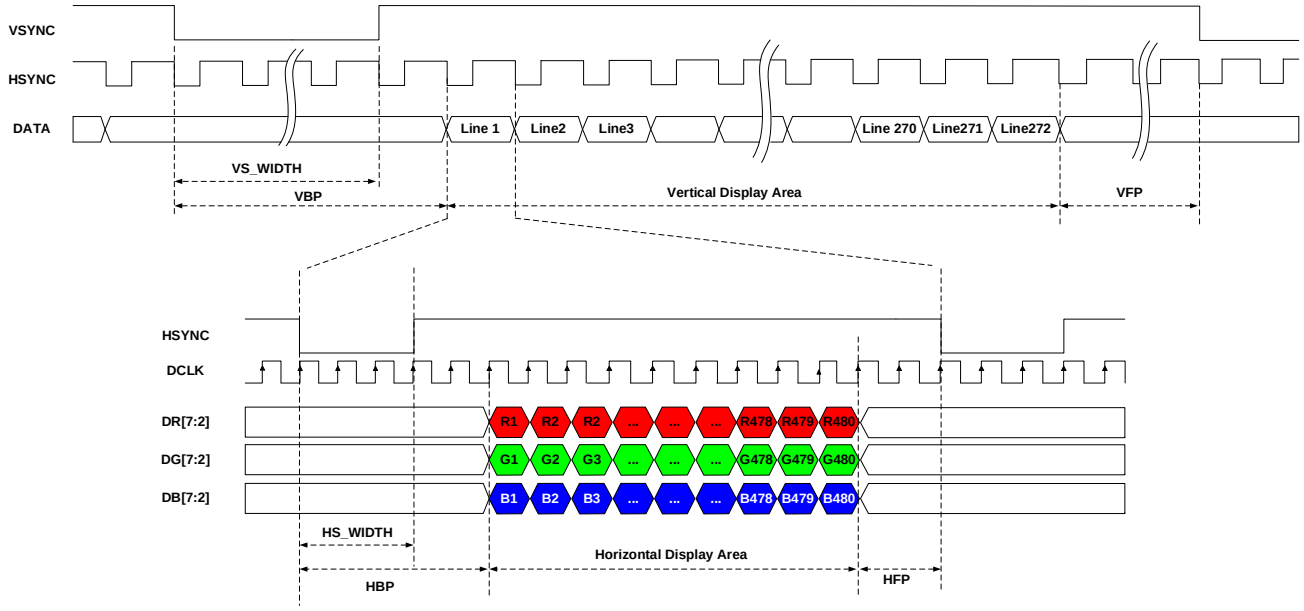
Item		Min	Typ	Max	Unit
DCLK		——	12	30	MHz
Horizontal Area	Period Time	——	1460	——	DCLK
	Display Area	——	1440	——	
	HBP	8	10	——	
	HFP	——	10	——	
	HS Width	2	4	——	
Veritcal Area	Period Time	——	292	——	H Period Time
	Display Area	——	272	——	
	HBP	2	10	——	
	HFP	2	10	——	
	VS Width	2	4	——	

Note: It is necessary to keep VBP=10 and HBP =10 in SYNC Mode. DE Mode is unnecessary to keep it.

6.5.4. SYNC Mode Timing Diagram

When RGB interface don't send DE signal, NV3041A will recognize this condition as SYNC MODE and generate DE signal internally. Pay attention that the porch VBP and HBP must be 10.

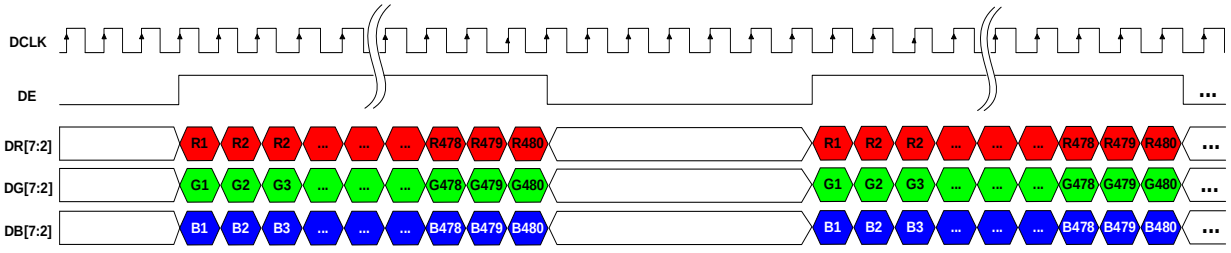
The sequence described in the figure as below



6.5.5. DE Mode Timing Diagram

When no sync signals have been sent, NV3041A will recognize this situation as DE Mode and generate sync signals internally. This mode does not need to consider any v-porch and h-porch settings.

The sequence described in the figure as below



7. Register

7.1. Register Summary

Reg Name	Address	Access	Default	D7	D6	D5	D4	D3	D2	D1	D0
NOP	00	W	00								
RD_SYSID	04	Multi-R	30	sys_id1[7:0]							
			41	sys_id2[7:0]							
			A1	sys_id3[7:0]							
RD_STATE	09	Multi-R		boost_on	my	mx	mv	ml	bgr		
							pxl_fmt	idle_en	partial_en	slpout	normal_on
				scroll_en		inv_en			dispon	te_en	
						te_sel					
RD_DISP	0A	R		boost_on	idle_en	partial_en	slpout	normal_on	dispon		
RD_MADCTL	0B	R		my	mx	mv	ml	bgr			
RD_IM	0D	R		scroll_en		inv_en					
RD_SM	0E	R		te_en	te_sel						
SLPIN	10	W	00								
SLPOUT	11	W	00								
PTLON	12	W									
NORMAL	13	W									
WR_SYSID	14	Multi-W	30	sys_id1[7:0]							
			41	sys_id2[7:0]							
			A1	sys_id3[7:0]							
INVOFF	20	W									
INVON	21	W									
DISPOFF	28	W									
DISPON	29	W									
COL_ADR	2A	Multi-W	00								col_st[8]
			00	col_st[7:0]							
			01								col_ed[8]
			df	col_ed[7:0]							
ROW_ADR	2B	Multi-W	00								row_st[8]
			00	row_st[7:0]							
			01								row_ed[8]
			0f	row_ed[7:0]							
PTL_ADR	30	Multi-W	00								ptl_st[8]
			00	ptl_st[7:0]							
			01								ptl_ed[8]
			0f	ptl_ed[7:0]							
SCROLL_ADR	33	Multi-W	00								tfa[8]
			00	tfa[7:0]							
			00								vsa[8]
			00	vsa[7:0]							
TEOFF	34	W	00								
TEON	35	W	00								te_sel
MACTL	36	W	00	my	mx	mv	ml	bgr			
VSCSAD	37	Multi-W	00								ssa[8]
			00	ssa[7:0]							
IDMOFF	38	W									
IDMON	39	W									
COLMOD	3A	W	01								pxl_fmt

Reg Name	Address	Access	Default	D7	D6	D5	D4	D3	D2	D1	D0
MACTL_USR	40	W	00	usr_my	usr_mx	usr_mv	usr_ml	usr_bgr			usr_rev
BUS_WD	41	W	00			bus16_type[1:0]				bus_width[1:0]	
QSPI_DCTL	43	W	00				qspi_bgr			qspi_dummy	qspi_sbyte
FSM_VBP	44	W	05			fsm_vbp[5:0]					
FSM_VFP	45	W	05			fsm_vfp[5:0]					
FSM_HBP_ODD	46	W	0a			fsm_hbp_o[5:0]					
FSM_HFP_ODD	47	W	0a			fsm_hfp_o[5:0]					
FSM_HBP_EVEN	48	W	1a			fsm_hbp_e[5:0]					
FSM_HFP_EVEN	49	W	1a			fsm_hfp_e[5:0]					
SCAN_VRES	4A	Multi-W	01								v_res[8]
			0F	v_res[7:0]							
SCAN_HRES	4B	Multi-W	01								h_res[8]
			DF	h_res[7:0]							
RGB_HBP_ODD	4C	W	1a			rgb_hbp_o[5:0]					
RGB_HFP_ODD	4D	W	1a			rgb_hfp_o[5:0]					
RGB_HBP_EVEN	4E	W	0a			rgb_hbp_e[5:0]					
RGB_HFP_EVEN	4F	W	0a			rgb_hfp_e[5:0]					
GATE_SCAN	50	W	03							gate_scan_seq[1:0]	
GATE_ST_O	51	W	0a	gate_st_o[7:0]							
GATE_ED_O	52	W	64	gate_ed_o[7:0]							
GATE_ST_E	53	W	0a	gate_st_e[7:0]							
GATE_ED_E	54	W	64	gate_ed_e[7:0]							
PANEL_CTRL	55	W	10				src_ss				gate_gs
SRC_LOAD	56	W	43	src_ld_wd[1:0]		src_ld_st[5:0]					
SRC_CS_ST	57	W	42		pn_cs_en	src_cs_st[5:0]					
SRC_CS_PW	58	W	3C		src_cs_p_wd[6:0]						
SRC_CS_NW	59	W	64		src_cs_n_wd[6:0]						
SRC_PC_ST_O	5A	W	67		src_pchg_st_o[6:0]						
SRC_PC_WD_O	5B	W	3C		src_pchg_wd_o[6:0]						
SRC_PC_ST_E	5C	W	02		src_pchg_st_e[6:0]						
SRC_PC_WD_E	5D	W	3C		src_pchg_wd_e[6:0]						
SRC_POL_SW	5E	W	1F	src_pol_sw[7:0]							
SRC_OP_ST_O	60	W	A4	src_op_st_o[7:0]							
SRC_OP_ST_E	61	W	3F	src_op_st_e[7:0]							
SRC_OP_ED_MSB	62	W	11			src_op_ed_o[9:8]				src_op_ed_e[9:8]	
SRC_OP_ED_O_LSB	63	W	E0	src_op_ed_o[7:0]							
SRC_OP_ED_E_LSB	64	W	E0	src_op_ed_e[7:0]							
SRC_OFC	65	W	01				gma_chop_en		src_ofc_sel[2:0]		
CLR_SCR	66	W	00			pwr_on_clr_sel[1:0]				pwr_off_clr_sel[1:0]	
SRC_IBIAS	67	W	33		src_ibp[2:0]				src_ibn[2:0]		
PTL_DAT	68	W	00								ptl_dat_sel
LVD_SET	6E	W	04				lvd_en		lvd_adj[2:0]		
USR_GVDD	6F	W	16		usr_gvdd[6:0]						

Reg Name	Address	Access	Default	D7	D6	D5	D4	D3	D2	D1	D0
USR_GVCL	78	W	47	usr_gvcl[6:0]							
USR_VGSP	7A	W	3f	usr_vgsp[6:0]							
GVREF2V	7C	W	07					gvref2v[3:0]			
VDDS_TRIM	7D	W	00						vdds_trim[2:0]		
GAM_VRP0	80	W	00	gam_vrp0[5:0]							
GAM_VRP1	81	W	00	gam_vrp1[5:0]							
GAM_VRP2	82	W	00	gam_vrp2[5:0]							
GAM_VRP3	83	W	00	gam_vrp3[5:0]							
GAM_VRP4	84	W	00	gam_vrp4[5:0]							
GAM_VRP5	85	W	00	gam_vrp5[5:0]							
GAM_PRP0	86	W	00	gam_prp0[6:0]							
GAM_PRP1	87	W	00	gam_prp1[6:0]							
GAM_PKP0	88	W	00	gam_pkp0[4:0]							
GAM_PKP1	89	W	00	gam_pkp1[4:0]							
GAM_PKP2	8A	W	00	gam_pkp2[4:0]							
GAM_PKP3	8B	W	00	gam_pkp3[4:0]							
GAM_PKP4	8C	W	00	gam_pkp4[4:0]							
GAM_PKP5	8D	W	00	gam_pkp5[4:0]							
GAM_PKP6	8E	W	00	gam_pkp6[4:0]							
GAM_PKP7	8F	W	00	gam_pkp7[4:0]							
GAM_PKP8	90	W	00	gam_pkp8[4:0]							
GAM_PKP9	91	W	00	gam_pkp9[4:0]							
GAM_PKP10	92	W	00	gam_pkp10[4:0]							
GAM_VRN0	A0	W	00	gam_vrn0[5:0]							
GAM_VRN1	A1	W	00	gam_vrn1[5:0]							
GAM_VRN2	A2	W	00	gam_vrn2[5:0]							
GAM_VRN3	A3	W	00	gam_vrn3[5:0]							
GAM_VRN4	A4	W	00	gam_vrn4[5:0]							
GAM_VRN5	A5	W	00	gam_vrn5[5:0]							
GAM_PRN0	A6	W	00	gam_prn0[6:0]							
GAM_PRN1	A7	W	00	gam_prn1[6:0]							
GAM_PKN0	A8	W	00	gam_pkn0[4:0]							
GAM_PKN1	A9	W	00	gam_pkn1[4:0]							
GAM_PKN2	AA	W	00	gam_pkn2[4:0]							
GAM_PKN3	AB	W	00	gam_pkn3[4:0]							
GAM_PKN4	AC	W	00	gam_pkn4[4:0]							
GAM_PKN5	AD	W	00	gam_pkn5[4:0]							
GAM_PKN6	AE	W	00	gam_pkn6[4:0]							
GAM_PKN7	AF	W	00	gam_pkn7[4:0]							
GAM_PKN8	B0	W	00	gam_pkn8[4:0]							
GAM_PKN9	B1	W	00	gam_pkn9[4:0]							
GAM_PKN10	B2	W	00	gam_pkn10[4:0]							
BIAS_VBG	C0	W	00	bias_adj[2:0]				vbg_adj[3:0]			
MV_CLP	C1	W	aa	avdd_clp_en	avdd_clp[1:0]			avcl_clp_en		avcl_clp[1:0]	
VGH_CLP	C2	W	15			vgh_clp_en			vgh_clp[2:0]		
VGL_CLP	C3	W	12			vgl_clp_en			vgl_clp[2:0]		
MV_TD	C4	W	22		vgh_skip	vgh_td[1:0]			vgl_skip	vgl_td[1:0]	
MV_SS_CTRL	C5	W	11			avdd_ss_en					avcl_ss_en
RATIO_CTRL	C6	W	35			avdd_ratio_sel	avcl_ratio_sel	vgh_ratio_sel[1:0]		vgl_ratio_sel[1:0]	
MV_PUMP_CLK	C7	W	2a			mv_clk_sel[1:0]		avdd_clk_sel[1:0]		avcl_clk_sel[1:0]	
HV_PUMP_CLK	C8	W	11			vgh_clk_sel[1:0]				vgl_clk_sel[1:0]	
MV_CLK_CLP	C9	W	37			avdd_fdb	avcl_fdbk_		vgh_freq_e	avdd_freq	avcl_freq

Reg Name	Address	Access	Default	D7	D6	D5	D4	D3	D2	D1	D0
						k_en	en		n	_en	_en
RD_SYSID1	DA	R		sys_id1[7:0]							
RD_SYSID2	DB	R		sys_id2[7:0]							
RD_SYSID3	DC	R		sys_id3[7:0]							
RGB_CTL	E1	W	80	auto_detect		sync_ctrl[1:0]				seri_db_sel[1:0]	
RGB_POL	E2	W	18				pol_auto	rgb_pclk_pol	rgb_vpol	rgb_hpol	rgb_depol
INTF_VBP	E3	W	0a	intf_vbp[7:0]							
INTF_HBP	E4	W	0a	intf_hbp[7:0]							
DVDD_TRIM	E5	W	00						dvdd_trim[2:0]		
ESD_CTRL	E6	W	70		esd_detect_en	esd_otp_en	esd_sfr_en			esd_level_sel[1:0]	
TE_CTRL	E7	W	00				te_out_oe				te_inv
OTP_CTRL1	F1	W	00	otp_pa[7:0]							
OTP_CTRL2	F2	W	00	otp_pdin[7:0]							
OTP_CTRL3	F3	W	00	otp_ptm[1:0]			otp_vpp_sel	otp_pprog		otp_pwe	otp_prd
OTP_CRCH	F4	R		otp_crc[15:8]							
OTP_CRCL	F5	R		otp_crc[7:0]							
OTP_RDD	F6	R		otp_rd_dat[7:0]							

Note: When GRB is low, all registers reset to default values.

7.2. SYSTEM COMMAND DESCRIPTION

7.2.1. NOP (00h)

Command Set		NOP								
Address	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
00h	Write	No Parameter								00h
Description	This command is an empty command. It does not have any effect on the NV3041A.									
Restriction	-									

7.2.2. RD_SYSID (04h)

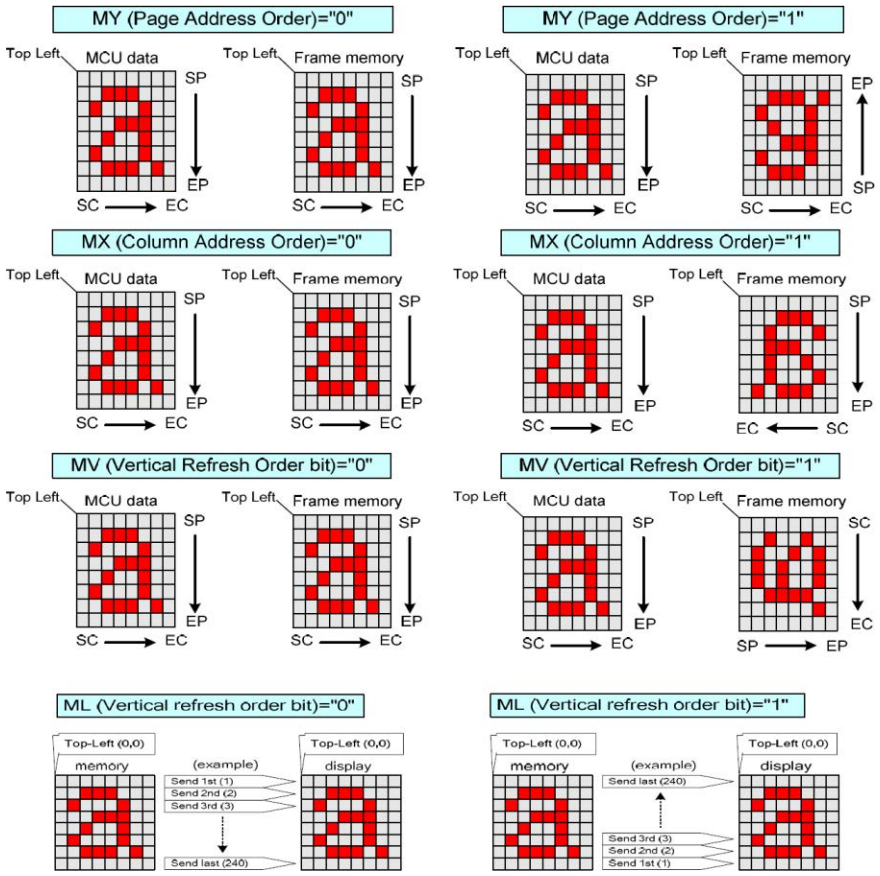
Command Set		RD_SYSID								
Address	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
04h	Multi-R	sys_id1[7:0]								30h
		sys_id2[7:0]								41h
		sys_id3[7:0]								A1h
Description	The read parameters are used to recognize the LCD driver version. It is defined by the display supplier (with User's agreement).									
Restriction	-									

7.2.3. RD_STATE (09h)

Command Set		RD_STATE								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R		my	mx	mv	ml	bgr			
2st Parameter					pxl_fmt	idle_en	partial_en	slpout	normal_on	
3st Parameter		scroll_en		inv_en			dispon	te_en		
4st Parameter				te_sel						

Description

Bit	Name	Value
my	Row Address Order(MY)	“1”=Decrement. (Bottom to Top), when MADCTL (36h) D7=“1”
		“0”=Increment.(Bottom to Top),when MADCTL (36h) D7=“0”
mx	Column Adress Order(MX)	“1”=Decrement.(Right to Left),when MADCTL(36h)D6=“1”
		“0”=Increment.(Left to Right),when MADCTL(36h)D6=“0”
mv	Row/Column Exchange(MV)	“1”=Row/column exchange. when MADCTL (36h) D5=“1”
		“0”=Normal(MV=0).when MADCTL (36h) D5=“0”
ml	Vertical refresh Order(ML)	“1”=Decrement.(LCD refresh Bottom to Top, when MADCTL (36h) D4=“1”
		“0”=Increment.(LCD refresh Top to Bottom), when MADCTL(36h)D4=“0”
bgr	RGB/BGR Order(RGB)	“1”=BGR.when MADCTL(36h)D3=“1”
		“0”=RGB.when MADCTL(36h)D3=“0”
pxl_fmt	Color depth	“1” = 5-6-5, “0” = 6-6-6.
Idle_en	Ldle Mode On/Off	“1”=On,”0”=Off
partial_en	Partial Mode On/Off	“1”=On,”0”=Off
slpout	Sleep In/Out	“1”=On,”0”=Off
normal_on	Display Normal Mode On/Off	“1”=Normal Display,”0”=Normal Display Off
scroll_en	Vertical Scrolling Status	“1”=Scroll On,”0”=Scroll Off
inv_en	Inversion Status	“1”=On,”0”=Off
dispon	Display On/Off	“1”=On,”0”=Off
te_en	Tearing effect line on/off	“1”=On,”0”=Off
te_sel		

	
Restriction	-

7.2.4. RD_DISP (0Ah)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">RD_DISP</th></tr>
<tr><th>Address</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>0Ah</td><td>Read</td><td></td><td>idle_en</td><td>partial_en</td><td>slpout</td><td>normal_on</td><td>dispon</td><td></td><td></td><td></td></tr>
<tr><td>Description</td><td colspan="10"><table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>IDLE_ON</td><td>Idle mode On/Off</td><td>“1”=Idle mode On
“0”=Idle mode Off</td></tr>
<tr><td>PTL_ON</td><td>Partial Mode On/Off</td><td>“1”=Partial Mode On
“0”=Partial Mode Off</td></tr>
<tr><td>SLPOUT</td><td>Sleep In/Off</td><td>“1”=Sleep Out
“0”=Sleep In</td></tr>
<tr><td>NORMAL_ON</td><td>Display Normal Mode On/Off</td><td>“1”=Normal Display
“0”=Partial Display</td></tr>
<tr><td>DISPON</td><td>Display On/Off</td><td>“1”=Display On
“0”=Display Off</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.2.5. RD_MADCTL (0Bh)

Command Set		RD_MADCTL								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Read	my	mx	mv	ml	bgr				

Description

Bit	Description	Value
MY	Page Address Order	“1”=Decrement,”0”=Increment
MX	Column Adress Order	“1”=Decrement,”0”=Increment
MV	Page/Column Order	“1”=Row/column exchange (MV=1) “0”=Normal(MV=0)
ML	Line Address Order	“1”=LCD Refresh Botton to top “0”=LCD Refresh top to Botton
BGR	RGB/BGR Order	“1”=BGR, “0”=RGB

Restriction: -

7.2.6. RD_IM (0Dh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">RD_IM</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Read</td><td>scroll_en</td><td></td><td>inv_en</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Description</td><td colspan="10"><table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>D7</td><td>Scrolling On/Off</td><td>“1”=Scrolling is On
“0”=Scrolling is Off</td></tr><tr><td>D5</td><td>Inversion On/Off</td><td>“1”=Inversion is On
“0”=Inversion is Off</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.2.7. RD_SM (0Eh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">RD_SM</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Read</td><td>te_en</td><td>te_sel</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Description</td><td colspan="10"><table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>D7</td><td>Tearing Effect Line On/Off</td><td>“0”=Off, “1”= On</td></tr><tr><td>D6</td><td>Tearing Effect Line Mode</td><td>“0”=Mode1,”1”= Mode2</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.2.8. SLPIN (10h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">SLPIN</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">sleep in</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command causes the LCD module to enter the minimum power consumption mode.
In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.
MCU interface and memory are still working and the memory keeps it’s contents.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120 msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>SLPIN</td></tr><tr><td>SW Reset</td><td>SLPIN</td></tr><tr><td>HW Reset</td><td>SLPIN</td></tr></table></td></tr>
</table>

7.2.9. SLPOUT (11h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">SLPOUT</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">Sleep out</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command turns off sleep mode.
In this mode e.g. the DC/DC converter is enabled. Intermal oscillator is started, and panel scanning is started.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in sleep out mode. Sleep Our Mode can only be left by the Sleep in Command (10h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the clock circuits to stabilize.
The display module loads all display supplier’s factory default values to the registers during this 120 msec and there cannot be any abnormal visual effect on the display image if faceory default and register values are same when this load is done and when the display module is already Sleep Out-mode.
The display module is doing self-diagnostic function during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.
This command has no effect when module is already in sleep out mode.
Sleep Out Mode can only be left by HW Reset, Software Reset (01h), Sleep In (10h), or a NMI event trigger.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table></td></tr>
</table>

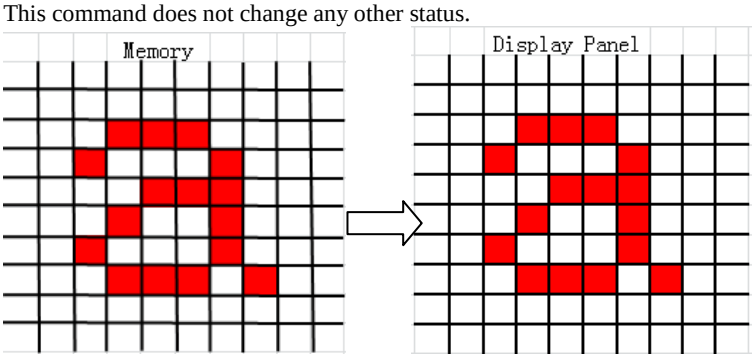
7.2.10. PTLON (12h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">PTLON</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">Partial on</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command turns on partial mode.The partial mode is described by the Partial Area command (30h).
To leave Partial mode, the Normal Display On command (13h) should be written.
X=Don’t care
Note: If a command is written in a frame cycle, the command becomes effective from the next frame.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect during Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>PTL OFF</td></tr><tr><td>SW Reset</td><td>PTL OFF</td></tr><tr><td>HW Reset</td><td>PTL OFF</td></tr></table></td></tr>
</table>

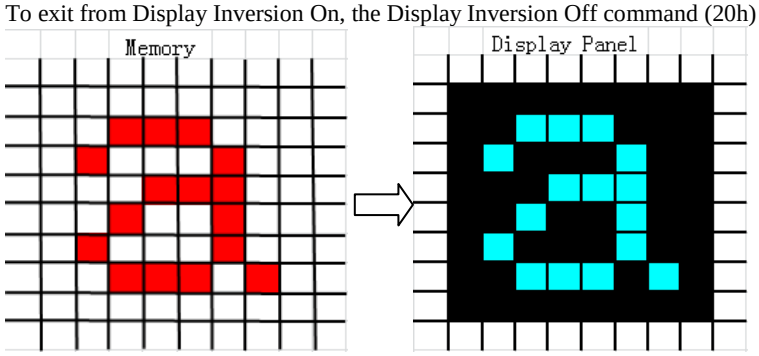
7.2.11. NORMAL (13h)

Command Set		NORMAL								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	Normal on								
Description	This command is used to exit partial and scrolling display mode.									
Restriction	-									

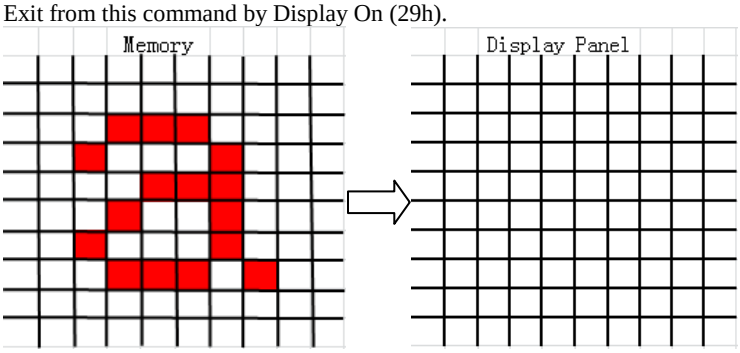
7.2.12. INVOFF (20h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">INVOFF</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">Inversion off</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.

</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in inversion off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>INV OFF</td></tr><tr><td>SW Reset</td><td>INV OFF</td></tr><tr><td>HW Reset</td><td>INV OFF</td></tr></table></td></tr>
</table>

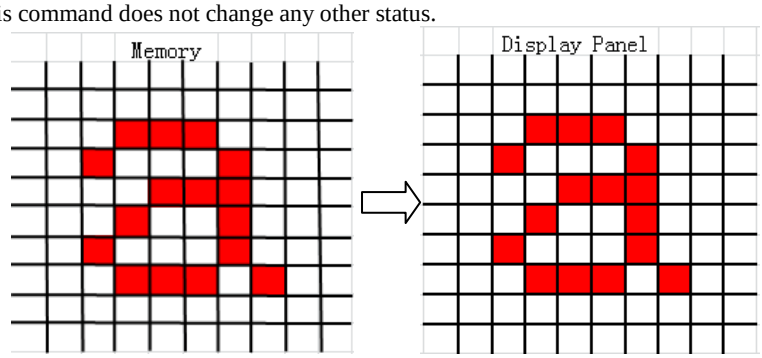
7.2.13. INVON (21h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">INVON</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">Inversion on</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into display inversion mode.
This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in inversion on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>INV OFF</td></tr><tr><td>SW Reset</td><td>INV OFF</td></tr><tr><td>HW Reset</td><td>INV OFF</td></tr></table></td></tr>
</table>

7.2.14. DISPOFF (28h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">DISPOFF</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">Display off</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
Exit from this command by Display On (29h).

</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>SW Reset</td><td>Display Off</td></tr><tr><td>HW Reset</td><td>Display Off</td></tr></table></td></tr>
</table>

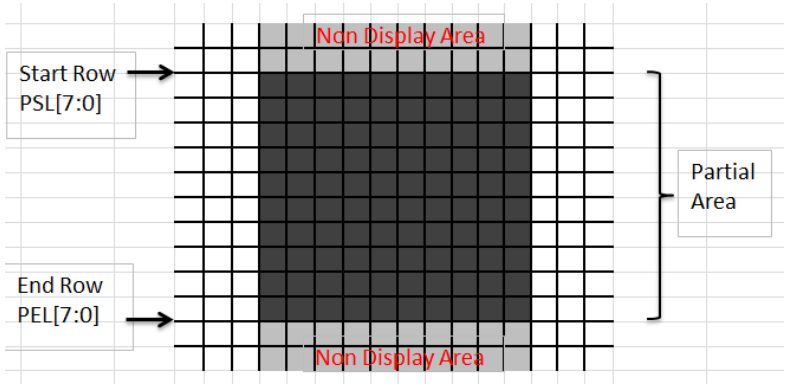
7.2.15. DISPON (29h)

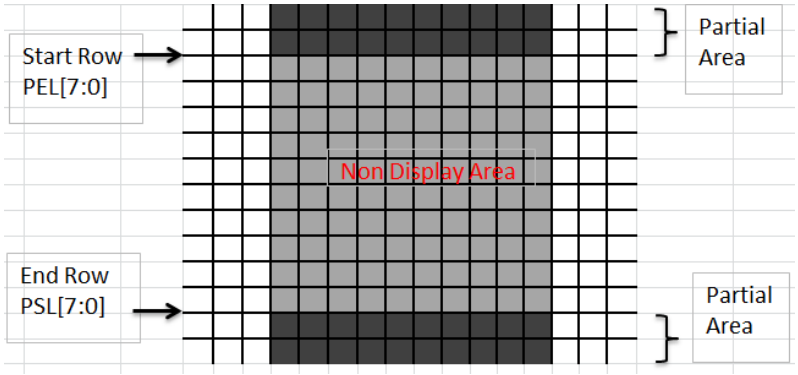
<table>
<tr><th colspan="2">Command Set</th><th colspan="9">DISPON</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">Display on</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memorry is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.

</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10"><table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>Display On</td></tr>
<tr><td>SW Reset</td><td>Display On</td></tr>
<tr><td>HW Reset</td><td>Display On</td></tr>
</table></td></tr>
</table>

7.2.16. COL_ADR / ROW_ADR (2A-2Bh)

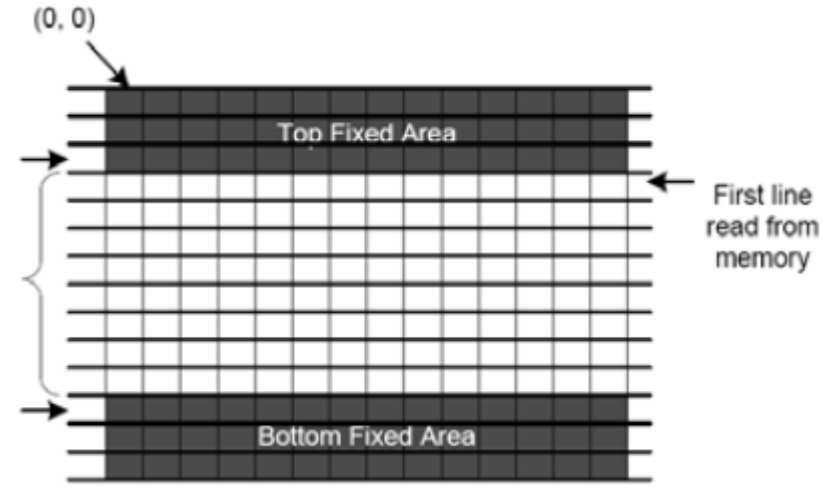
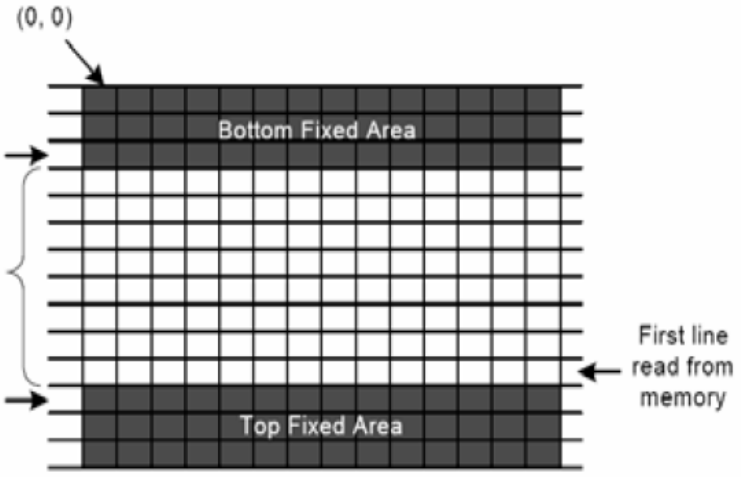
Command Set		COL_ADR/ ROW_ADR								
Address	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
2Ah	Multi-W								col_st[8]	00h
		col_st[7:0]								00h
									col_ed[8]	01h
		col_ed[7:0]								DFh
2Bh	Multi-W								row_st[8]	00h
		row_st[7:0]								00h
									row_ed[8]	01h
		row_ed[7:0]								DFh
Description	“col_st” is sram column access start point. mv = 0, value is 0 ~ 479; mv = 1, value is 0 ~ 271. “col_ed” is sram column access end point. Value range is same as “col_st”. “row_st” is sram row access start point. mv = 0, value is 0 ~ 271; mv=1 , value is 0~479. “row_ed” is sram row access end point. Value range is same as “row_st”.									
Restriction	——									

7.2.17. PTL_ADR (30h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">PTL_ADR</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td rowspan="4">Multi-W</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>ptl_st[8]</td><td>00H</td></tr>
<tr><td>2ndParameter</td><td colspan="8">ptl_st[7:0]</td><td>00H</td></tr>
<tr><td>3rd Parameter</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>ptl_ed[8]</td><td>01H</td></tr>
<tr><td>4thParameter</td><td colspan="8">ptl_ed[7:0]</td><td>0FH</td></tr>
<tr><td>Description</td><td colspan="10">This command defines the partial mode’s display area.There are 2 parameters associated with this command, the first defines the Start Row(PSL) and the second the End Row(PEL),as illustrated in the figure below.PSL and PEL refer to the Frame Memory Line Pointer.
If End Row>Start Row:


If End Row<Start Row:

</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.2.18. SCROLL_ADR (33h)

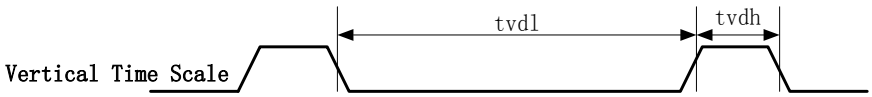
Command Set		SCROLL_ADR								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								tfa[8]	00H
2ndParameter		tfa[7:0]								00H
3rd Parameter									vsa[8]	00H
4thParameter		vsa[7:0]								00H
Description		This command defines the Vertical Scrolling Area of the display. When MADCTL ML=0 The 1st &2nd parameter TFA[7:0]describes the Top Fixed Area (in No.of lines from TOP of the Frame Memory and Display). The 3rd &4th parameter VSA[7:0]describes the height of the Vertical Scrolling Area(in No.of lines of the Frame Memory[not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. TFA, VSA refer to the Frame Memory Line Point.  When MADCTL ML=1 The 1st &2nd parameter TFA[7:0] describes the Top Fixed Area (in No.of lines from Bottom of the Frame Memory and Display). The 3rd &4th parameter VSA[7:0] describes the height of the Vertical Sxrolling Area (in No.of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.  								

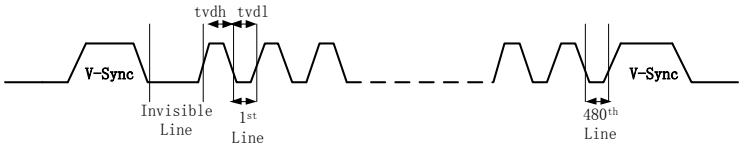
Restriction	1 . (TFA+VSA+BFA)=272 2 . In Vertical Scrol Mode, MADCTL(36H) parameter MV should be set to “0” this affects the Frame memory Write.

7.2.19. TEOFF (34h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">TEOFF</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to turn OFF (Active Low) the Tearing Effect output single from the TE signal line.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
</table>

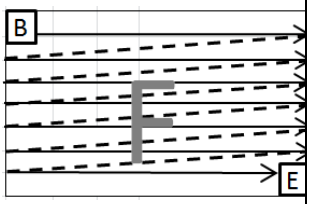
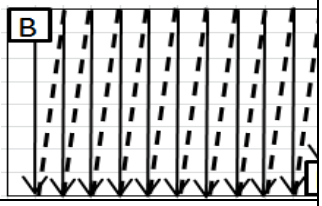
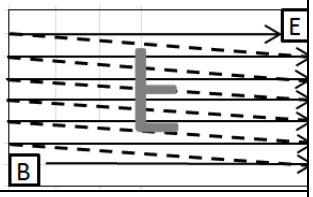
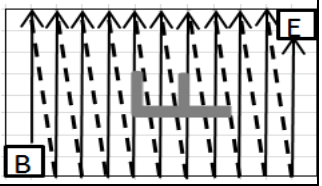
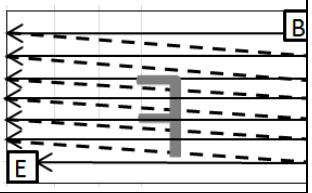
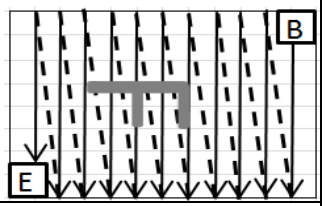
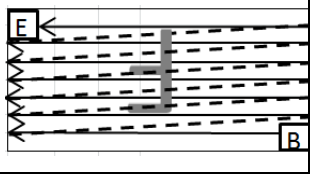
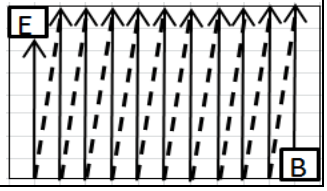
7.2.20. TEON (35h)

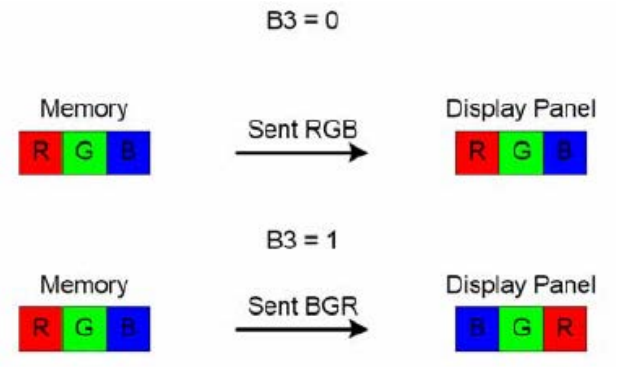
<table>
<tr><th colspan="2">Command Set</th><th colspan="9">TEON</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>te_sel</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to turn ON the Tearing Effect output signal from the TE signal line.This output is not affected by charging MADCTL bit ML.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don’t Care).
When M=0:
The Tearing Effect Output line consists of V-Blanking information only:


When M=1:
The Tearing Effect Output line consists of both V-Blanking and H-Blanking information:


Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active LOW. Display Data Format for color coding (18 bit cases), when there is used 8,9,16 or 18 data line for image data.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when Tearing Effect output is already ON.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Tearing effect off & M=0</td></tr><tr><td>SW Reset</td><td>Tearing effect off & M=0</td></tr><tr><td>HW Reset</td><td>Tearing effect off & M=0</td></tr></table></td></tr>
</table>

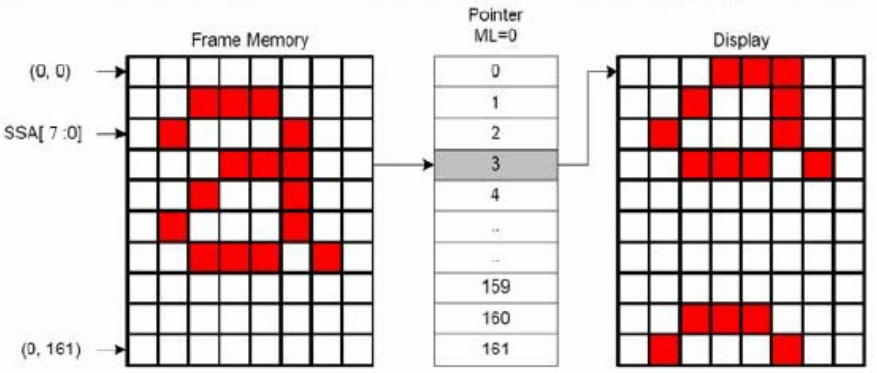
7.2.21. MACTL (36h)

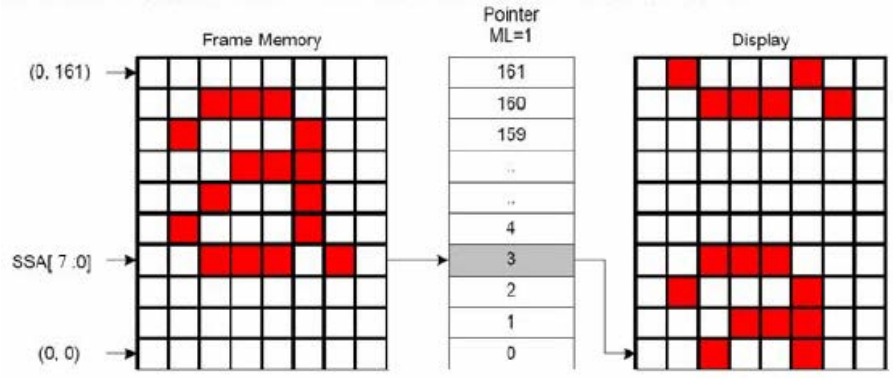
<table>
<tr><th colspan="2">Command Set</th><th colspan="9">MACTL</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td>my</td><td>mx</td><td>mv</td><td>ml</td><td>bgr</td><td></td><td></td><td></td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
Bit Assignment
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>MY</td><td>Row Address Order</td><td rowspan="3">These 3 bits controls MPU to memory write/read direction.</td></tr>
<tr><td>MX</td><td>Column Address Order</td></tr>
<tr><td>MV</td><td>Page/Column Selection</td></tr>
<tr><td>ML</td><td>Vertical Order</td><td>LCD Vertical refresh direction control</td></tr>
<tr><td>RGB</td><td>RGB/BGR Order</td><td>Color selector switch control
0=RGB color filter panel
1=BGR color filter panel</td></tr>
</table>
<table>
<tr><th>B5</th><th>B6</th><th>B7</th><th>Image in Frame Memory</th><th></th><th>B5</th><th>B6</th><th>B7</th><th>Image in Frame Memory</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td></td><td></td><td>1</td><td>0</td><td>0</td><td></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td></td><td></td><td>1</td><td>0</td><td>1</td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td></td><td></td><td>1</td><td>1</td><td>0</td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td></td><td></td><td>1</td><td>1</td><td>1</td><td></td></tr>
</table></td></tr>
</table>

	
Restriction	-

7.2.22. VSCSAD (37h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">VSCSAD</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td rowspan="2">Multi-W</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>ssa[8]</td><td>00H</td></tr>
<tr><td>2nd Parameter</td><td colspan="8">ssa[7:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">This command is used together with Vertical Scrolling Definition(33h).These two command describe the scrolling area and scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last lin of the Top Fixed Area on thd display as illustrated below.
This command Start the scrolling.

When MADCTL ML=0
Exanple: GM=000,132RGBx162
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=162 and Vertical Scrolling Pointer SSA=“3”.


When MADCTL ML=1
Exanple:GM=000,132RGBx162
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=162 and SSA=“3”.


Note:
When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory scan address.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr></table></td></tr>
</table>

	Normal Mode on,ldle Mode On,Sleep Out: Yes Partial Mode on,ldle Mode Off,Sleep Out: Yes Partial Mode on,ldle Mode On,Sleep Out: Yes Sleep In: Yes
Default	**Status** / **Default Value** Power On Sequence: 8'h00 SW Reset: 8'h00 HW Reset: 8'h00

7.2.23. IDMOFF (38h)

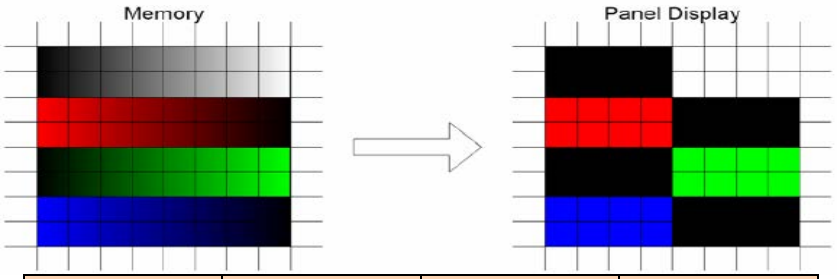
<table>
<tr><th colspan="2">Command Set</th><th colspan="9">IDMOFF</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">Idle off</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the Idle off mode
1, LCD can display maximum 65k, 262k colors.
2, Normal frame frequency is applied.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr><tr><td>HW Reset</td><td>Idle Mode Off</td></tr></table></td></tr>
</table>

7.2.24. IDMON (39h)

Command Set		IDMON								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	Idle on								

Description

This command is used to enter into Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the Idle mode.
Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
8-Color mode frame frequency is applied.
Exit from IDMON by Idle Mode Off (38h) command.



Reduced Color	R[5:0]	G[5:0]	B[5:0]
Black	0XXXX	0XXXX	0XXXX
Blue	0XXXX	0XXXX	1XXXX
Red	1XXXX	0XXXX	0XXXX
Magenta	1XXXX	0XXXX	1XXXX
Green	0XXXX	1XXXX	0XXXX
Cyan	0XXXX	1XXXX	1XXXX
Yellow	1XXXX	1XXXX	0XXXX
White	1XXXX	1XXXX	1XXXX

Restriction: This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes
Partial Mode on,ldle Mode On,Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value(D7 to D0)
Power On Sequence	Idle Mode On
SW Reset	Idle Mode On
HW Reset	Idle Mode On

7.2.25. COLMOD (3Ah)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">COLMOD</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>pxl_fmt</td><td>01H</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to define the format of RGB picture data, pxl_fmt = 0, 6-6-6; pxl_fmt = 1, 5-6-5.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h01</td></tr><tr><td>SW Reset</td><td>8’h01</td></tr><tr><td>HW Reset</td><td>8’h01</td></tr></table></td></tr>
</table>

7.3. Customer Command List and Description

7.3.1. MACTL_USR (40h)

Command Set		MACTL_USR								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	usr_my	usr_mx	usr_mv	usr_ml	usr_bgr			usr_rev	00H
Description	These registers make “XOR” logic with MADCTR (36H). In case of default 36H values are not what you need.									
Restriction	-									

7.3.2. BUS_WD (41h)

Command Set		BUS_WD								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write			bus16_type[1:0]				bus_width[1:0]		00H
Description	Illustrated in section 6.4.5~6.4.9 and 6.4.14~6.4.15									
Restriction										

7.3.3. QSPI_DCTL (43h)

Command Set		QSPI_DCTL								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write				qspi_bgr			qspi_dummy	qspi_sbyte	00H
Description	qspi_bgr is illustrated in section 6.4.13 qspi_sbyte is illustrated in section 6.4.12 qspi_dummy : “1” insert 8 dummy clocks between address and data.									
Restriction	-									

7.3.4. FSM_V-Porch (44-49h)

Command Set		FSM_V-Porch								
Address	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
44h	Write			fsm_vbp[5:0]						05H
45h	Write			fsm_vfp[5:0]						05H
46h	Write			fsm_hbp_o[5:0]						0AH
47h	Write			fsm_hfp_o[5:0]						0AH
48h	Write			fsm_hbp_e[5:0]						1AH
49h	Write			fsm_hfp_e[5:0]						1AH
Description	fsm_vbp[5:0]: internal scan vbp; fsm_vfp[5:0]: internal scan vfp; fsm_hbp_o[5:0]: internal scan hbp for odd line; fsm_hfp_o[5:0]: internal scan hfp for odd line; fsm_hbp_e[5:0]: internal scan hbp for even line; fsm_hfp_e[5:0]: internal scan hfp for even line;									
Restriction	-									

7.3.5. SCAN_VRES (4A-4Bh)

Command Set		SCAN_VRES								
Address	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
4Ah	Multi-W								v_res[8]	01H
		v_res[7:0]								0FH
4Bh	Multi-W								h_res[8]	01H
		h_res[7:0]								0FH
Description	v_res[8:0]: Scan vertical resolution; h_res[8:0]: Scan horizontal resolution;									
Restriction	-									

7.3.6. RGB_H-Porch (4C-4Fh)

Command Set		RGB_H-Porch								
Address	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
4Ch	Write			rgb_hbp_o[5:0]						1AH
4Dh	Write			rgb_hfp_o[5:0]						1AH
4Eh	Write			rgb_hbp_e[5:0]						0AH
4Fh	Write			rgb_hfp_e[5:0]						0AH
Description	rgb_hbp_o[5:0]: rgb scan hbp for odd line; rgb_hfp_o[5:0]: rgb scan hfp for odd line; rgb_hbp_e[5:0]: rgb scan hbp for even line; rgb_hfp_e[5:0]: rgb scan hfp for even line;									
Restriction	-									

7.3.7. GATE_SCAN (50h)

Command Set		GATE_SCAN								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write							gate_scan_seq[1:0]		03H
Description	gate_scan_seq[1:0]: 2'b00 : gate scan sequence 1 ->2 -> 3 -> 4 2'b01 : gate scan sequence 1-> 2 -> 4 -> 3 2'b10 : gate scan sequence in odd frame 1->2->3->4 gate scan sequence in even frame 2->1->4->3 2'b11 : gate scan sequence in odd frame 1->2->4->3 gate scan sequence in even frame 2->1->3->4									
Restriction	-									

7.3.8. GATE_Setting (51h)

Command Set		GATE_Setting								
Address	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
51h	Write	gate_st_o[7:0]								0AH
52h	Write	gate_ed_o[7:0]								64H
53h	Write	gate_st_e[7:0]								0AH
54h	Write	gate_ed_e[7:0]								64H
Description	gate_st_o[7:0]: Gate odd enables start position setting. gate_ed_o[7:0]: Gate odd enables end position setting. gate_st_e[7:0]: Gate even enables start position setting. gate_ed_e[7:0]: Gate even enables end position setting.									
Restriction	-									

7.3.9. PANEL_CTRL (55h)

Command Set		PANEL_CTRL								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write				src_ss				gate_gs	10H
Description	panel display settings: SRC_SS: source reverse scan control. “1” is reverse, “0” is normal. GATE_GS: gate reverse scan control. “1” is reverse, “0” is normal.									
Restriction	-									

7.3.10. PTL_DAT (68h)

Command Set		PTL_DAT								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write								ptl_dat_sel	00H
Description	partial invalid area pixel select, “1” : fill source data with “1” “0” : fill source data with “0”									
Restriction	-									

7.3.11. LVD_SET (6Eh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">LVD_SET</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td>lvd_en</td><td></td><td colspan="3">lvd_adj[2:0]</td><td>04H</td></tr>
<tr><td>Description</td><td colspan="10">LVD_EN：Enable LVD block.
<table><tr><th>LVD_EN</th><th>Description</th></tr><tr><td>0</td><td>Disable LVD block</td></tr><tr><td>1</td><td>Enable LVD block</td></tr></table>LVD_ADJ[2:0]: Low voltage detector range
<table><tr><th>LVD_ADJ[2:0]</th><th>Value (V)</th></tr><tr><td>000</td><td>2.86</td></tr><tr><td>001</td><td>2.76</td></tr><tr><td>010</td><td>2.66</td></tr><tr><td>011</td><td>2.56</td></tr><tr><td>100</td><td>2.36</td></tr><tr><td>101</td><td>2.16</td></tr><tr><td>110</td><td>1.96</td></tr><tr><td>111</td><td>1.76</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.12. USR_GVDD (6Fh)

Command Set		USR_GVDD								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write		usr_gvdd[6:0]							16H

Description

GVDD level adjustment:

usr_gvdd[6:0]	GVDD	usr_gvdd[6:0]	GVDD	usr_gvdd[6:0]	GVDD	usr_gvdd[6:0]	GVDD
0000000	6.2224	0100000	5.7105	1000000	5.1985	1100000	6.2374
0000001	6.2065	0100001	5.6945	1000001	5.1825	1100001	6.2374
0000010	6.1905	0100010	5.6785	1000010	5.1665	1100010	6.2374
0000011	6.1745	0100011	5.6625	1000011	5.1505	1100011	6.2374
0000100	6.1585	0100100	5.6465	1000100	5.1345	1100100	6.2374
0000101	6.1425	0100101	5.6305	1000101	5.1185	1100101	6.2374
0000110	6.1265	0100110	5.6145	1000110	5.1025	1100110	6.2374
0000111	6.1105	0100111	5.5985	1000111	5.0866	1100111	6.2374
0001000	6.0945	0101000	5.5825	1001000	5.0706	1101000	6.2374
0001001	6.0785	0101001	5.5665	1001001	5.0546	1101001	6.2374
0001010	6.0625	0101010	5.5505	1001010	5.0386	1101010	6.2374
0001011	6.0465	0101011	5.5345	1001011	5.0226	1101011	6.2374
0001100	6.0305	0101100	5.5185	1001100	5.0066	1101100	6.2374
0001101	6.0145	0101101	5.5025	1001101	4.9906	1101101	6.2374
0001110	5.9985	0101110	5.4865	1001110	4.9746	1101110	6.2374
0001111	5.9825	0101111	5.4705	1001111	4.9586	1101111	6.2374
0010000	5.9665	0110000	5.4545	1010000	4.9426	1110000	6.2374
0010001	5.9505	0110001	5.4385	1010001	4.9266	1110001	6.2374
0010010	5.9345	0110010	5.4225	1010010	4.9106	1110010	6.2374
0010011	5.9185	0110011	5.4065	1010011	4.8946	1110011	6.2374
0010100	5.9025	0110100	5.3905	1010100	4.8786	1110100	6.2374
0010101	5.8865	0110101	5.3745	1010101	4.8626	1110101	6.2374
0010110	5.8705	0110110	5.3585	1010110	4.8466	1110110	6.2374
0010111	5.8545	0110111	5.3425	1010111	4.8306	1110111	6.2374
0011000	5.8385	0111000	5.3265	1011000	4.8146	1111000	6.2374
0011001	5.8225	0111001	5.3105	1011001	4.7986	1111001	6.2374
0011010	5.8065	0111010	5.2945	1011010	4.7826	1111010	6.2374
0011011	5.7905	0111011	5.2785	1011011	4.7666	1111011	6.2374
0011100	5.7745	0111100	5.2625	1011100	4.7506	1111100	6.2374
0011101	5.7585	0111101	5.2465	1011101	4.7346	1111101	6.2374
0011110	5.7425	0111110	5.2305	1011110	4.7186	1111110	6.2374
0011111	5.7265	0111111	5.2145	1011111	4.7026	1111111	6.2374

Restriction	-

7.3.13. USR_GVCL (78h)

Command Set		USR_GVCL								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write		usr_gvcl[6:0]							47H

Description

GVCL LDO output voltage level adjustment:

gvcl_adj[6:0]	GVCL	gvcl_adj[6:0]	GVCL	gvcl_adj[6:0]	GVCL	gvcl_adj[6:0]	GVCL
0000000	-4.7371	0100000	-4.2253	1000000	-3.7135	1100000	-3.2018
0000001	-4.7211	0100001	-4.2093	1000001	-3.6975	1100001	-3.1858
0000010	-4.7051	0100010	-4.1933	1000010	-3.6815	1100010	-3.1699
0000011	-4.6891	0100011	-4.1773	1000011	-3.6655	1100011	-3.1539
0000100	-4.6731	0100100	-4.1613	1000100	-3.6495	1100100	-3.1379
0000101	-4.6572	0100101	-4.1453	1000101	-3.6336	1100101	-3.1219
0000110	-4.6412	0100110	-4.1293	1000110	-3.6176	1100110	-3.1059
0000111	-4.6252	0100111	-4.1133	1000111	-3.6016	1100111	-3.0899
0001000	-4.6092	0101000	-4.0973	1001000	-3.5856	1101000	-3.0739
0001001	-4.5932	0101001	-4.0814	1001001	-3.5696	1101001	-3.0579
0001010	-4.5772	0101010	-4.0654	1001010	-3.5536	1101010	-3.0419
0001011	-4.5612	0101011	-4.0494	1001011	-3.5376	1101011	-3.0259
0001100	-4.5452	0101100	-4.0334	1001100	-3.5216	1101100	-3.0099
0001101	-4.5292	0101101	-4.0174	1001101	-3.5056	1101101	-2.9939
0001110	-4.5132	0101110	-4.0014	1001110	-3.4896	1101110	-2.978
0001111	-4.4972	0101111	-3.9854	1001111	-3.4736	1101111	-2.962
0010000	-4.4812	0110000	-3.9694	1010000	-3.4577	1110000	-2.946
0010001	-4.4652	0110001	-3.9534	1010001	-3.4417	1110001	-2.93
0010010	-4.4492	0110010	-3.9374	1010010	-3.4257	1110010	-2.914
0010011	-4.4332	0110011	-3.9214	1010011	-3.4097	1110011	-2.898
0010100	-4.4172	0110100	-3.9054	1010100	-3.3937	1110100	-2.882
0010101	-4.4012	0110101	-3.8894	1010101	-3.3777	1110101	-2.866
0010110	-4.3852	0110110	-3.8734	1010110	-3.3617	1110110	-2.85
0010111	-4.3693	0110111	-3.8574	1010111	-3.3457	1110111	-2.834
0011000	-4.3533	0111000	-3.8415	1011000	-3.3297	1111000	-2.8181
0011001	-4.3373	0111001	-3.8255	1011001	-3.3138	1111001	-2.8021
0011010	-4.3213	0111010	-3.8095	1011010	-3.2978	1111010	-2.7861
0011011	-4.3053	0111011	-3.7935	1011011	-3.2818	1111011	-2.7701
0011100	-4.2893	0111100	-3.7775	1011100	-3.2658	1111100	-2.7541
0011101	-4.2733	0111101	-3.7615	1011101	-3.2498	1111101	-2.7381
0011110	-4.2573	0111110	-3.7455	1011110	-3.2338	1111110	-2.7221
0011111	-4.2413	0111111	-3.7295	1011111	-3.2178	1111111	-2.7061

Restriction: -

7.3.14. USR_VGSP (7A)

Command Set		USR_VGSP								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write		usr_vgsp[6:0]							3FH

Description

VGSP level adjustment

vgsp_adj[6:0]	VGSP	vgsp_adj[6:0]	VGSP	vgsp_adj[6:0]	VGSP	vgsp_adj[6:0]	VGSP
0000000	2.064	0100000	1.552	1000000	1.04	1100000	0.528
0000001	2.048	0100001	1.536	1000001	1.024	1100001	0.512
0000010	2.032	0100010	1.52	1000010	1.008	1100010	0.496
0000011	2.016	0100011	1.504	1000011	0.992	1100011	0.48
0000100	2	0100100	1.488	1000100	0.976	1100100	0.464
0000101	1.984	0100101	1.472	1000101	0.96	1100101	0.448
0000110	1.968	0100110	1.456	1000110	0.944	1100110	0.432
0000111	1.952	0100111	1.44	1000111	0.928	1100111	0.416
0001000	1.936	0101000	1.424	1001000	0.912	1101000	0.4
0001001	1.92	0101001	1.408	1001001	0.896	1101001	0.384
0001010	1.904	0101010	1.392	1001010	0.88	1101010	0.368
0001011	1.888	0101011	1.376	1001011	0.864	1101011	0.352
0001100	1.872	0101100	1.36	1001100	0.848	1101100	0.336
0001101	1.856	0101101	1.344	1001101	0.832	1101101	0.32
0001110	1.84	0101110	1.328	1001110	0.816	1101110	0.304
0001111	1.824	0101111	1.312	1001111	0.8	1101111	0.288
0010000	1.808	0110000	1.296	1010000	0.784	1110000	0.272
0010001	1.792	0110001	1.28	1010001	0.768	1110001	0.256
0010010	1.776	0110010	1.264	1010010	0.752	1110010	0.24
0010011	1.76	0110011	1.248	1010011	0.736	1110011	0.224
0010100	1.744	0110100	1.232	1010100	0.72	1110100	0.208
0010101	1.728	0110101	1.216	1010101	0.704	1110101	0.192
0010110	1.712	0110110	1.2	1010110	0.688	1110110	0.176
0010111	1.696	0110111	1.184	1010111	0.672	1110111	0.16
0011000	1.68	0111000	1.168	1011000	0.656	1111000	0.144
0011001	1.664	0111001	1.152	1011001	0.64	1111001	0.128
0011010	1.648	0111010	1.136	1011010	0.624	1111010	0.112
0011011	1.632	0111011	1.12	1011011	0.608	1111011	0.096
0011100	1.616	0111100	1.104	1011100	0.592	1111100	0.080
0011101	1.6	0111101	1.088	1011101	0.576	1111101	0.064
0011110	1.584	0111110	1.072	1011110	0.56	1111110	0.048
0011111	1.568	0111111	1.056	1011111	0.544	1111111	0.032

Restriction: -

7.3.15. GVREF2V (7Ch)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">GVREF2V</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td colspan="4">gvref2v[3:0]</td><td>07H</td></tr>
<tr><td>Description</td><td colspan="10">gvref2v[3:0]:VREF2V level adjustment
<table>
<tr><th>VREF2V_ADJ[3:0]</th><th>Vref</th><th>VREF2V_ADJ[3:0]</th><th>Vref</th></tr>
<tr><td>0000</td><td>2.1919</td><td>1000</td><td>2.0639</td></tr>
<tr><td>0001</td><td>2.176</td><td>1001</td><td>2.0479</td></tr>
<tr><td>0010</td><td>2.16</td><td>1010</td><td>2.0319</td></tr>
<tr><td>0011</td><td>2.144</td><td>1011</td><td>2.0159</td></tr>
<tr><td>0100</td><td>2.128</td><td>1100</td><td>1.9999</td></tr>
<tr><td>0101</td><td>2.112</td><td>1101</td><td>1.9839</td></tr>
<tr><td>0110</td><td>2.096</td><td>1110</td><td>1.9679</td></tr>
<tr><td>0111</td><td>2.08</td><td>1111</td><td>1.9519</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.16. VDDS_TRIM (7Dh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">VDDS_TRIM</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">vdds_trim[2:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10"><table><tr><th>VDDS_TRIM[2:0]</th><th>Value (V)</th></tr><tr><td>000</td><td>1.79</td></tr><tr><td>001</td><td>1.90</td></tr><tr><td>010</td><td>2.03</td></tr><tr><td>011</td><td>2.07</td></tr><tr><td>100</td><td>2.15</td></tr><tr><td>101</td><td>2.23</td></tr><tr><td>110</td><td>2.40</td></tr><tr><td>111</td><td>2.50</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.17. Gamma P Selection (80h~92h)

Command Set		Gamma P Selection								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
80h	Write			gam_vrp0[5:0]						00h
81h	Write			gam_vrp1[5:0]						00h
82h	Write			gam_vrp2[5:0]						00h
83h	Write			gam_vrp3[5:0]						00h
84h	Write			gam_vrp4[5:0]						00h
85h	Write			gam_vrp5[5:0]						00h
86h	Write		gam_prp0[6:0]							00h
87h	Write		gam_prp1[6:0]							00h
88h	Write				gam_pkp0[4:0]					00h
89h	Write				gam_pkp1[4:0]					00h
8Ah	Write				gam_pkp2[4:0]					00h
8Bh	Write				gam_pkp3[4:0]					00h
8Ch	Write				gam_pkp4[4:0]					00h
8Dh	Write				gam_pkp5[4:0]					00h
8Eh	Write				gam_pkp6[4:0]					00h
8Fh	Write				gam_pkp7[4:0]					00h
90h	Write				gam_pkp8[4:0]					00h
91h	Write				gam_pkp9[4:0]					00h
92h	Write				gam_pkp10[4:0]					00h
Description	Gamma adjusts registers. See gamma correction section for reference.									
Restriction	-									

7.3.18. Gamma N Selection (A0~B2h)

Command Set		Gamma N Selection								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A0h	Write			gam_vrn0[5:0]						00h
A1h	Write			gam_vrn1[5:0]						00h
A2h	Write			gam_vrn2[5:0]						00h
A3h	Write			gam_vrn3[5:0]						00h
A4h	Write			gam_vrn4[5:0]						00h
A5h	Write			gam_vrn5[5:0]						00h
A6h	Write		gam_prn0[6:0]							00h
A7h	Write		gam_prn1[6:0]							00h
A8h	Write				gam_pkn0[4:0]					00h
89h	Write				gam_pkn1[4:0]					00h
8Ah	Write				gam_pkn2[4:0]					00h
ABh	Write				gam_pkn3[4:0]					00h
ACh	Write				gam_pkn4[4:0]					00h
ADh	Write				gam_pkn5[4:0]					00h
AEh	Write				gam_pkn6[4:0]					00h
AFh	Write				gam_pkn7[4:0]					00h
B0h	Write				gam_pkn8[4:0]					00h
B1h	Write				gam_pkn9[4:0]					00h
B2h	Write				gam_pkn10[4:0]					00h
Description	Gamma adjusts registers. See gamma correction section for reference.									
Restriction	-									

7.3.19. BIAS_VBG (C0h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">BIAS_VBG</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td colspan="3">bias_adj[2:0]</td><td colspan="4">vbg_adj[3:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">bias_adj[2:0]: Adjust the Ibias
<table>
<tr><th>D2A_BIAS_ADJ[2:0]</th><th>Current(uA)</th></tr>
<tr><td>000</td><td>1.000</td></tr>
<tr><td>001</td><td>1.060</td></tr>
<tr><td>010</td><td>1.120</td></tr>
<tr><td>011</td><td>1.380</td></tr>
<tr><td>100</td><td>2.240</td></tr>
<tr><td>101</td><td>0.948</td></tr>
<tr><td>110</td><td>0.901</td></tr>
<tr><td>111</td><td>0.721</td></tr>
</table>
vbg_adj[3:0]：Adjust the Vout of Bandgap.
<table>
<tr><th>VBG_ADJ[3:0]</th><th>Bandgap</th><th>VBG_ADJ[3:0]</th><th>Bandgap</th></tr>
<tr><td>0000</td><td>1.316</td><td>1000</td><td>1.326</td></tr>
<tr><td>0001</td><td>1.307</td><td>1001</td><td>1.335</td></tr>
<tr><td>0010</td><td>1.298</td><td>1010</td><td>1.344</td></tr>
<tr><td>0011</td><td>1.289</td><td>1011</td><td>1.353</td></tr>
<tr><td>0100</td><td>1.279</td><td>1100</td><td>1.362</td></tr>
<tr><td>0101</td><td>1.271</td><td>1101</td><td>1.371</td></tr>
<tr><td>0110</td><td>1.252</td><td>1110</td><td>1.39</td></tr>
<tr><td>0111</td><td>1.234</td><td>1111</td><td>1.407</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.20. MV_CLP (C1h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">MV_CLP</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td>avdd_clp_en</td><td></td><td colspan="2">avdd_clp[1:0]</td><td>avcl_clp_en</td><td></td><td colspan="2">avcl_clp[1:0]</td><td>BBH</td></tr>
<tr><td>Description</td><td colspan="10">avdd_clp_en: AVDD pump clamp enable
avdd_clp[1:0]: AVDD pump value adjust
<table>
<tr><th>D2A_AVDD_CLP[1:0]</th><th>AVDD</th></tr>
<tr><td>00</td><td>5.93</td></tr>
<tr><td>01</td><td>6.13</td></tr>
<tr><td>10(def)</td><td>6.54</td></tr>
<tr><td>11</td><td>6.74</td></tr>
</table>
avcl_clp_en: AVCL pump clamp enable
avcl_clp[1:0]: AVCL pump value adjust
<table>
<tr><th>D2A_AVCL_CLP[1:0]</th><th>AVCL</th></tr>
<tr><td>00</td><td>-4.34</td></tr>
<tr><td>01</td><td>-4.55</td></tr>
<tr><td>10(def)</td><td>-4.96</td></tr>
<tr><td>11</td><td>-5.16</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.21. VGH_CLP (C2h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">VGH_CLP</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td>vgh_clp_en</td><td></td><td colspan="3">vgh_clp[2:0]</td><td>15H</td></tr>
<tr><td>Description</td><td colspan="10">VGH_CLP_EN: VGH Pump clamp enable signal
<table>
<tr><th>VGH_CLP_EN</th><th>Description</th></tr>
<tr><td>0</td><td>Disable clamp</td></tr>
<tr><td>1</td><td>Enable clamp</td></tr>
</table>
VGH_CLP_ADJ[2:0]: VGH level adjustment
<table>
<tr><th>VGH_CLP_ADJ[2:0]</th><th>VGH(V)</th></tr>
<tr><td>000</td><td>13.36</td></tr>
<tr><td>001</td><td>13.77</td></tr>
<tr><td>010</td><td>14.17</td></tr>
<tr><td>011</td><td>14.58</td></tr>
<tr><td>100</td><td>14.98</td></tr>
<tr><td>101</td><td>15.39</td></tr>
<tr><td>110</td><td>15.79</td></tr>
<tr><td>111</td><td>16.197</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.22. VGL_CLP (C3h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">VGL_CLP</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td>vgl_clp_en</td><td></td><td colspan="3">vgl_clp[2:0]</td><td>12H</td></tr>
<tr><td>Description</td><td colspan="10">Vgl_clp_en: VGL pump clamp enable signal (default: 1)
Vgl_clp[2:0]: VGL pump clamp value
<table>
<tr><th>Vgl_clp[2:0]</th><th>VGL (unit:V)</th></tr>
<tr><td>000</td><td>-10.951</td></tr>
<tr><td>001</td><td>-10.551</td></tr>
<tr><td>010</td><td>-10.150</td></tr>
<tr><td>011</td><td>-9.751</td></tr>
<tr><td>100</td><td>-9.346</td></tr>
<tr><td>101</td><td>-8.946</td></tr>
<tr><td>110</td><td>-8.543</td></tr>
<tr><td>111</td><td>-8.145</td></tr>
</table>
Default value: 010</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.23. MV_TD (C4h)

Command Set		MV_TD								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write		vgh_skip	vgh_td[1:0]			vgl_skip	vgl_td[1:0]		22H
Description	vgl_skip: clamp choose function vgl_td[1:0]: Vgl overlap setting									
Restriction	-									

7.3.24. MV_SS_CTRL (C5h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">MV_SS_CTRL</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td>avdd_ss_en</td><td></td><td></td><td></td><td>avcl_ss_en</td><td>11H</td></tr>
<tr><td>Description</td><td colspan="10">AVDD_SS_EN: AVDD Pump soft start enable signal.
<table>
<tr><th>AVDD_SS_EN</th><th>Description</th></tr>
<tr><td>0</td><td>Disable soft start</td></tr>
<tr><td>1</td><td>Enable soft start</td></tr>
</table>
AVCL_SS_EN: AVCL Pump soft start enable signal.
<table>
<tr><th>AVCL_SS_EN</th><th>Description</th></tr>
<tr><td>0</td><td>Disable soft start</td></tr>
<tr><td>1</td><td>Enable soft start</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.25. RATIO_CTRL (C6h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">RATIO_CTRL</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td>avdd_ratio_sel</td><td>avcl_ratio_sel</td><td colspan="2">vgh_ratio_sel[1:0]</td><td colspan="2">vgl_ratio_sel[1:0]</td><td>35H</td></tr>
<tr><td>Description</td><td colspan="10">
avdd_ratio_sel: AVDD pump ratio select
<table>
<tr><th>avdd_ratio_sel[1:0]</th><th>AVDD</th></tr>
<tr><td>0</td><td>2*VCI</td></tr>
<tr><td>1</td><td>3*VCI</td></tr>
</table>
avcl_ratio_sel: AVCL pump ratio select
<table>
<tr><th>avcl_ratio_sel[1:0]</th><th>AVCL</th></tr>
<tr><td>0</td><td>-1*VCI</td></tr>
<tr><td>1</td><td>-2*VCI</td></tr>
</table>
vgh_ratio_sel[1:0]: vgh ratio setting
<table>
<tr><th>Vgh_ratio_sel[1:0]</th><th>VGH</th></tr>
<tr><td>00</td><td>6*VCIP</td></tr>
<tr><td>01</td><td>7*VCIP</td></tr>
<tr><td>10</td><td>8*VCIP</td></tr>
<tr><td>11</td><td>9*VCIP</td></tr>
</table>
vgl_ratio_sel[1:0]: vgl ratio setting
<table>
<tr><th>Vgl_ratio_sel[1:0]</th><th>VGL</th></tr>
<tr><td>00</td><td>4*VCI</td></tr>
<tr><td>01</td><td>5*VCI</td></tr>
<tr><td>10</td><td>6*VCI</td></tr>
<tr><td>11</td><td>6*VCI</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.26. MV_PUMP_CLK (C7h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">MV_PUMP_CLK</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td colspan="2">mv_clk_sel[1:0]</td><td colspan="2">avdd_clk_sel[1:0]</td><td colspan="2">avcl_clk_sel[1:0]</td><td>2AH</td></tr>
<tr><td>Description</td><td colspan="10">mv_clk_sel: gamma pump clk frequency selection
<table>
<tr><th>mv_clk_sel</th><th>frequency</th></tr>
<tr><td>2’b00</td><td>F_{osc}/4</td></tr>
<tr><td>2’b01</td><td>F_{osc}/8</td></tr>
<tr><td>2’b10</td><td>F_{osc}/16</td></tr>
<tr><td>2’b11</td><td>F_{osc}/32</td></tr>
</table>
AVDD_CLK_SEL[1:0]: AVDD clock frequency adjustment
<table>
<tr><th>AVDD_CLK_SEL[1:0]</th><th>Frequency(MHz)</th></tr>
<tr><td>00</td><td>F_{osc}/4</td></tr>
<tr><td>01</td><td>F_{osc}/8</td></tr>
<tr><td>10</td><td>F_{osc}/16</td></tr>
<tr><td>11</td><td>F_{osc}/32</td></tr>
</table>
AVCL_CLK_SEL[1:0]: AVCL clock frequency adjustment
<table>
<tr><th>AVCL_CLK_SEL[1:0]</th><th>Frequency(MHz)</th></tr>
<tr><td>00</td><td>F_{osc}/4</td></tr>
<tr><td>01</td><td>F_{osc}/8</td></tr>
<tr><td>10</td><td>F_{osc}/16</td></tr>
<tr><td>11</td><td>F_{osc}/32</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.27. HV_PUMP_CLK (C8h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">HV_PUMP_CLK</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td colspan="2">vgh_clk_sel[1:0]</td><td></td><td></td><td colspan="2">vgl_clk_sel[1:0]</td><td>11H</td></tr>
<tr><td>Description</td><td colspan="10">vgh_clk_sel[1:0]: vgh clk setting
<table>
<tr><th>Vgh_ratio_sel[1:0]</th><th>VGH</th></tr>
<tr><td>00</td><td>Fosc/4</td></tr>
<tr><td>01</td><td>Fosc/8</td></tr>
<tr><td>10</td><td>Fosc/16</td></tr>
<tr><td>11</td><td>Fosc/32</td></tr>
</table>
vgl_clk_sel[1:0]: vgl clk setting
<table>
<tr><th>Vgl_ratio_sel[1:0]</th><th>VGL</th></tr>
<tr><td>00</td><td>Fosc/4</td></tr>
<tr><td>01</td><td>Fosc/8</td></tr>
<tr><td>10</td><td>Fosc/16</td></tr>
<tr><td>11</td><td>Fosc/32</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.28. MV_CLK_CLP (C9h)

Command Set		MV_CLK_CLP								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write			avdd_fdbk_en	avcl_fdbk_en		vgh_freq_en	avdd_freq_en	avcl_freq_en	37H
Description	avdd_fdbk_en : avdd frequency switching enable control for positive source charging avcl_fdbk_en : avcl frequency switching enable control for positive source charging avdd_freq_en : avdd frequency switching enable control for positive source charging avcl_freq_en : avcl frequency switching enable control for negative source charging									
Restriction	-									

7.3.29. RD_SYSID (DA-DCh)

Command Set		RD_SYSID1								
Address	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
DAh	Read	sys_id1[7:0]								30
DBh	Read	sys_id2[7:0]								41
DCh	Read	sys_id3[7:0]								A1
Description	The read parameters are used to recognize the LCD driver version. It is defined by the display supplier (with User's agreement).									
Restriction	-									

7.3.30. RGB_CTL (E1h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">RGB_CTL</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td>auto_detect</td><td></td><td colspan="2">sync_ctrl[1:0]</td><td></td><td></td><td colspan="2">seri_db_sel[1:0]</td><td>80H</td></tr>
<tr><td>Description</td><td colspan="10">DPI interface has two working mode: sync_mode, de_mode.
a. Auto_detect=1’b1, auto switch interface mode according to RGB information
b. Auto_detect=1’b0 and sync_ctrl[1]=2’b0, PAD_SYNC = 1 sync mode, PAD_SYNC=0 de mode.
c. Auto_detect=1’b0 and sync_ctrl[1]=1’b1, sync_ctrl[0] = 1 sync mode, sync_ctrl[0]=0 de mode.
serial_db_sel: Select which 6bit is used to serial DPI mode.
<table><tr><th>seri_db_sel[1:0]</th><th>Data Bus for Serial Mode</th></tr><tr><td>2’b00</td><td>DG[7:2]</td></tr><tr><td>2’b11</td><td>DG[7:2]</td></tr><tr><td>2’b01</td><td>DR[7:2]</td></tr><tr><td>2’b10</td><td>DB[7:2]</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.31. RGB_POL (E2h)

Command Set		RGB_POL								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write				pol_auto	rgb_pclk_pol	rgb_vpol	rgb_hpol	rgb_depol	18H
Description	pol_auto: checking and correcting polarity of vsync, de and hsync signals. rgb_pclk_pol: “1” inverted pclk , “0” original pclk rgb_vpol: “1”inverted vsync input rgb_hpol: “1” inverted hsync input rgb_depol: “1” inverted de input Note: when pol_auto is “1”， rgb_vpol, rgb_hpol and rgb_depol are disabled.									
Restriction										

7.3.32. INTF_Porch (E3-E4h)

Command Set		INTF_Porch								
Address	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E3h	Write	intf_vbp[7:0]								0AH
E4h	Write	intf_hbp[7:0]								0AH
Description	DPI Interface vbp and hbp configuration at SYNC MODE.									
Restriction	-									

7.3.33. DVDD_TRIM (E5h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">DVDD_TRIM</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">dvdd_trim[2:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10"><table><tr><th>D2A_DVDD_TRIM<1:0></th><th>DVDD（V）</th></tr><tr><td>000</td><td>1.55</td></tr><tr><td>001</td><td>1.5</td></tr><tr><td>010</td><td>1.45</td></tr><tr><td>011</td><td>1.4</td></tr><tr><td>100</td><td>1.6</td></tr><tr><td>101</td><td>1.65</td></tr><tr><td>110</td><td>1.7</td></tr><tr><td>111</td><td>1.75</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.34. ESD_CTRL (E6h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">ESD_CTRL</th></tr>
<tr><th>Command</th><th>Write/Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td>esd_detect_en</td><td>esd_otp_en</td><td>esd_sfr_en</td><td></td><td></td><td colspan="2">esd_level_sel[1:0]</td><td>70H</td></tr>
<tr><td>Description</td><td colspan="10">
<table>
<tr><th>esd_level_sel[1:0]</th><th>a2d_esd_dvdd</th><th>Description</th></tr>
<tr><td>00</td><td>a2d_esd_dvdd[0]</td><td>ESD pulse amplitude signal is greater than +1V,output from low voltage level to high voltage level</td></tr>
<tr><td>01</td><td>a2d_esd_dvdd[1]</td><td>ESD pulse amplitude signal is less than -1V,output from low voltage level to high voltage level</td></tr>
<tr><td>10</td><td>a2d_esd_dvdd[2]</td><td>ESD pulse amplitude signal is greater than +2V,output from low voltage level to high voltage level</td></tr>
<tr><td>11</td><td>a2d_esd_dvdd[3]</td><td>ESD pulse amplitude signal is less than -2V,output from low voltage level to high voltage level</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

7.3.35. TE_CTRL (E7h)

Command Set		TE_CTRL								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write				te_out_oe				te_inv	00H
Description	te_out_oe : TE output pad open enable te_inv: inverted TE output									
Restriction										

7.3.36. OTP_CTRL (F1-F6h)

Command Set		OTP_CTRL								
Address	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
F1h	Write	otp_pa[7:0]								00H
F2h	Write	otp_pdin[7:0]								00H
F3h	Write	otp_ptm[1:0]			otp_vpp_sel	otp_prog		otp_pwe	otp_prd	00H
F4h	Read	otp_crc[15:8]								
F5h	Read	otp_crc[7:0]								
F6h	Read	otp_rd_dat[7:0]								
Description	otp_ptm: otp mode selection; otp_vpp_sel: high voltage seletion for programming; otp_prog: otp program enable; otp_pwe: otp write operation enable; otp_prd: otp read operation enable; otp_crc: CRC checking of OTP values; otp_rd_dat[7:0]:This command is used to read otp contents;									
Restriction										

8. Electrical specifications

8.1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	VDD	- 0.3 ~ +4.6	V
IO Supply Voltage	IOVCC	- 0.3 ~ +4.6	V
Charge Pump Supply Voltage	VCIP	- 0.3 ~ +4.6	V
Logic Input Voltage Range	VIN	-0.3 ~ IOVCC + 0.3	V
Logic Output Voltage Range	VO	-0.3 ~ IOVCC + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

8.2. DC Characteristics

8.2.1. Recommended Operating Range

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCI	3	3.3	3.6	V	
IO Supply Voltage	IOVCC	1.65	-	VCI	V	
Charge Pump Supply Voltage	VCIP	3	3.3	3.6	V	
NVM Supply Voltage	VPP	7.4	7.5	7.6	V	

8.2.2. DC Characteristics for Digital Circuit

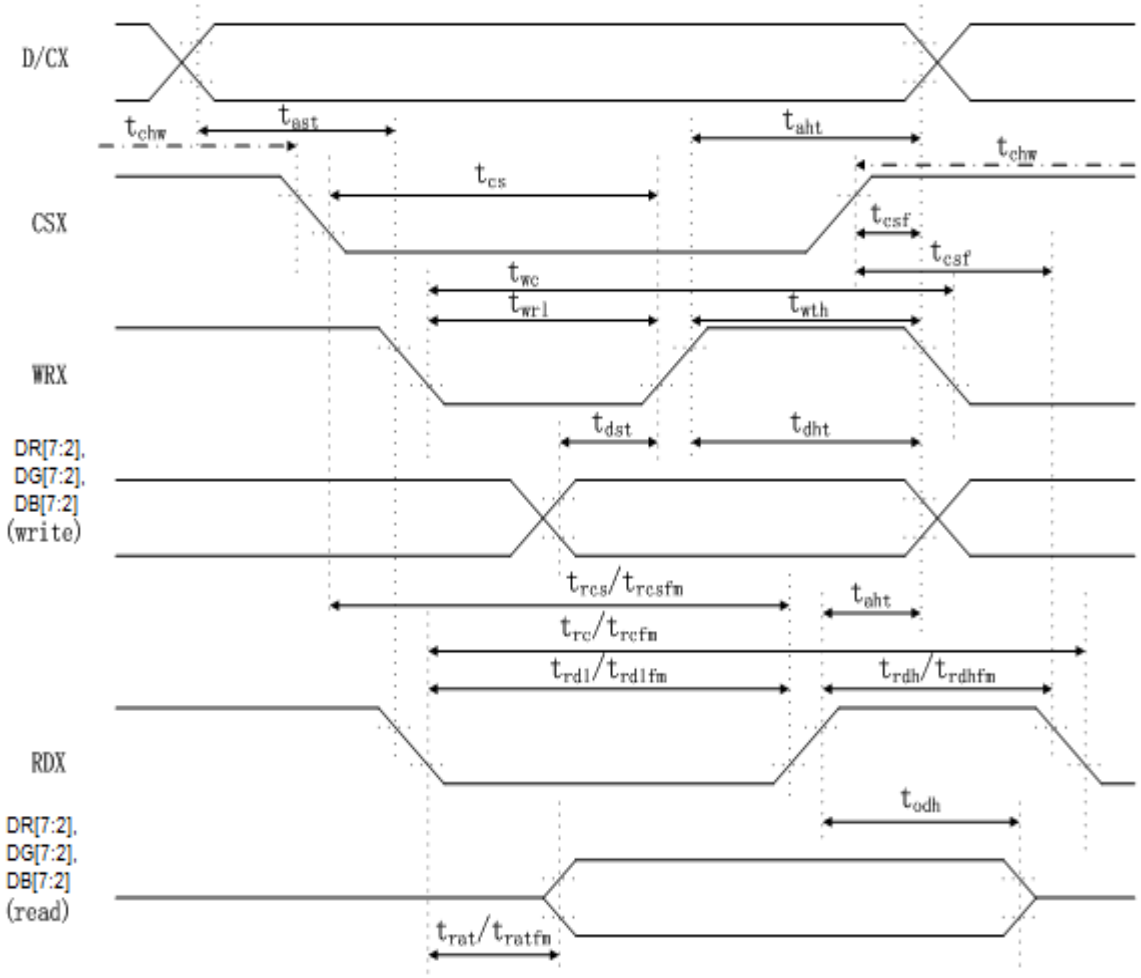
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7IOVCC	-	IOVCC	V	IOVCC=3.3V
Logic-Low Input Voltage	Vil	DGND	-	0.3IOVCC	V	IOVCC=3.3V
Logic-High Output Voltage	Voh	IOVCC-0.4	-	IOVCC	V	IOVCC=3.3V
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	IOVCC=3.3V

8.2.3. DC Characteristics for Analog Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-voltage power	VGH	13	15		V	VCIP=3.3V
Negative High-voltage power	VGL	-11	-9		V	VCIP=3.3V
Output Voltage Deviation	Vod		±35		mV	
Standby Current	Isc		70		uA	VCI=VCIP=3.3V
Operation Current	Ioc		30		mA	No Load, VCI=IOVCC=VCIP=3.3V @ FR=60Hz

8.3. AC Characteristics

8.3.1. Parallel MCU 16/9/8-bit BUS



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 8.3.1 AC characteristics of parallel MCU in asynchronous mode

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
D/CX	T_{AST}	Address Setup Time	0		ns	
	T_{AHT}	Address Hold Time (W/R)	10		ns	
CSX	T_{CHW}	"S" "H" Pulse Width	25		ns	
	T_{CS}	Chip Select Setup Time(W)	10		ns	
	T_{RCS}	Chip Select Setup Time (Read ID)	45		ns	
	T_{RCSFM}	Chip Select Setup Time (Read FM)	355		ns	
	T_{CSF}	Chip Select Wait Time (W/R)	10		ns	

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
WRX	T_{WC}	Write Cycle	50		ns	MCU 16 Bit Format (5-6-5): Twc>100ns (see “6.4.8.”) MCU 16 Bit Format (6-6-6): Twc>66ns (see “6.4.9.” Figure 6.4.9.4) Other Format Twc>50ns
	T_{WRH}	Control Pulse H Duration	T_{WC} /2		ns	
	T_{WRL}	Control Pulse L Duration	T_{WC} /2		ns	
RDX	T_{RC}	Read Cycle(ID)	160		ns	When Read ID
	T_{RDH}	Control Pulse H Duration(ID)	T_{RC} /2		ns	
	T_{RDL}	Control Pulse L Duration(ID)	T_{RC} /2		ns	
RDX	T_{RCFM}	Read Cycle(FM)	450		ns	When Read From Frame Memory
	T_{RDHFM}	Control Pulse H Duration(FM)	T_{RCFM} /2		ns	
	T_{RDLFM}	Control Pulse L Duration(FM)	T_{RCFM} /2		ns	
DR[7:2], DG[7:2], DB[7:2]	T_{DST}	Data Setup Time	10		ns	CLmax=30pF Clmin=8pF
	T_{DHT}	Data Hold Time	10		ns	
	T_{RAT}	Read Access Time(ID)		40	ns	
	T_{RATFM}	Read Access Time(FM)		340	ns	
	T_{ODH}	Output Disable Time	20	80	ns	

Note 1: IOVCC 1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 °C (to +85°C no damage)
Note 2: This input signal rise time and fall time (Tr, Tf) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals

8.3.2. Display Serial Interface (SPI/Dual-SPI/Quad-SPI)

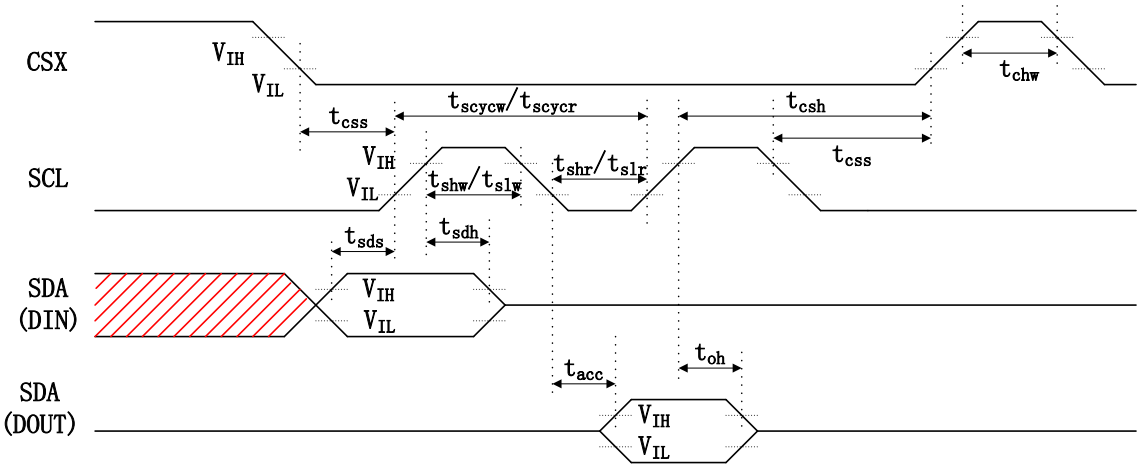


Table 8.3.2.1: Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
CSX	T_{CSS}	Chip Select Setup Time	10		ns	
	T_{CSH}	Chip Select Hold Time	30		ns	
	T_{CHW}	Chip Select "H" Pulse Width	30		ns	
SCL	T_{SCYCW}	Serial Clock Cycle(Write)	12.5		ns	QSPI 4 lane format (5-6-5): T_{SCYCW} >25ns (see "6.4.12.") QSPI 4 lane format (6-6-6): T_{SCYCW} >16ns(see "6.4.13") Other Format T_{SCYCW} >12.5ns
	T_{SHW}	S"L" "H" Pulse Width(Write)	T_{SCYCW} /2		ns	
	T_{SLW}	S"L" "L" Pulse Width(Write)	T_{SCYCW} /2		ns	
	T_{SCYCR}	Serial Clock Cycle(Read)	150		ns	
	T_{SHR}	S"L" "H" Pulse Width(Read)	T_{SCYCR} /2		ns	
	T_{SLR}	S"L" "L" Pulse Width(Read)	T_{SCYCR} /2		ns	
SDA(DIN) /(DOUT)	T_{SDS}	Data Setup Time	5		ns	
	T_{SDH}	Data Hold Time	5		ns	
	T_{ACC}	Access Time	5	50	ns	CLmax=30pF CLmin=8pF
	T_{OH}	Output Disable Time	10		ns	

Note 1: IOVCC=1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70℃ (to +85℃ no damage)
Note 2: The input signal rise time and fall time(Tr, Tf) is specified at 15 ns or less. Logic high and low levels are specified as 10% and 90% of IOVCC for Input signals.

Table 8.3.2.2: 4 wire Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
CSX	T_{CSS}	Chip Select Setup Time	10		ns	
	T_{CSH}	Chip Select Hold Time	30		ns	
	T_{CHW}	Chip Select “H” Pulse Width	30		ns	
SCL	T_{SCYCW}	Serial Clock Cycle(Write)	12.5		ns	
	T_{SHW}	S “L” “H” Pulse Width(Write)	T_{SCYCW} /2		ns	
	T_{SLW}	S “L” “L” Pulse Width(Write)	T_{SCYCW} /2		ns	
	T_{SCYCR}	Serial Clock Cycle(Read)	150		ns	
	T_{SHR}	S “L” “H” “Pulse Width(Read)	T_{SCYCR} /2		ns	
	T_{SLR}	S“L” “L” Pulse Width(Read)	T_{SCYCR} /2		ns	
D/CX	T_{DCS}	D/CX Setup Time	5		ns	
	T_{DCH}	D/CX Hold Time	5		ns	
SDA(DIN) (DOUT)	T_{SDS}	Data Setup Time	5		ns	
	T_{SDH}	Data Hold Time	5		ns	
	T_{ACC}	Access Time	5	50	ns	CLmax=30pF CLmin=8pF
	T_{OH}	Output Disable Time	10		ns	

Note 1: IOVCC=1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70℃ (to +85℃ no damage)
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 10% and 90% of IOVCC for Input signals.

8.3.3. Parallel RGB 18/16/6-bit BUS

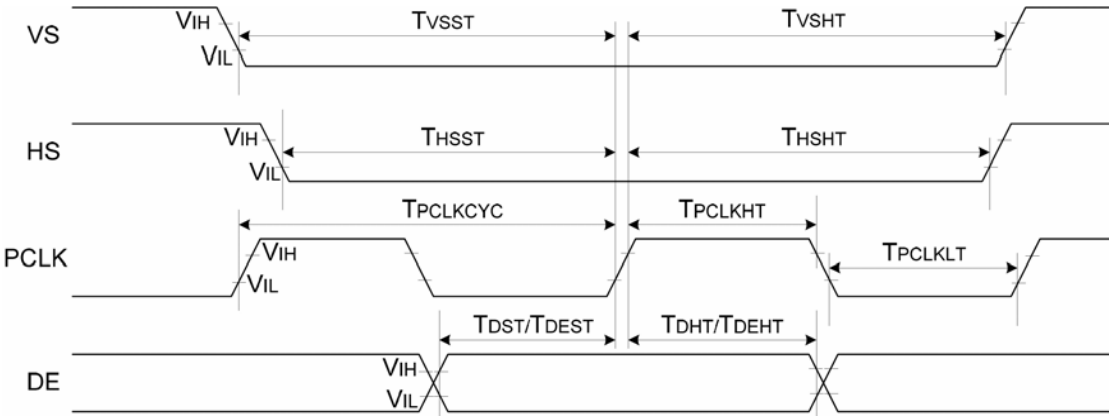


Table 8.3.3.1 Parallel 18-bit RGB Interface Charateristics

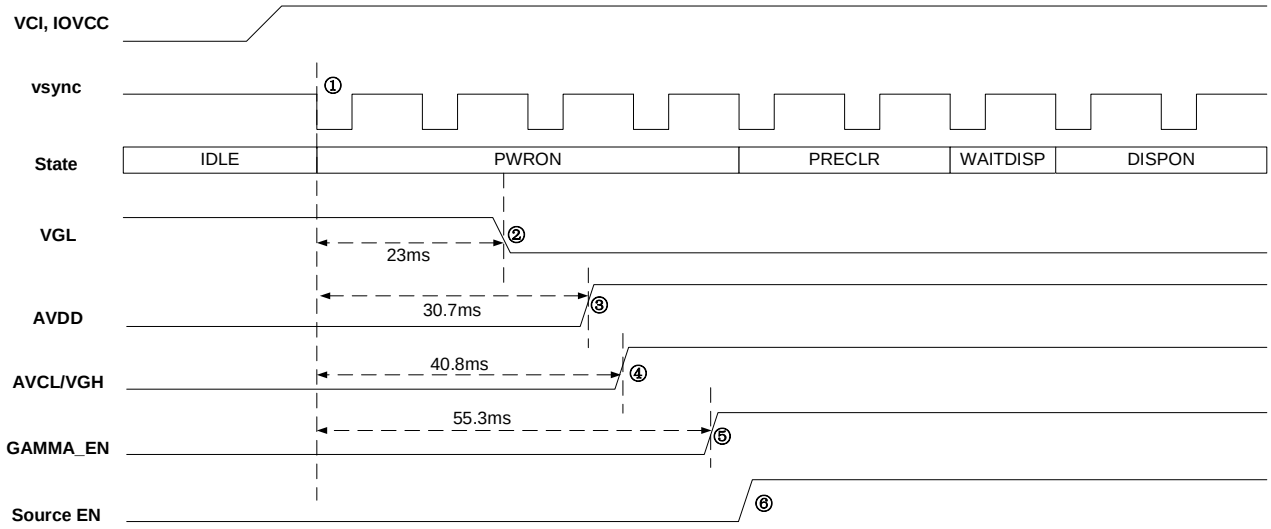
Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
PCLK	$T_{PCLKCYC}$	TPCLK Cycle Time	100	-	ns	
	T_{PCLKLT}	Pixel Low Pulse Width	$T_{PCLKCYC}$ /2	-	ns	
	T_{PCLKHT}	Pixel High Pulse Width	$T_{PCLKCYC}$ /2	-	ns	
VS	T_{VSST}	Vertical Sync.setup time	15	-	ns	
	T_{VSHT}	Vertical Sync.hold time	15	-	ns	
HS	T_{HSST}	Horizontal Sync.setup time	15	-	ns	
	T_{HSHT}	Horizontal Sync.hold time	15	-	ns	
DE	T_{DEST}	Data Enable Setup Time	15	-	ns	
	T_{DEHT}	Data Enable Hold Time	15	-	ns	
DR[7:2], DG[7:2], DB[7:2]	T_{DST}	Data Setup Time	15	-	ns	
	T_{DHT}	Data Hold Time	15	-	ns	

Table 8.3.3.2 Serial 6-bit RGB Interface Charateristics

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
PCLK	$T_{PCLKCYC}$	TPCLK Cycle Time	33	-	ns	
	T_{PCLKLT}	Pixel Low Pulse Width	$T_{PCLKCYC}$ /2	-	ns	
	T_{PCLKHT}	Pixel High Pulse Width	$T_{PCLKCYC}$ /2	-	ns	
VS	T_{VSST}	Vertical Sync.setup time	15	-	ns	
	T_{VSHT}	Vertical Sync.hold time	15	-	ns	
HS	T_{HSST}	Horizontal Sync.setup time	15	-	ns	
	T_{HSHT}	Horizontal Sync.hold time	15	-	ns	
DE	T_{DEST}	Data Enable Setup Time	15	-	ns	
	T_{DEHT}	Data Enable Hold Time	15	-	ns	
DR[7:2], DG[7:2], DB[7:2]	T_{DST}	Data Setup Time	15	-	ns	
	T_{DHT}	Data Hold Time	15	-	ns	

9. Power on/off sequence

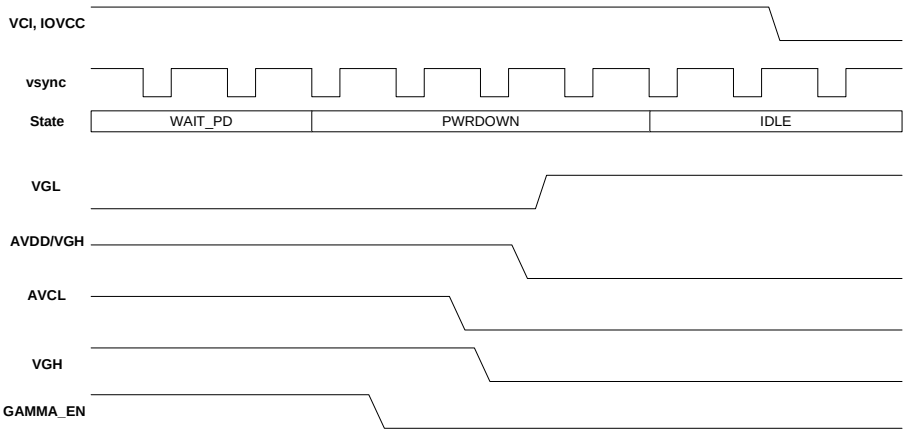
9.1. Power On Sequence



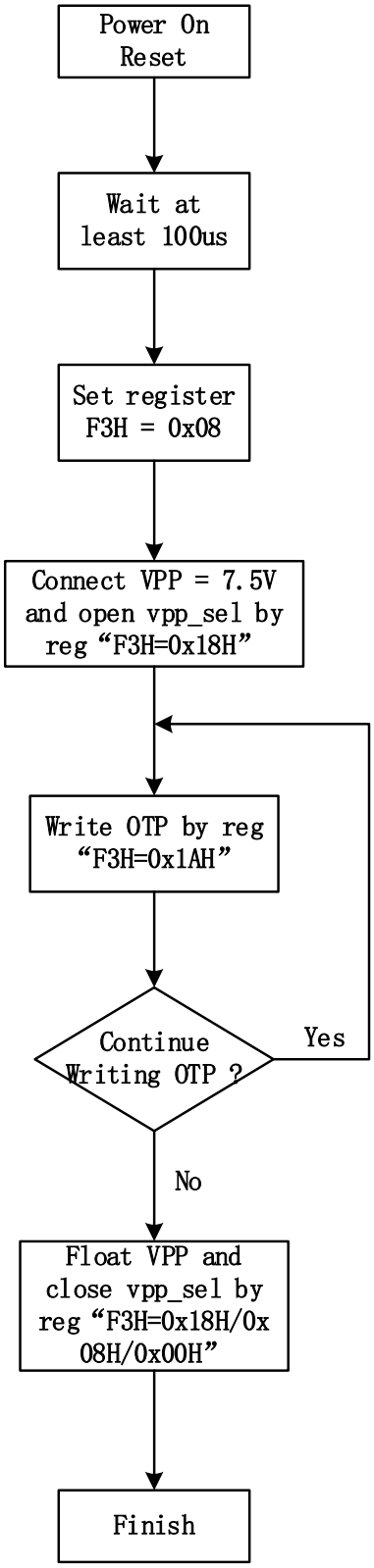
No.	Description	Min. Time
1	After VCI/IOVCC become stable , reset finished and host send command “11H”	Decide by host 11H command
2	VGL from 0V to -11.5V	23ms
3	AVDD from VCI to 6.6V	30.7ms
4	AVCL from 0 to -5V and VGH from AVDD to 15.4	40.8ms
5	Gamma output enable	55.3ms
6	Source output enable	Decide by host “29H” command

9.2. Power Off Sequence

When host sends “10H” command, State from WAIT_PD to PWRDOWN, in which power disabled sequentially.



10. OTP Flow


Power On Reset
Wait at least 100us
Set register F3H = 0x08
Connect VPP = 7.5V and open vpp_sel by reg “F3H=0x18H”
Write OTP by reg “F3H=0x1AH”
Continue Writing OTP ?
Yes
No
Float VPP and close vpp_sel by reg “F3H=0x18H/0x08H/0x00H”
Finish

Step 1: Attach LCD module on OTP programming machine.

LCD module condition	
VCI(V)	3.3
VPP(V)	7.5

Step 2: Initialize the non-programmed module by software.

Function	W/R	CMD	Par	Note
HW reset				HW reset sequence
Waiting 100ms				
Display On LCD Module				Refer Power On Sequence
Display Check Pattern				Recommend Flicker Pattern
Enable Command 1	W	F3	08	
Adjust VCOM	W	40	XX	Fine tune VMF to reduce flicker

Step 3: Check the image quality of display module. If flicker can be still observed on the panel, repeat the command 40h until the flicker disappearance.

Step 4: Read Optimization VCOM Value

Function	W/R	CMD	Par	Note
Read Optimization VMF	R	40		VMF=Read(0x40);
Waiting 100ms				

Step 5: HW reset LCD Module

Function	W/R	CMD	Par	Note
HW reset				HW reset sequence
Waiting 20ms				

Step 6: Hardware setting

Action	Note
RGB signal OFF	
External Power 7.5V to VPP Pin	

Step 7: Enable OTP programming Mode and parameter setup

Function	W/R	CMD	Par	Note
Enable Command 2	W	F3	18	
Waiting 5ms				

Step 8: Program OTP.

Function	W/R	CMD	Par	Note
OTP Write Command	W	F3	1A	Program OTP
Waiting 320000ms				

Step 9: Hardware setting

Action	Note
Remove 7.5V form VPP Pin	

Step 10: Disable OTP programming Mode.

Function	W/R	CMD	Par	Note
Disable OTP Programming Mode	W	F3	18	
Waiting 5ms				
Disable OTP Programming Mode	W	F3	08	
Waiting 20ms				
Disable OTP Programming Mode	W	F3	00	
Waiting 15000ms				

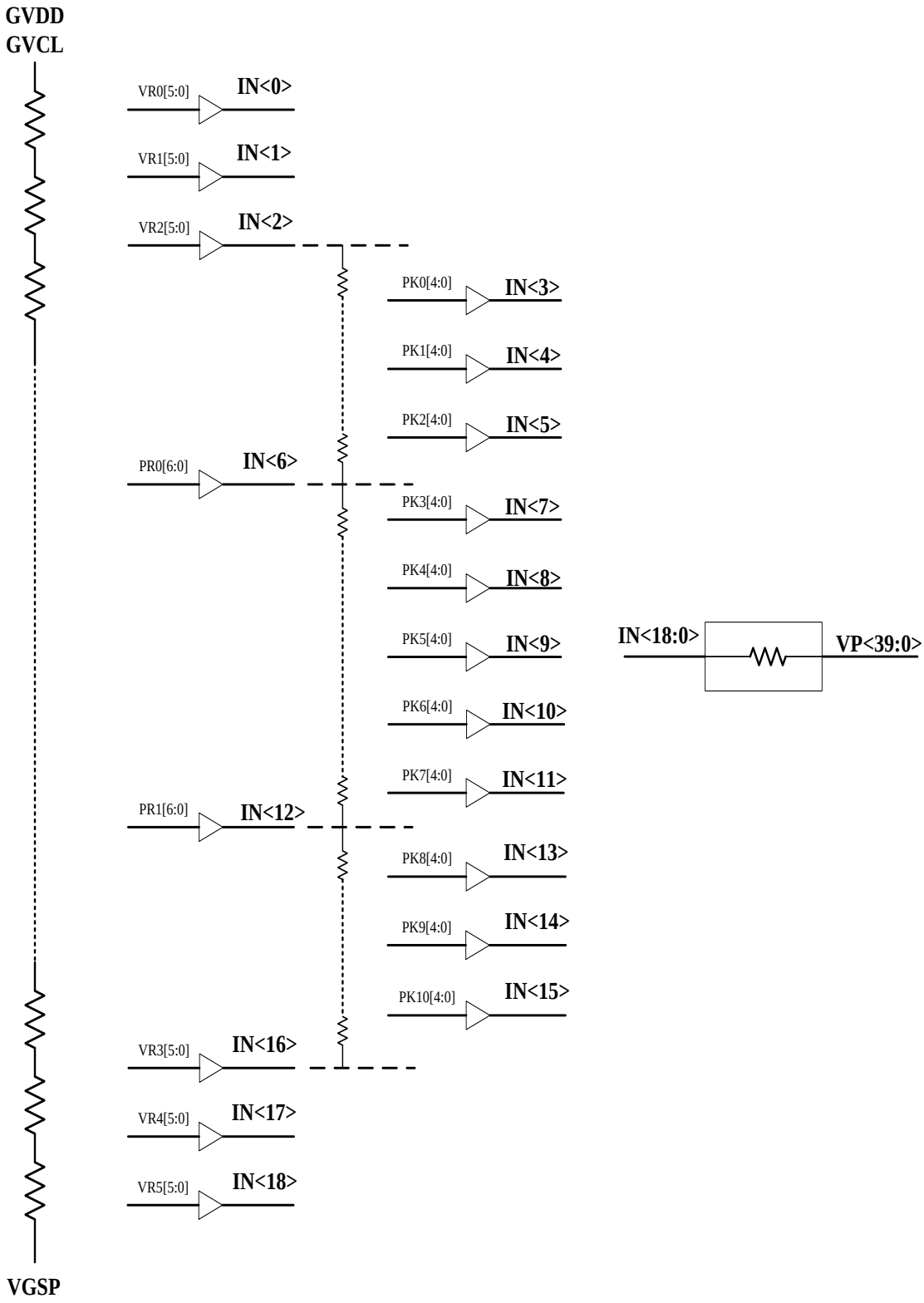
Step 11: Turn off VCI and IOVCC, waiting for 200ms then and turn on again.

Step 12: Execute normal display on sequence.

Function	W/R	CMD	Par	Note
HW reset				HW reset sequence
Waiting 100ms				
Display On LCD Module				Refer Power On Sequence
Display Check Pattern				Recommend Flicker Pattern

Step 13: Check the image quality.

11. Gamma Structure



12. Recommended panel routing resistance

The recommended wiring resistance values are given below. The wiring resistance values affect the current capability of the power supply blocks and thus must be designed within the given range.

Item	Pin Name	Unit: ohm
1	VPP	<3
2	GVDD	<50
3	GVCL	<50
4	VGSP	<50
5	VCOM	<3
6	DGND	<3
7	DVDD	<50
8	IOVCC	<3
9	VCI	<3
10	VSYNC	<50
11	HSYNC	<50
12	DCLK	<50
13	VDPOL	<50
14	HDPOL	<50
15	DCLKPOL	<50
16	SBGR	<50
17	DE	<50
18	PARA_SERI	<50
19	RDX	<50
20	HDIR	<50
21	VDIR	<50
22	CS	<50

Item	Pin Name	Unit: ohm
23	SDA	<50
24	WRX	<50
25	DISP	<50
26	GRB	<50
27	SYNC	<50
28	DR7-DR2	<50
29	DG7-DG2	<50
30	DB7-DB2	<50
31	DCX	<50
32	TE	<50
33	DR0	<50
34	IM<0>	<50
35	IM<1>	<50
36	IM<2>	<50
37	SPI4W	<50
38	AGND	<3
39	AVCL	<50
40	AVDD	<50
41	PGND	<3
42	VCIP	<3
43	VGH	<50
44	VGL	<50

13. Revision history

Revision	Description	Date
1.0	Frist Release	8/8/2022
1.1	2 nd Release	9/21/2022
1.2	3 th Release	10/10/2022