SH1126

384 X 96 16 Grayscale
Dot Matrix OLED/PLED Driver with Controller

Features

- Support maximum 384 X 96 dot matrix panel with 16 grayscale
- Embedded 384 X 96 X 4bits SRAM
- Operating voltage:
  - I/O voltage supply: V_{DD1} = 1.65V - 3.5V
  - Logic voltage supply: V_{DD2} = 1.65V - 3.5V
    $V_{DD1} = V_{DD2}$
  - DC-DC voltage supply: AV_{DD} = 2.4V - 3.5V
  - OLED Operating voltage supply: V_{PP} = 7.0V -14V
- Maximum segment output current: 500μA
- Maximum common sink current: 192mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, 3 wire/4 wire serial peripheral interface
- 400KHZ fast I^2C bus interface
- Programmable frame frequency and multiplexing ratio
- Row re-mapping and column re-mapping (ADC)
- Vertical scrolling
- On-chip oscillator
- Available internal DC-DC converter
- 256-step contrast control on monochrome passive OLED panel
- Low power consumption
  - Sleep mode: < 5μA
- Wide range of operating temperatures: -40 to +85°C
- Available in COG form

General Description

SH1126 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SH1126 consists of 384 segments, 96 commons with 16 grayscale that can support a maximum display resolution of 384 X 96. It is designed for Common Cathode type OLED panel.

SH1126 embeds with contrast control, display RAM oscillator and efficient DC-DC converter, which reduces the number of external components and power consumption. SH1126 is suitable for a wide range of compact portable applications, such as car audio, and calculator, etc.

Block Diagram

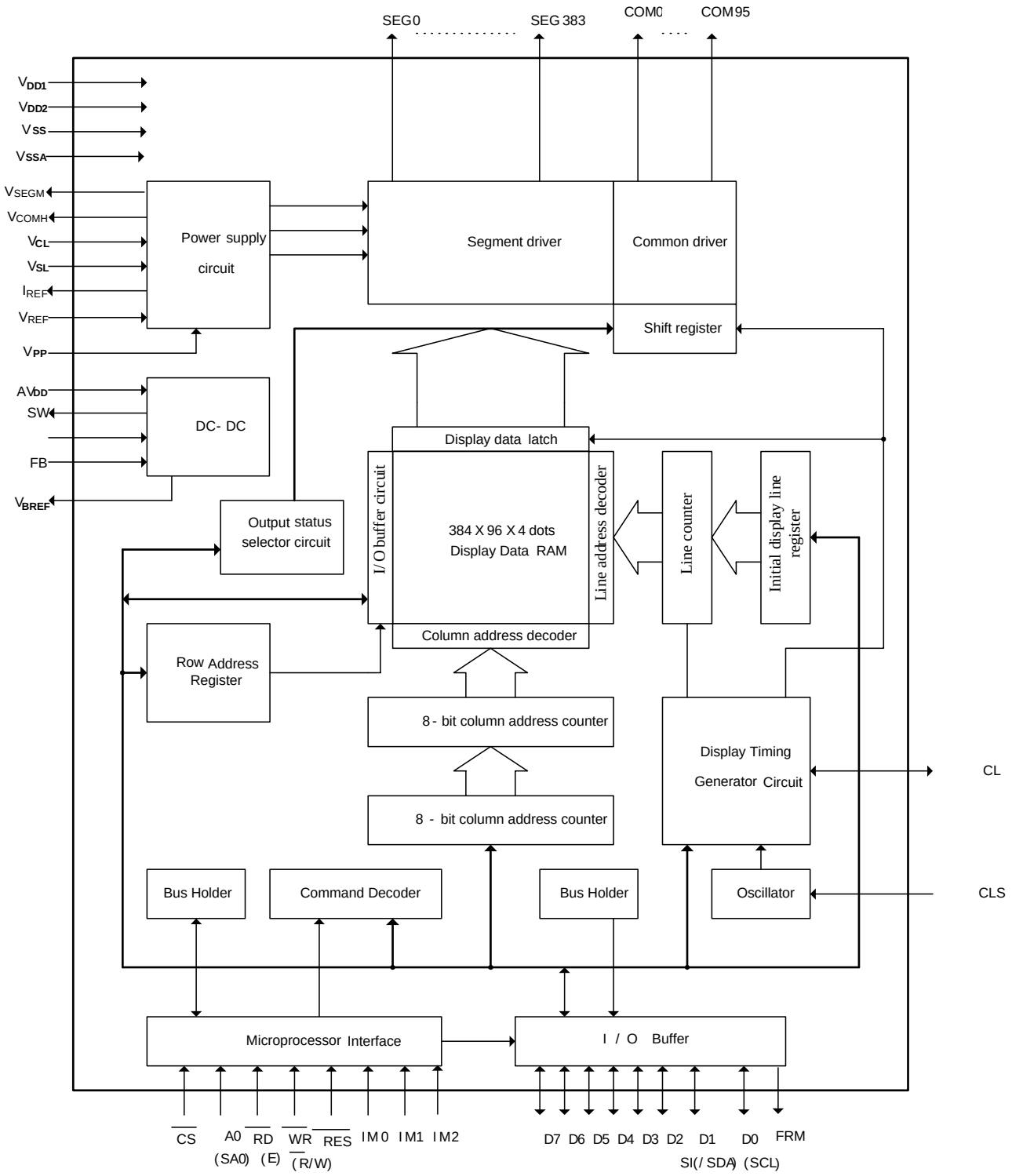


Figure 1 SH1126 Block Diagram

Pad Description

Power Supply

Pad No.	Symbol	I/O	Description
71,72	V_{DD2}	Supply	1.65 - 3.5V power supply input pad for logic
78,79	V_{DD1}	Supply	1.65 - 3.5V power supply input pad
74	V_{DD1}	Supply	1.65 - 3.5V power supply output for pad option
66,67	AV_{DD}	Supply	2.4 - 3.5V power supply pad for the internal buffer of the DC-DC voltage converter
54	V_{SSA}	Supply	Ground for VSL.
55~57	V_{SS}	Supply	Ground for analog, logic&buffer respectively.
76,81	V_{SS}	Supply	Ground output for pad option
16~19,50~53, 100~103	V_{PP}	Supply	This is the most positive voltage supply pad of the chip It should be supplied externally
40~42	V_{SL}	Supply	This is a segment voltage reference pad A capacitor should be connected between this pad and V_{SS}
58~64	V_{CL}	Supply	This is a common voltage reference pad This pad should be connected to V_{SS} externally

OLED Driver Supplies

Pad No.	Symbol	I/O	Description
43,44	V_{REF}	I	This is a voltage reference pad for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can either be supplied externally or by connecting to V_{PP}.
48,49	I_{REF}	O	This is a segment current reference pad A resistor should be connected between this pad and V_{SS}. Set the current at 15.625μA
37~39	V_{COMH}	O	This is a pad for the voltage output high level for common signals A capacitor should be connected between this pad and V_{SS}
34~36	V_{SEGM}	O	This is a pad for the voltage output level for segment pre-charge. A capacitor should be connected between this pad and V_{SS}.
70	SW	O	This is an output pad driving the gate of the external NMOS of the booster circuit
68	FB	I	This is a feedback resistor input pad for the booster circuit It is used to adjust the booster output voltage level, V_{PP}
65	SENSE	I	This is a source current pad of the external NMOS of the booster circuit
69	V_{BREF}	O	This is an internal voltage reference pad for booster circuit

System Bus Connection Pads

<table>
<tr><th>Pad No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>87</td><td>CL</td><td>I/O</td><td>This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source.</td></tr>
<tr><td>73</td><td>CLS</td><td>I</td><td>This is the internal clock enable pad.
CLS = “H”: Internal oscillator circuit is enabled.
CLS = “L”: Internal oscillator circuit is disabled (requires external input).
When CLS = “L”, an external clock source must be connected to the CL pad for normal operation.</td></tr>
<tr><td>75
77
80</td><td>IM0
IM1
IM2</td><td>I</td><td>These are the MPU interface mode select pads.
<table>
<tr><th></th><th>8080</th><th>I²C</th><th>6800</th><th>4-wire SPI</th><th>3-wire SPI</th></tr>
<tr><td>IM0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>IM1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>IM2</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>82</td><td>$\overline{CS}$</td><td>I</td><td>This pad is the chip select input. When $\overline{CS}$ = “L”, then the chip select becomes active, and data/command I/O is enabled.</td></tr>
<tr><td>83</td><td>$\overline{RES}$</td><td>I</td><td>This is a reset signal input pad. When $\overline{RES}$ is set to “L”, the settings are initialized.
The reset operation is performed by the $\overline{RES}$ signal level.</td></tr>
<tr><td>84</td><td>A0
(SA0)</td><td>I</td><td>This is the Data/Command control pad that determines whether the data bits are a data or a command.
A0 = “H”: the inputs at D0 to D7 are treated as display data.
A0 = “L”: the inputs at D0 to D7 are transferred to the command registers.
In I²C interface, this pad serves as SA0 to distinguish the different address of OLED driver.</td></tr>
<tr><td>85</td><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
When connected to a 6800 Series MPU: This is the read/write control signal input terminal.
When R/$\overline{W}$ = “H”: Read.
When R/$\overline{W}$ = “L”: Write.</td></tr>
<tr><td>86</td><td>$\overline{RD}$
(E)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 series MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080 series MPU, and the SH1126 data bus is in an output status when this signal is “L”.
When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.</td></tr>
<tr><td>92~99</td><td>D0 - D7
(SCL)
(SI /SDA)</td><td>I/O
I
I</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance.
When the I2C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDA). At this time, D2 to D7 are set to high impedance.
When the chip select is inactive, D0 to D7 are set to high impedance.</td></tr>
<tr><td>91</td><td>FRM</td><td>O</td><td>This pad is No Connection pad. Its signal varies with the frame frequency. Its voltage is equal to VDD1 when the last common output of every frame is active, and is equal to Vss during other time.</td></tr>
</table>

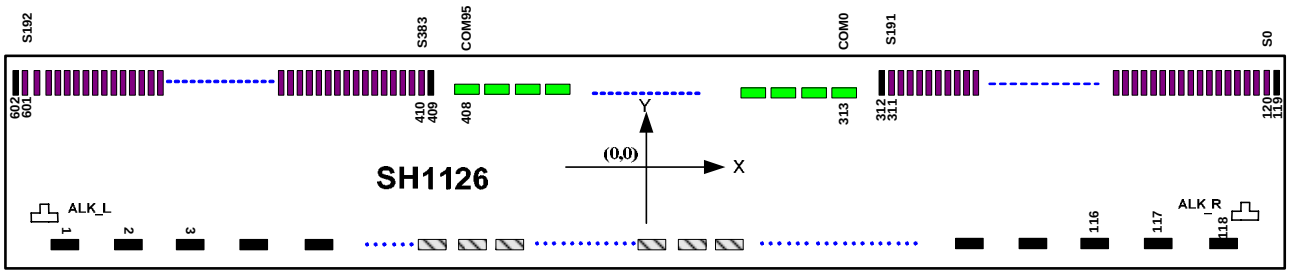
OLED Drive Pads

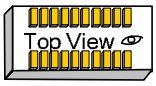
Pad No.	Symbol	I/O	Description
313~408	COM0 – 95	O	These pads are Common signal output for OLED display.
120~311, 601~410	SEG0 – 383	O	These pads are Segment signal output for OLED display.

Test Pads

Pad No.	Symbol	I/O	Description
88	TEST1	I	Test pads, internal pull low, no connection for user.
89	TEST2	O	Test pads, no connection for user.
90	TEST3	I	Test pads, no connection for user.
1~15,20~33,45~47,104~119,312, 409,602	Dummy	-	NC pads, no connection for user.

Pad Configuration





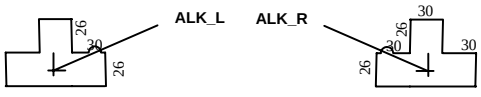
Chip Outline Dimensions

Item	Pad No.	Size (μm)	
		X	Y
Chip boundary	-	24244+18	1034+18
Chip height	All pads	300	
Bump size	I/O	110	40
	SEG	26	70
	COM	64	39
	Dummy (No.119,312,409,602)	26	70
	Dummy (No.1~15,20~33,45~47,104~118)	110	40
Pad pitch	COM	80	
	SEG	41	
	I/O	130 & 195 & 260	
Bump height	All pads	9±2	

Alignment Mark Location

Unit: μm

NO	X	Y
ALK_L	-11956	-355
ALK_R	11956	-355



Pad location (Total: 602pads)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	DUMMY	-11872	-421	82	CSB	3552	-421	163	SEG[43]	10251	419.5	244	SEG[124]	6848	419.5
2	DUMMY	-11612	-421	83	RESB	3812	-421	164	SEG[44]	10210	419.5	245	SEG[125]	6807	419.5
3	DUMMY	-11352	-421	84	A0	4072	-421	165	SEG[45]	10169	419.5	246	SEG[126]	6766	419.5
4	DUMMY	-11092	-421	85	WRB	4332	-421	166	SEG[46]	10128	419.5	247	SEG[127]	6725	419.5
5	DUMMY	-10832	-421	86	RDB	4592	-421	167	SEG[47]	10087	419.5	248	SEG[128]	6684	419.5
6	DUMMY	-10572	-421	87	CL	4787	-421	168	SEG[48]	10046	419.5	249	SEG[129]	6643	419.5
7	DUMMY	-10312	-421	88	TEST1	4917	-421	169	SEG[49]	10005	419.5	250	SEG[130]	6602	419.5
8	DUMMY	-10052	-421	89	TEST2	5047	-421	170	SEG[50]	9964	419.5	251	SEG[131]	6561	419.5
9	DUMMY	-9792	-421	90	TEST3	5177	-421	171	SEG[51]	9923	419.5	252	SEG[132]	6520	419.5
10	DUMMY	-9532	-421	91	FRM	5372	-421	172	SEG[52]	9882	419.5	253	SEG[133]	6479	419.5
11	DUMMY	-9272	-421	92	D[0]	5632	-421	173	SEG[53]	9841	419.5	254	SEG[134]	6438	419.5
12	DUMMY	-9012	-421	93	D[1]	5892	-421	174	SEG[54]	9800	419.5	255	SEG[135]	6397	419.5
13	DUMMY	-8752	-421	94	D[2]	6152	-421	175	SEG[55]	9759	419.5	256	SEG[136]	6356	419.5
14	DUMMY	-8492	-421	95	D[3]	6412	-421	176	SEG[56]	9718	419.5	257	SEG[137]	6315	419.5
15	DUMMY	-8232	-421	96	D[4]	6672	-421	177	SEG[57]	9677	419.5	258	SEG[138]	6274	419.5
16	VPP	-8037	-421	97	D[5]	6932	-421	178	SEG[58]	9636	419.5	259	SEG[139]	6233	419.5
17	VPP	-7907	-421	98	D[6]	7192	-421	179	SEG[59]	9595	419.5	260	SEG[140]	6192	419.5
18	VPP	-7777	-421	99	D[7]	7452	-421	180	SEG[60]	9554	419.5	261	SEG[141]	6151	419.5
19	VPP	-7647	-421	100	VPP	7647	-421	181	SEG[61]	9513	419.5	262	SEG[142]	6110	419.5
20	DUMMY	-7452	-421	101	VPP	7777	-421	182	SEG[62]	9472	419.5	263	SEG[143]	6069	419.5
21	DUMMY	-7192	-421	102	VPP	7907	-421	183	SEG[63]	9431	419.5	264	SEG[144]	6028	419.5
22	DUMMY	-6932	-421	103	VPP	8037	-421	184	SEG[64]	9390	419.5	265	SEG[145]	5987	419.5
23	DUMMY	-6672	-421	104	DUMMY	8232	-421	185	SEG[65]	9349	419.5	266	SEG[146]	5946	419.5
24	DUMMY	-6412	-421	105	DUMMY	8492	-421	186	SEG[66]	9308	419.5	267	SEG[147]	5905	419.5
25	DUMMY	-6152	-421	106	DUMMY	8752	-421	187	SEG[67]	9267	419.5	268	SEG[148]	5864	419.5
26	DUMMY	-5892	-421	107	DUMMY	9012	-421	188	SEG[68]	9226	419.5	269	SEG[149]	5823	419.5
27	DUMMY	-5632	-421	108	DUMMY	9272	-421	189	SEG[69]	9185	419.5	270	SEG[150]	5782	419.5
28	DUMMY	-5372	-421	109	DUMMY	9532	-421	190	SEG[70]	9144	419.5	271	SEG[151]	5741	419.5
29	DUMMY	-5112	-421	110	DUMMY	9792	-421	191	SEG[71]	9103	419.5	272	SEG[152]	5700	419.5
30	DUMMY	-4852	-421	111	DUMMY	10052	-421	192	SEG[72]	9062	419.5	273	SEG[153]	5659	419.5
31	DUMMY	-4592	-421	112	DUMMY	10312	-421	193	SEG[73]	9021	419.5	274	SEG[154]	5618	419.5
32	DUMMY	-4332	-421	113	DUMMY	10572	-421	194	SEG[74]	8980	419.5	275	SEG[155]	5577	419.5
33	DUMMY	-4053	-421	114	DUMMY	10832	-421	195	SEG[75]	8939	419.5	276	SEG[156]	5536	419.5
34	VSEGM	-3923	-421	115	DUMMY	11092	-421	196	SEG[76]	8898	419.5	277	SEG[157]	5495	419.5
35	VSEGM	-3793	-421	116	DUMMY	11352	-421	197	SEG[77]	8857	419.5	278	SEG[158]	5454	419.5
36	VSEGM	-3663	-421	117	DUMMY	11612	-421	198	SEG[78]	8816	419.5	279	SEG[159]	5413	419.5
37	VCOMH	-3533	-421	118	DUMMY	11872	-421	199	SEG[79]	8775	419.5	280	SEG[160]	5372	419.5
38	VCOMH	-3403	-421	119	DUMMY	12055	419.5	200	SEG[80]	8734	419.5	281	SEG[161]	5331	419.5
39	VCOMH	-3273	-421	120	SEG[0]	12014	419.5	201	SEG[81]	8693	419.5	282	SEG[162]	5290	419.5
40	VSL	-3143	-421	121	SEG[1]	11973	419.5	202	SEG[82]	8652	419.5	283	SEG[163]	5249	419.5
41	VSL	-3013	-421	122	SEG[2]	11932	419.5	203	SEG[83]	8611	419.5	284	SEG[164]	5208	419.5
42	VSL	-2883	-421	123	SEG[3]	11891	419.5	204	SEG[84]	8570	419.5	285	SEG[165]	5167	419.5
43	VREF	-2753	-421	124	SEG[4]	11850	419.5	205	SEG[85]	8529	419.5	286	SEG[166]	5126	419.5
44	VREF	-2623	-421	125	SEG[5]	11809	419.5	206	SEG[86]	8488	419.5	287	SEG[167]	5085	419.5
45	DUMMY	-2428	-421	126	SEG[6]	11768	419.5	207	SEG[87]	8447	419.5	288	SEG[168]	5044	419.5
46	DUMMY	-2168	-421	127	SEG[7]	11727	419.5	208	SEG[88]	8406	419.5	289	SEG[169]	5003	419.5
47	DUMMY	-1908	-421	128	SEG[8]	11686	419.5	209	SEG[89]	8365	419.5	290	SEG[170]	4962	419.5
48	IREF	-1713	-421	129	SEG[9]	11645	419.5	210	SEG[90]	8324	419.5	291	SEG[171]	4921	419.5
49	IREF	-1583	-421	130	SEG[10]	11604	419.5	211	SEG[91]	8283	419.5	292	SEG[172]	4880	419.5
50	VPP	-1453	-421	131	SEG[11]	11563	419.5	212	SEG[92]	8242	419.5	293	SEG[173]	4839	419.5
51	VPP	-1323	-421	132	SEG[12]	11522	419.5	213	SEG[93]	8201	419.5	294	SEG[174]	4798	419.5
52	VPP	-1193	-421	133	SEG[13]	11481	419.5	214	SEG[94]	8160	419.5	295	SEG[175]	4757	419.5
53	VPP	-1063	-421	134	SEG[14]	11440	419.5	215	SEG[95]	8119	419.5	296	SEG[176]	4716	419.5
54	VSSA	-933	-421	135	SEG[15]	11399	419.5	216	SEG[96]	7996	419.5	297	SEG[177]	4675	419.5
55	VSS(ana)	-803	-421	136	SEG[16]	11358	419.5	217	SEG[97]	7955	419.5	298	SEG[178]	4634	419.5
56	VSS(logic)	-673	-421	137	SEG[17]	11317	419.5	218	SEG[98]	7914	419.5	299	SEG[179]	4593	419.5
57	VSS(buf)	-543	-421	138	SEG[18]	11276	419.5	219	SEG[99]	7873	419.5	300	SEG[180]	4552	419.5
58	VCL	-413	-421	139	SEG[19]	11235	419.5	220	SEG[100]	7832	419.5	301	SEG[181]	4511	419.5
59	VCL	-283	-421	140	SEG[20]	11194	419.5	221	SEG[101]	7791	419.5	302	SEG[182]	4470	419.5
60	VCL	-153	-421	141	SEG[21]	11153	419.5	222	SEG[102]	7750	419.5	303	SEG[183]	4429	419.5
61	VCL	-23	-421	142	SEG[22]	11112	419.5	223	SEG[103]	7709	419.5	304	SEG[184]	4388	419.5
62	VCL	107	-421	143	SEG[23]	11071	419.5	224	SEG[104]	7668	419.5	305	SEG[185]	4347	419.5
63	VCL	237	-421	144	SEG[24]	11030	419.5	225	SEG[105]	7627	419.5	306	SEG[186]	4306	419.5
64	VCL	367	-421	145	SEG[25]	10989	419.5	226	SEG[106]	7586	419.5	307	SEG[187]	4265	419.5
65	SENSE	562	-421	146	SEG[26]	10948	419.5	227	SEG[107]	7545	419.5	308	SEG[188]	4224	419.5
66	AVDD	757	-421	147	SEG[27]	10907	419.5	228	SEG[108]	7504	419.5	309	SEG[189]	4183	419.5
67	AVDD	887	-421	148	SEG[28]	10866	419.5	229	SEG[109]	7463	419.5	310	SEG[190]	4142	419.5
68	FB	1017	-421	149	SEG[29]	10825	419.5	230	SEG[110]	7422	419.5	311	SEG[191]	4101	419.5
69	VBREF	1147	-421	150	SEG[30]	10784	419.5	231	SEG[111]	7381	419.5	312	DUMMY	4060	419.5
70	SW	1342	-421	151	SEG[31]	10743	419.5	232	SEG[112]	7340	419.5	313	COM[0]	3880	384.5
71	VDD2	1537	-421	152	SEG[32]	10702	419.5	233	SEG[113]	7299	419.5	314	COM[1]	3800	384.5
72	VDD2	1667	-421	153	SEG[33]	10661	419.5	234	SEG[114]	7258	419.5	315	COM[2]	3720	384.5
73	CLS	1862	-421	154	SEG[34]	10620	419.5	235	SEG[115]	7217	419.5	316	COM[3]	3640	384.5
74	VDD1	2057	-421	155	SEG[35]	10579	419.5	236	SEG[116]	7176	419.5	317	COM[4]	3560	384.5
75	IM0	2252	-421	156	SEG[36]	10538	419.5	237	SEG[117]	7135	419.5	318	COM[5]	3480	384.5
76	VSS	2447	-421	157	SEG[37]	10497	419.5	238	SEG[118]	7094	419.5	319	COM[6]	3400	384.5
77	IM1	2642	-421	158	SEG[38]	10456	419.5	239	SEG[119]	7053	419.5	320	COM[7]	3320	384.5
78	VDD1	2837	-421	159	SEG[39]	10415	419.5	240	SEG[120]	7012	419.5	321	COM[8]	3240	384.5
79	VDD1	2967	-421	160	SEG[40]	10374	419.5	241	SEG[121]	6971	419.5	322	COM[9]	3160	384.5
80	IM2	3162	-421	161	SEG[41]	10333	419.5	242	SEG[122]	6930	419.5	323	COM[10]	3080	384.5
81	VSS	3357	-421	162	SEG[42]	10292	419.5	243	SEG[123]	6889	419.5	324	COM[11]	3000	384.5

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
325	COM[12]	2920	384.5	406	COM[93]	-3720	384.5	487	SEG[306]	-7258	419.5	568	SEG[225]	-10661	419.5
326	COM[13]	2840	384.5	407	COM[94]	-3800	384.5	488	SEG[305]	-7299	419.5	569	SEG[224]	-10702	419.5
327	COM[14]	2760	384.5	408	COM[95]	-3880	384.5	489	SEG[304]	-7340	419.5	570	SEG[223]	-10743	419.5
328	COM[15]	2680	384.5	409	DUMMY	-4060	419.5	490	SEG[303]	-7381	419.5	571	SEG[222]	-10784	419.5
329	COM[16]	2600	384.5	410	SEG[383]	-4101	419.5	491	SEG[302]	-7422	419.5	572	SEG[221]	-10825	419.5
330	COM[17]	2520	384.5	411	SEG[382]	-4142	419.5	492	SEG[301]	-7463	419.5	573	SEG[220]	-10866	419.5
331	COM[18]	2440	384.5	412	SEG[381]	-4183	419.5	493	SEG[300]	-7504	419.5	574	SEG[219]	-10907	419.5
332	COM[19]	2360	384.5	413	SEG[380]	-4224	419.5	494	SEG[299]	-7545	419.5	575	SEG[218]	-10948	419.5
333	COM[20]	2280	384.5	414	SEG[379]	-4265	419.5	495	SEG[298]	-7586	419.5	576	SEG[217]	-10989	419.5
334	COM[21]	2200	384.5	415	SEG[378]	-4306	419.5	496	SEG[297]	-7627	419.5	577	SEG[216]	-11030	419.5
335	COM[22]	2120	384.5	416	SEG[377]	-4347	419.5	497	SEG[296]	-7668	419.5	578	SEG[215]	-11071	419.5
336	COM[23]	2040	384.5	417	SEG[376]	-4388	419.5	498	SEG[295]	-7709	419.5	579	SEG[214]	-11112	419.5
337	COM[24]	1960	384.5	418	SEG[375]	-4429	419.5	499	SEG[294]	-7750	419.5	580	SEG[213]	-11153	419.5
338	COM[25]	1880	384.5	419	SEG[374]	-4470	419.5	500	SEG[293]	-7791	419.5	581	SEG[212]	-11194	419.5
339	COM[26]	1800	384.5	420	SEG[373]	-4511	419.5	501	SEG[292]	-7832	419.5	582	SEG[211]	-11235	419.5
340	COM[27]	1720	384.5	421	SEG[372]	-4552	419.5	502	SEG[291]	-7873	419.5	583	SEG[210]	-11276	419.5
341	COM[28]	1640	384.5	422	SEG[371]	-4593	419.5	503	SEG[290]	-7914	419.5	584	SEG[209]	-11317	419.5
342	COM[29]	1560	384.5	423	SEG[370]	-4634	419.5	504	SEG[289]	-7955	419.5	585	SEG[208]	-11358	419.5
343	COM[30]	1480	384.5	424	SEG[369]	-4675	419.5	505	SEG[288]	-7996	419.5	586	SEG[207]	-11399	419.5
344	COM[31]	1400	384.5	425	SEG[368]	-4716	419.5	506	SEG[287]	-8119	419.5	587	SEG[206]	-11440	419.5
345	COM[32]	1320	384.5	426	SEG[367]	-4757	419.5	507	SEG[286]	-8160	419.5	588	SEG[205]	-11481	419.5
346	COM[33]	1240	384.5	427	SEG[366]	-4798	419.5	508	SEG[285]	-8201	419.5	589	SEG[204]	-11522	419.5
347	COM[34]	1160	384.5	428	SEG[365]	-4839	419.5	509	SEG[284]	-8242	419.5	590	SEG[203]	-11563	419.5
348	COM[35]	1080	384.5	429	SEG[364]	-4880	419.5	510	SEG[283]	-8283	419.5	591	SEG[202]	-11604	419.5
349	COM[36]	1000	384.5	430	SEG[363]	-4921	419.5	511	SEG[282]	-8324	419.5	592	SEG[201]	-11645	419.5
350	COM[37]	920	384.5	431	SEG[362]	-4962	419.5	512	SEG[281]	-8365	419.5	593	SEG[200]	-11686	419.5
351	COM[38]	840	384.5	432	SEG[361]	-5003	419.5	513	SEG[280]	-8406	419.5	594	SEG[199]	-11727	419.5
352	COM[39]	760	384.5	433	SEG[360]	-5044	419.5	514	SEG[279]	-8447	419.5	595	SEG[198]	-11768	419.5
353	COM[40]	680	384.5	434	SEG[359]	-5085	419.5	515	SEG[278]	-8488	419.5	596	SEG[197]	-11809	419.5
354	COM[41]	600	384.5	435	SEG[358]	-5126	419.5	516	SEG[277]	-8529	419.5	597	SEG[196]	-11850	419.5
355	COM[42]	520	384.5	436	SEG[357]	-5167	419.5	517	SEG[276]	-8570	419.5	598	SEG[195]	-11891	419.5
356	COM[43]	440	384.5	437	SEG[356]	-5208	419.5	518	SEG[275]	-8611	419.5	599	SEG[194]	-11932	419.5
357	COM[44]	360	384.5	438	SEG[355]	-5249	419.5	519	SEG[274]	-8652	419.5	600	SEG[193]	-11973	419.5
358	COM[45]	280	384.5	439	SEG[354]	-5290	419.5	520	SEG[273]	-8693	419.5	601	SEG[192]	-12014	419.5
359	COM[46]	200	384.5	440	SEG[353]	-5331	419.5	521	SEG[272]	-8734	419.5	602	DUMMY	-12055	419.5
360	COM[47]	40	384.5	441	SEG[352]	-5372	419.5	522	SEG[271]	-8775	419.5				
361	COM[48]	-40	384.5	442	SEG[351]	-5413	419.5	523	SEG[270]	-8816	419.5				
362	COM[49]	-120	384.5	443	SEG[350]	-5454	419.5	524	SEG[269]	-8857	419.5				
363	COM[50]	-200	384.5	444	SEG[349]	-5495	419.5	525	SEG[268]	-8898	419.5				
364	COM[51]	-280	384.5	445	SEG[348]	-5536	419.5	526	SEG[267]	-8939	419.5				
365	COM[52]	-360	384.5	446	SEG[347]	-5577	419.5	527	SEG[266]	-8980	419.5				
366	COM[53]	-440	384.5	447	SEG[346]	-5618	419.5	528	SEG[265]	-9021	419.5				
367	COM[54]	-520	384.5	448	SEG[345]	-5659	419.5	529	SEG[264]	-9062	419.5				
368	COM[55]	-600	384.5	449	SEG[344]	-5700	419.5	530	SEG[263]	-9103	419.5				
369	COM[56]	-680	384.5	450	SEG[343]	-5741	419.5	531	SEG[262]	-9144	419.5				
370	COM[57]	-760	384.5	451	SEG[342]	-5782	419.5	532	SEG[261]	-9185	419.5				
371	COM[58]	-840	384.5	452	SEG[341]	-5823	419.5	533	SEG[260]	-9226	419.5				
372	COM[59]	-920	384.5	453	SEG[340]	-5864	419.5	534	SEG[259]	-9267	419.5				
373	COM[60]	-1080	384.5	454	SEG[339]	-5905	419.5	535	SEG[258]	-9308	419.5				
374	COM[61]	-1160	384.5	455	SEG[338]	-5946	419.5	536	SEG[257]	-9349	419.5				
375	COM[62]	-1240	384.5	456	SEG[337]	-5987	419.5	537	SEG[256]	-9390	419.5				
376	COM[63]	-1320	384.5	457	SEG[336]	-6028	419.5	538	SEG[255]	-9431	419.5				
377	COM[64]	-1400	384.5	458	SEG[335]	-6069	419.5	539	SEG[254]	-9472	419.5				
378	COM[65]	-1480	384.5	459	SEG[334]	-6110	419.5	540	SEG[253]	-9513	419.5				
379	COM[66]	-1560	384.5	460	SEG[333]	-6151	419.5	541	SEG[252]	-9554	419.5				
380	COM[67]	-1640	384.5	461	SEG[332]	-6192	419.5	542	SEG[251]	-9595	419.5				
381	COM[68]	-1720	384.5	462	SEG[331]	-6233	419.5	543	SEG[250]	-9636	419.5				
382	COM[69]	-1800	384.5	463	SEG[330]	-6274	419.5	544	SEG[249]	-9677	419.5				
383	COM[70]	-1880	384.5	464	SEG[329]	-6315	419.5	545	SEG[248]	-9718	419.5				
384	COM[71]	-1960	384.5	465	SEG[328]	-6356	419.5	546	SEG[247]	-9759	419.5				
385	COM[72]	-2040	384.5	466	SEG[327]	-6397	419.5	547	SEG[246]	-9800	419.5				
386	COM[73]	-2120	384.5	467	SEG[326]	-6438	419.5	548	SEG[245]	-9841	419.5				
387	COM[74]	-2200	384.5	468	SEG[325]	-6479	419.5	549	SEG[244]	-9882	419.5				
388	COM[75]	-2280	384.5	469	SEG[324]	-6520	419.5	550	SEG[243]	-9923	419.5				
389	COM[76]	-2360	384.5	470	SEG[323]	-6561	419.5	551	SEG[242]	-9964	419.5				
390	COM[77]	-2440	384.5	471	SEG[322]	-6602	419.5	552	SEG[241]	-10005	419.5				
391	COM[78]	-2520	384.5	472	SEG[321]	-6643	419.5	553	SEG[240]	-10046	419.5				
392	COM[79]	-2600	384.5	473	SEG[320]	-6684	419.5	554	SEG[239]	-10087	419.5				
393	COM[80]	-2680	384.5	474	SEG[319]	-6725	419.5	555	SEG[238]	-10128	419.5				
394	COM[81]	-2760	384.5	475	SEG[318]	-6766	419.5	556	SEG[237]	-10169	419.5				
395	COM[82]	-2840	384.5	476	SEG[317]	-6807	419.5	557	SEG[236]	-10210	419.5				
396	COM[83]	-2920	384.5	477	SEG[316]	-6848	419.5	558	SEG[235]	-10251	419.5				
397	COM[84]	-3000	384.5	478	SEG[315]	-6889	419.5	559	SEG[234]	-10292	419.5				
398	COM[85]	-3080	384.5	479	SEG[314]	-6930	419.5	560	SEG[233]	-10333	419.5				
399	COM[86]	-3160	384.5	480	SEG[313]	-6971	419.5	561	SEG[232]	-10374	419.5				
400	COM[87]	-3240	384.5	481	SEG[312]	-7012	419.5	562	SEG[231]	-10415	419.5				
401	COM[88]	-3320	384.5	482	SEG[311]	-7053	419.5	563	SEG[230]	-10456	419.5				
402	COM[89]	-3400	384.5	483	SEG[310]	-7094	419.5	564	SEG[229]	-10497	419.5				
403	COM[90]	-3480	384.5	484	SEG[309]	-7135	419.5	565	SEG[228]	-10538	419.5				
404	COM[91]	-3560	384.5	485	SEG[308]	-7176	419.5	566	SEG[227]	-10579	419.5				
405	COM[92]	-3640	384.5	486	SEG[307]	-7217	419.5	567	SEG[226]	-10620	419.5				

Functional Description

Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface, Serial Interface (SPI) or I^2C Interface can be selected by different selections of IM0~2 as shown in Table 1.

Table 1

Interface	Config			Data signal								Control signal				
	IM0	IM1	IM2	D7	D6	D5	D4	D3	D2	D1	D0	E/$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
6800	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	E	R/$\overline{W}$	$\overline{CS}$	A0	$\overline{RES}$
8080	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
4-Wire SPI	0	0	0	Hz						SI	SCL	Pull High or Low		$\overline{CS}$	A0	$\overline{RES}$
3-Wire SPI	1	0	0	Hz						SI	SCL	Pull High or Low		$\overline{CS}$	Pull Low	$\overline{RES}$
I^2C	0	1	0	Hz						SDA	SCL	Pull High or Low		Pull Low	SA0	$\overline{RES}$

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. When $\overline{WR}$ (R/$\overline{W}$) = "H", read operation from the display RAM or the status register occurs. When $\overline{WR}$ (R/$\overline{W}$) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of A0 input. The $\overline{RD}$ (E) input serves as data latch signal (clock) when it is "H", provided that $\overline{CS}$ = "L" as shown in Table 2.

Table 2

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
0	0	1	6800 microprocessor bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D0 to D7

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure 2 below.

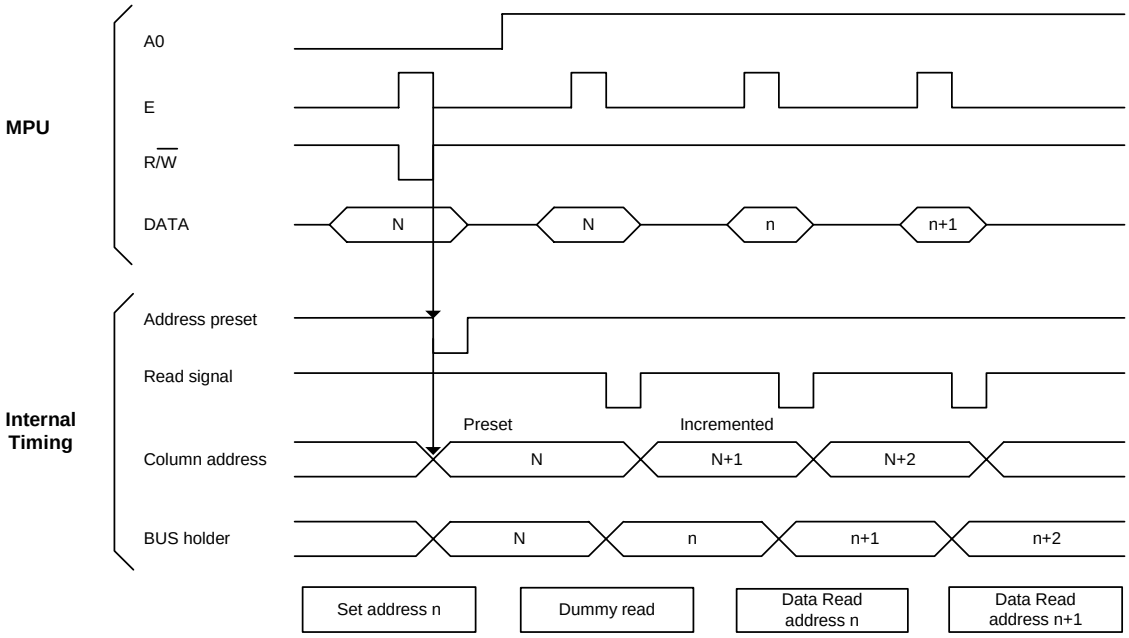


Figure 2

8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. The $\overline{RD}$ (E) input serves as data read latch signal (clock) when it is "L" provided that $\overline{CS}$ = "L". Display data or status register read is controlled by A0 signal. The $\overline{WR}$ (R/$\overline{W}$) input serves as data write latch signal (clock) when it is "L" and provided that $\overline{CS}$ = "L". Display data or command register write is controlled by A0 as shown in Table 3.

Table 3

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
0	1	1	8080 microprocessor bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

Data Bus Signals

The SH1126 identifies the data bus signal according to A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals.

Table 4

Common	6800 processor	8080 processor		Function
A0	(R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

4 Wire Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and $\overline{CS}$. SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, … and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM or command register in the same clock. See Figure 3.

Table 5

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	0	0	4-wire SPI	$\overline{CS}$	A0	-	-	SCL	SI	(Hz)

Note: "-" Must always be HIGH or LOW.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

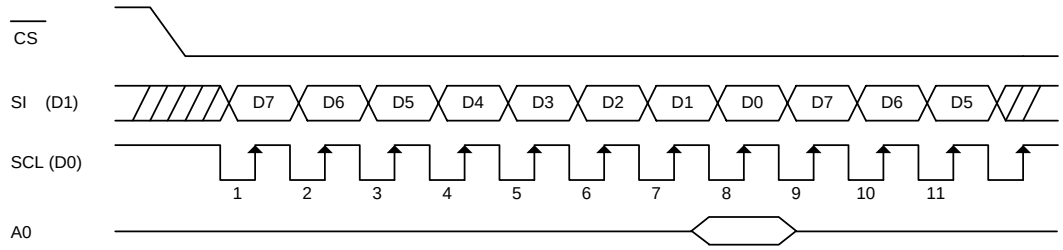


Figure 3 4-wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

3 Wire Serial Interface (3-wire SPI)

The 3 wire serial interface consists of serial clock SCL, serial data SI, and $\overline{CS}$. SI is shifted into an 9-bit shift register on every rising edge of SCL in the order of $D/\overline{C}$, D7, D6, … and D0. The $D/\overline{C}$ bit (first of the 9 bit) will determine the transferred data is written to the display data RAM ($D/\overline{C}$=1) or command register ($D/\overline{C}$=0). See Figure **3** 4.

Table 6

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
1	0	0	3-wire SPI	$\overline{CS}$	Pull Low	-	-	SCL	SI	(Hz)

Note: "-" and Hz pin Must always be HIGH or LOW.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

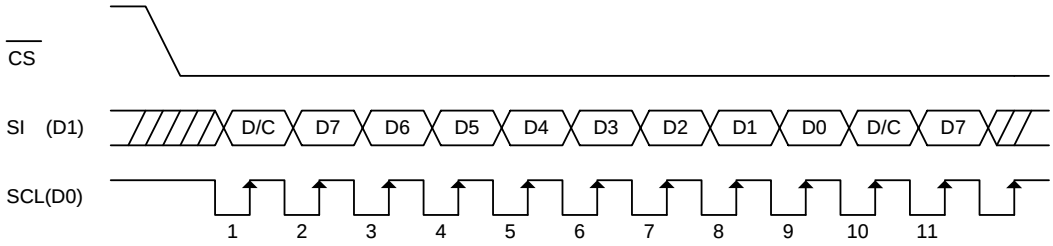


Figure 4 3-wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial status.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

I^2C-bus Interface

The SH1126 can transfer data via a standard I^2C-bus and has slave mode only in communication. The command or RAM data can be written into the chip, the status and RAM data can be read out of the chip.

Table 7

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	1	0	I^2C Interface	Pull Low	SA0	-	-	SCL	SDA	(Hz)

Note: "-" and Hz pin Must always be HIGH or LOW.

$\overline{CS}$ signal can always pull low in I^2C-bus application.

Characteristics of the I^2C-bus

The I^2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Note: The positive supply of pull-up resistor must equal to the value of V_{DD1}.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

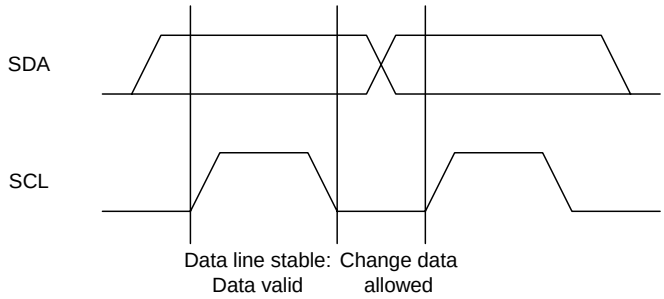


Figure 5 Bit Transfer

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

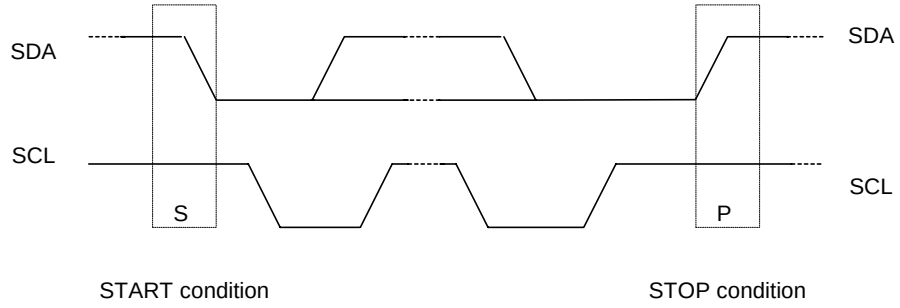


Figure 6 Start and Stop conditions

System configuration

- Transmitter: The device that sends the data to the bus.
- Receiver: The device that receives the data from the bus.
- Master: The device that initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

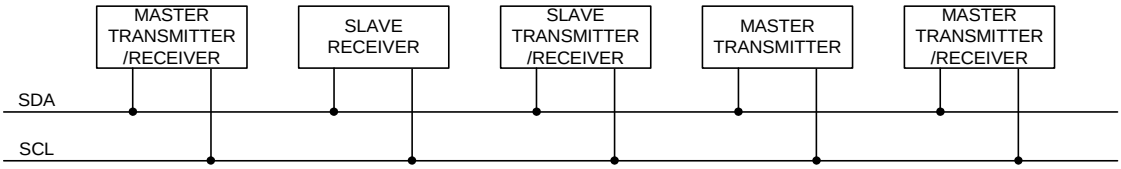


Figure 7 System configuration

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

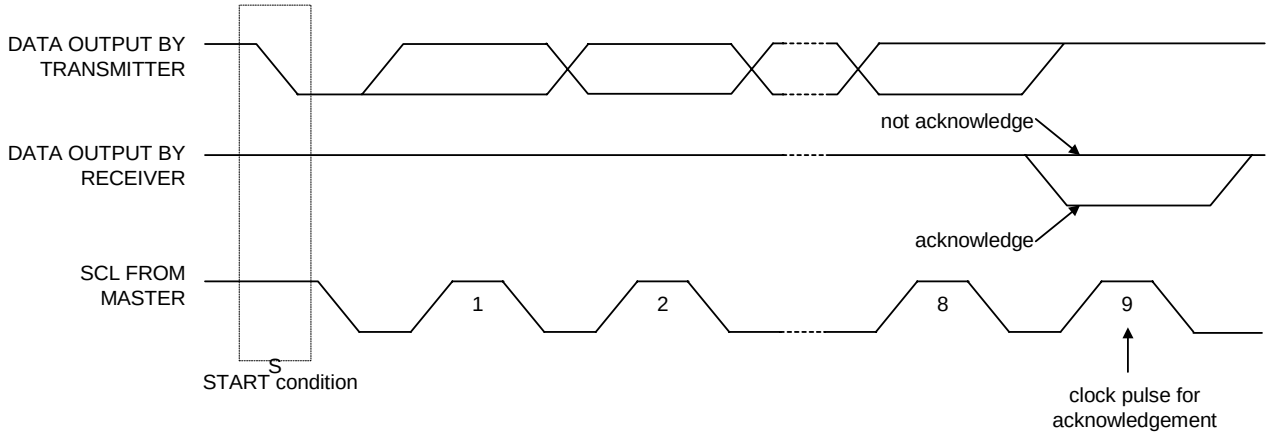


Figure 8 Acknowledge

Protocol

The SH1126 supports both read and write access. The $R/\overline{W}$ bit is part of the slave address. Before any data is transmitted on the I^2C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the SH1126. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(V_{SS}) or 1 (VDD1). The I^2C-bus protocol is illustrated in Fig.9. The sequence is initiated with a START condition (S) from the I^2C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^2C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and $D/\overline{C}$ (note1), plus a data byte (see Fig.7). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the $D/\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the $D/\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the $D/\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SH1126 device. If the $D/\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I^2C-bus master issues a stop condition (P). If the $R/\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the $D/\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

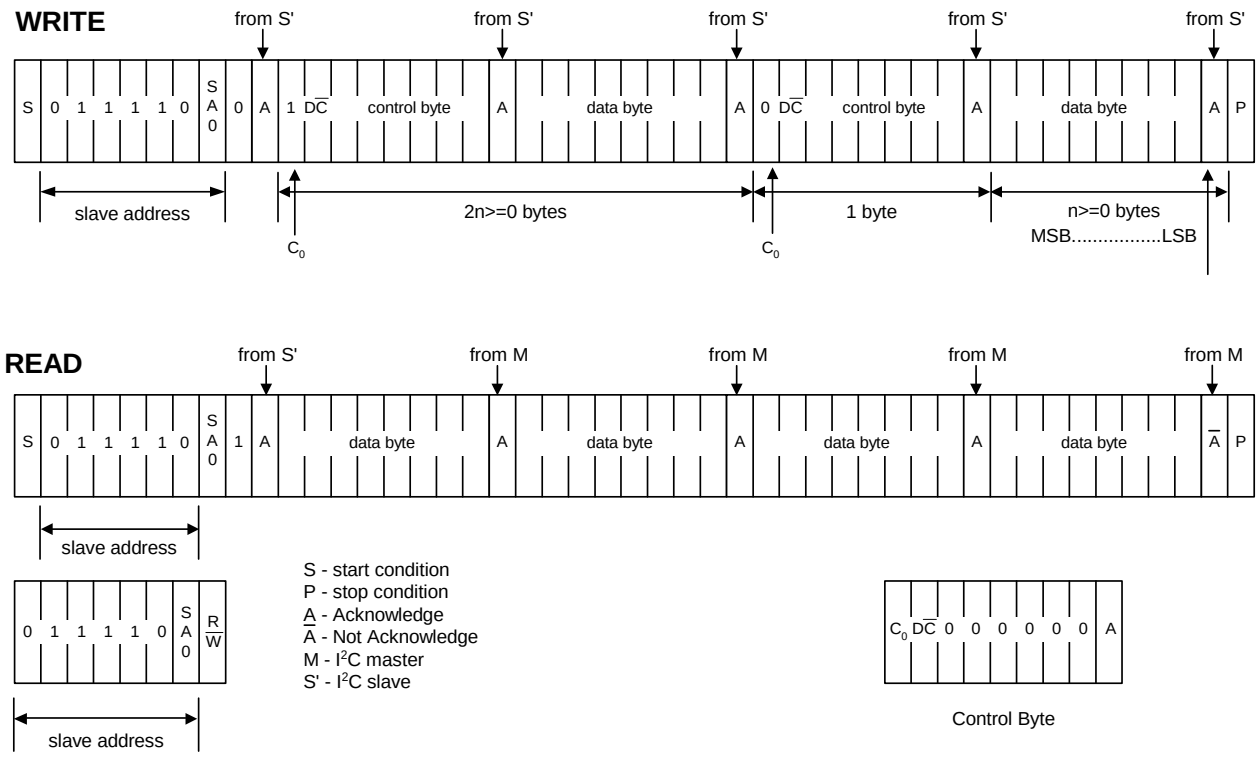


Figure 9 I²C Protocol

Note1:

1. Co＝“0”: The last control byte , only data bytes to follow,
   Co＝“1”: Next two bytes are a data byte and another control byte;
2. D/C＝“0”: The data byte is for command operation,
   D/C＝“1”: The data byte is for RAM operation.

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = “H”, the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = “L”, the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 384X 96 X 4 bits as shown in Figure 10.

For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software.

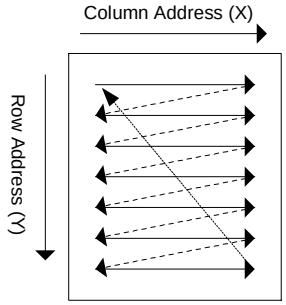
For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Row \ Column		COL0								---	COL191							
0		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
1		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
2		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
---		---								---								
94		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
95		D7	D6	D5	D4	D3	D2	D1	D0	---	D7	D6	D5	D4	D3	D2	D1	D0
ADC	= 0	SEG0				SEG1				---	SEG382				SEG383			
	= 1	SEG383				SEG382				---	SEG1				SEG0			

Figure 10

The Column/Row Address

As shown in **Figure 11**, the display data RAM column address is specified by the Column and Row Address Set command. The specified column address is incremented (+1) with each display data read/ write command. When the Column address reaches the edge, it will be cleared and the row address will be incremented 1.



RAM Address Increment Direction

Figure 11

Furthermore, as shown in Table 8, the Column re-mapping (ADC) command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the OLED module is assembled can be minimized.

Table 8

Segment Output	SEG0		SEG383
ADC "0"	0 (H) →	Column Address	→ BF (H)
ADC "1"	BF (H) ←	Column Address	← 0 (H)

The Row Address Circuit

The Row address circuit specifies the Row address of display RAM and the Row address relating to the common output using the display start line set command, what is normally the top line of the display can be specified.

The screen scrolling function is active by changing display start line dynamically using the display start line set command.

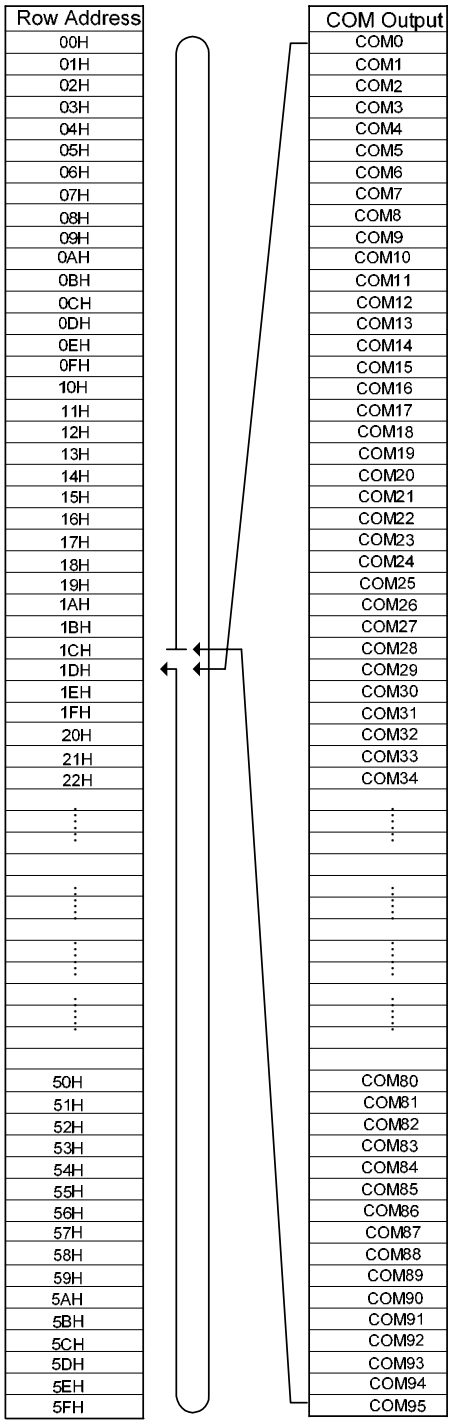


Figure 12 Display Start Line Setting Function

The Oscillator Circuit

This is a RC type oscillator (Figure 13) that produces the display clock. The oscillator circuit is only enabled when CLS = “H”. When CLS = “L”, the oscillation stops and the display clock is inputted through the CL terminal.

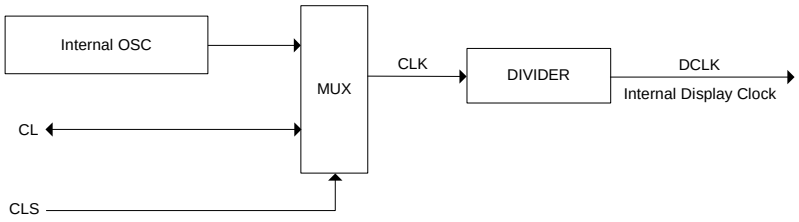


Figure 13

DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for hand held applications. In SH1126, built-in DC-DC voltage converter accompanied with an external application circuit (shown in Figure 14) can generate a high voltage supply V_{PP} from a low voltage supply input AV_{DD}. V_{PP} is the voltage supply to the OLED driver block.

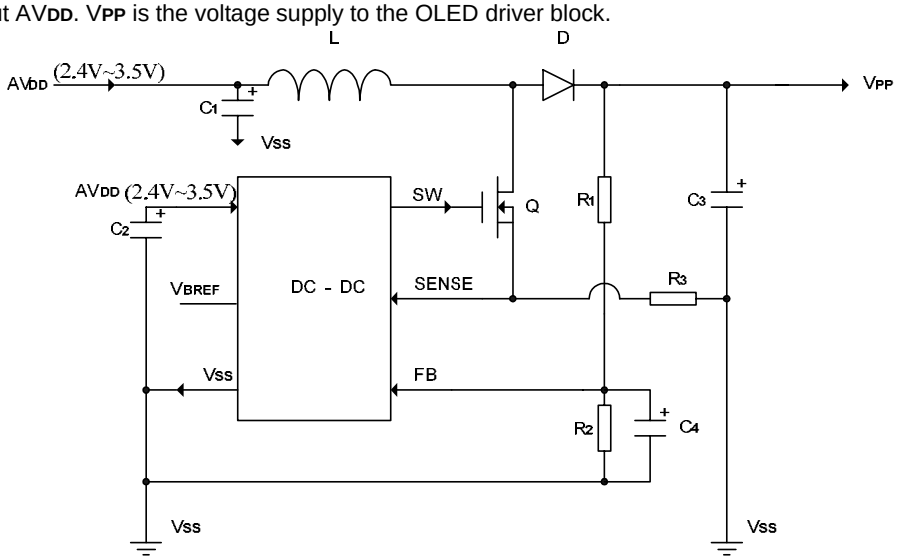


Figure 14

$V_{PP}=(1+\frac{R1}{R2})$ X V_{BREF}, (R_2: 80 - 120kΩ)

Current Control and Voltage Control

This block is used to derive the incoming power sources into different levels of internal use voltage and current. V_{PP} and V_{DD2} are external power supplies. I_{REF} is a reference current source for segment current drivers.

Common Drivers/Segment Drivers

Segment drivers deliver 256 current sources to drive OLED panel. The driving current can be adjusted up to 500μA with 256 steps. Common drivers generate voltage scanning pulses.

16 Grayscale

There are 16 level grayscale for segment driver. The grayscale table is as following.

RAM Data	Pulse Duty	Pulse width
0000	0	0 (DCLK)
0001	1/15	4 (DCLK)
0010	2/15	8 (DCLK)
0011	3/15	12 (DCLK)
…	…	…
1110	14/15	56 (DCLK)
1111	15/15	60 (DCLK)

Reset Circuit

When the $\overline{RES}$ input falls to “L”, these reenter their default state. The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 384X 96 Display mode.
3. Normal segment and display data column address and row address mapping (SEG0 is mapped to column address 00H and COM0 mapped to row address 00H).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM Row address 00H.
6. Column address counter is set at 0.
7. Normal scanning direction of the common outputs.
8. Contrast control register is set at 80H.
9. Internal DC-DC is selected.

Commands

The SH1126 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R / $\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R / $\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1 (HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Set Lower Column Address of display RAM: (00H – 0FH)

2. Set Higher Column Address of display RAM: (10H – 1BH)

Specify column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 191 is accessed. The row address is not changed during this time.

	A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	1	1	1	1	1	1	191

3. - 5. Blank

6. Set Display Start Line:（Double Bytes Command）

Specify Row address to determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the Row address, the smooth scrolling or page change takes place.

■ The Display Start line Mode Set: (40H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	0	0	0	0	0

■ The Display Start line Register Set: (00H - 5FH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Row address
0	1	0	*	0	0	0	0	0	0	0	0(POR)
0	1	0	*	0	0	0	0	0	0	1	1
0	1	0	*	0	0	0	0	0	1	0	2
0	1	0	*				:				:
0	1	0	*								
0	1	0	*				:				:
0	1	0	*	1	0	1	1	1	1	0	94
0	1	0	*	1	0	1	1	1	1	1	95

7. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: I_{SEG} = α/256 X I_{REF} X scale factor

Where: α is contrast step; I_{REF} is reference current equals 15.625μA; Scale factor = 32.

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

■ Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register，the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	I_{SEG}
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	0	1	
0	1	0	0	0	0	0	0	0	1	0	
0	1	0					:				:
0	1	0	1	0	0	0	0	0	0	0	POR
0	1	0					:				:
0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	Large

8. Set Segment Re-map: (A0H - A1H)

Change the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the column address section of ADC. When display data is written or read, the column address is incremented by 1 as shown in Figure 2.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

When ADC = “L”, the right rotates (normal direction). (POR)

When ADC = “H”, the left rotates (reverse direction).

Note:

The Set Segment Re-map command will change the address counter value, so it is recommended to set segment re-map in the initial program.

9. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = “L”, the normal display status is provided. (POR)

When D = “H”, the entire display ON status is provided.

10. Set Normal/Reverse Display: (A6H - A7H)

Reverse the display ON/OFF status without rewriting the contents of the display data RAM.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = “L”, the RAM data is high, being OLED ON potential (normal display). (POR)

When D = “H”, the RAM data is low, being OLED ON potential (reverse display).

11. Set Multiplex Ration: (Double Bytes Command)

This command switches default 96 multiplex modes to any multiplex ratio from 1 to 96. The output pads COM0-COM95 will be switched to corresponding common signal.

■ Multiplex Ration Mode Set: (A8H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

■ Multiplex Ration Data Set: (00H - 5FH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Multiplex Ratio
0	1	0	*	0	0	0	0	0	0	0	1
0	1	0	*	0	0	0	0	0	0	1	2
0	1	0	*	0	0	0	0	0	1	0	3
0	1	0					:				:
0	1	0	*	1	0	1	1	1	1	0	95
0	1	0	*	1	0	1	1	1	1	1	96 (POR)

12. DC-DC Setting: (Double Bytes Command)

This command is to control the DC-DC voltage converter status and the switch frequency. Issuing this command then display ON command will turn on the converter. The panel display must be off while issuing this command.

■ DC-DC Control Mode Set: (ADH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	1

■ DC-DC ON/OFF Mode Set:

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	F2	F1	F0	D

When D = “L”, DC-DC is disable.
When D = “H”, DC-DC will be turned on when display on. (POR)

DC-DC STATUS	DISPLAY ON/OFF STATUS	Description
0	0	Sleep mode
0	1	External V_{PP} must be used
1	0	Sleep mode
1	1	Built-in DC-DC is used, Normal Display

F2	F1	F0	Switch Frequency
0	0	0	0.6SF (POR)
0	0	1	0.7SF
0	1	0	0.8SF
0	1	1	0.9SF
1	0	0	SF
1	0	1	1.1SF
1	1	0	1.2SF
1	1	1	1.3SF

SF = 500KHZ ± 25%

13. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = “L”, Display OFF OLED. (POR)
When D = “H”, Display ON OLED.
When the display OFF command is executed, power saver mode will be entered.

Sleep Mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and DC-DC circuit.
(2) Stops the OLED drive and outputs HZ as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access to the built-in display RAM.

14. Set Row Address of Display RAM: (Double Bytes Command)

Specify Row address to load display RAM data to Row address register. Any RAM data bit can be accessed when its row address and column address are specified. The display remains unchanged even when the Row address is changed.

■ Row address Mode Setting: (B0H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	0	0	0

■ Row address setting:

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	*	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Row address
0	0	0	0	0	0	0	0 (POR)
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
…		…	…	…	…	…	…
1	0	1	1	1	0	1	5DH
1	0	1	1	1	1	0	5EH
1	0	1	1	1	1	1	5FH

15. Set Common Output Scan Direction: (C0H - C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

When D = “L”, Scan from COM0 to COM [N-1]. (POR)
When D = “H”, Scan from COM [N-1] to COM0.

16. Set Display Offset: (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-95 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 7-bit data in the second byte should be given by 0010000.

■ Display Offset Mode Set: (D3H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	1

■ Display Offset Data Set: (00H – 5FH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	*	0	0	0	0	0	0	0	0 (POR)
0	1	0	*	0	0	0	0	0	0	1	1
0	1	0	*	0	0	0	0	0	1	0	2
0	1	0					:				:
0	1	0	*	1	0	1	1	1	1	0	94
0	1	0	*	1	0	1	1	1	1	1	95

Note: “*” stands for “Don’t care”

17. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1 Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

■ Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1

■ Divide Ratio/Oscillator Frequency Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A_3 - A_0 defines the divide ration of the display clocks (DCLK). Divide Ration = A[3:0]+1.

A_3	A_2	A_1	A_0	Divide Ration
0	0	0	0	1 (POR)
		:		:
1	1	1	1	16

A_7 - A_4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

A_7	A_6	A_5	A_4	Oscillator Frequency of fosc
0	0	0	0	-25%
0	0	0	1	-20%
0	0	1	0	-15%
0	0	1	1	-10%
0	1	0	0	-5%
0	1	0	1	fosc (POR)
0	1	1	0	+5%
0	1	1	1	+10%
1	0	0	0	+15%
1	0	0	1	+20%
1	0	1	0	+25%
1	0	1	1	+30%
1	1	0	0	+35%
1	1	0	1	+40%
1	1	1	0	+45%
1	1	1	1	+50%

18. Set Discharge/Precharge Period: (Double Bytes Command)

This command is used to set the duration of the Precharge/Discharge period. The interval is counted in number of DCLK. POR is 2 DCLKs.

■ Precharge/Discharge Period Mode Set: (D9H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1

■ Precharge/Discharge Period Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

Precharge Period Adjust: (A3 - A0)

A_3	A_2	A_1	A_0	Pre-charge Period
0	0	0	0	Note
0	0	0	1	1 DCLK
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Discharge Period Adjust: (A_7 - A_4)

A_7	A_6	A_5	A_4	Dis-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Note：when set A[3:0]=0, the period for display will increase 2 DCLKs. And there is no pre-charge period so that it will save power consumption.

19. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

■ VCOM Deselect Level Mode Set: (DBH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

■ VCOM Deselect Level Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

$V_{COMH} = \beta_1 \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β_1	A[7:0]	β_1
00H	0.430	20H	0.635
01H	0.436	21H	0.642
02H	0.443	22H	0.648
03H	0.449	23H	0.655
04H	0.456	24H	0.661
05H	0.462	25H	0.667
06H	0.468	26H	0.674
07H	0.475	27H	0.680
08H	0.481	28H	0.687
09H	0.488	29H	0.693
0AH	0.494	2AH	0.699
0BH	0.501	2BH	0.706
0CH	0.507	2CH	0.712
0DH	0.513	2DH	0.719
0EH	0.520	2EH	0.725
0FH	0.526	2FH	0.732
10H	0.533	30H	0.738
11H	0.539	31H	0.744
12H	0.545	32H	0.751
13H	0.552	33H	0.757
14H	0.558	34H	0.764
15H	0.565	35H	0.770 (POR)
16H	0.571	36H	0.776
17H	0.578	37H	0.783
18H	0.584	38H	0.789
19H	0.590	39H	0.796
1AH	0.597	3AH	0.802
1BH	0.603	3BH	0.808
1CH	0.610	3CH	0.815
1DH	0.616	3DH	0.821
1EH	0.622	3EH	0.828
1FH	0.629	3FH	0.834
40H - FFH	1		

20. Set VSEGM Level: (Double Bytes Command)

This command is to set the segment pad output voltage level at pre-charge stage.

■ V_{SEGM} Level Mode Set: (DCH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	1	0	0

■ V_{SEGM} Level Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

$V_{SEGM} = \beta_2 \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β_2	A[7:0]	β_2
00H	0.430	20H	0.635
01H	0.436	21H	0.642
02H	0.443	22H	0.648
03H	0.449	23H	0.655
04H	0.456	24H	0.661
05H	0.462	25H	0.667
06H	0.468	26H	0.674
07H	0.475	27H	0.680
08H	0.481	28H	0.687
09H	0.488	29H	0.693
0AH	0.494	2AH	0.699
0BH	0.501	2BH	0.706
0CH	0.507	2CH	0.712
0DH	0.513	2DH	0.719
0EH	0.520	2EH	0.725
0FH	0.526	2FH	0.732
10H	0.533	30H	0.738
11H	0.539	31H	0.744
12H	0.545	32H	0.751
13H	0.552	33H	0.757
14H	0.558	34H	0.764
15H	0.565	35H	0.770 (POR)
16H	0.571	36H	0.776
17H	0.578	37H	0.783
18H	0.584	38H	0.789
19H	0.590	39H	0.796
1AH	0.597	3AH	0.802
1BH	0.603	3BH	0.808
1CH	0.610	3CH	0.815
1DH	0.616	3DH	0.821
1EH	0.622	3EH	0.828
1FH	0.629	3FH	0.834
40H - FFH	1		

21. Set Discharge VSL Level (30H - 3FH)

This command is to set the Segment output discharge voltage level.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	D3	D2	D1	D0

This command is to set the segment discharge voltage level

D[3:0]	V_{SL}
00H	0V (Default)
01H	0.1 V_{REF}
02H	0.125 V_{REF}
03H	0.150 V_{REF}
04H	0.175 V_{REF}
05H	0.2 V_{REF}
06H	0.225 V_{REF}
07H	0.250 V_{REF}
08H	0.275 V_{REF}
09H	0.3 V_{REF}
0AH	0.325 V_{REF}
0BH	0.350 V_{REF}
0CH	0.375 V_{REF}
0DH	0.4 V_{REF}
0EH	0.425 V_{REF}
0FH	0.450 V_{REF}

22. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. Once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

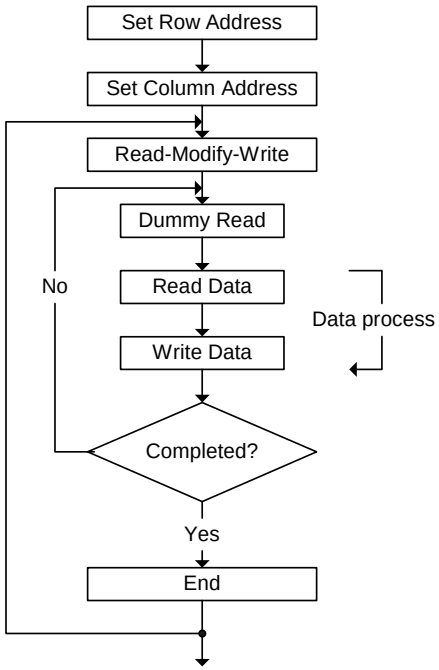


Figure 15

23. End: (EEH)

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued.)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

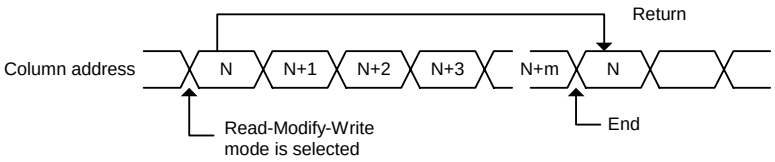


Figure 16

24. NOP: (E3H)

Non-Operation Command.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

25. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write RAM data							

26. Read Status

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ON/OFF	*	*	*	0	0	0

BUSY: When high, the SH1126 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ON/OFF: Indicates whether the display is on or off. When goes low, the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

27. Read Display Data

Read 8-bit data from display RAM area specified by column address and Row address. As the column address increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read RAM data							

Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2. Set Column Address 3 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3. Reserved Command	0	1	0	0	0	1	0	0	1	0	0	Reserved
4. Reserved Command	0	1	0	0	0	1	0	0	1	1	0	Reserved
5. Reserved Command	0	1	0	0	0	1	0	1	1	1	D	Reserved
6. The Display Start Line Mode Set	0	1	0	0	1	0	0	0	0	0	0	Specifies RAM display line for COM0. (POR = 00H)
Display Start Line Register Set	0	1	0	*	Start Line address							
7. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
Contrast Data Register Set	0	1	0	Contrast Data								
8. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The right (0) or left (1) rotation. (POR = A0H)
9. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
10. Set Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
11. Multiplex Ration Mode Set	0	1	0	1	0	1	0	1	0	0	0	This command switches default 96 multiplex mode to any multiplex ration from 1 to 96. (POR = 5FH)
Multiplex Ration Data Set	0	1	0	*	Multiplex Ratio							
12. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage and the switch frequency. (POR = 81H)
DC-DC ON/OFF Mode Set	0	1	0	1	0	0	0	F2	F1	F0	D	
13. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
14. Row Address Set	0	1	0	1	0	1	1	0	0	0	0	Specifies Row address to load display RAM data to Row address register. (POR = 00H)
Row Address	0	1	0	*	Row Address							
15. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
16. Display Offset Mode Set	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command that specifies the mapping of display start line to one of COM0-95. (POR = 00H)
Display Offset Data Set	0	1	0	*	COMx							
17. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				

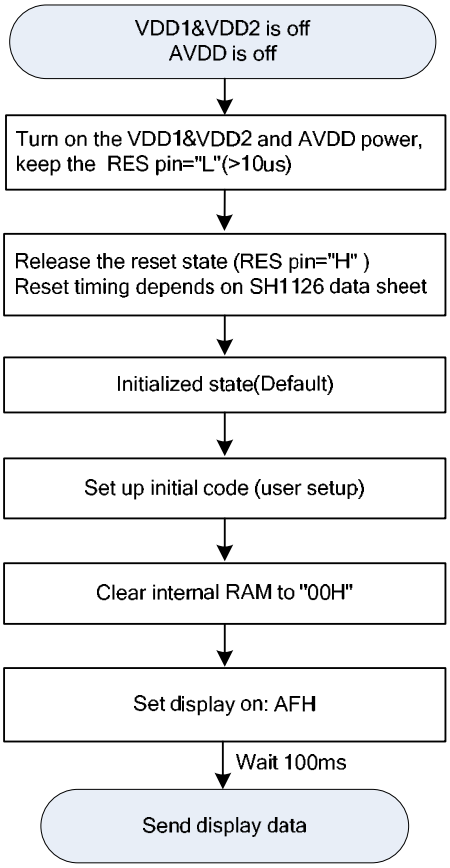
Command Table (Continued)

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
18. Dis-charge/Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge/Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
19. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOMH= (β_1 X V_{REF})								
20. VSEGM Level Mode Set	0	1	0	1	1	0	1	1	1	0	0	This command is to set the segment pad output voltage level at pre-charge stage. (POR = 35H)
VSEGM Level Data Set	0	1	0	VSEGM= (β_2 X V_{REF})								
21. Discharge voltage VSL level setting	0	1	0	0	0	1	1	D3	D2	D1	D0	Set the discharge voltage level.
22. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
23. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
24. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
25. Write Display Data	1	1	0	Write RAM data								
26. Read Status	0	0	1	BUSY	ON/OFF	*	*	*	0	0	0	
27. Read Display Data	1	0	1	Read RAM data								

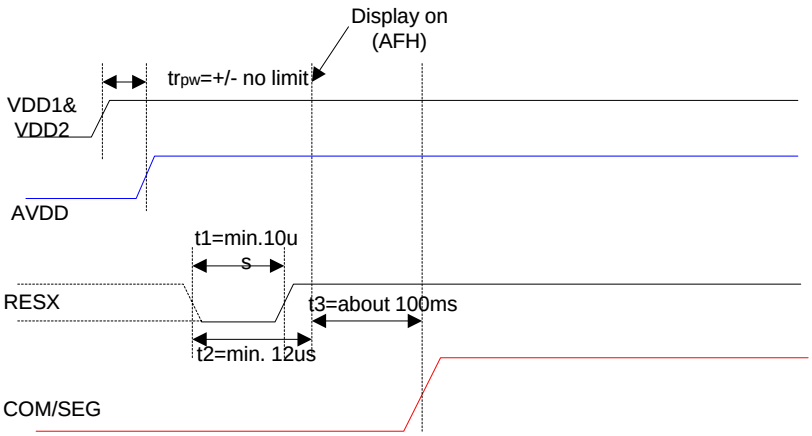
Note: Do not use any other commands, or the system malfunction may result.

1. Power On and Initialization

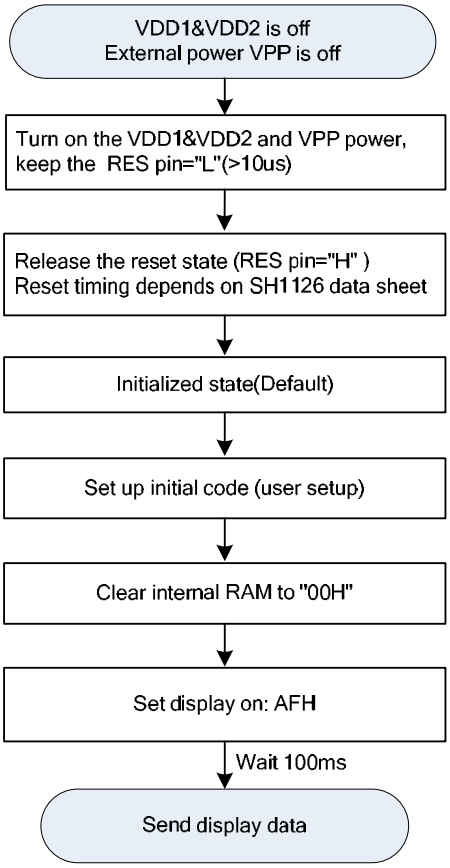
1.1. Built-in DC-DC pump power is being used immediately after turning on the power:



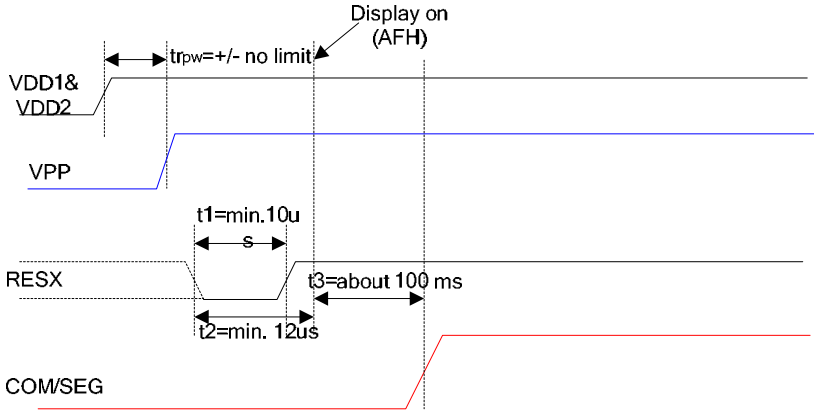
Power on sequence:



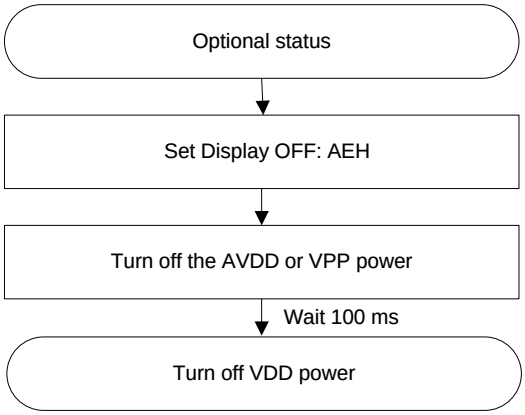
1.2. External power is being used immediately after turning on the power:



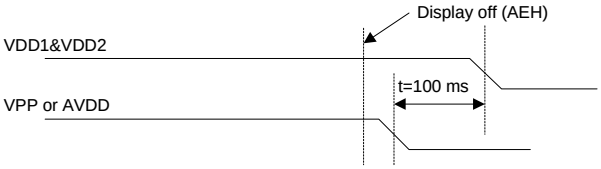
Power on sequence:



2. Power Off



Power off sequence:



Note：There will be no damages to the display module if the power sequences are not met.

Absolute Maximum Rating*

DC Supply Voltage (VDD1) . . . . . -0.3V to +3.6V

DC Supply Voltage (VDD2) . . . . . -0.3V to +3.6V

DC Supply Voltage (V_{PP}) . . . . . -0.3V to +14.5V

Input Voltage . . . . . -0.3V to V_{DD1} + 0.3V

Operating Ambient Temperature . . . . . .-40°C to +85°C

Storage Temperature . . . . . -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (V_{SS} = 0V, V_{DD1} = 1.65 - 3.5V, V_{DD2} = 1.65 - 3.5V, AV_{DD} =2.4-3.5V, T_A = +25°C, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD1}	Power supply of I/O	1.65	-	3.5	V	
V_{DD2}	Power supply of logic device	1.65	-	3.5	V	
AV_{DD}	DC-DC voltage supply	2.4	3.0	3.5	V	
V_{PP}	OLED Operating voltage	7.0	-	14	V	
V_{BREF}	Internal voltage reference	1.20	1.26	1.32	V	
I_{DD1}	Dynamic current Consumption 1(in V_{DD1}& V_{DD2})	-	110	160	μA	V_{DD1} = 3V, V_{DD2} = 3V, AV_{DD} =3V ,I_{REF} = -15.625A, Contrast α = 256, Bulid-in DC-DC OFF, Display ON, display data = All ON, No panel attached
I_{DD2}	Dynamic current Consumption 2 (in AV_{DD})	-	190	285	μA	V_{DD1} = 3V, V_{DD2} = 3V, AV_{DD} =3V ,V_{PP} = 12V, I_{REF} = -15.625μA, Contrast α = 256, Bulid-in DC-DC ON, Display ON, Display data = All ON, No panel attached
I_{PP}	OLED dynamic current consumption	-	1.8	2.54	mA	V_{DD1} = 3V, V_{DD2} = 3V, AV_{DD} =3V ,V_{PP} = 12V, I_{REF} = -15.625μA, Contrast α = 256, Display ON, Display data = All ON, No panel attached
I_{SP}	Sleep mode current Consumption in V_{DD1} & V_{DD2}& AV_{DD}	-	0.01	5	μA	During sleep, T_A = +25°C, V_{DD1} = 3V, V_{DD2} = 3V, AV_{DD} =3V
	Sleep mode current Consumption in V_{PP}	-	0.01	5	μA	During sleep, T_A = +25°C, V_{PP} = 12V
I_{SEG}	Segment output current	-	-500	-	μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} = -15.625μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 256
		-	-343.75	-	μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} = -15.625μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 176
		-	-187.5	-	μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} = -15.625μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 96
		-	-31.25	-	μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} = -15.625μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 16
ΔI_{SEG1}	Segment output current uniformity	-	-	±3	%	ΔI_{SEG1} = (I_{SEG} - I_{MID})/I_{MID} X 100% I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} [0:255] at contrast α = 256
ΔI_{SEG2}	Adjacent segment output Current uniformity	-	-	±2	%	ΔI_{SEG2} = (I_{SEG} [N] - I_{SEG} [N+1])/(I_{SEG} [N] + I_{SEG} [N+1]) X 100% I_{SEG} [0:255] at contrast α = 256

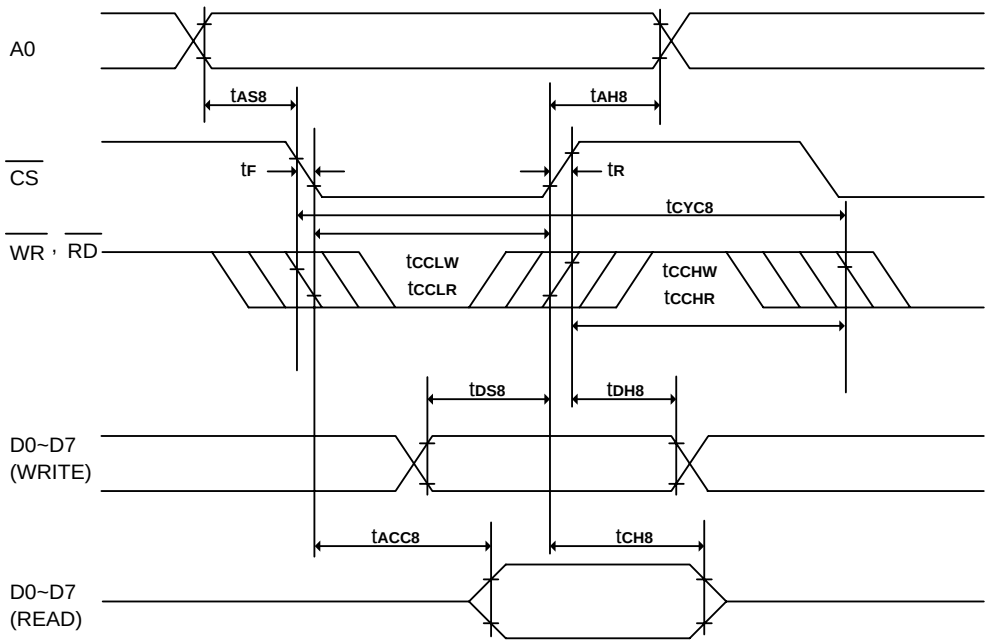
DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IHC}	High-level input voltage	0.8 X V_{DD1}	-	V_{DD1}	V	A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, CL, IM0, IM1, IM2 and $\overline{RES}$
V_{ILC}	Low-level input voltage	V_{SS}	-	0.2 X V_{DD1}	V	
V_{OHC}	High-level output voltage	0.8 X V_{DD1}	-	V_{DD1}	V	I_{OH} = -0.5mA (D0 - D7, and CL)
V_{OLC}	Low -level output voltage	V_{SS}	-	0.2 X V_{DD1}	V	I_{OL} = 0.5mA (D0 - D7, and CL)
V_{OLCS}	SDA low -level output voltage	V_{SS}	-	0.2 X V_{DD1}	V	VDD1<2V; I_{OL}=2mA (SDA)
				0.4		VDD1>2V; I_{OL}=3mA (SDA)
I_{LI}	Input leakage current	-1.0	-	1.0	μA	V_{IN} = V_{DD1} or V_{SS} (A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, IM0, IM1, IM2 and $\overline{RES}$
I_{HZ}	HZ leakage current	-1.0	-	1.0	μA	When the D0 - D7, and CL are in high impedance
f_{OSC}	Oscillation frequency	-	676	-	KHZ	T_A = +25°C
f_{FRM}	Frame frequency for 96 Commons	-	110	-	HZ	When f_{OSC} = 676KHZ, Divide ratio = 1, common width = 64 DCLKs
R_{ON1}	Common switch resistance	-	10	12	Ω	V_{PP} = 12V, V_{COM} = V_{SS} + 0.4V
R_{ON2}	Common switch resistance	-	350	-	Ω	V_{PP} = 12V, V_{COM} = 0.770 X V_{PP} - 0.4V

AC Characteristics

Application Circuit (for reference only)

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



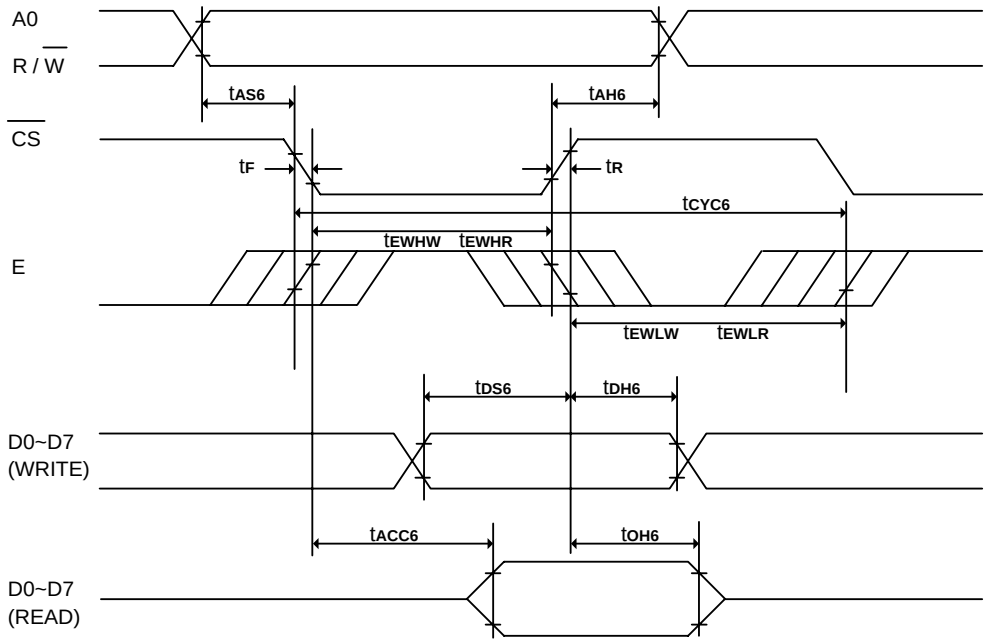
(V_{DD1} = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	600	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	80	-	-	ns	
t_{DH8}	Data hold time	30	-	-	ns	
t_{CH8}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	280	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	200	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	240	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	200	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DH8}	Data hold time	15	-	-	ns	
t_{CH8}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	100	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	120	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	100	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



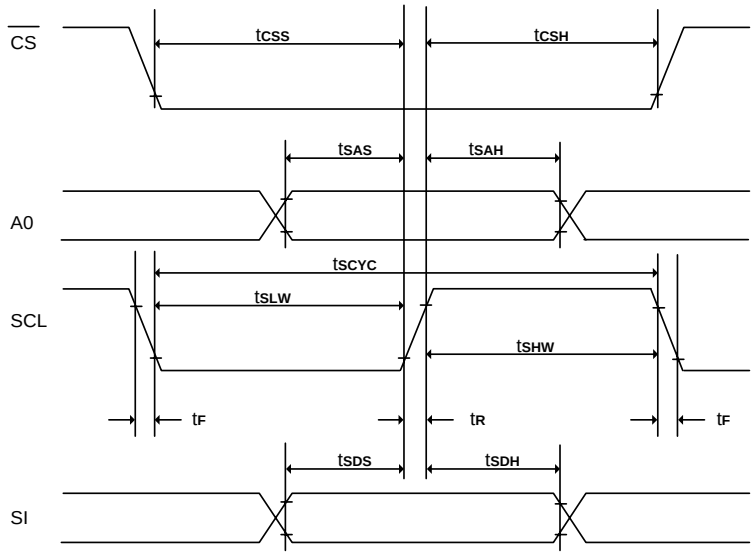
(V_{DD1} = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	600	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	80	-	-	ns	
t_{DH6}	Data hold time	30	-	-	ns	
t_{OH6}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	280	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	200	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	240	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	200	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DH6}	Data hold time	15	-	-	ns	
t_{OH6}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	140	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(3) System buses Write characteristics 3 (For 4 wire SPI)



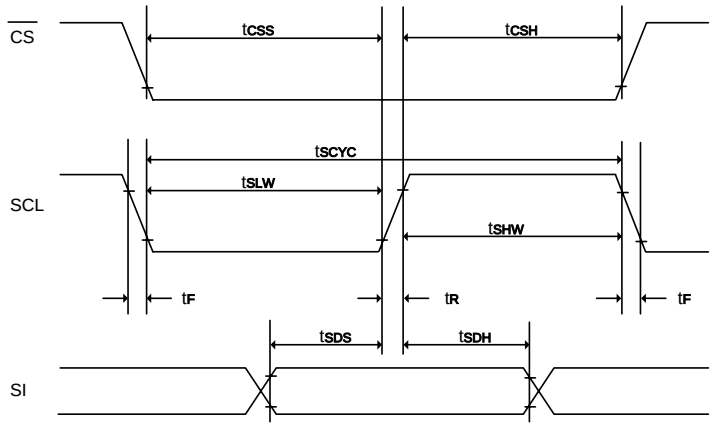
(V_{DD1} =1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SAS}	Address setup time	300	-	-	ns	
t_{SAH}	Address hold time	300	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SAS}	Address setup time	150	-	-	ns	
t_{SAH}	Address hold time	150	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse width	100	-	-	ns	
t_{SLW}	Serial clock L pulse width	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(4) System buses Write characteristics 4(For 3 wire SPI)



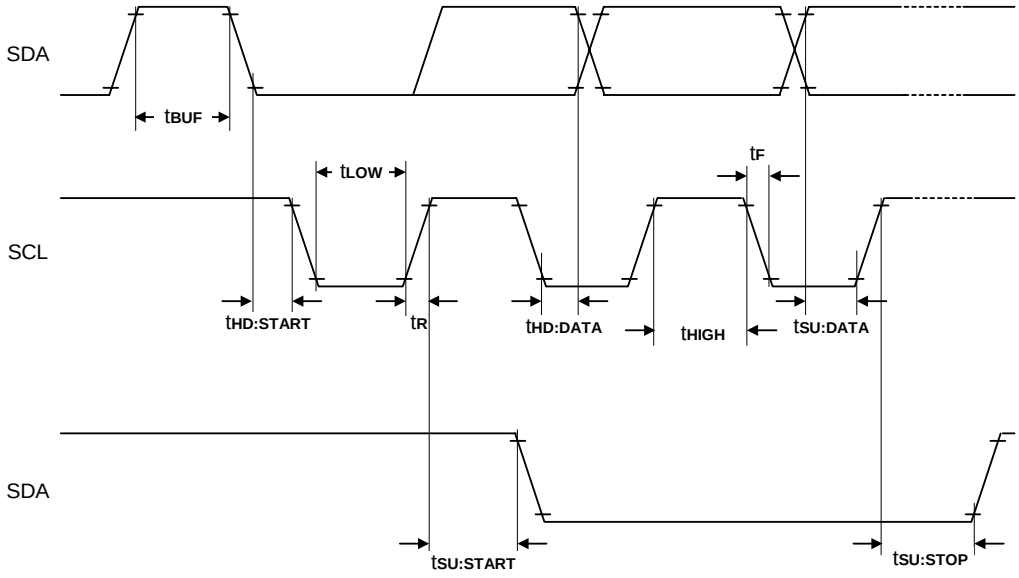
(V_{DD1} = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse width	100	-	-	ns	
t_{SLW}	Serial clock L pulse width	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

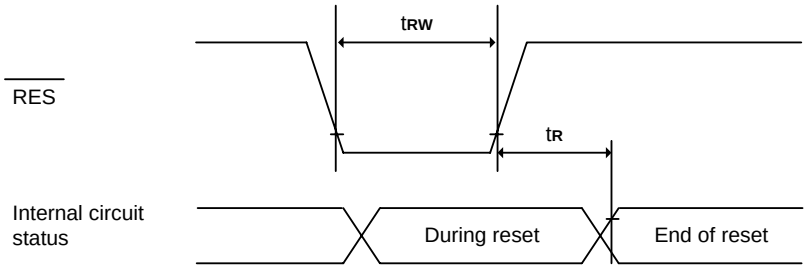
(5) I²C interface characteristics



(V_{DD1} = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{SCL}	SCL clock frequency	DC	-	400	KHZ	
T_{LOW}	SCL clock Low pulse width	1.3	-	-	uS	
T_{HIGH}	SCL clock H pulse width	0.6	-	-	uS	
$T_{SU:DATA}$	data setup time	100	-	-	nS	
$T_{HD:DATA}$	data hold time	0	-	0.9	uS	
T_R	SCL, SDA rise time	20+0.1Cb	-	300	nS	
T_F	SCL, SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
$T_{SU:START}$	Setup timefor re-START	0.6	-	-	uS	
$T_{HD:START}$	START Hold time	0.6	-	-	uS	
$T_{SU:STOP}$	Setup time for STOP	0.6	-	-	uS	
T_{BUF}	Bus free times between STOP and START condition	1.3	-	-	uS	

(6) Reset Timing



(V_{DD1} = 1.65 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	2.0	μs	
t_{RW}	Reset low pulse width	10.0	-	-	μs	

(V_{DD1} = 2.4 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	1.0	μs	
t_{RW}	Reset low pulse width	5.0	-	-	μs	

Reference Connection to MPU:

1. 8080 Series Interface: (Internal Oscillator, External V_{PP})

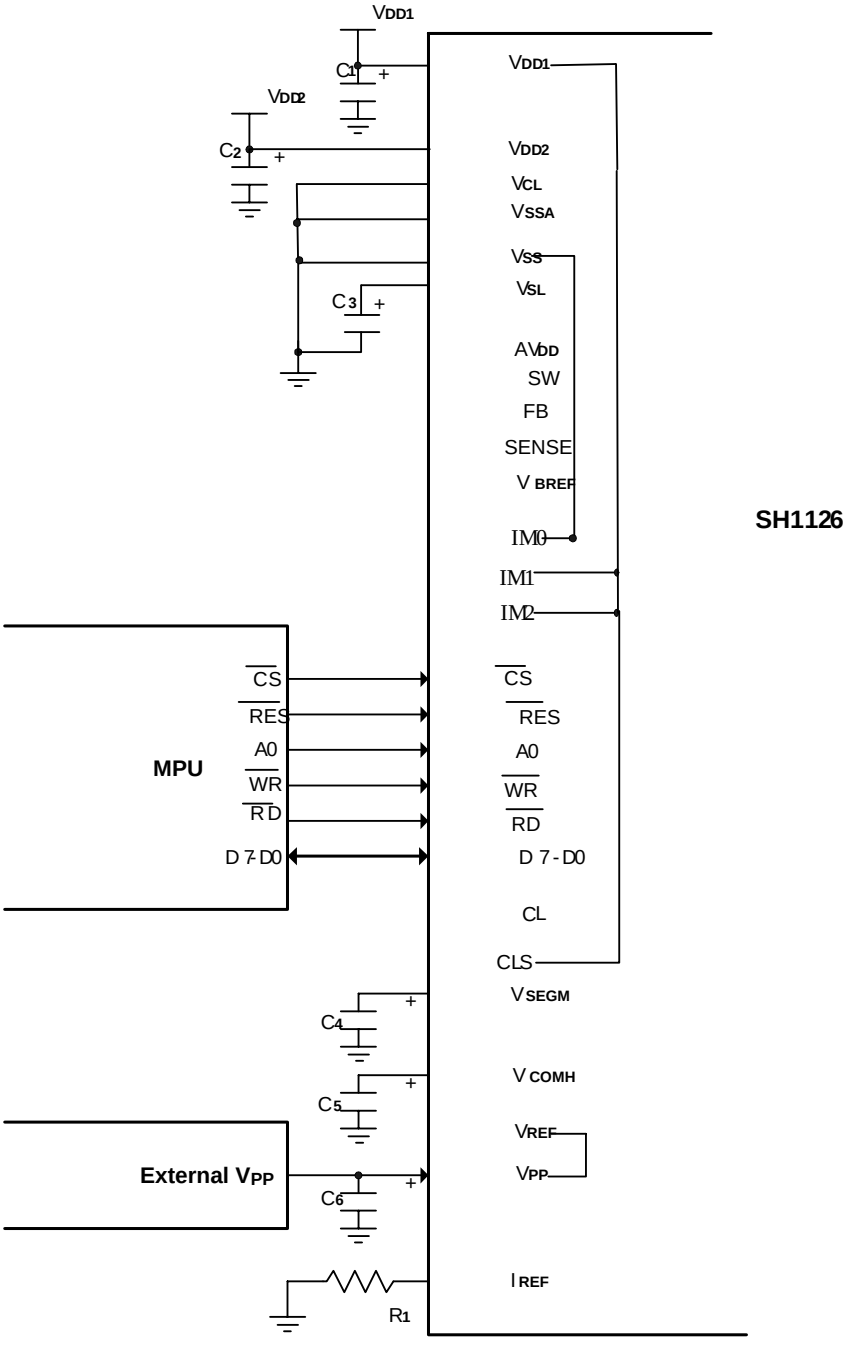


Figure 17

Note:

C_1 – C_6: 4.7μF

R_1: about 620kΩ, R_1 = (Voltage at I_{REF} - V_{SS})/I_{REF}

2. 6800 Series Interface: (Internal Oscillator, Built-in DC-DC)

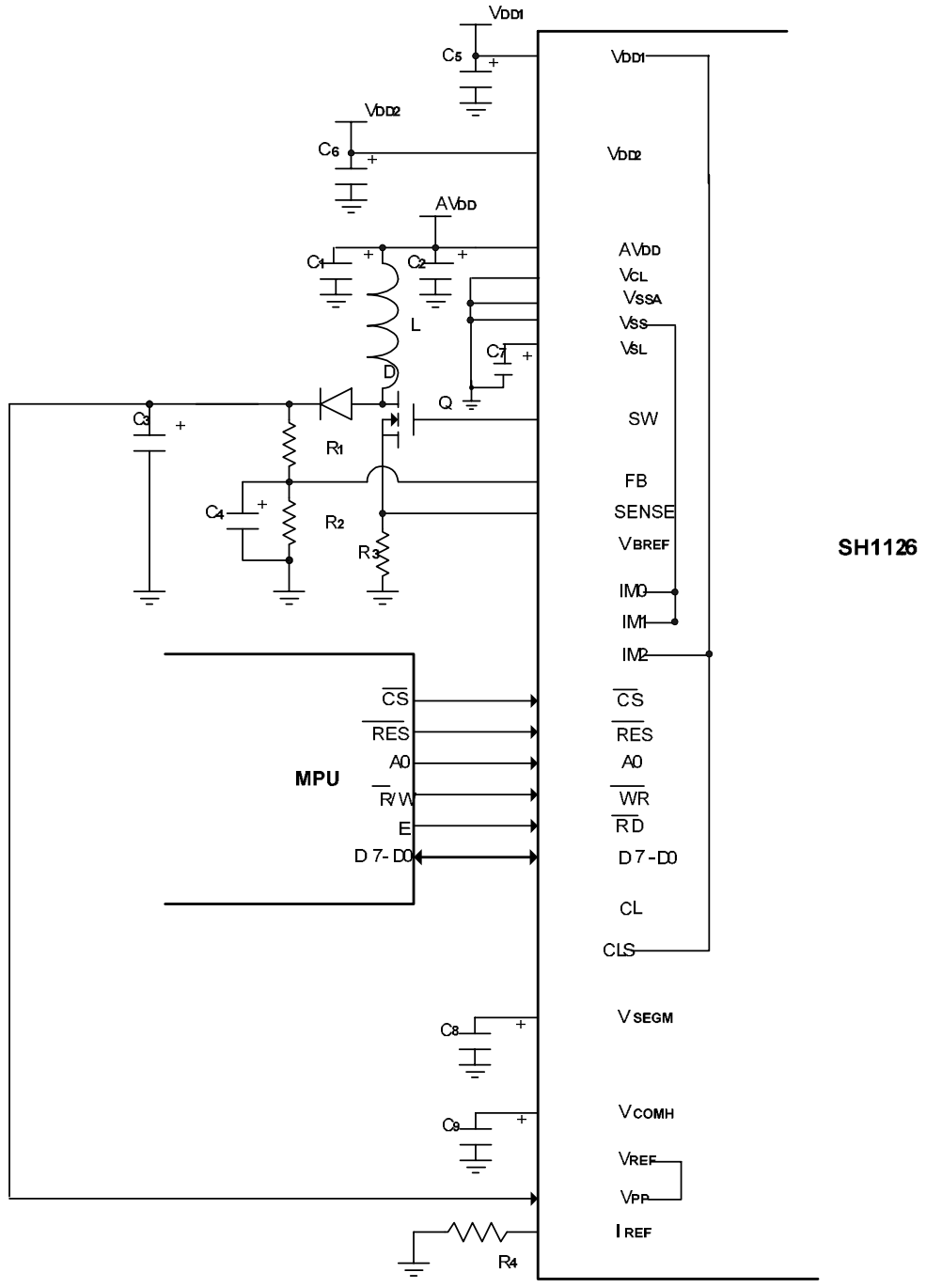


Figure 18

Note:

L, D, Q, R_1, R_2, R_3, C_1 – C_4: Please refer to following description of DC-DC module.
C_5, C_6, C_7, C_8, C_9: 4.7μF
R_4: about 620kΩ, R_4 = (Voltage at I_{REF} - V_{SS})/I_{REF}

3. Serial Interface (3-wire or 4-wire SPI): (External Oscillator, External V_{PP})

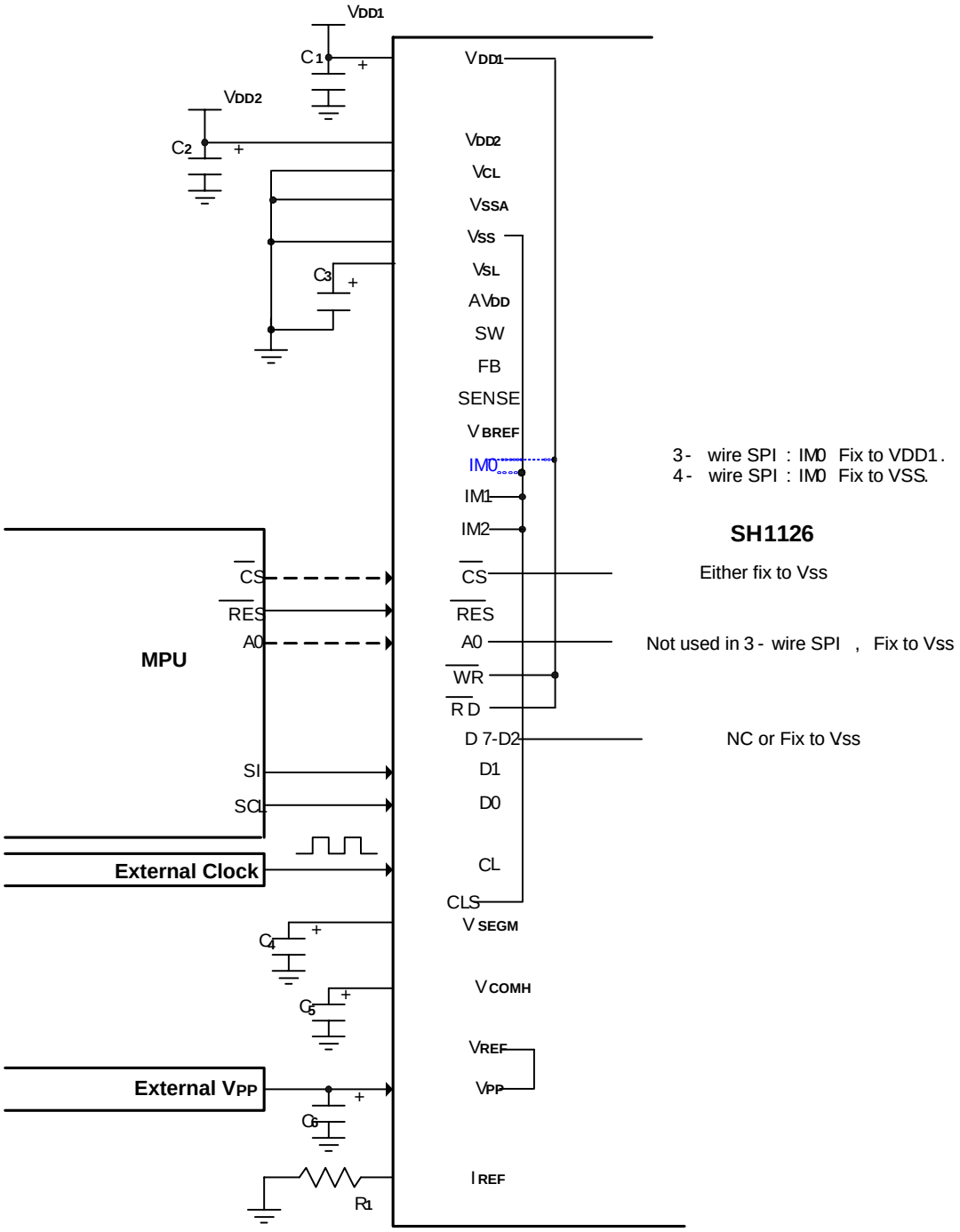


Figure 19

Note:

$C_1 - C_6$: 4.7μF

R_1: about 620kΩ, R_1 = (Voltage at I_{REF} - V_{SS})/I_{REF}

4. I²C Interface: (Internal oscillator, External VPP)

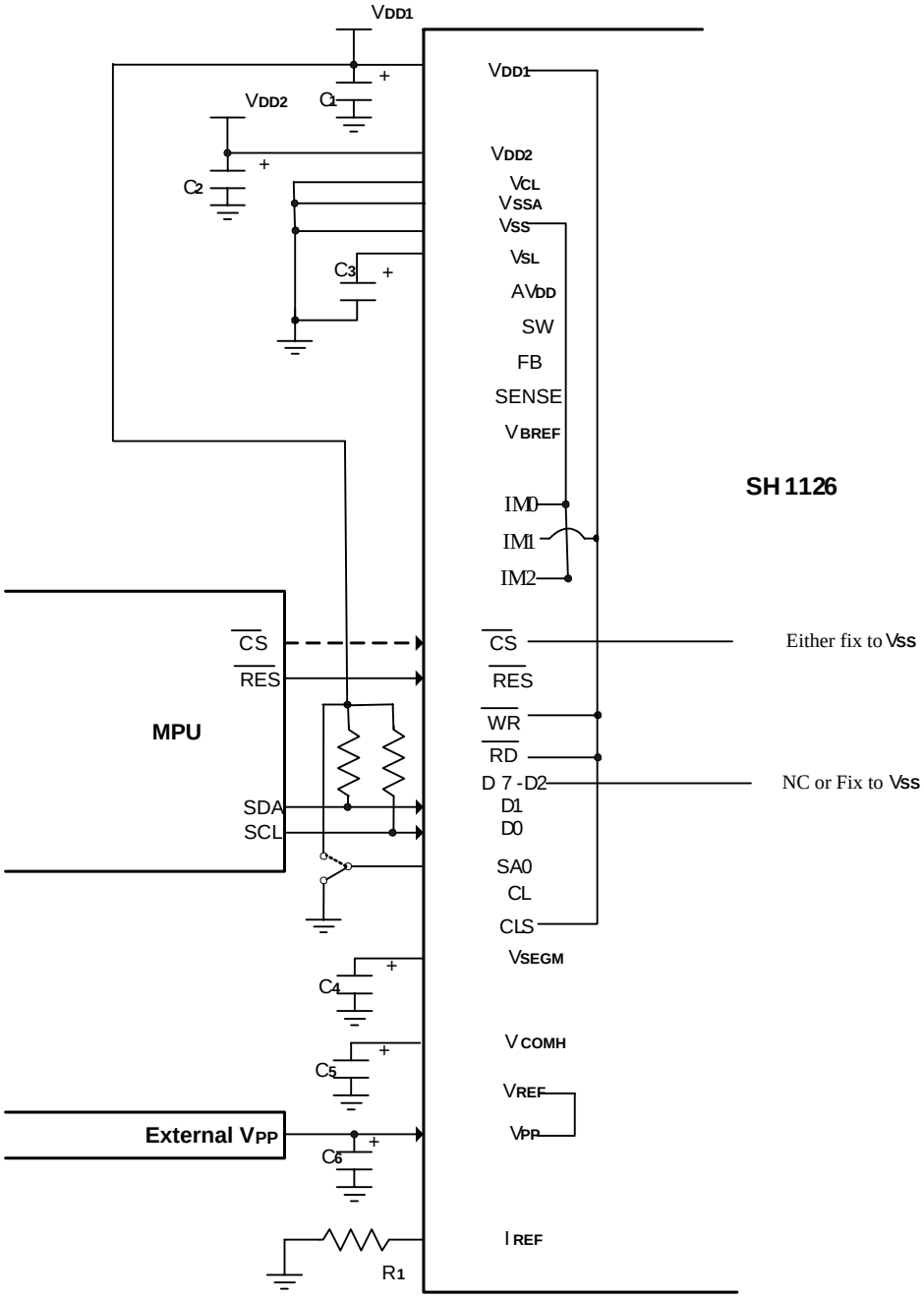


Figure 20

Note:

C1 – C6: 4.7μF
R1: about 620kΩ, R1 = (Voltage at IREF - VSS)/IREF
The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(Vss) or 1 (VDD1).
WR and RD are not used in I²C mode, should fix to Vss or VDD1.
CS can fix to Vss in I²C mode.
The positive supply of pull-up resistor must equal to the value of VDD1.

DC-DC:

Below application circuit is an example for the input voltage of 3V AV_{DD} to generate V_{PP} of about 12V@10mA-25mA application.

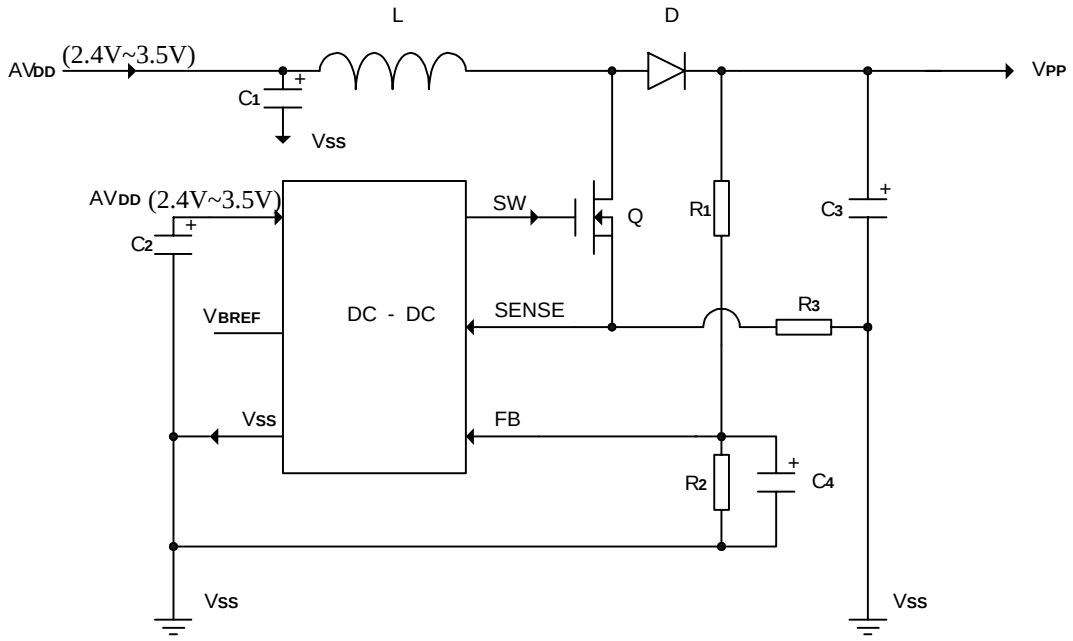


Figure 21

Symbol	Value	Recommendation
L	10μH	LQH3C100K24
D	SCHOTTKY DIODE	20V@0.5A, MBR0520
Q	MOSFET	N-FET with low $R_{DS(ON)}$ and low V_{TH}, MGSF1N02LT1
R_1	820kΩ	1%, 1/8W
R_2	100kΩ	1%, 1/8W
R_3	0.12Ω	1%, 1/2W
C_1	22μF	Ceramic / 16V
C_2	0.1 - 1μF	Ceramic/16V
C_3	10μF	Low ESR/16V
C_4	56pF	Ceramic/16V

Ordering Information

Part No.	Package
SH1126G	Gold bump on chip tray

Data Sheet History

Version	Contents	Date
2.0	P37：Modify the I_{OL} of VDD1<2V	Oct. 2013
1.0	Original	Jun. 2013