SOLOMON SYSTECH
SEMICONDUCTOR TECHNICAL DATA

SSD1326

Advance Information

256x32, 16 Gray Scale Dot Matrix
OLED/PLED Segment/Common Driver with Controller
CMOS

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SOLOMON SYSTECH

CONTENTS

TABLES

FIGURES

1   GENERAL DESCRIPTION

SSD1326 is a single-chip CMOS OLED/PLED driver with controller for 16 gray scale levels organic / polymer light emitting diode dot-matrix graphic display system. SSD1326 consists of 256 segments, 32 commons. This IC is designed for Common Cathode type OLED / PLED panel.

SSD1326 displays data directly from its internal 256 x 32 x 4 bits Graphic Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable I^2C Interface, 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

2   FEATURES

- Support max. 256 x 32 matrix panel
- Power supply: V_{DD} = 2.4V -3.5V
                     V_{DDIO} = 1.7V - V_{DD}
                     V_{CC} = 9.0V - 15.0V
- OLED driving output voltage, 15V maximum
- Maximum segment source current: 100uA
- Dual Common maximum sink current: 25mA
- Embedded 256 x 32 x 4 bit SRAM display buffer
- 256 steps contrast current control
- Selectable to either 16 gray scale or mono display
- Internal oscillator
- Programmable frame rate
- Continuous horizontal scrolling with flexible scrolling window
- Pin selectable MCU interface
    o I^2C interface
    o 8-bit 6800-series parallel interface
    o 8-bit 8080-series parallel interface
    o Serial Peripheral Interface
- Wide range of operating temperature: -40 to 85 °C

3   ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1326Z	256	32 dual	COG	Page 8	Min SEG pad pitch : 40.08um Min COM pad pitch : 45um
SSD1326U	256	32 dual	COF	Page 14 ,57	− Punched COF, Sn plating − This package is for I^2C interface and the slave address is set as b0111100 (SA0=0). − SEG lead pitch 0.11mm x0.999=0.10989mm − COM lead pitch 0.11mmx0.999=0.10989mm
SSD1326U1	256	32 dual	COF	Page 16, 60	− Punched COF, Au plating − This package is for I^2C interface and the slave address is set as b0111100 (SA0=0). − SEG lead pitch 0.11mm x0.999=0.10989mm − COM lead pitch 0.11mmx0.999=0.10989mm

4 BLOCK DIAGRAM

Figure 4-1 : SSD1326 Block Diagram
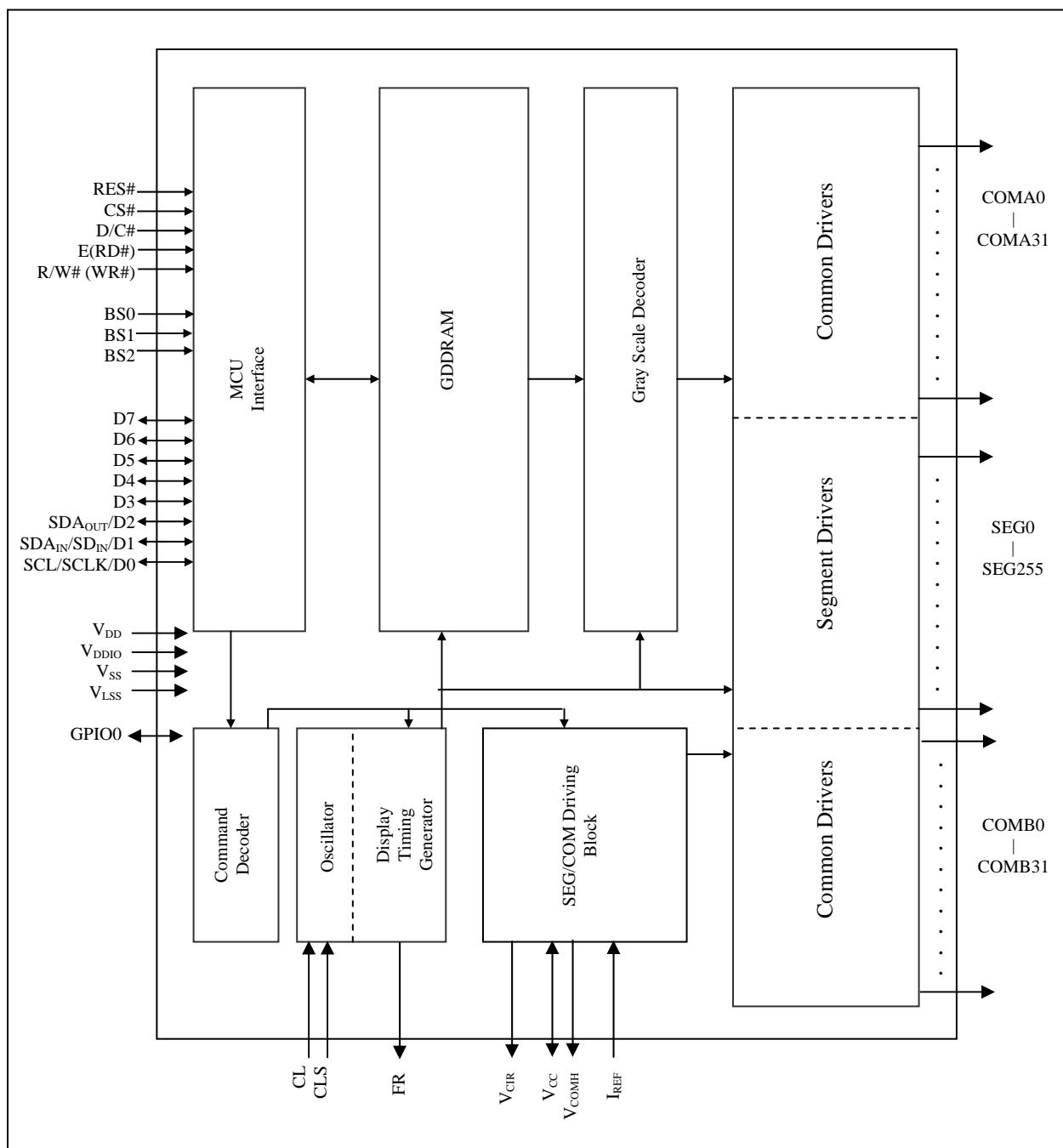
5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1326Z Die Drawing

Pad 1 ——→

SSD1326Z
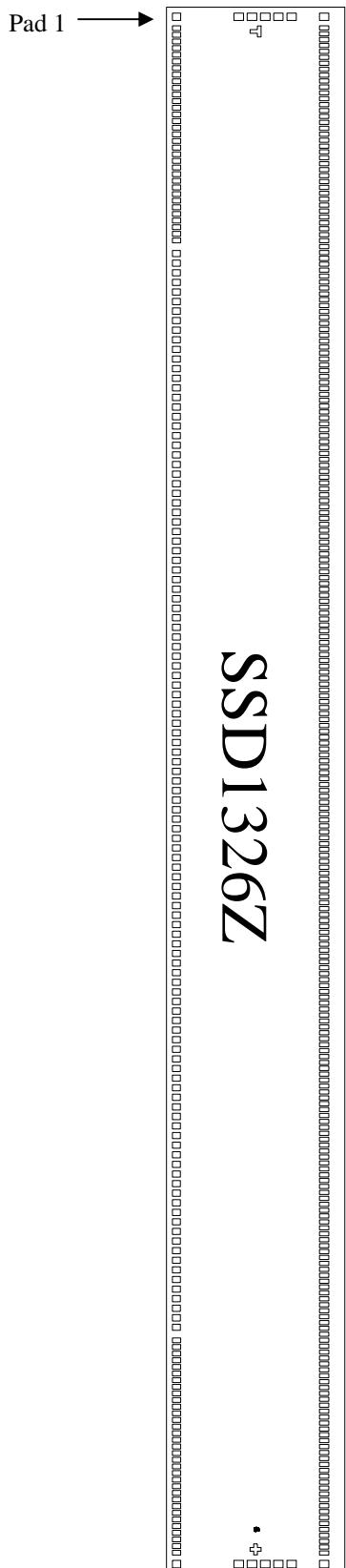
Alignment key	X-pos	Y-pos	Size
T shape	-5145.000	0.000	75um x 75um
+ shape	5145.000	0.000	75um x 75um

Die size	10620um x 1210um
Die thickness	457um +/- 25um
Min I/O pad pitch	65um
Min SEG pad pitch	40.08um
Min COM pad pitch	45um
Bump height Nominal	15um

Bump Size

Pad#	X(um)	Y(um)
188-315, 319-446	28	64.3
316-318,	28	64.3
2-33, 149-180	32	56.26
34, 148	32	56.26
36-146	42	55
35, 147	42	55
187, 447	50	64.3
1,181	50	56.26
182-186, 448-452	50	64.3

Y

Pad# 447   Pad#187

SSD1326   X

Pad#1   Pad#181
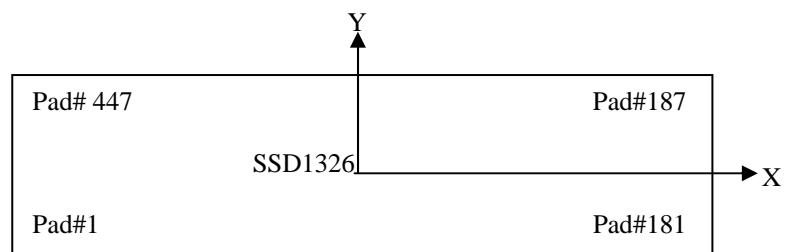
Bump pad face up

Figure 5-2 : SSD1326Z Alignment Mark Dimensions
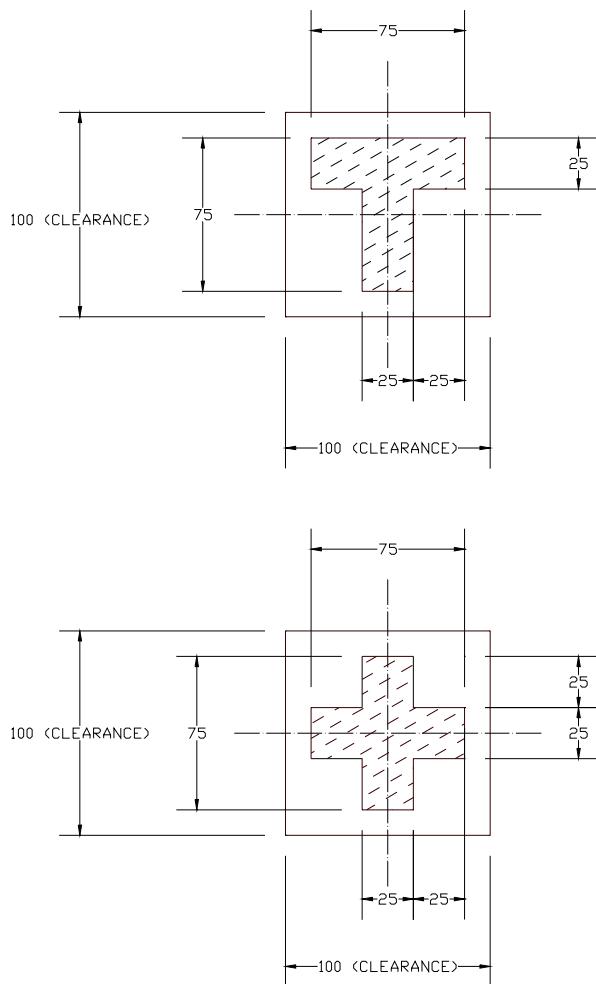
Table 5-1 : SSD1326Z Bump Die Pad Coordinates

Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos
1	DUMMY	-5245	-536.87	81	VCC	-649.74	-537.5	161	COMA19	4312.86	-536.87
2	COMB0	-5167.86	-536.87	82	VDDIO	-584.74	-537.5	162	COMA18	4357.86	-536.87
3	COMB1	-5122.86	-536.87	83	VDDIO	-519.74	-537.5	163	COMA17	4402.86	-536.87
4	COMB2	-5077.86	-536.87	84	VDDIO	-454.74	-537.5	164	COMA16	4447.86	-536.87
5	COMB3	-5032.86	-536.87	85	VSS	-389.74	-537.5	165	COMA15	4492.86	-536.87
6	COMB4	-4987.86	-536.87	86	GPIO0	-324.74	-537.5	166	COMA14	4537.86	-536.87
7	COMB5	-4942.86	-536.87	87	VDDIO	-259.74	-537.5	167	COMA13	4582.86	-536.87
8	COMB6	-4897.86	-536.87	88	BS0	-194.74	-537.5	168	COMA12	4627.86	-536.87
9	COMB7	-4852.86	-536.87	89	VSS	-129.74	-537.5	169	COMA11	4672.86	-536.87
10	COMB8	-4807.86	-536.87	90	VSS	-64.74	-537.5	170	COMA10	4717.86	-536.87
11	COMB9	-4762.86	-536.87	91	VSS	0.26	-537.5	171	COMA9	4762.86	-536.87
12	COMB10	-4717.86	-536.87	92	VSS	65.26	-537.5	172	COMA8	4807.86	-536.87
13	COMB11	-4672.86	-536.87	93	BS1	130.26	-537.5	173	COMA7	4852.86	-536.87
14	COMB12	-4627.86	-536.87	94	VDDIO	195.26	-537.5	174	COMA6	4897.86	-536.87
15	COMB13	-4582.86	-536.87	95	BS2	260.26	-537.5	175	COMA5	4942.86	-536.87
16	COMB14	-4537.86	-536.87	96	VSS	325.26	-537.5	176	COMA4	4987.86	-536.87
17	COMB15	-4492.86	-536.87	97	FR	390.26	-537.5	177	COMA3	5032.86	-536.87
18	COMB16	-4447.86	-536.87	98	CL	455.26	-537.5	178	COMA2	5077.86	-536.87
19	COMB17	-4402.86	-536.87	99	VDDIO	520.26	-537.5	179	COMA1	5122.86	-536.87
20	COMB18	-4357.86	-536.87	100	CS#	585.26	-537.5	180	COMA0	5167.86	-536.87
21	COMB19	-4312.86	-536.87	101	RES#	650.26	-537.5	181	DUMMY	5245	-536.87
22	COMB20	-4267.86	-536.87	102	D/C#	715.26	-537.5	182	DUMMY	5245	-114.75
23	COMB21	-4222.86	-536.87	103	VSS	780.26	-537.5	183	DUMMY	5245	-24.75
24	COMB22	-4177.86	-536.87	104	R/W#(WR#)	845.26	-537.5	184	DUMMY	5245	65.25
25	COMB23	-4132.86	-536.87	105	E(RD#)	910.26	-537.5	185	DUMMY	5245	155.25
26	COMB24	-4087.86	-536.87	106	VDDIO	975.26	-537.5	186	DUMMY	5245	245.25
27	COMB25	-4042.86	-536.87	107	VDDIO	1040.26	-537.5	187	DUMMY	5245	465.15
28	COMB26	-3997.86	-536.87	108	VDD	1105.26	-537.5	188	SEG0	5170.26	465.15
29	COMB27	-3952.86	-536.87	109	VDD	1170.26	-537.5	189	SEG1	5130.18	465.15
30	COMB28	-3907.86	-536.87	110	VCC	1235.26	-537.5	190	SEG2	5090.1	465.15
31	COMB29	-3862.86	-536.87	111	VCC	1300.26	-537.5	191	SEG3	5050.02	465.15
32	COMB30	-3817.86	-536.87	112	VCC	1365.26	-537.5	192	SEG4	5009.94	465.15
33	COMB31	-3772.86	-536.87	113	VLSS	1430.26	-537.5	193	SEG5	4969.86	465.15
34	DUMMY	-3727.86	-536.87	114	VLSS	1495.26	-537.5	194	SEG6	4929.78	465.15
35	DUMMY	-3639.74	-537.5	115	VDDIO	1560.26	-537.5	195	SEG7	4889.7	465.15
36	VCC	-3574.74	-537.5	116	VSS	1625.26	-537.5	196	SEG8	4849.62	465.15
37	VCC	-3509.74	-537.5	117	D0	1690.26	-537.5	197	SEG9	4809.54	465.15
38	VCC	-3444.74	-537.5	118	D1	1755.26	-537.5	198	SEG10	4769.46	465.15
39	VCOMH	-3379.74	-537.5	119	D2	1820.26	-537.5	199	SEG11	4729.38	465.15
40	VCOMH	-3314.74	-537.5	120	D3	1885.26	-537.5	200	SEG12	4689.3	465.15
41	VCOMH	-3249.74	-537.5	121	VSS	1950.26	-537.5	201	SEG13	4649.22	465.15
42	IREF	-3184.74	-537.5	122	D4	2015.26	-537.5	202	SEG14	4609.14	465.15
43	VLSS	-3119.74	-537.5	123	D5	2080.26	-537.5	203	SEG15	4569.06	465.15
44	VLSS	-3054.74	-537.5	124	D6	2145.26	-537.5	204	SEG16	4528.98	465.15
45	VLSS	-2989.74	-537.5	125	D7	2210.26	-537.5	205	SEG17	4488.9	465.15
46	VDD	-2924.74	-537.5	126	VSS	2275.26	-537.5	206	SEG18	4448.82	465.15
47	VDD	-2859.74	-537.5	127	CLS	2340.26	-537.5	207	SEG19	4408.74	465.15
48	VDDIO	-2794.74	-537.5	128	VDDIO	2405.26	-537.5	208	SEG20	4368.66	465.15
49	VDDIO	-2729.74	-537.5	129	VDDIO	2470.26	-537.5	209	SEG21	4328.58	465.15
50	VDDIO	-2664.74	-537.5	130	VDD	2535.26	-537.5	210	SEG22	4288.5	465.15
51	VDDIO	-2599.74	-537.5	131	VDD	2600.26	-537.5	211	SEG23	4248.42	465.15
52	VSS	-2534.74	-537.5	132	VDD	2665.26	-537.5	212	SEG24	4208.34	465.15
53	TR8	-2469.74	-537.5	133	VSS	2730.26	-537.5	213	SEG25	4168.26	465.15
54	TR7	-2404.74	-537.5	134	VSS	2795.26	-537.5	214	SEG26	4128.18	465.15
55	TR6	-2339.74	-537.5	135	VLSS	2860.26	-537.5	215	SEG27	4088.1	465.15
56	TR5	-2274.74	-537.5	136	VLSS	2925.26	-537.5	216	SEG28	4048.02	465.15
57	VSS	-2209.74	-537.5	137	VLSS	2990.26	-537.5	217	SEG29	4007.94	465.15
58	TR4	-2144.74	-537.5	138	VCOMH	3055.26	-537.5	218	SEG30	3967.86	465.15
59	TR3	-2079.74	-537.5	139	VCOMH	3120.26	-537.5	219	SEG31	3927.78	465.15
60	TR2	-2014.74	-537.5	140	VCOMH	3185.26	-537.5	220	SEG32	3887.7	465.15
61	TR1	-1949.74	-537.5	141	VCC	3250.26	-537.5	221	SEG33	3847.62	465.15
62	TR0	-1884.74	-537.5	142	VCC	3315.26	-537.5	222	SEG34	3807.54	465.15
63	VLSS	-1819.74	-537.5	143	VCC	3380.26	-537.5	223	SEG35	3767.46	465.15
64	VLSS	-1754.74	-537.5	144	VCC	3445.26	-537.5	224	SEG36	3727.38	465.15
65	VLSS	-1689.74	-537.5	145	VCC	3510.26	-537.5	225	SEG37	3687.3	465.15
66	VSS	-1624.74	-537.5	146	VCC	3575.26	-537.5	226	SEG38	3647.22	465.15
67	VSS	-1559.74	-537.5	147	DUMMY	3640.26	-537.5	227	SEG39	3607.14	465.15
68	VSS	-1494.74	-537.5	148	DUMMY	3727.86	-536.87	228	SEG40	3567.06	465.15
69	BGGND	-1429.74	-537.5	149	COMA31	3772.86	-536.87	229	SEG41	3526.98	465.15
70	VBREF	-1364.74	-537.5	150	COMA30	3817.86	-536.87	230	SEG42	3486.9	465.15
71	VCIR	-1299.74	-537.5	151	COMA29	3862.86	-536.87	231	SEG43	3446.82	465.15
72	VCIR	-1234.74	-537.5	152	COMA28	3907.86	-536.87	232	SEG44	3406.74	465.15
73	VCIR	-1169.74	-537.5	153	COMA27	3952.86	-536.87	233	SEG45	3366.66	465.15
74	VCIR	-1104.74	-537.5	154	COMA26	3997.86	-536.87	234	SEG46	3326.58	465.15
75	VDD	-1039.74	-537.5	155	COMA25	4042.86	-536.87	235	SEG47	3286.5	465.15
76	VDD	-974.74	-537.5	156	COMA24	4087.86	-536.87	236	SEG48	3246.42	465.15
77	VDD	-909.74	-537.5	157	COMA23	4132.86	-536.87	237	SEG49	3206.34	465.15
78	VDD	-844.74	-537.5	158	COMA22	4177.86	-536.87	238	SEG50	3166.26	465.15
79	VCC	-779.74	-537.5	159	COMA21	4222.86	-536.87	239	SEG51	3126.18	465.15
80	VCC	-714.74	-537.5	160	COMA20	4267.86	-536.87	240	SEG52	3086.1	465.15

Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos
241	SEG53	3046.02	465.15	321	SEG130	-160.38	465.15	401	SEG210	-3366.78	465.15
242	SEG54	3005.94	465.15	322	SEG131	-200.46	465.15	402	SEG211	-3406.86	465.15
243	SEG55	2965.86	465.15	323	SEG132	-240.54	465.15	403	SEG212	-3446.94	465.15
244	SEG56	2925.78	465.15	324	SEG133	-280.62	465.15	404	SEG213	-3487.02	465.15
245	SEG57	2885.7	465.15	325	SEG134	-320.7	465.15	405	SEG214	-3527.1	465.15
246	SEG58	2845.62	465.15	326	SEG135	-360.78	465.15	406	SEG215	-3567.18	465.15
247	SEG59	2805.54	465.15	327	SEG136	-400.86	465.15	407	SEG216	-3607.26	465.15
248	SEG60	2765.46	465.15	328	SEG137	-440.94	465.15	408	SEG217	-3647.34	465.15
249	SEG61	2725.38	465.15	329	SEG138	-481.02	465.15	409	SEG218	-3687.42	465.15
250	SEG62	2685.3	465.15	330	SEG139	-521.1	465.15	410	SEG219	-3727.5	465.15
251	SEG63	2645.22	465.15	331	SEG140	-561.18	465.15	411	SEG220	-3767.58	465.15
252	SEG64	2605.14	465.15	332	SEG141	-601.26	465.15	412	SEG221	-3807.66	465.15
253	SEG65	2565.06	465.15	333	SEG142	-641.34	465.15	413	SEG222	-3847.74	465.15
254	SEG66	2524.98	465.15	334	SEG143	-681.42	465.15	414	SEG223	-3887.82	465.15
255	SEG67	2484.9	465.15	335	SEG144	-721.5	465.15	415	SEG224	-3927.9	465.15
256	SEG68	2444.82	465.15	336	SEG145	-761.58	465.15	416	SEG225	-3967.98	465.15
257	SEG69	2404.74	465.15	337	SEG146	-801.66	465.15	417	SEG226	-4008.06	465.15
258	SEG70	2364.66	465.15	338	SEG147	-841.74	465.15	418	SEG227	-4048.14	465.15
259	SEG71	2324.58	465.15	339	SEG148	-881.82	465.15	419	SEG228	-4088.22	465.15
260	SEG72	2284.5	465.15	340	SEG149	-921.9	465.15	420	SEG229	-4128.3	465.15
261	SEG73	2244.42	465.15	341	SEG150	-961.98	465.15	421	SEG230	-4168.38	465.15
262	SEG74	2204.34	465.15	342	SEG151	-1002.06	465.15	422	SEG231	-4208.46	465.15
263	SEG75	2164.26	465.15	343	SEG152	-1042.14	465.15	423	SEG232	-4248.54	465.15
264	SEG76	2124.18	465.15	344	SEG153	-1082.22	465.15	424	SEG233	-4288.62	465.15
265	SEG77	2084.1	465.15	345	SEG154	-1122.3	465.15	425	SEG234	-4328.7	465.15
266	SEG78	2044.02	465.15	346	SEG155	-1162.38	465.15	426	SEG235	-4368.78	465.15
267	SEG79	2003.94	465.15	347	SEG156	-1202.46	465.15	427	SEG236	-4408.86	465.15
268	SEG80	1963.86	465.15	348	SEG157	-1242.54	465.15	428	SEG237	-4448.94	465.15
269	SEG81	1923.78	465.15	349	SEG158	-1282.62	465.15	429	SEG238	-4489.02	465.15
270	SEG82	1883.7	465.15	350	SEG159	-1322.7	465.15	430	SEG239	-4529.1	465.15
271	SEG83	1843.62	465.15	351	SEG160	-1362.78	465.15	431	SEG240	-4569.18	465.15
272	SEG84	1803.54	465.15	352	SEG161	-1402.86	465.15	432	SEG241	-4609.26	465.15
273	SEG85	1763.46	465.15	353	SEG162	-1442.94	465.15	433	SEG242	-4649.34	465.15
274	SEG86	1723.38	465.15	354	SEG163	-1483.02	465.15	434	SEG243	-4689.42	465.15
275	SEG87	1683.3	465.15	355	SEG164	-1523.1	465.15	435	SEG244	-4729.5	465.15
276	SEG88	1643.22	465.15	356	SEG165	-1563.18	465.15	436	SEG245	-4769.58	465.15
277	SEG89	1603.14	465.15	357	SEG166	-1603.26	465.15	437	SEG246	-4809.66	465.15
278	SEG90	1563.06	465.15	358	SEG167	-1643.34	465.15	438	SEG247	-4849.74	465.15
279	SEG91	1522.98	465.15	359	SEG168	-1683.42	465.15	439	SEG248	-4889.82	465.15
280	SEG92	1482.9	465.15	360	SEG169	-1723.5	465.15	440	SEG249	-4929.9	465.15
281	SEG93	1442.82	465.15	361	SEG170	-1763.58	465.15	441	SEG250	-4969.98	465.15
282	SEG94	1402.74	465.15	362	SEG171	-1803.66	465.15	442	SEG251	-5010.06	465.15
283	SEG95	1362.66	465.15	363	SEG172	-1843.74	465.15	443	SEG252	-5050.14	465.15
284	SEG96	1322.58	465.15	364	SEG173	-1883.82	465.15	444	SEG253	-5090.22	465.15
285	SEG97	1282.5	465.15	365	SEG174	-1923.9	465.15	445	SEG254	-5130.3	465.15
286	SEG98	1242.42	465.15	366	SEG175	-1963.98	465.15	446	SEG255	-5170.38	465.15
287	SEG99	1202.34	465.15	367	SEG176	-2004.06	465.15	447	DUMMY	-5245	465.15
288	SEG100	1162.26	465.15	368	SEG177	-2044.14	465.15	448	DUMMY	-5245	245.25
289	SEG101	1122.18	465.15	369	SEG178	-2084.22	465.15	449	DUMMY	-5245	155.25
290	SEG102	1082.1	465.15	370	SEG179	-2124.3	465.15	450	DUMMY	-5245	65.25
291	SEG103	1042.02	465.15	371	SEG180	-2164.38	465.15	451	DUMMY	-5245	-24.75
292	SEG104	1001.94	465.15	372	SEG181	-2204.46	465.15	452	DUMMY	-5245	-114.75
293	SEG105	961.86	465.15	373	SEG182	-2244.54	465.15				
294	SEG106	921.78	465.15	374	SEG183	-2284.62	465.15				
295	SEG107	881.7	465.15	375	SEG184	-2324.7	465.15				
296	SEG108	841.62	465.15	376	SEG185	-2364.78	465.15				
297	SEG109	801.54	465.15	377	SEG186	-2404.86	465.15				
298	SEG110	761.46	465.15	378	SEG187	-2444.94	465.15				
299	SEG111	721.38	465.15	379	SEG188	-2485.02	465.15				
300	SEG112	681.3	465.15	380	SEG189	-2525.1	465.15				
301	SEG113	641.22	465.15	381	SEG190	-2565.18	465.15				
302	SEG114	601.14	465.15	382	SEG191	-2605.26	465.15				
303	SEG115	561.06	465.15	383	SEG192	-2645.34	465.15				
304	SEG116	520.98	465.15	384	SEG193	-2685.42	465.15				
305	SEG117	480.9	465.15	385	SEG194	-2725.5	465.15				
306	SEG118	440.82	465.15	386	SEG195	-2765.58	465.15				
307	SEG119	400.74	465.15	387	SEG196	-2805.66	465.15				
308	SEG120	360.66	465.15	388	SEG197	-2845.74	465.15				
309	SEG121	320.58	465.15	389	SEG198	-2885.82	465.15				
310	SEG122	280.5	465.15	390	SEG199	-2925.9	465.15				
311	SEG123	240.42	465.15	391	SEG200	-2965.98	465.15				
312	SEG124	200.34	465.15	392	SEG201	-3006.06	465.15				
313	SEG125	160.26	465.15	393	SEG202	-3046.14	465.15				
314	SEG126	120.18	465.15	394	SEG203	-3086.22	465.15				
315	SEG127	80.1	465.15	395	SEG204	-3126.3	465.15				
316	DUMMY	40.02	465.15	396	SEG205	-3166.38	465.15				
317	DUMMY	-0.06	465.15	397	SEG206	-3206.46	465.15				
318	DUMMY	-40.14	465.15	398	SEG207	-3246.54	465.15				
319	SEG128	-80.22	465.15	399	SEG208	-3286.62	465.15				
320	SEG129	-120.3	465.15	400	SEG209	-3326.7	465.15				

6 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
IO = Bi-directional (input/output)	Pull HIGH= connect to V_{DDIO}
P = Power pin	

Table 6-1 : Pin Descriptions

Pin Name	Pin Type	Description
RES#	I	This pin is reset signal input. When the pin is LOW, initialization of the chip is executed. Keep this pin HIGH during normal operation.
CS#	I	This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled LOW.
D/C#	I	This pin is Data/Command control pin. When the pin is pulled HIGH and serial interface mode is selected, the data at SD_{IN} is treated as data. When the pin is pulled LOW, the data at SD_{IN} will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection.
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled LOW and the chip is selected.
R/W# (WR#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode will be carried out when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
D[7:0]	IO	These is 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D1 will be the serial data input, SD_{IN}, and D_0 will be the serial clock input, SCLK. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
BS[2:0]	I	MCU bus interface selection pins.<table><tr><td>Pin Name</td><td>I^2C Interface</td><td>6800-parallel interface (8 bit)</td><td>8080-parallel interface (8 bit)</td><td>Serial interface</td></tr><tr><td>BS0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>BS1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>BS2</td><td>0</td><td>1</td><td>1</td><td>0</td></tr></table>
V_{DDIO}	P	This pin is a power supply pin of I/O buffer. It should be connected to V_{DD} or external source. All I/O signal should have voltage high reference to V_{DDIO}. When I/O signal pins (BS0, CLS, CL, interface signals…) pull HIGH, they should be connected to V_{DDIO}.
V_{DD}	P	Power Supply pin. It must be connected to external source.
$V_{SS,} V_{LSS}$	P	These pins are ground pin and also act as ground reference for the logic pins. They must be connected to external ground.

Pin Name	Pin Type	Description
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This pin is internal clock enable. When this pin is pulled HIGH, internal oscillator is selected. The internal clock will be disabled when it is pulled LOW, an external clock source must be connected to CL pin for normal operation.
V_{CC}	P	This is the most positive voltage supply pin of the chip. It is supplied either by external high voltage source.
V_{COMH}	P	A capacitor should be connected between this pin and V_{SS}.
V_{CIR}	O	This is a reserved pin. It should be kept NC (i.e. Float during normal operation).
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieve to prevent tearing effect. Keep NC if not used.
GPIO0	IO	This is reserved pin. It should be kept NC (i.e. Float during normal operation).
I_{REF}	I	This pin is the segment output current reference pin. I_{SEG} is derived from I_{REF}. A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA.
V_{BREF}	-	This is a reserved pin. It should be floated.
BGGND	P	This is a reserved pin. It should be connected to V_{SS}.
TR[8:0]	-	This is a reserved pin. It should be floated.
COM0 ~ COM31	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF. SSD1326 is in dual COM: COM0 = COMA0 and COMB0. COM1 = COMA1 and COMB1. COM2 = COMA2 and COMB2. : COM29 = COMA29 and COMB29. COM30 = COMA30 and COMB30. COM31 = COMA31 and COMB31
SEG0 ~ SEG255	O	These pins provide the OLED segment driving signals. These pins are in high impedance state when display is OFF.
Dummy	-	Dummy pin.

7 PIN ARRANGEMENT

7.1 SSD1326U pin assignment

Figure 7-1 : SSD1326U Pin Assignment

Table 7-1 : SSD1326U Pin Assignment Table

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VCC	81	SEG230	161	SEG150	241	SEG70	321	NC
2	VCOMH	82	SEG229	162	SEG149	242	SEG69	322	NC
3	NC	83	SEG228	163	SEG148	243	SEG68	323	COMA0
4	SDA	84	SEG227	164	SEG147	244	SEG67	324	COMA1
5	SCL	85	SEG226	165	SEG146	245	SEG66	325	COMA2
6	RES#	86	SEG225	166	SEG145	246	SEG65	326	COMA3
7	VDDIO	87	SEG224	167	SEG144	247	SEG64	327	COMA4
8	VDD	88	SEG223	168	SEG143	248	SEG63	328	COMA5
9	VSS	89	SEG222	169	SEG142	249	SEG62	329	COMA6
10	IREF	90	SEG221	170	SEG141	250	SEG61	330	COMA7
11	NC	91	SEG220	171	SEG140	251	SEG60	331	COMA8
12	NC	92	SEG219	172	SEG139	252	SEG59	332	COMA9
13	COMB31	93	SEG218	173	SEG138	253	SEG58	333	COMA10
14	COMB30	94	SEG217	174	SEG137	254	SEG57	334	COMA11
15	COMB29	95	SEG216	175	SEG136	255	SEG56	335	COMA12
16	COMB28	96	SEG215	176	SEG135	256	SEG55	336	COMA13
17	COMB27	97	SEG214	177	SEG134	257	SEG54	337	COMA14
18	COMB26	98	SEG213	178	SEG133	258	SEG53	338	COMA15
19	COMB25	99	SEG212	179	SEG132	259	SEG52	339	COMA16
20	COMB24	100	SEG211	180	SEG131	260	SEG51	340	COMA17
21	COMB23	101	SEG210	181	SEG130	261	SEG50	341	COMA18
22	COMB22	102	SEG209	182	SEG129	262	SEG49	342	COMA19
23	COMB21	103	SEG208	183	SEG128	263	SEG48	343	COMA20
24	COMB20	104	SEG207	184	SEG127	264	SEG47	344	COMA21
25	COMB19	105	SEG206	185	SEG126	265	SEG46	345	COMA22
26	COMB18	106	SEG205	186	SEG125	266	SEG45	346	COMA23
27	COMB17	107	SEG204	187	SEG124	267	SEG44	347	COMA24
28	COMB16	108	SEG203	188	SEG123	268	SEG43	348	COMA25
29	COMB15	109	SEG202	189	SEG122	269	SEG42	349	COMA26
30	COMB14	110	SEG201	190	SEG121	270	SEG41	350	COMA27
31	COMB13	111	SEG200	191	SEG120	271	SEG40	351	COMA28
32	COMB12	112	SEG199	192	SEG119	272	SEG39	352	COMA29
33	COMB11	113	SEG198	193	SEG118	273	SEG38	353	COMA30
34	COMB10	114	SEG197	194	SEG117	274	SEG37	354	COMA31
35	COMB9	115	SEG196	195	SEG116	275	SEG36	355	NC
36	COMB8	116	SEG195	196	SEG115	276	SEG35	356	NC
37	COMB7	117	SEG194	197	SEG114	277	SEG34		
38	COMB6	118	SEG193	198	SEG113	278	SEG33		
39	COMB5	119	SEG192	199	SEG112	279	SEG32		
40	COMB4	120	SEG191	200	SEG111	280	SEG31		
41	COMB3	121	SEG190	201	SEG110	281	SEG30		
42	COMB2	122	SEG189	202	SEG109	282	SEG29		
43	COMB1	123	SEG188	203	SEG108	283	SEG28		
44	COMB0	124	SEG187	204	SEG107	284	SEG27		
45	NC	125	SEG186	205	SEG106	285	SEG26		
46	NC	126	SEG185	206	SEG105	286	SEG25		
47	NC	127	SEG184	207	SEG104	287	SEG24		
48	NC	128	SEG183	208	SEG103	288	SEG23		
49	NC	129	SEG182	209	SEG102	289	SEG22		
50	NC	130	SEG181	210	SEG101	290	SEG21		
51	NC	131	SEG180	211	SEG100	291	SEG20		
52	NC	132	SEG179	212	SEG99	292	SEG19		
53	NC	133	SEG178	213	SEG98	293	SEG18		
54	NC	134	SEG177	214	SEG97	294	SEG17		
55	NC	135	SEG176	215	SEG96	295	SEG16		
56	SEG255	136	SEG175	216	SEG95	296	SEG15		
57	SEG254	137	SEG174	217	SEG94	297	SEG14		
58	SEG253	138	SEG173	218	SEG93	298	SEG13		
59	SEG252	139	SEG172	219	SEG92	299	SEG12		
60	SEG251	140	SEG171	220	SEG91	300	SEG11		
61	SEG250	141	SEG170	221	SEG90	301	SEG10		
62	SEG249	142	SEG169	222	SEG89	302	SEG9		
63	SEG248	143	SEG168	223	SEG88	303	SEG8		
64	SEG247	144	SEG167	224	SEG87	304	SEG7		
65	SEG246	145	SEG166	225	SEG86	305	SEG6		
66	SEG245	146	SEG165	226	SEG85	306	SEG5		
67	SEG244	147	SEG164	227	SEG84	307	SEG4		
68	SEG243	148	SEG163	228	SEG83	308	SEG3		
69	SEG242	149	SEG162	229	SEG82	309	SEG2		
70	SEG241	150	SEG161	230	SEG81	310	SEG1		
71	SEG240	151	SEG160	231	SEG80	311	SEG0		
72	SEG239	152	SEG159	232	SEG79	312	NC		
73	SEG238	153	SEG158	233	SEG78	313	NC		
74	SEG237	154	SEG157	234	SEG77	314	NC		
75	SEG236	155	SEG156	235	SEG76	315	NC		
76	SEG235	156	SEG155	236	SEG75	316	NC		
77	SEG234	157	SEG154	237	SEG74	317	NC		
78	SEG233	158	SEG153	238	SEG73	318	NC		
79	SEG232	159	SEG152	239	SEG72	319	NC		
80	SEG231	160	SEG151	240	SEG71	320	NC		

7.2   SSD1326U1 pin assignment

Figure 7-2 : SSD1326U1 Pin Assignment

Table 7-2 : SSD1326U1 Pin Assignment Table

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VCC	81	SEG230	161	SEG150	241	SEG70	321	NC
2	VCOMH	82	SEG229	162	SEG149	242	SEG69	322	NC
3	NC	83	SEG228	163	SEG148	243	SEG68	323	COMA0
4	SDA	84	SEG227	164	SEG147	244	SEG67	324	COMA1
5	SCL	85	SEG226	165	SEG146	245	SEG66	325	COMA2
6	RES#	86	SEG225	166	SEG145	246	SEG65	326	COMA3
7	VDD	87	SEG224	167	SEG144	247	SEG64	327	COMA4
8	NC	88	SEG223	168	SEG143	248	SEG63	328	COMA5
9	VSS	89	SEG222	169	SEG142	249	SEG62	329	COMA6
10	IREF	90	SEG221	170	SEG141	250	SEG61	330	COMA7
11	NC	91	SEG220	171	SEG140	251	SEG60	331	COMA8
12	NC	92	SEG219	172	SEG139	252	SEG59	332	COMA9
13	COMB31	93	SEG218	173	SEG138	253	SEG58	333	COMA10
14	COMB30	94	SEG217	174	SEG137	254	SEG57	334	COMA11
15	COMB29	95	SEG216	175	SEG136	255	SEG56	335	COMA12
16	COMB28	96	SEG215	176	SEG135	256	SEG55	336	COMA13
17	COMB27	97	SEG214	177	SEG134	257	SEG54	337	COMA14
18	COMB26	98	SEG213	178	SEG133	258	SEG53	338	COMA15
19	COMB25	99	SEG212	179	SEG132	259	SEG52	339	COMA16
20	COMB24	100	SEG211	180	SEG131	260	SEG51	340	COMA17
21	COMB23	101	SEG210	181	SEG130	261	SEG50	341	COMA18
22	COMB22	102	SEG209	182	SEG129	262	SEG49	342	COMA19
23	COMB21	103	SEG208	183	SEG128	263	SEG48	343	COMA20
24	COMB20	104	SEG207	184	SEG127	264	SEG47	344	COMA21
25	COMB19	105	SEG206	185	SEG126	265	SEG46	345	COMA22
26	COMB18	106	SEG205	186	SEG125	266	SEG45	346	COMA23
27	COMB17	107	SEG204	187	SEG124	267	SEG44	347	COMA24
28	COMB16	108	SEG203	188	SEG123	268	SEG43	348	COMA25
29	COMB15	109	SEG202	189	SEG122	269	SEG42	349	COMA26
30	COMB14	110	SEG201	190	SEG121	270	SEG41	350	COMA27
31	COMB13	111	SEG200	191	SEG120	271	SEG40	351	COMA28
32	COMB12	112	SEG199	192	SEG119	272	SEG39	352	COMA29
33	COMB11	113	SEG198	193	SEG118	273	SEG38	353	COMA30
34	COMB10	114	SEG197	194	SEG117	274	SEG37	354	COMA31
35	COMB9	115	SEG196	195	SEG116	275	SEG36	355	NC
36	COMB8	116	SEG195	196	SEG115	276	SEG35	356	NC
37	COMB7	117	SEG194	197	SEG114	277	SEG34		
38	COMB6	118	SEG193	198	SEG113	278	SEG33		
39	COMB5	119	SEG192	199	SEG112	279	SEG32		
40	COMB4	120	SEG191	200	SEG111	280	SEG31		
41	COMB3	121	SEG190	201	SEG110	281	SEG30		
42	COMB2	122	SEG189	202	SEG109	282	SEG29		
43	COMB1	123	SEG188	203	SEG108	283	SEG28		
44	COMB0	124	SEG187	204	SEG107	284	SEG27		
45	NC	125	SEG186	205	SEG106	285	SEG26		
46	NC	126	SEG185	206	SEG105	286	SEG25		
47	NC	127	SEG184	207	SEG104	287	SEG24		
48	NC	128	SEG183	208	SEG103	288	SEG23		
49	NC	129	SEG182	209	SEG102	289	SEG22		
50	NC	130	SEG181	210	SEG101	290	SEG21		
51	NC	131	SEG180	211	SEG100	291	SEG20		
52	NC	132	SEG179	212	SEG99	292	SEG19		
53	NC	133	SEG178	213	SEG98	293	SEG18		
54	NC	134	SEG177	214	SEG97	294	SEG17		
55	NC	135	SEG176	215	SEG96	295	SEG16		
56	SEG255	136	SEG175	216	SEG95	296	SEG15		
57	SEG254	137	SEG174	217	SEG94	297	SEG14		
58	SEG253	138	SEG173	218	SEG93	298	SEG13		
59	SEG252	139	SEG172	219	SEG92	299	SEG12		
60	SEG251	140	SEG171	220	SEG91	300	SEG11		
61	SEG250	141	SEG170	221	SEG90	301	SEG10		
62	SEG249	142	SEG169	222	SEG89	302	SEG9		
63	SEG248	143	SEG168	223	SEG88	303	SEG8		
64	SEG247	144	SEG167	224	SEG87	304	SEG7		
65	SEG246	145	SEG166	225	SEG86	305	SEG6		
66	SEG245	146	SEG165	226	SEG85	306	SEG5		
67	SEG244	147	SEG164	227	SEG84	307	SEG4		
68	SEG243	148	SEG163	228	SEG83	308	SEG3		
69	SEG242	149	SEG162	229	SEG82	309	SEG2		
70	SEG241	150	SEG161	230	SEG81	310	SEG1		
71	SEG240	151	SEG160	231	SEG80	311	SEG0		
72	SEG239	152	SEG159	232	SEG79	312	NC		
73	SEG238	153	SEG158	233	SEG78	313	NC		
74	SEG237	154	SEG157	234	SEG77	314	NC		
75	SEG236	155	SEG156	235	SEG76	315	NC		
76	SEG235	156	SEG155	236	SEG75	316	NC		
77	SEG234	157	SEG154	237	SEG74	317	NC		
78	SEG233	158	SEG153	238	SEG73	318	NC		
79	SEG232	159	SEG152	239	SEG72	319	NC		
80	SEG231	160	SEG151	240	SEG71	320	NC		

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface Selection

SSD1326 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 6-1 for BS[2:0] setting).

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I²C	Tie LOW					SDA$_{OUT}$	SDA$_{IN}$	SCL	Tie LOW			SA0	RES#

8.1.1 MCU I^{2}C Interface

The I^{2}C communication interface consists of slave address bit SA0, I^{2}C-bus data signal SDA (SDA$_{OUT}$/D$_2$ for output and SDA$_{IN}$/D$_1$ for input) and I^{2}C-bus clock signal SCL (D$_0$). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

    a) Slave address bit (SA0)
SSD1326 has to recognize the slave address before transmitting or receiving any information by the I^{2}C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,
b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
0 1 1 1 1 0 SA0 R/W#
"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1326. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I^{2}C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

    b) I^{2}C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA. If SDA in is connected to the "SDA out", the device becomes fully I^{2}C bus compatible.
It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
"SDA$_{IN}$" and "SDA$_{OUT}$" are tied together and serve as SDA. The "SDA$_{IN}$" pin must be connected to act as SDA. The "SDA$_{OUT}$" pin may be disconnected. When "SDA$_{OUT}$" pin is disconnected, the acknowledgement signal will be ignored in the I^{2}C-bus.

    c) I^{2}C-bus clock signal (SCL)
The transmission of information in the I^{2}C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

8.1.1.1 I2C-bus Write data and read register status

The I^{2}C-bus interface gives access to write data and command into the device. Please refer to Figure 8-1 : I2C-bus data format for the write mode of I^{2}C-bus in chronological order.

Figure 8-1 : I^{2}C-bus data format
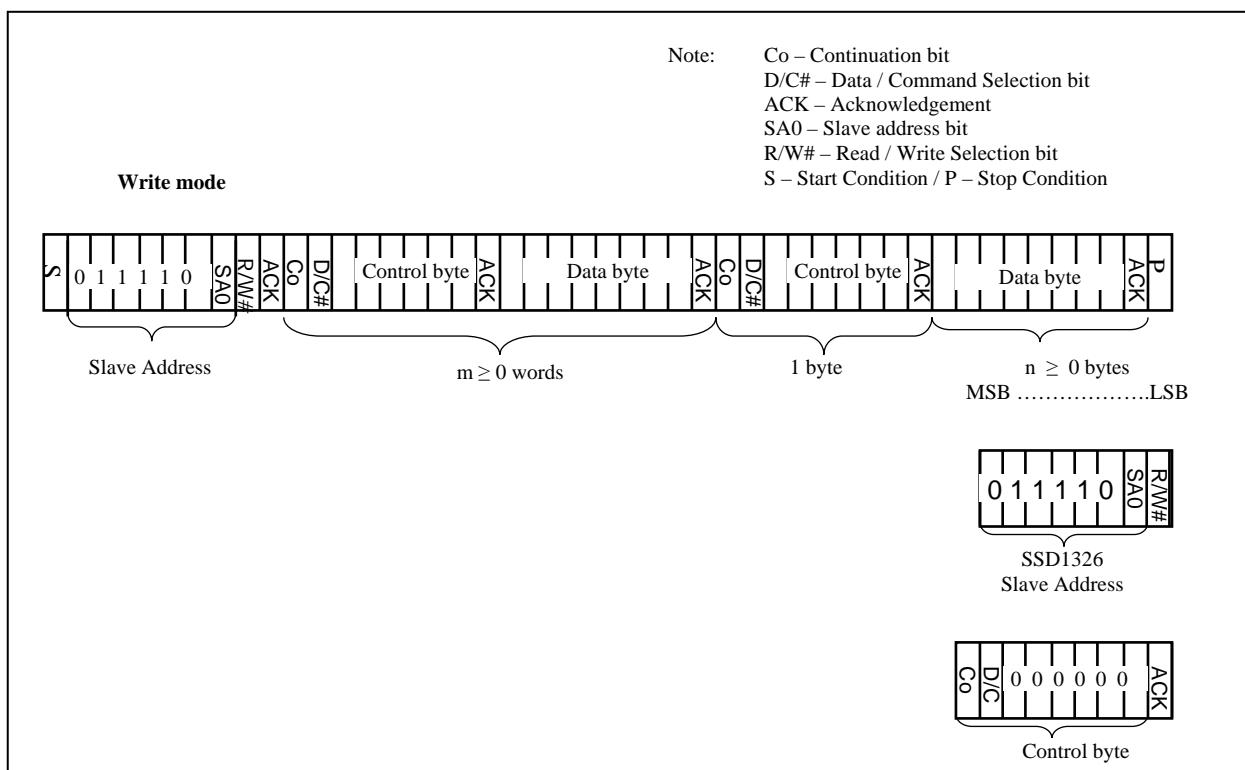
8.1.1.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-2. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1326, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH.
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-3 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-2. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 8-2 : Definition of the Start and Stop Condition
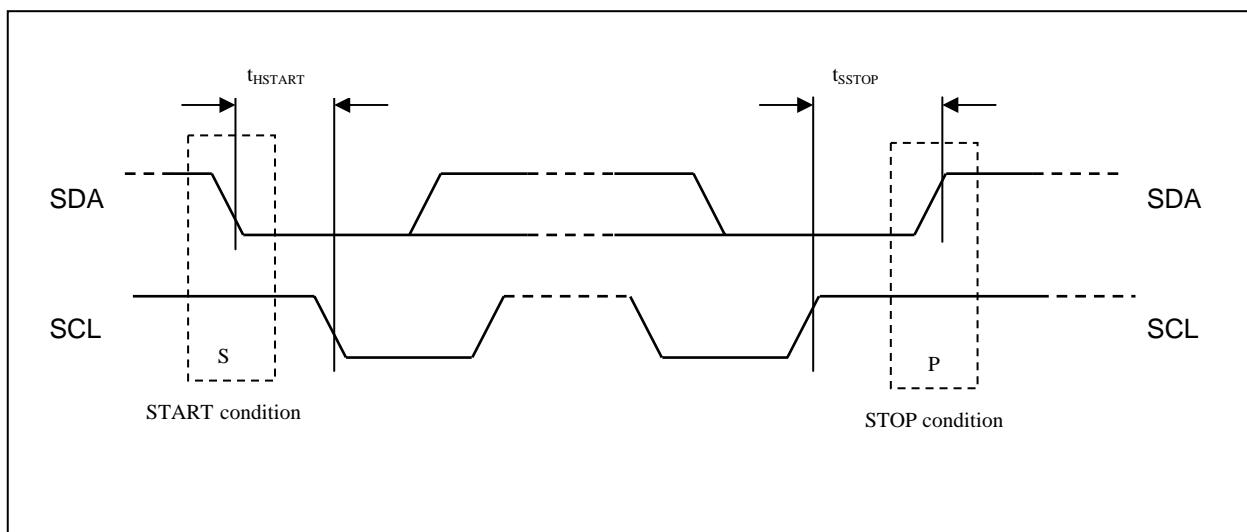
Figure 8-3 : Definition of the acknowledgement condition
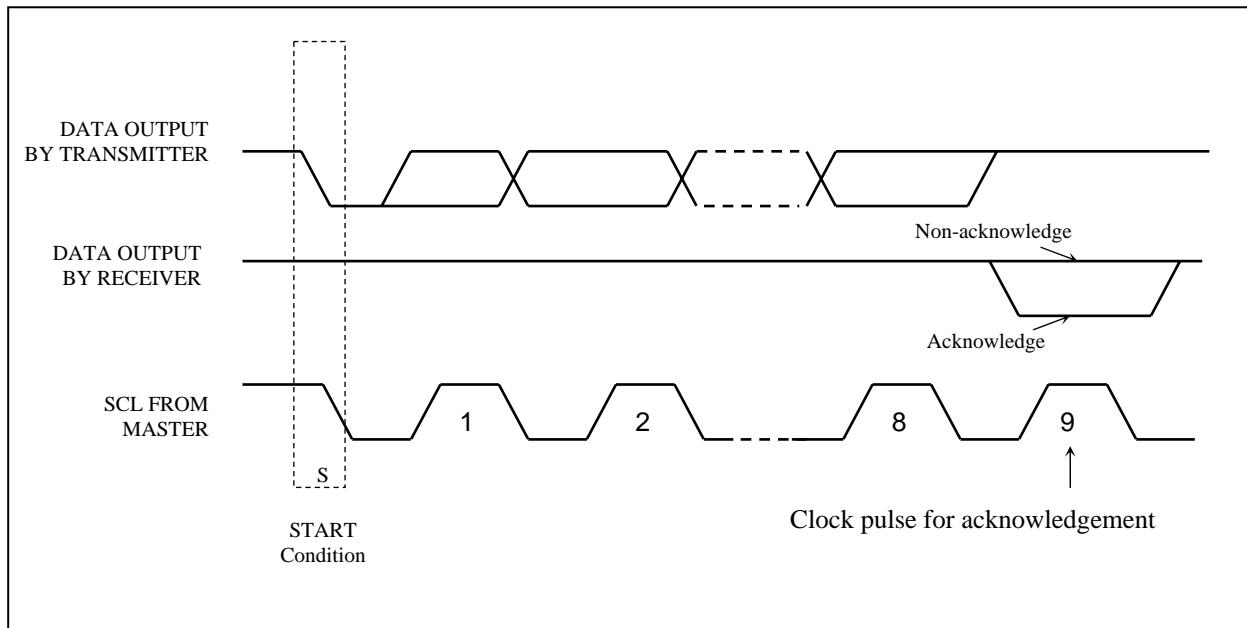
Please be noted that the transmission of the data bit has some limitations.
1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 8-4 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 8-4 : Definition of the data transfer condition
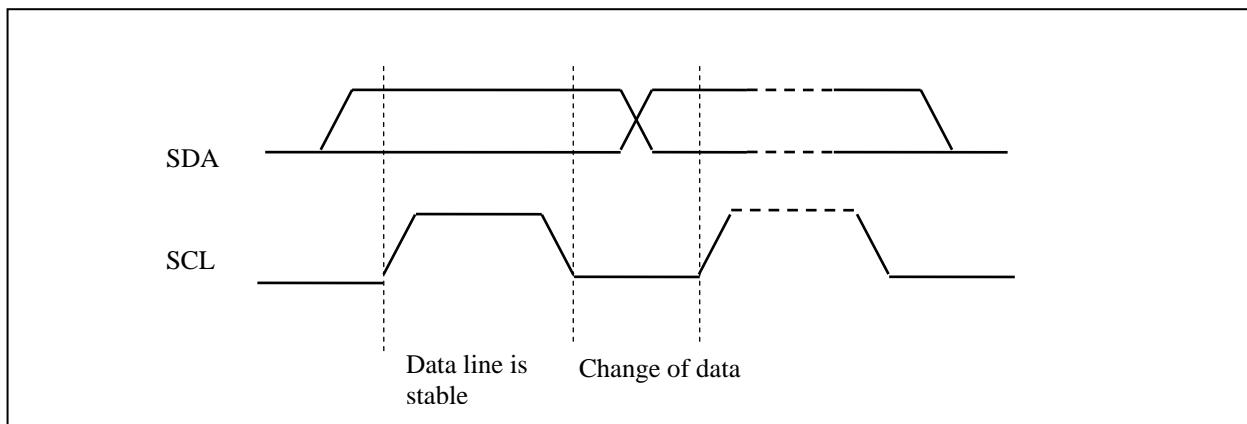
8.1.2 MCU Serial Interface

The serial interface consists of serial clock SCLK, serial data SD_{IN}, D/C#, CS#.

Table 8-2 : Control pins of Serial interface

Function	E	R/W#	CS#	D/C#
Write command	Tie LOW	Tie LOW	L	L
Write data	Tie LOW	Tie LOW	L	H

SD_{IN} is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in SPI mode
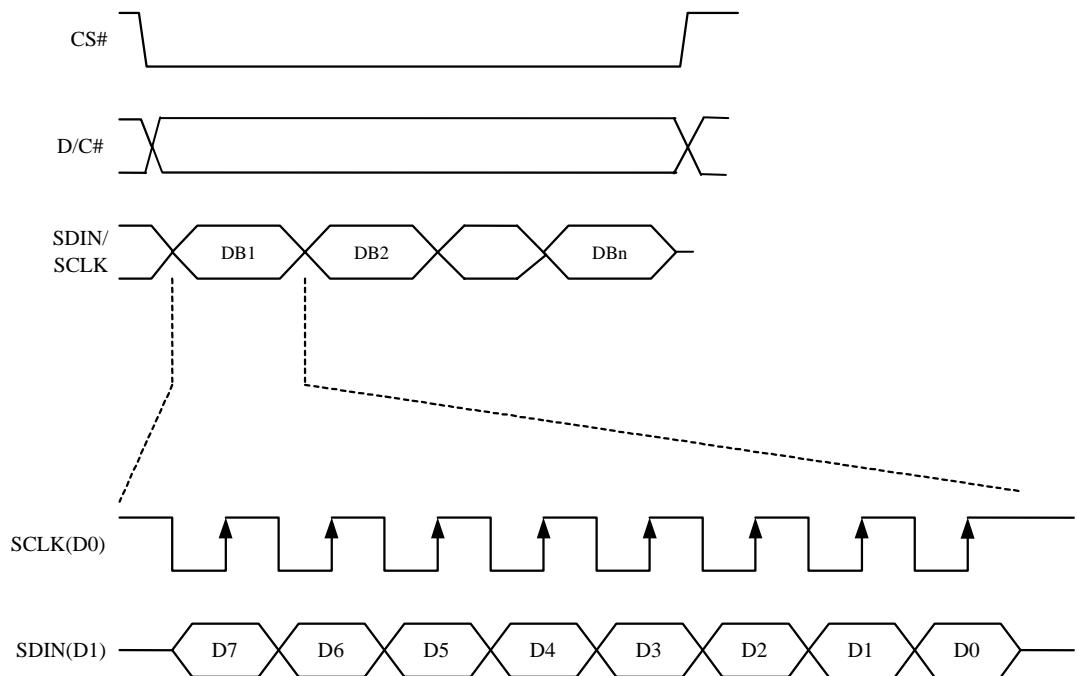
8.1.3 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

Table 8-3 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
  H stands for HIGH in signal
  L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-6.

Figure 8-6 : Data read back procedure - insertion of dummy read
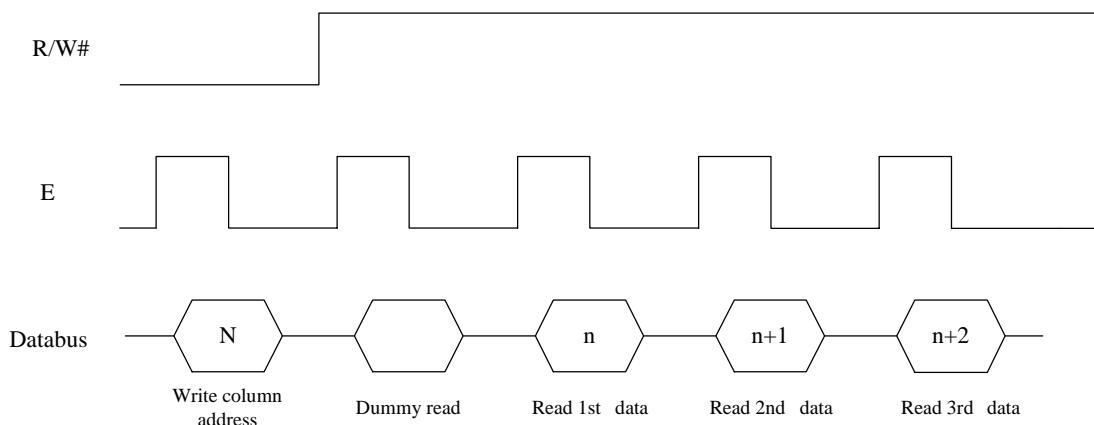
8.1.4 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-7 : Example of Write procedure in 8080 parallel interface mode
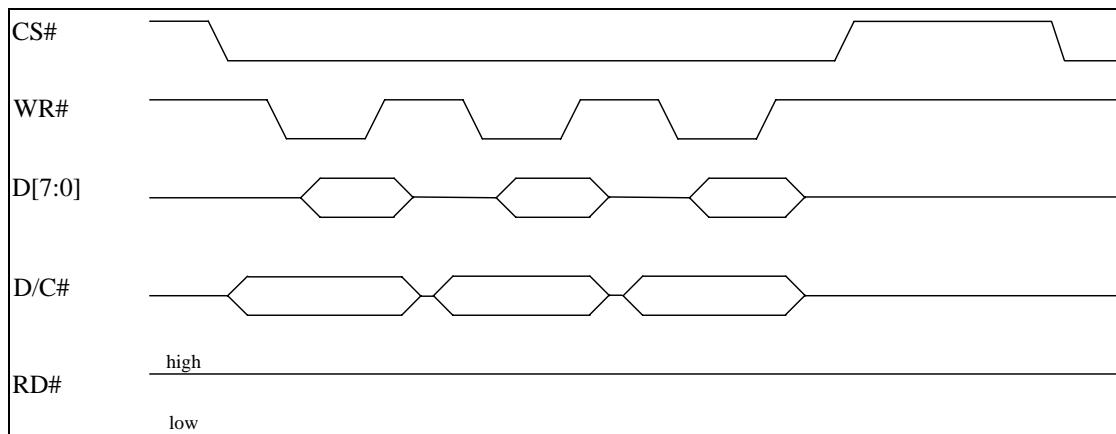
Figure 8-8 : Example of Read procedure in 8080 parallel interface mode
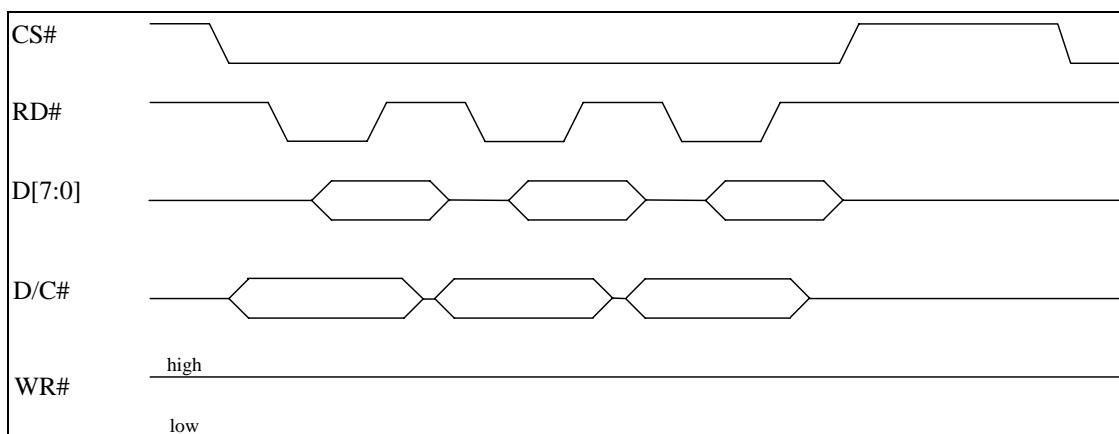
Table 8-4 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
[1] ↑ stands for rising edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-9.

Figure 8-9 : Display data read back procedure - insertion of dummy read
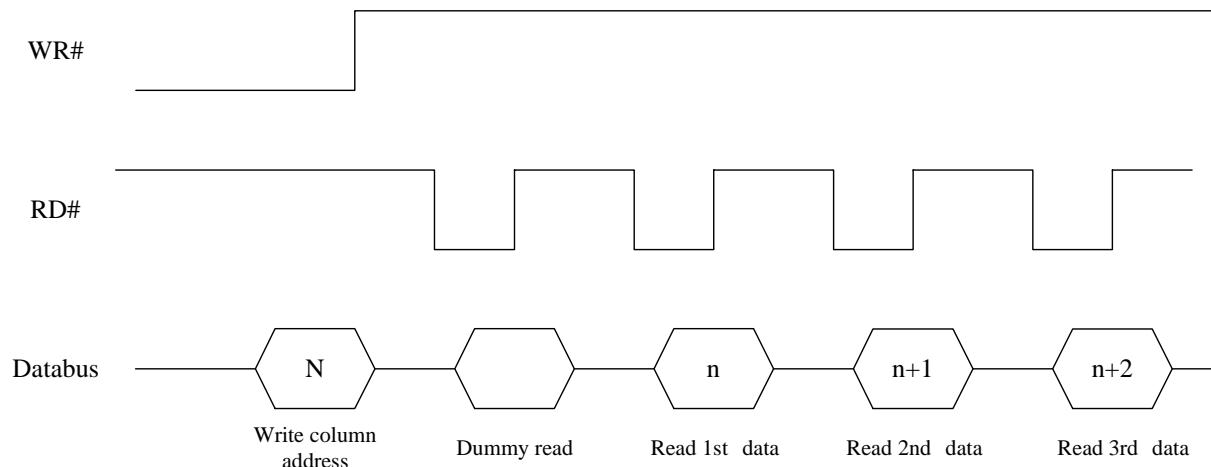
8.2 Segment Drivers/Common Drivers

Segment drivers have 256 current sources to drive OLED panel. The driving current can be adjusted from 0 to 100uA with 8 bits, 256 steps. Common drivers generate voltage scanning pulses. The block diagrams and waveforms of the segment and common driver are shown as follow.

Figure 8-10 : Segment and Common Driver Block Diagram
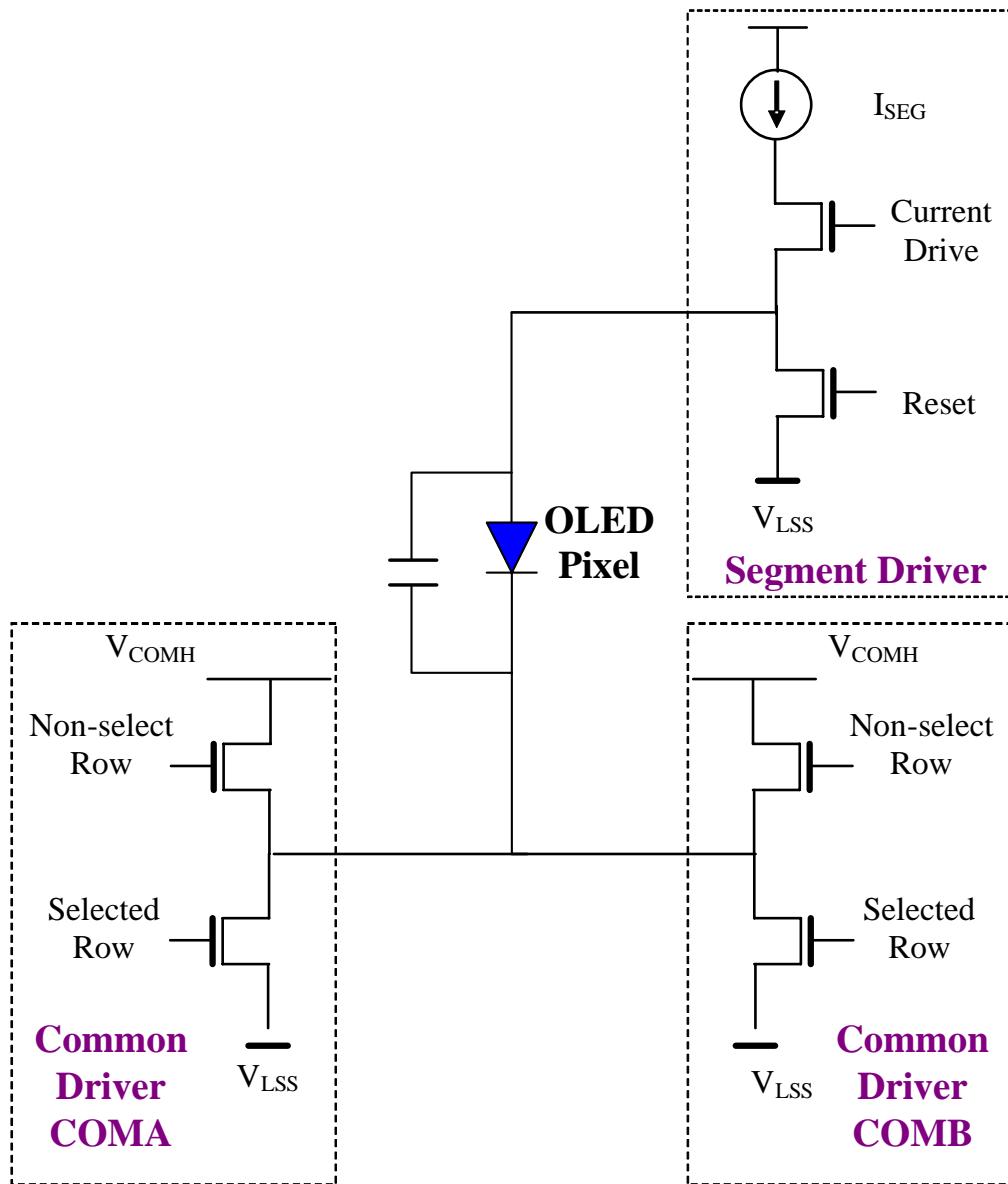
The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 8-11.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 8-11 : Segment and Common Driver Signal Waveform (Gray scale mode)

One Frame Period

COM0

Non-select Row

V_{COMH}

V_{LSS}

Selected Row

COM1

V_{COMH}

V_{LSS}

COM Voltage

This row is selected to turn ON

V_{COMH}

V_{LSS}

Time

Segment Voltage

Waveform for ON

V_P

Waveform for OFF

V_{LSS}

Time
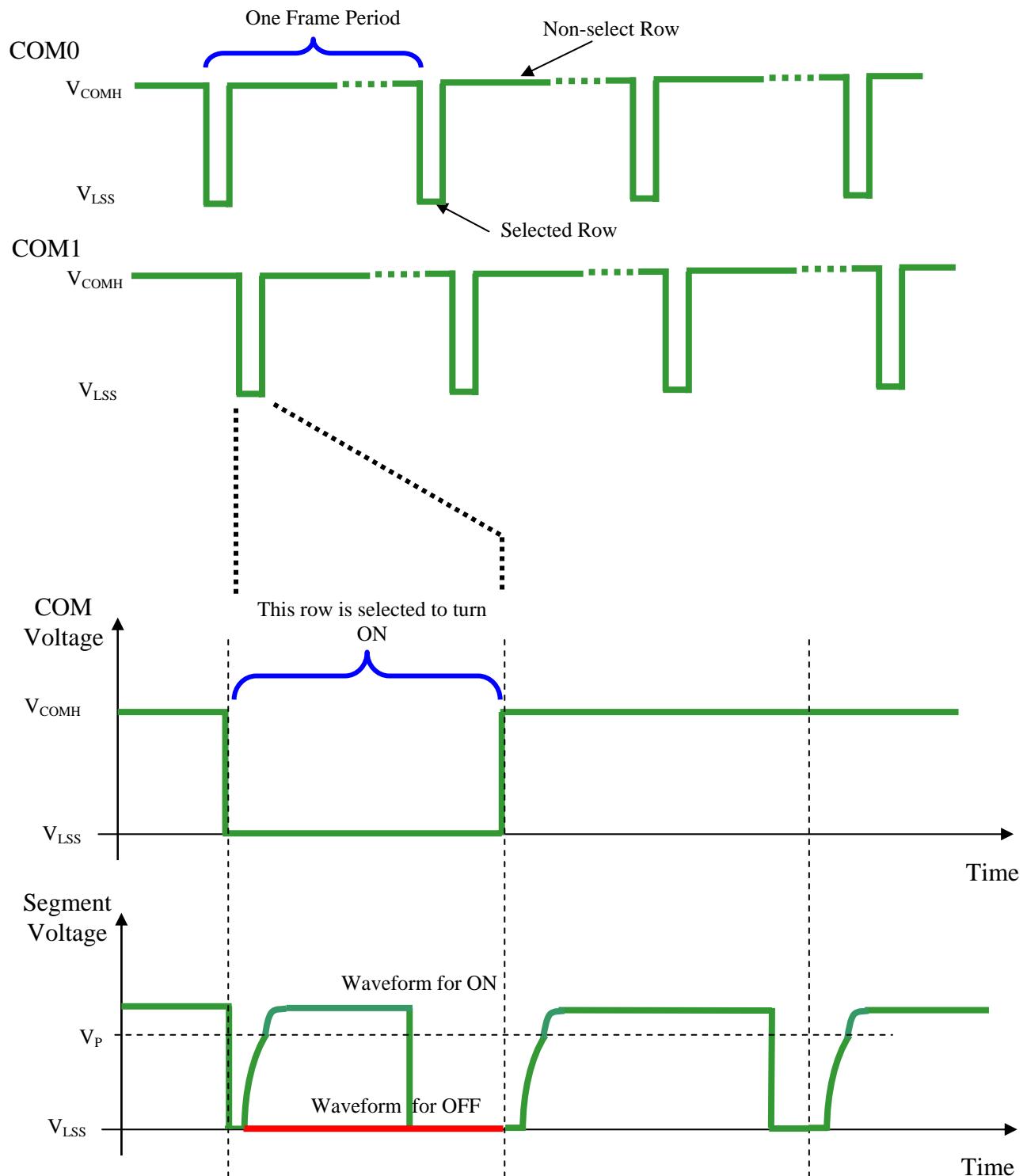
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0] from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS}. The amplitude of V_P can be programmed by the command BCh. The period of phase 2 can be programmed in length from 1 to 16 DCLK by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The setup of phase 3 can be programmed by command BBh.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The wider pulse widths in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.

Figure 8-12: Gray Scale Control by PWM in Segment
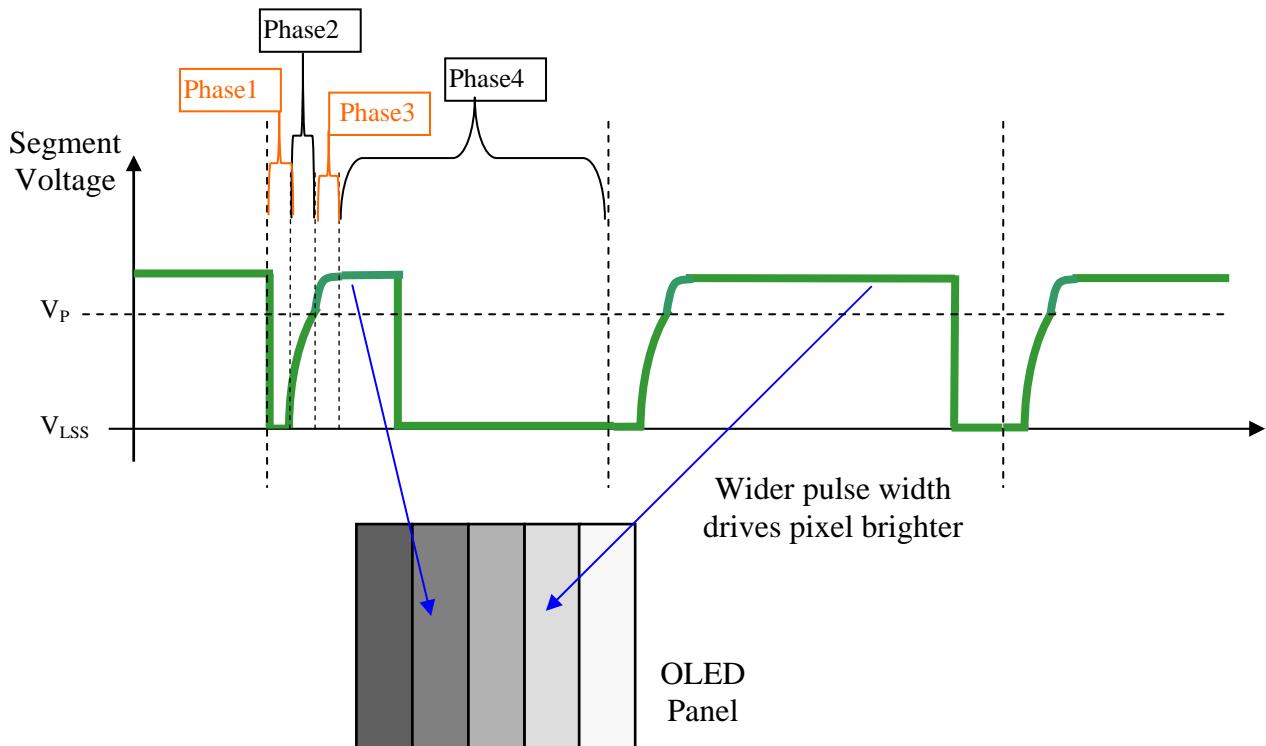
After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command B7h "Select Default Gray Scale Table" or B8h "Set Gray Scale Table". In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

8.3   Oscillator Circuit and Display Time Generator

Figure 8-13 : Oscillator Circuit and Display Time Generator
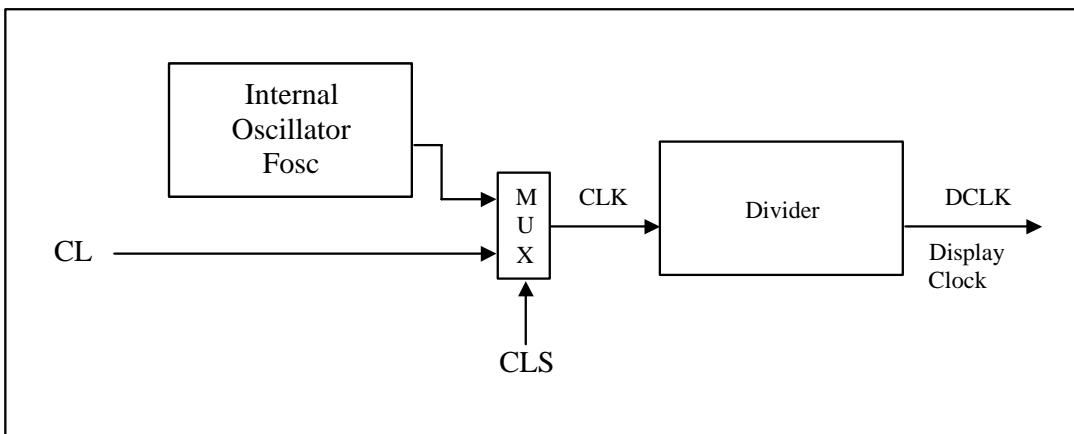
This module is an On-Chip low power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency F_{OSC} can be changed by command B3h, please refer to Table 9-1.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command B3h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times No.\,of\,MUX}$$

where
- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16.
- K is row period and it is equal to

     K = Phase 1 length + Gray Scale 15 level Pulse width

  where phase 1 length is controlled by command B1h A[3:0] and gray scale 15 level pulse width is controlled by command B7h or B8h.
- Number of multiplex ratio is set by command A8h. The power ON reset value is 32MUX..
- F_{OSC} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in faster frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.4   Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is treated as either the data bytes of multiple byte command or display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

8.5   Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:
1. Display is OFF
2. 256 x 32 Display in Gray Scale Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80h

8.6   Gray Scale Decoder

In SSD1326 there are 16 gray levels from GS0 to GS15. The gray scale of the display is defined by the pulse width (PW) of current drive phase, except GS0 there is no pre-charge (phase 2,3) and current drive (phase 4).

8.7   Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 256x32x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

8.7.1 GDDRAM in Gray Scale mode

The GDDRAM address map in Figure 8-14 shows the GDDRAM in Gray Scale mode. Since in Gray Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel. For example D3969[3:0] in Figure 8-14 corresponds to the pixel located in (COM31, SEG2). So the lower nibble and higher nibble of D0 ,D1, D2, …,D4093, D4094, D4095 in Figure 8-14 represent the 256x32 data nibbles in the GDDRAM.

Figure 8-14 : GDDRAM in Gray Scale mode (RESET)

COM Outputs	RAM Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG252	SEG253	SEG254	SEG255	SEG Outputs
		00		01			7E		7F		RAM Column address (HEX)
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM1	01	D128[3:0]	D128[7:4]	D129[3:0]	D129[7:4]		D254[3:0]	D254[7:4]	D255[3:0]	D255[7:4]	
COM30	1E	D3840[3:0]	D3840[7:4]	D3841[3:0]	D3841[7:4]		D3966[3:0]	D3966[7:4]	D3967[3:0]	D3967[7:4]	
COM31	1F	D3968[3:0]	D3968[7:4]	D3969[3:0]	D3969[7:4]		D4094[3:0]	D4094[7:4]	D4095[3:0]	D4095[7:4]	

Corresponding to one pixel

8.7.2 GDDRAM in Mono mode

The GDDRAM address map in Figure 8-15 shows the GDDRAM in Mono mode. Since in Mono mode, one bit is allocated for each pixel. For example bit D993[0] in Figure 8-15 corresponds to the pixel located in (COM31, SEG8). So each bit of D0 ,D1, D2, …,D1021, D1022, D1023 in Figure 8-15 represents the 256x32 data bits in the GDDRAM.

Figure 8-15 : GDDRAM in Mono mode (RESET)

COM Outputs	RAM Row Address (HEX)	SEG0–SEG7	SEG8–SEG15		SEG240–SEG247	SEG248–SEG255	SEG Outputs
		00	01		1E	1F	RAM Column address (HEX)
COM0	00	D0 (0 1 2 3 4 5 6 7)	D1 (0 1 2 3 4 5 6 7)		D30 (0 1 2 3 4 5 6 7)	D31 (0 1 2 3 4 5 6 7)	
COM1	01	D32 (0 1 2 3 4 5 6 7)	D33 (0 1 2 3 4 5 6 7)		D62 (0 1 2 3 4 5 6 7)	D63 (0 1 2 3 4 5 6 7)	
|	|						
COM30	1E	D960 (0 1 2 3 4 5 6 7)	D961 (0 1 2 3 4 5 6 7)		D990 (0 1 2 3 4 5 6 7)	D991 (0 1 2 3 4 5 6 7)	
COM31	1F	D992 (0 1 2 3 4 5 6 7)	D993 (0 1 2 3 4 5 6 7)		D1022 (0 1 2 3 4 5 6 7)	D1023 (0 1 2 3 4 5 6 7)	

Corresponding to one pixel

8.8 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1326 (assume V_{DD} and V_{DDIO} are at the same voltage level).

Power ON sequence:
1. Power ON V_{DD}, V_{DDIO}.
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic LOW) for at least 2us (t_1) [4] and then HIGH (logic HIGH).
3. After set RES# pin LOW (logic LOW), wait for at least 2us (t_2). Then Power ON V_{CC} [1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

Figure 8-16 : The Power ON sequence
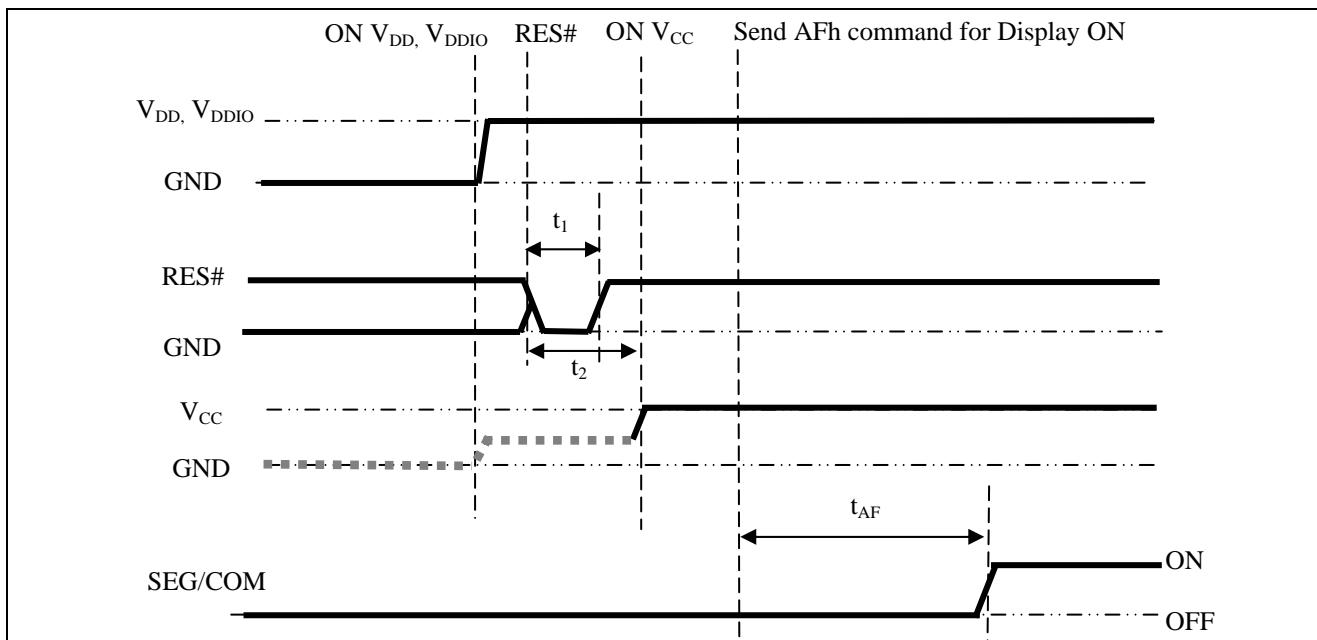
Power OFF sequence:
1. Send command AEh for display OFF.
2. Power OFF V_{CC} [1], [2], [3]
3. Wait for t_{OFF}. Power OFF V_{DD}, V_{DDIO}. (where Minimum t_{OFF}=0ms[5], Typical t_{OFF} = 100ms)

Figure 8-17 : The Power OFF sequence
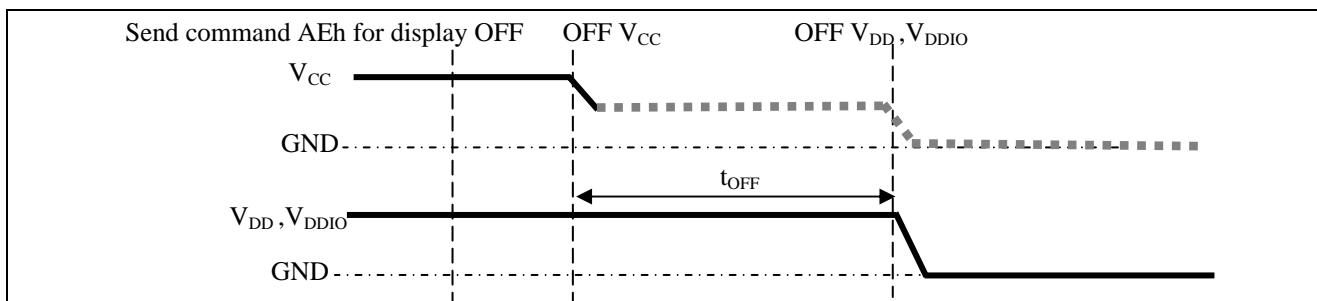
Note:
[1] Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-16 and Figure 8-17.
[2] V_{CC} should be kept float (disable) when it is OFF.
[3] Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
[4] The register values are reset after t_1.
[5] V_{DD} should not be Power OFF before V_{CC} Power OFF.

9 COMMAND TABLE

Table 9-1 : Command Table

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 0 0	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup Column start and end address A[6:0]: Start column address, range:00h~7Fh, (RESET = 00h) B[6:0]: End column address, range:00h~7Fh, (RESET = 7Fh (127) for Gray Scale mode; RESET = 1Fh (31) for Mono mode)
0 0 0	75 A[4:0] B[4:0]	0 * *	1 * *	1 * *	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Setup Row start and end address A[4:0]: Start row address, range:00h~1Fh, (RESET = 00h) B[4:0]: End row address, range:00h~1Fh, (RESET = 1Fh)
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Current	A[7:0]: Contrast current value, range:00h~FFh, i.e. 256 steps for I_{SEG} current. (RESET = 80h)
0 0 0	84 85 87	1 1 1	0 0 0	0 0 0	0 0 0	0 0 0	1 1 1	0 0 1	0 1 1	Set Current Range	84h = Quarter Current Range 85h = Half Current Range (RESET) 87h = Full Current Range
0 0	A0 A[4:0]	1 *	0 *	1 *	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Re-map and Gray Scale /Mono mode	Re-map setting in Graphic Display Data RAM (GDDRAM) A[0] = 0b, Disable Column Address Re-map (RESET) A[0] = 1b, Enable Column Address Re-map A[1] = 0b, Disable COM Re-map (RESET) A[1] = 1b, Enable COM Re-map A[2] = 0b, Disable Bit Re-map (RESET) A[2] = 1b, Enable Bit Re-map A[3] = 0b, Enable Horizontal Address Increment(RESET) A[3] = 1b, Enable Vertical Address Increment A[4] = 0b, Gray Scale Mode (RESET) A[4] = 1b, Mono Mode Please refer to Section 10.1.5 for the details setting in Gray Scale Mode and Mono Mode.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 0	A1 A[4:0]	1 *	0 *	1 *	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	A[4:0]: Vertical shift by setting the starting address of display RAM from 0 ~ 31 (RESET = 00h)
0 0	A2 A[4:0]	1 *	0 *	1 *	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	A[4:0]: Set vertical offset by COM from 0 ~ 31 (RESET = 00h)
0 0 0 0	A4 A5 A6 A7	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	Set Display Mode	A4: Normal display (RESET) A5: All ON (All pixels have gray scale of 15, GS15) A6: All OFF (All pixels have gray scale of 0, GS0) A7: Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)
0 0	A8 A[4:0]	0 *	0 *	0 *	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set MUX Ratio	A[4:0]: Set MUX ratio from 16MUX ~ 32MUX: A[4:0] = 15 represents 16MUX ⋮ A[4:0] = 31 represents 32MUX (RESET) It should be noted that A[4:0]=0~14 is not allowed.
0	AE/AF	1	0	1	0	1	1	1	X_0	Display ON / OFF	X[0] = 0b, display OFF X[0] = 1b, display ON
0 0	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[7:0]: Reset and first pre-charge phase length (RESET=53h) A[3:0] Phase 1 period (Reset) of 1~16 DCLKs (RESET=3h)

A[3:0]	DCKS	A[3:0]	DCKS
0000b	Invalid	1000b	9
0001b	2	1001b	10
0010b	3	1010b	11
0011b	4	1011b	12
0100b	5	1100b	13
0101b	6	1101b	14
0110b	7	1110b	15
0111b	8	1111b	16

A[7:4] Phase 2 period (first pre-charge)of 1~16 DCLKs (RESET=5h)

A[7:4]	DCKS	A[7:4]	DCKS
0000b	Invalid	1000b	9
0001b	2	1001b	10
0010b	3	1010b	11
0011b	4	1011b	12
0100b	5	1100b	13
0101b	6	1101b	14
0110b	7	1110b	15
0111b	8	1111b	16

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 0	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Front Clock Divider / Oscillator Frequency	$A[3:0]$: Define divide ratio (D) of display clock (DCLK) Divide ratio (D)=$A[3:0]$+1 ($A[3:0]$RESET is 0001b, i.e. divide ratio (D) = 2) $A[7:4]$: Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of $A[7:4]$ and vice versa. Range:0h~Fh (RESET= 3h)
0	B7	1	0	1	1	0	1	1	1	Select Default Gray Scale Table	The default gray scale table is set in unit of DCLK's as follow: GS1 level Pulse width = 2 GS2 level Pulse width = 4 GS3 level Pulse width = 6 … GS13 level Pulse width = 26 GS14 level Pulse width = 28 GS15 level Pulse width = 30
0 0 0 … … … 0 0	B8 A1[5:0] A2[5:0] … … … A14[5:0] A15[5:0]	1 * * ... ... * *	0 * * ... ... * *	1 $A1_5$ $A2_5$ ... ... $A14_5$ $A15_5$	1 $A1_4$ $A2_4$ ... ... $A14_4$ $A15_4$	1 $A1_3$ $A2_3$ ... ... $A14_3$ $A15_3$	0 $A1_2$ $A2_2$ ... ... $A14_2$ $A15_2$	0 $A1_1$ $A2_1$ ... ... $A14_1$ $A15_1$	0 $A1_0$ $A2_0$ ... ... $A14_0$ $A15_0$	Set Gray Scale Table	The next 15 data bytes set the gray scale pulse width in unit of DCLK's. $A1[5:0]$, value for GS1 level Pulse width $A2[5:0]$, value for GS2 level Pulse width … $A14[5:0]$, value for GS14 level Pulse width $A15[5:0]$, value for GS15 level Pulse width **Note** [1] The pulse width value of GS1, GS2, ... , GS15 should not be equal. i.e. 0<GS1<GS2 … <GS15
0	BB A[5:0] B[7:0]	1 * B_7	0 * B_6	1 A_5 B_5	1 A_4 B_4	1 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Second Pre-charge Setup	$A[5:4]$: Second Pre-charge speed range 00b ¼ x speed range 01b ½ x speed range 10b ¾ x speed range 11b Full speed range $A[3:0]$: Set Second pre-charge period 0000b 0 DCLK (RESET) 0001b 1 DCLKs 0010b 2 DCLKs : 1111b 15 DCLKs **Note**: [1] Set $A[3:0]$= 0000b is equivalent to disable second pre-charge. $B[7:0]$: Set Second Pre-charge Speed. This speed increases with the value of $B[7:0]$ and vice versa. Range: 00h~FFh. Please refer to Figure 10-18 for the illustration of different Second Pre-charge speed settings.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 0	BC A[4:0]	1 *	0 *	1 *	1 A_4	1 A_3	1 A_2	0 A_1	0 A_0	Set Pre-charge voltage, V_P	A[4:0]: Pre-charge voltage (RESET = 10111b) 00000b 0.10 x V_{CC} … ... 10111b (RESET) … ... 11111b 0.50 x V_{CC} (always <= V_{COMH})
0 0	BE A[3:0]	1 *	0 *	1 *	1 0	1 A_3	1 A_2	1 A_1	0 A_0	Set V_{COMH}	A[3:0] : Output level high voltage for COM signal (RESET=1010b) 0000b 0.44 x V_{CC} … ... … ... 1111b 0.83 x V_{CC}
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.

Note
(1) "*" stands for "Don't care".

Graphic Acceleration Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	26	0	0	1	0	0	1	1	0	Horizontal Scrolling by Window	$A[6:0]$: Column Address of Start In Gray scale mode: Range: 0~127 In mono mode: Range: 0~31 $B[4:0]$: Row Address of Start, Range: 0~31 $C[6:0]$: Column Address of End In Gray scale mode: Range: 0~127 In mono mode: Range: 0~31 $D[4:0]$: Row address of End, Range: 0~31 **Note** [1] $C[6:0] > A[6:0]$ and $D[4:0] > B[4:0]$ $E[1:0]$: Set time interval per scrolling each column 00b (~0.02 esc) 01b (~0.04 esc) 10b (~0.08 esc) 11b (~0.16 esc) $E[4]$: Set scrolling direction 0b Scroll in direction of increasing column address 1b Scroll in direction of decreasing column address **Note**: [1] The parameters should not be changed after scrolling is activated
0	$A[6:0]$	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	$B[4:0]$	*	*	*	B_4	B_3	B_2	B_1	B_0		
0	$C[6:0]$	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	$D[4:0]$	*	*	*	D_4	D_3	D_2	D_1	D_0		
0	$E[4:0]$	*	*	*	E_4	*	*	E_1	E_0		
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling **Note** [1] After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	This command activates the scrolling function according to the setting done by Continuous Horizontal & Vertical Scrolling Setup command 26h.

10 COMMAND DESCRIPTIONS

10.1 Fundamental Command

10.1.1 Set Column Address (15h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The diagram below shows the way of column and row address pointer movement through the example (Gray Scale Mode), column start address is set to 2 and column end address is set to 125, row start address is set to 1 and row end address is set to 31. **Horizontal address increment mode** is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 125 and from row 1 to row 31 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 10-1).* Whenever the column address pointer finishes accessing the end column 125, it is reset back to column 2 and row address is automatically increased by 1 (*solid line in Figure 10-1*). While the end row 30 and end column 125 RAM location is accessed, the row address is reset back to 1 and the column address is reset back to 2(*dotted line in Figure 10-1*).

Figure 10-1 : Example of Column and Row Address Pointer Movement (Gray Scale Mode)
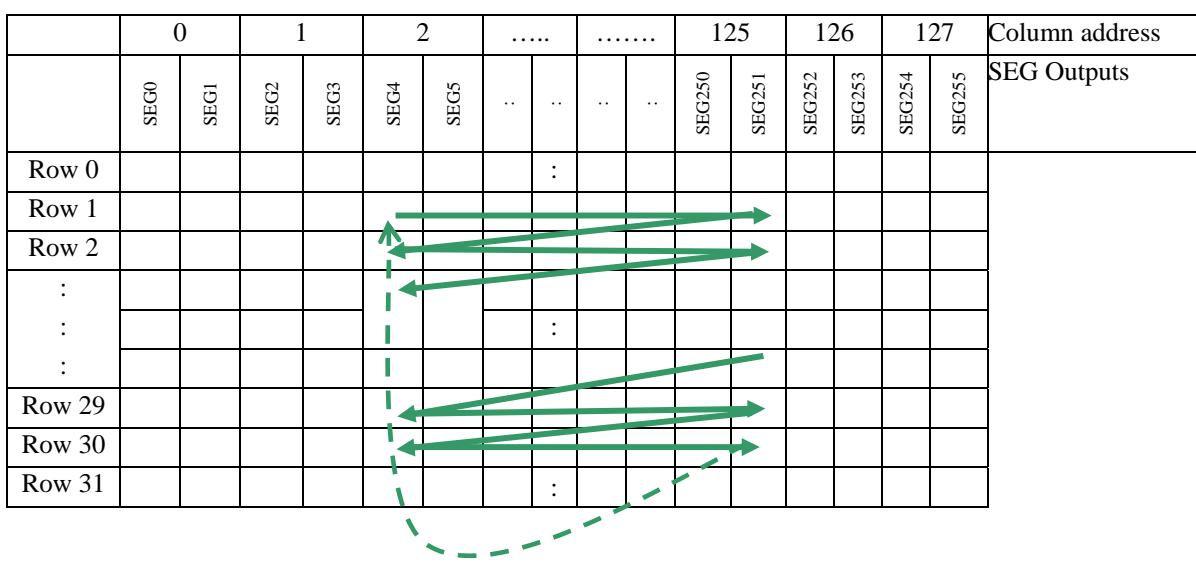
10.1.3 Set Contrast Current (81h)

This double byte command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases linearly with the increase of contrast step

Figure 10-2 : Segment current vs Contrast setting (half current range)

Segment current vs Contrast setting
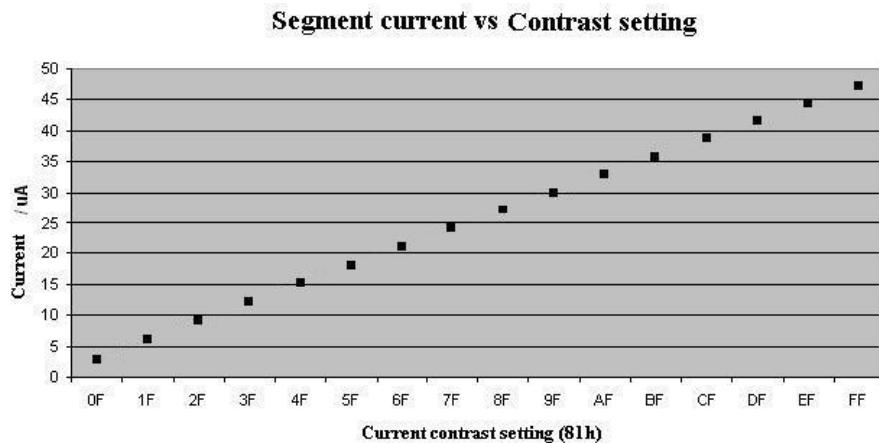
10.1.4 Set Current Range (84h, 85h, 87h)

This command selects one of the I_{SEG} current ranges: quarter range (84h), half range (85h) or full range (87h). With the same contrast level, the I_{SEG} current in half range mode is a half of that in full range mode. Similarly, the I_{SEG} current in quarter range mode is a quarter of that in full range mode. Half range current mode is default setting upon hardware RESET.

10.1.5 Set Re-Map and Gray Scale/Mono mode (A0h)

This double command has multiple configurations and each bit setting is described as follows:
- Column Address Remapping (A[0])
  This bit is made for increase the flexibility layout of segment signals in OLED module with segment arranged from left to right (when A[0] is set to 0) or from right to left (when A[0] is set to 1).

  In Gray scale mode
  > A[0] = 0 (RESET): RAM Column 0 ~ 127 map to SEG0-SEG1 ~ SEG254-SEG255
  > A[0] = 1: RAM Column 0 ~ 127 map to SEG254-SEG255 ~ SEG0-SEG1

Figure 10-3 : GDDRAM in Gray Scale mode with or without column address and COM remapping

Normal, A[0]=0	SEG0	SEG1	SEG2	SEG3		SEG252	SEG253	SEG254	SEG255	SEG Outputs
Remap, A[0]=1	SEG255	SEG254	SEG253	SEG252		SEG3	SEG2	SEG1	SEG0	
Normal, A[1]=0 / Remap, A[1]=1	00		01			7E		7F		RAM Column address (HEX)
C0M0 / COM31 — 00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM1 / COM30 — 01	D128[3:0]	D128[7:4]	D129[3:0]	D129[7:4]		D254[3:0]	D254[7:4]	D255[3:0]	D255[7:4]	
| / | — |										
COM30 / COM1 — 1E	D3840[3:0]	D3840[7:4]	D3841[3:0]	D3841[7:4]		D3966[3:0]	D3966[7:4]	D3967[3:0]	D3967[7:4]	
COM31 / COM0 — 1F	D3968[3:0]	D3968[7:4]	D3969[3:0]	D3969[7:4]		D4094[3:0]	D4094[7:4]	D4095[3:0]	D4095[7:4]	
COM Outputs	RAM Row Address (HEX)									

Corresponding to one pixel

In Mono mode
> A[0] = 0 (RESET): RAM Column 0 ~ 31 map to SEG0-SEG1 ~ SEG254-SEG255
> A[0] = 1: RAM Column 0 ~ 31 map to SEG254-SEG255 ~ SEG0-SEG1

Figure 10-4 : GDDRAM in Mono mode with or without column address and COM remapping

Normal, A[0]=0	SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7	SEG8 SEG9 SEG10 SEG11 SEG12 SEG13 SEG14 SEG15		SEG240 SEG241 SEG242 SEG243 SEG244 SEG245 SEG246 SEG247	SEG248 SEG249 SEG250 SEG251 SEG252 SEG253 SEG254 SEG255	SEG Outputs
Remap, A[0]=1	SEG255 SEG254 SEG253 SEG252 SEG251 SEG250 SEG249 SEG248	SEG247 SEG246 SEG245 SEG244 SEG243 SEG242 SEG241 SEG240		SEG15 SEG14 SEG13 SEG12 SEG11 SEG10 SEG9 SEG8	SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1 SEG0	

Normal, A[1]=0	Remap, A[1]=1		00	01	1E	1F	RAM Column address (HEX)
COM0	COM31	00	D0 0 1 2 3 4 5 6 7	D1 0 1 2 3 4 5 6 7	D30 0 1 2 3 4 5 6 7	D31 0 1 2 3 4 5 6 7	
COM1	COM30	01	D32 0 1 2 3 4 5 6 7	D33 0 1 2 3 4 5 6 7	D62 0 1 2 3 4 5 6 7	D63 0 1 2 3 4 5 6 7	
|	|	|					
COM30	COM1	1E	D960 0 1 2 3 4 5 6 7	D961 0 1 2 3 4 5 6 7	D990 0 1 2 3 4 5 6 7	D991 0 1 2 3 4 5 6 7	
COM31	COM0	1F	D992 0 1 2 3 4 5 6 7	D993 **0** 1 2 3 4 5 6 7	D1022 0 1 2 3 4 5 6 7	D1023 0 1 2 3 4 5 6 7	
COM Outputs	RAM Row Address (HEX)						

Corresponding to one pixel

- COM Remapping (A[1])
  This bit defines the scanning direction of the common for flexible layout of common signals in OLED module.

    A[1] = 0 (RESET): Scan from up to down

    A[1] = 1: Scan from bottom to up

  Refer to Figure 10-3 and Figure 10-4 for details.

- Bit Remapping (A[2])
  In Gray Scale mode,

    A[2] = 0 (RESET): Data bits direct mapping is performed as shown in Figure 10-3.

    A[2] = 1: The two nibbles of the data bus for RAM access are re-mapped, such that :

      (D7, D6, D5, D4, D3, D2, D1, D0) acts like (D3, D2, D1, D0, D7, D6, D5, D4)

Figure 10-5 : GDDRAM in Gray Scale mode with bit remapping (A[2]=1)

Normal, A[0]=0			SEG0		SEG1		SEG2		SEG3		SEG252		SEG253		SEG254		SEG255		SEG Outputs
Remap, A[0]=1			SEG255		SEG254		SEG253		SEG252		SEG3		SEG2		SEG1		SEG0		

Normal, A[1]=0	Remap, A[1]=1		00		01		7E		7F		RAM Column address (HEX)
C0M0	COM31	00	D0[7:4]	D0[3:0]	D1[7:4]	D1[3:0]	D126[7:4]	D126[3:0]	D127[7:4]	D127[3:0]	
COM1	COM30	01	D128[7:4]	D128[3:0]	D129[7:4]	D129[3:0]	D254[7:4]	D254[3:0]	D255[7:4]	D255[3:0]	
|	|	|									
COM30	COM1	1E	D3840[7:4]	D3840[3:0]	D3841[7:4]	D3841[3:0]	D3966[7:4]	D3966[3:0]	D3967[7:4]	D3967[3:0]	
COM31	COM0	1F	D3968[7:4]	D3968[3:0]	**D3969[7:4]**	D3969[3:0]	D4094[7:4]	D4094[3:0]	D4095[7:4]	D4095[3:0]	
COM Outputs	RAM Row Address (HEX)										

Corresponding to one pixel

In Mono mode,

    A[2] = 0 (RESET): Data bits direct mapping is performed like the one shown in Figure 10-4

A[2] = 1: The two nibbles of the data bus for RAM access are re-mapped, such that :
(D7,D6,D5,D4,D3,D2,D1,D0) acts like (D0,D1,D2,D3,D4,D5,D6,D7)

Figure 10-6 : GDDRAM in Mono mode with bit remapping (A[2]=1)

Normal, A[0]=0	SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7	SEG8 SEG9 SEG10 SEG11 SEG12 SEG13 SEG14 SEG15		SEG240 SEG241 SEG242 SEG243 SEG244 SEG245 SEG246 SEG247	SEG248 SEG249 SEG250 SEG251 SEG252 SEG253 SEG254 SEG255	SEG Outputs
Remap, A[0]=1	SEG255 SEG254 SEG253 SEG252 SEG251 SEG250 SEG249 SEG248	SEG247 SEG246 SEG245 SEG244 SEG243 SEG242 SEG241 SEG240		SEG15 SEG14 SEG13 SEG12 SEG11 SEG10 SEG9 SEG8	SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1 SEG0	

Normal, A[1]=0	Remap, A[1]=1		00	01		1E	1F	RAM Column address (HEX)
COM0	COM31	00	D0 / 7 6 5 4 3 2 1 0	D1 / 7 6 5 4 3 2 1 0		D30 / 7 6 5 4 3 2 1 0	D31 / 7 6 5 4 3 2 1 0	
COM1	COM30	01	D32 / 7 6 5 4 3 2 1 0	D33 / 7 6 5 4 3 2 1 0		D62 / 7 6 5 4 3 2 1 0	D63 / 7 6 5 4 3 2 1 0	
│	│	│						
COM30	COM1	1E	D960 / 7 6 5 4 3 2 1 0	D961 / 7 6 5 4 3 2 1 0		D990 / 7 6 5 4 3 2 1 0	D991 / 7 6 5 4 3 2 1 0	
COM31	COM0	1F	D992 / 7 6 5 4 3 2 1 0	D993 / 7 6 5 4 3 2 1 0		D1022 / 7 6 5 4 3 2 1 0	D1023 / 7 6 5 4 3 2 1 0	
COM Outputs	RAM Row Address (HEX)							

Corresponding to one pixel

If this feature works together with Column Address Re-map, it would produce an effect of flipping the outputs from SEG0~255 to SEG255~SEG0.

- Address increment mode (A[3])

When A[3] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 10-7.

Figure 10-7 : Address Pointer Movement of Horizontal Address Increment Mode (Example for Gray Scale mode)

	0	1	…..	126	127	Column address
Row 0						
Row 1						
:	.	:	:	.	:	
Row 30						
Row 31						
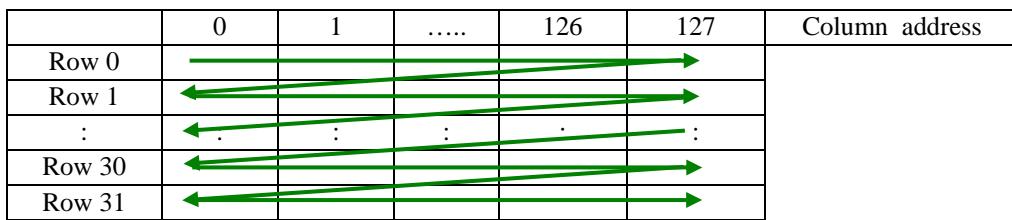
When A[3] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 10-8.

Figure 10-8 : Address Pointer Movement of Vertical Address Increment Mode (Example for Gray Scale mode)

	0	1	…..	126	127	Column address
Row 0			…..			
Row 1			…..			
:			:			
Row 30			…			
Row 31			…..			
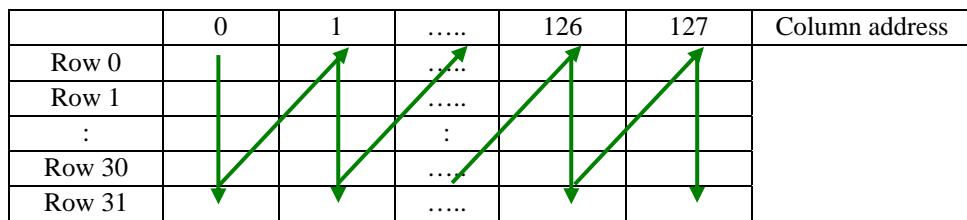
- Mode selection (A[4])

  When A[4] is set to 0, Gray Scale mode is selected. When A[4] is set to 1, Mono mode is selected. The interpretation of data under Gray Scale mode and Mono mode is explained as following example (with the same RAM content):

  For example, on RESET Gray Scale mode is selected and the display become:

Figure 10-9 : Example of Gray Scale mode display
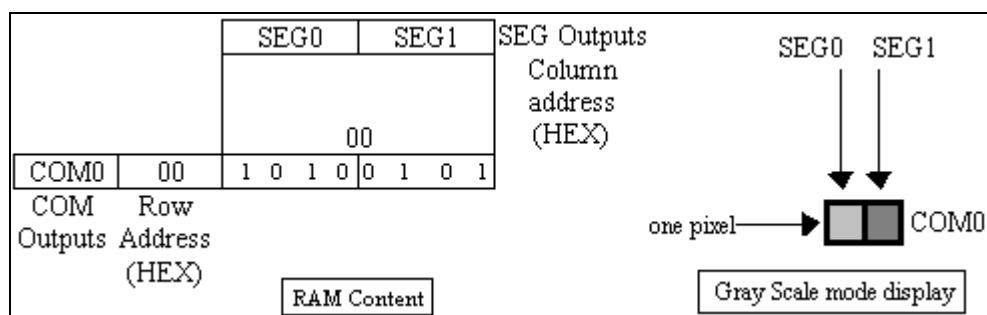
If Mono mode is selected by setting A[4] to 1, then the display will become:

Figure 10-10 : Example of Mono mode display
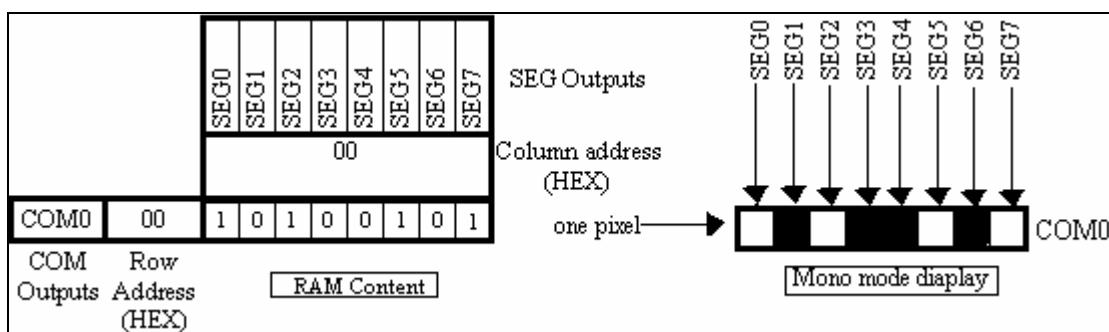
10.1.6 Set Display Start Line (A1h)

This double byte command is to set Display Start Line register for determining the starting address of display RAM to be displayed by selecting a value from 0 to 31. Figure 10-11 shows an example using this command of this command when MUX ratio= 32 and MUX ratio= 30 and Display Start Line = 04h. In there, "ROW" means the graphic display data RAM row.

Figure 10-11 : Example of Set Display Start Line with no Remapping

COM Pin	MUX ratio (A8h) = 32 Display Start Line (A1h) = 0h	MUX ratio (A8h) = 32 Display Start Line (A1h) = 8h	MUX ratio (A8h) = 24 Display Start Line (A1h) = 0h	MUX ratio (A8h) = 24 Display Start Line (A1h) = 8h
COM0	ROW0	ROW8	ROW0	ROW8
COM1	ROW1	ROW9	ROW1	ROW9
COM2	ROW2	ROW10	ROW2	ROW10
COM3	ROW3	ROW11	ROW3	ROW11
:	:	:	:	:
:	:	:	:	:
COM21	ROW21	ROW29	ROW21	ROW29
COM22	ROW22	ROW30	ROW22	ROW30
COM23	ROW23	ROW31	ROW23	ROW31
COM24	ROW24	ROW0	-	-
COM25	ROW25	ROW1	-	-
COM26	ROW26	ROW2	-	-
COM27	ROW27	ROW3	-	-
COM28	ROW28	ROW4	-	-
COM29	ROW29	ROW5	-	-
COM30	ROW30	ROW6	-	-
COM31	ROW31	ROW7	-	-
Gray scale Display examples	Refer to a	Refer to b	Refer to c	Refer to d

a	Solomon Systech	b	Solomon Systech
c	Solomon Systech	d	Solomon Systech
RAM:	Solomon Systech		
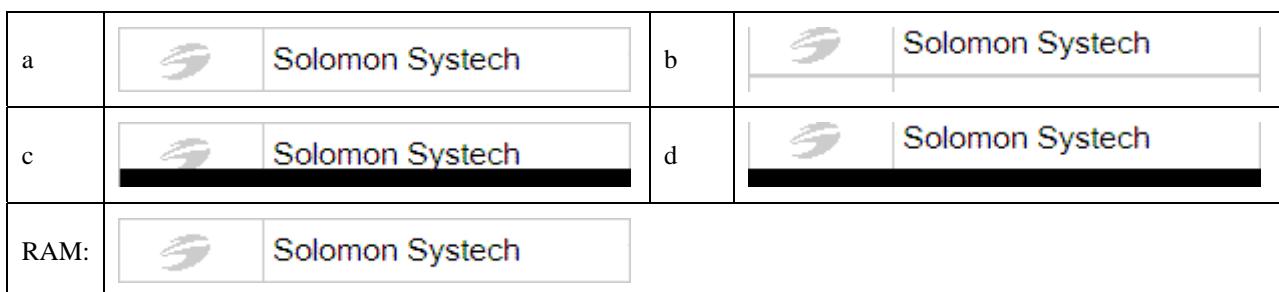
10.1.7 Set Display Offset (A2h)

This double byte command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0~COM31. Figure 10-12 shows an example using this command when MUX ratio= 31 and MUX ratio= 30 and Display Offset = 04h. In there, "Row" means the graphic display data RAM row.

Figure 10-12 : Example of Set Display Offset with no Remapping

COM Pin	MUX ratio (A8h) = 32 Display Offset (A2h) = 0h	MUX ratio (A8h) = 32 Display Offset (A2h) = 8h	MUX ratio (A8h) = 30 Display Offset (A2h) = 0h	MUX ratio (A8h) = 30 Display Offset (A2h) = 8h
COM0	ROW0	ROW8	ROW0	ROW8
COM1	ROW1	ROW9	ROW1	ROW9
COM2	ROW2	ROW10	ROW2	ROW10
COM3	ROW3	ROW11	ROW3	ROW11
:	:	:	:	:
:	:	:	:	:
COM14	ROW14	ROW22	ROW14	ROW22
COM15	ROW15	ROW23	ROW15	ROW23
COM16	ROW16	ROW24	ROW16	-
COM17	ROW17	ROW25	ROW17	-
COM18	ROW18	ROW26	ROW18	-
COM19	ROW19	ROW27	ROW19	-
COM20	ROW20	ROW28	ROW20	-
COM21	ROW21	ROW29	ROW21	-
COM22	ROW22	ROW30	ROW22	-
COM23	ROW23	ROW31	ROW23	-
COM24	ROW24	ROW0	-	ROW0
COM25	ROW25	ROW1	-	ROW1
COM26	ROW26	ROW2	-	ROW2
COM27	ROW27	ROW3	-	ROW3
COM28	ROW28	ROW4	-	ROW4
COM29	ROW29	ROW5	-	ROW5
COM30	ROW30	ROW6	-	ROW6
COM31	ROW31	ROW7	-	ROW7
Gray scale Display examples	Refer to a	Refer to b	Refer to c	Refer to d

a	Solomon Systech	b		Solomon Systech
c	Solomon Systech	d		Solomon Systech
RAM:	Solomon Systech			

10.1.8　Set Display Mode (A4h ~ A7h)

These are single byte commands and are used to set display status to Normal Display, Entire Display ON, Entire Display OFF or Inverse Display.

- Normal Display (A4h)
  Reset the above effects and turn the data to ON at the corresponding gray level. Figure 10-13 shows an example of Normal Display.

**Figure 10-13 : Example of Normal Display**

- Set Entire Display ON (A5h)
  Force the entire display to be at gray scale level GS15, regardless of the contents of the display data RAM. Figure 10-14

Figure 10-14 : Example of Entire Display ON

- Set Entire Display OFF (A6h)
  Force the entire display to be at gray scale level GS0, regardless of the contents of the display data RAM. Figure 10-15

Figure 10-15 : Example of Entire Display OFF

- Inverse Display (A7h)
  For Gray scale mode, the gray scale level of display data are swapped such that "GS0" <-> "GS15", "GS1" <-> "GS14", etc. Figure 10-16 shows an example of inverse display (Gray scale mode). For mono mode, the display data are swapped like "0"<-> "1", "1" <-> "0".

Figure 10-16 : Example of Inverse Display (Gray scale mode)

10.1.9　Set MUX Ratio (A8h)

This double byte command sets multiplex ratio from 16MUX to 32MUX. In RESET, multiplex ratio is 32MUX.

10.1.10　Display ON/OFF (AEh / AFh)

These single byte commands are used to turn the matrix display on the OLED panel display either ON or OFF. For AEh, the display is OFF, the segment and common output are in high impedance state and circuits will be turned OFF. For AFh, the display is ON.

10.1.11 Set Phase Length (B1h)

In the second byte of this double command, lower nibble and higher nibble is defined separately. The lower nibble adjusts the phase length of Reset (phase 1). The higher nibble is used to select the phase length of first pre-charge phase (phase 2). The phase length is ranged from 1 to 16 DCLK's.
RESET for A[3:0] is set to 3h which means 4 DCLK's selected for Reset phase. RESET for A[7:4] is set to 5h which means 6 DCLK's is selected for first pre-charge phase. Please refer to Table 9-1 for detail breakdown levels of each step.

10.1.12 Set Frame Frequency (B2h)

This double byte command is used to set the number of DCLK's per row between the range of 14h and 7Fh. Then the Frame frequency of the matrix display is equal to DCLK frequency / A[6:0].

10.1.13 Set Front Clock Divider / Oscillator Frequency (B3h)

This double command is used to set the frequency of the internal display clocks, DCLK's. It is defined by dividing the oscillator frequency by the divide ratio (Value from 1 to 16). Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency. The lower nibble of the second byte is used to select the oscillator frequency. Please refer to Table 9-1 for detail breakdown levels of each step.

10.1.14 Select Default Gray Scale Table (B7h)

This single byte command is used to set the gray scale table to initial default setting.

10.1.15 Set Gray Scale Table (B8h)

This command is used to set each individual gray scale level for the display. Except gray scale level GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like example below can compensate this effect.

Figure 10-17 : Example of gamma correction by gray scale table setting
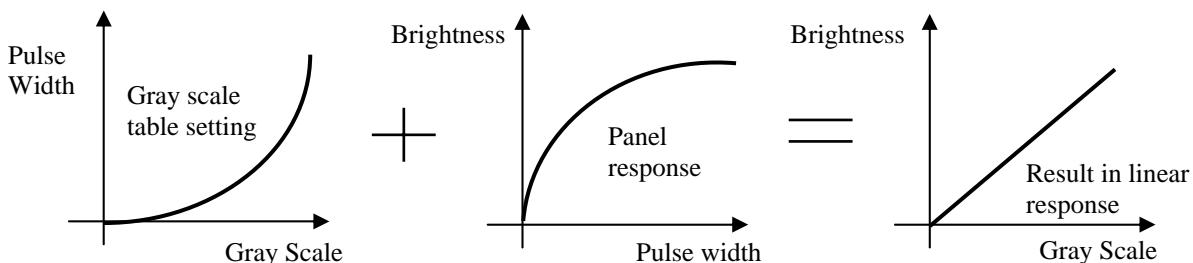
10.1.16 Second Pre-charge Setup (BBh)

This triple byte command is used to set the second pre-charge speed range, period and speed magnitude. Please refer to Table 9-1 for detail information and breakdown levels of each step. Figure 10-19 shows the effect of setting second pre-charge under different speeds through using command BBh.

Figure 10-18 : Effect of setting the second pre-charge under different speeds
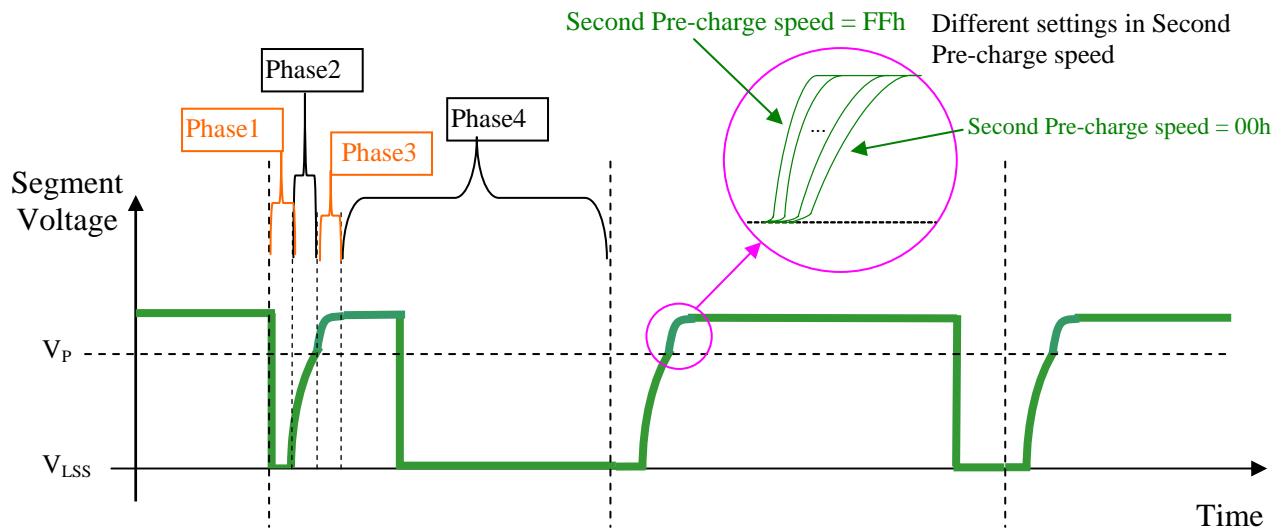
10.1.17 Set Pre-charge voltage, V$_P$ (BCh)

This double byte command is used to set first pre-charge voltage (phase 2) level. It can be programmed to set the first pre-charge voltage. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.1.18 Set V$_{COMH}$ (BEh)

This double byte command sets the high voltage level of common pins, V$_{COMH}$. The level of V$_{COMH}$ is programmed with reference to V$_{CC}$. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.1.19 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call "Lock" state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the "Lock" state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the "Lock" state. And the driver IC will then respond to the command and memory access.

10.2 Graphic Acceleration Command

10.2.1 Horizontal Scrolling by Window (26h)

This command consists of 6 consecutive bytes to set up the horizontal scroll parameters and determines the scrolling start column/row, end column/row and scrolling speed. The area bounded by scrolling start column/row, end column/row forms scrolling window. Horizontal scrolling only executes within the scrolling window and area outside the scrolling window is frozen during scrolling. Figure 10-19 shows the examples of using the horizontal scroll:

Figure 10-19 : Example of horizontal scrolling by window (Gray scale mode)
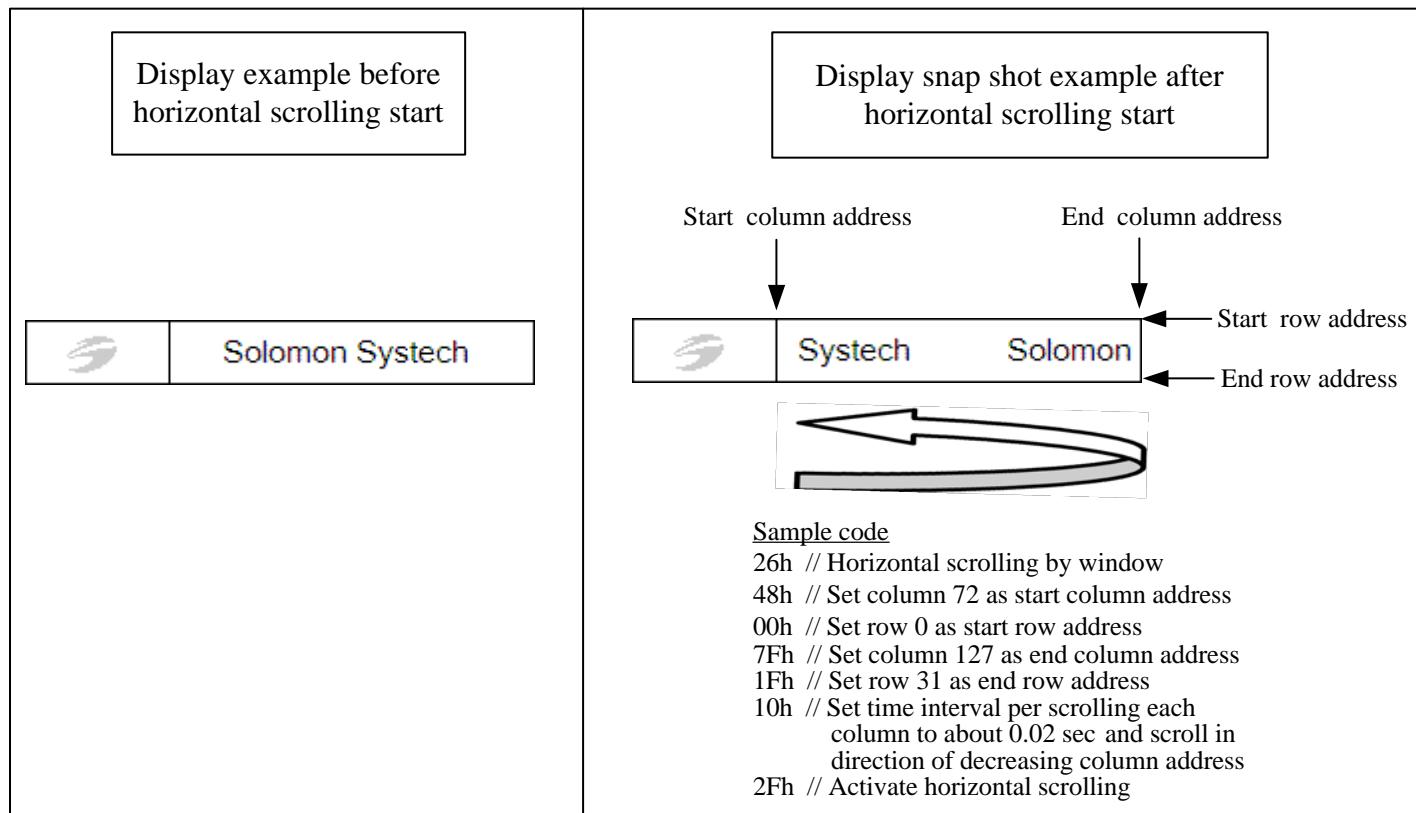
Before issuing this command the horizontal scroll must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

10.2.2 Deactivate Horizontal Scroll (2Eh)

This command stops the motion of horizontal scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

10.2.3 Activate Horizontal Scroll (2Fh)

This command starts the motion of horizontal scrolling and should only be issued after the horizontal scroll setup parameters have been defined.

The following actions are prohibited after the horizontal scroll is activated
1. RAM access (Data write or read)
2. Changing the horizontal scroll setup parameters

11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings (Voltage Referenced to V$_{SS}$)

Symbol	Parameter	Value	Unit
V$_{DD}$		-0.3 to +4	V
V$_{DDIO}$	Supply Voltage	-0.3 to V$_{DD}$+0.5	V
V$_{CC}$		0 to 16	V
V$_{SEG}$	SEG output voltage	0 to V$_{CC}$	V
V$_{COM}$	COM output voltage	0 to 0.9*V$_{CC}$	V
V$_{in}$	Input voltage	V$_{SS}$-0.3 to V$_{DD}$+0.3	V
T$_A$	Operating Temperature	-40 to +85	℃
T$_{stg}$	Storage Temperature Range	-65 to +150	℃

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

 This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

V_{DD} = 2.4 to 3.5V

T_A = 25°C

Table 12-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	9	-	15	V
V_{DD}	Logic Supply Voltage	-	2.4	-	3.5	V
V_{DDIO}	Power Supply for I/O pins	-	1.7	-	V_{DD}	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA	-	0.9* V_{DDIO}	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA	-	0.1* V_{DDIO}	-	V
V_{IH}	High Logic Input Level	-	-	0.8* V_{DDIO}	-	V
V_{IL}	Low Logic Input Level	-	-	0.2* V_{DDIO}	-	V
$I_{CC, SLEEP}$	Sleep mode Current	V_{DD}=V_{DDIO}=2.7V, display OFF, No panel attached	-	-	10	uA
$I_{DD, SLEEP}$	Sleep mode Current	V_{DD}=V_{DDIO}=2.7V, display OFF, No panel attached	-	-	10	uA
$I_{DDIO, SLEEP}$	Sleep mode Current	V_{DD}=V_{DDIO}=2.7V, display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD}=V_{DDIO}=2.7V, V_{CC}=12V, I_{REF} = 10uA No loading, Display ON, All ON	Contrast = FFh	-	620	750	uA
I_{DD}	V_{DD} Supply Current V_{DD}=V_{DDIO}=2.7V, V_{CC}=12V, I_{REF} = 10uA No loading, Display ON, All ON		-	36	45	uA
I_{SEG}	Segment Output Current V_{DD}=V_{DDIO}=2.7V, V_{CC}=12V, I_{REF}=10uA, Display ON, Segment pin under test is connected with a 20K resistive load to V_{SS}	Contrast=FFh	-	82	-	uA
		Contrast=AFh	-	62	-	
		Contrast=7Fh	-	41	-	
		Contrast=3Fh	-	21	-	
		Contrast=0Fh	-	5.5	-	
Dev	Segment output current uniformity	Dev = $(I_{SEG} - I_{MID})/I_{MID}$ where, $I_{MID} = (I_{MAX} + I_{MIN})/2$, $I_{SEG}[0:255]$ = Segment current at contrast = FFh	-3	-	+3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	+2	%

13 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD}=2.4 to3.5V
$T_A = 25°C$

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} [1]	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.7V	234	260	286	kHz
F_{FRM}	Frame Frequency for 32 MUX Mode	256x32 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1/(DxKx32) [2]	-	Hz
RES#	Reset low pulse width	-	2	-	-	us

Note

[1] F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value.

[2] D: Divide ratio (RESET value = 2)
   K: Row period (Refer to Section 8.3)

Conditions:

$V_{DD} - V_{SS} = 2.4$ to $3.5V$
$V_{DDIO} = V_{DD}$
$T_A = 25°C$

Table 13-2 : I²C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Figure 13-1 : I²C interface characteristics
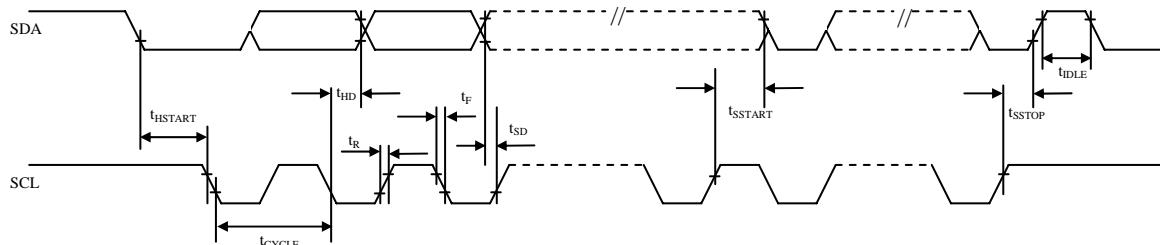
Conditions:

$V_{DD} - V_{SS} = 2.4$ to $3.5V$
$V_{DDIO} = V_{DD}$
$T_A = 25°C$

Table 13-3 : Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-2 : Serial interface characteristics
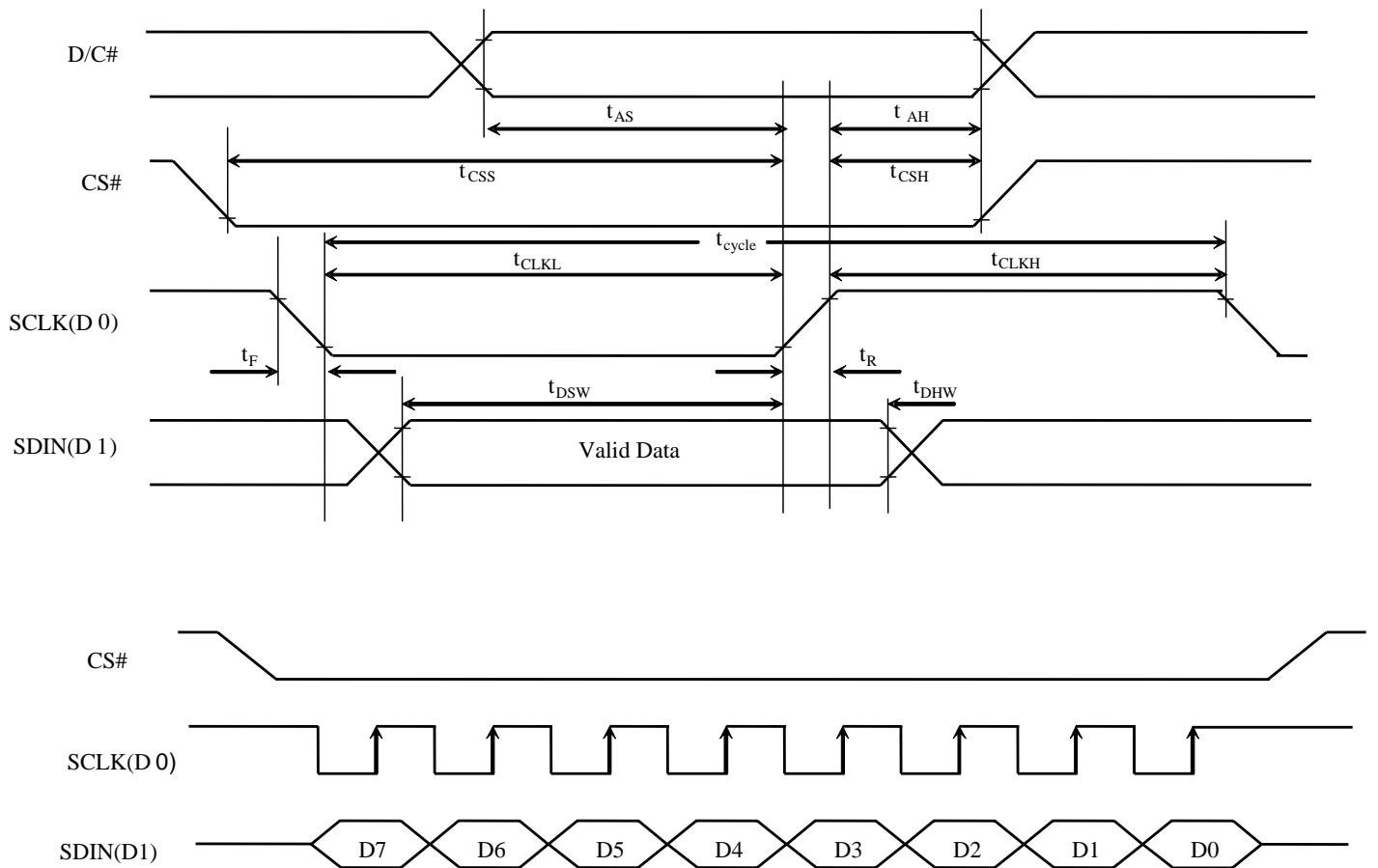
Conditions:

$V_{DD} - V_{SS} = 2.4$ to $3.5V$
$V_{DDIO} = V_{DD}$
$T_A = 25°C$

Table 13-4 : 6800-Series MCU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-3 : 6800-series MCU parallel interface characteristics
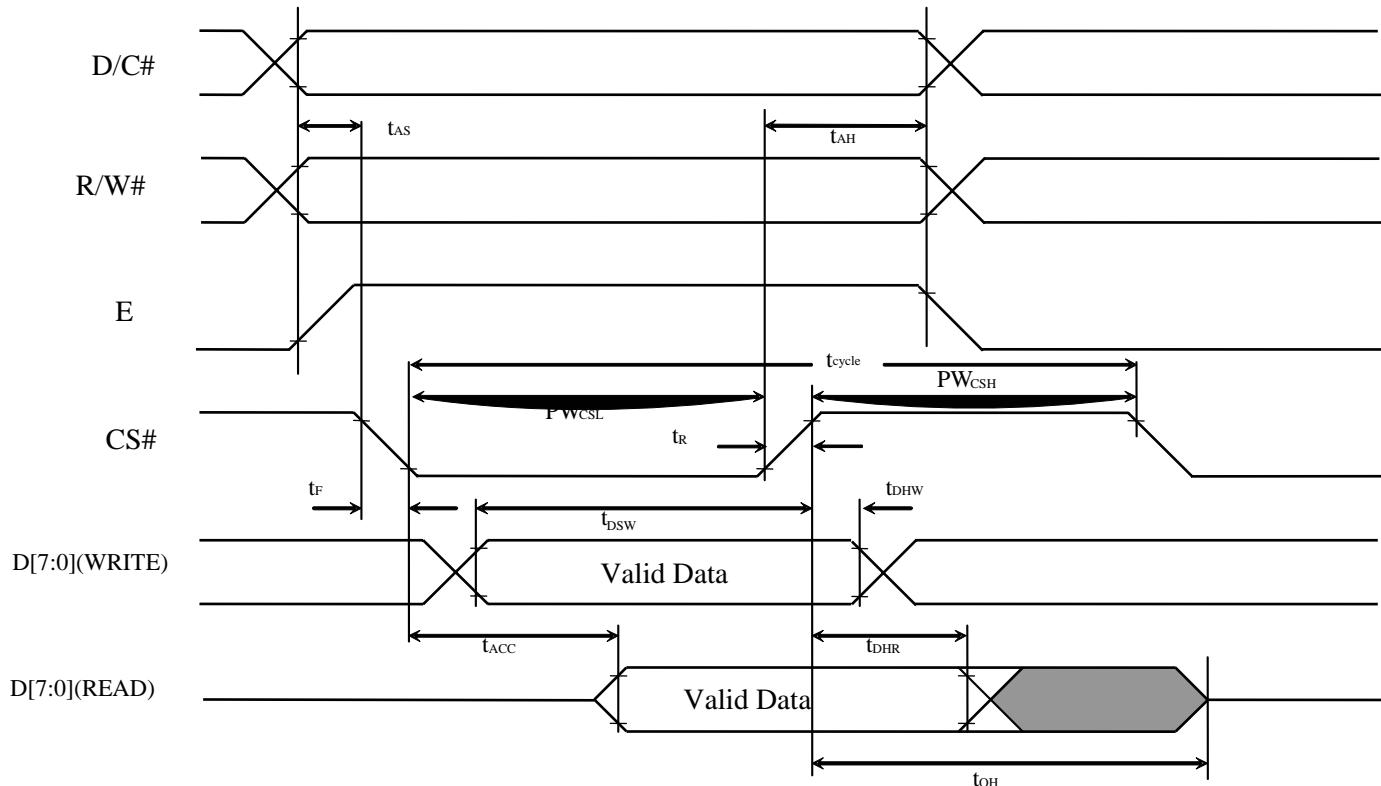
Conditions:

$V_{DD} - V_{SS} = 2.4$ to $3.5V$
$V_{DDIO} = V_{DD}$
$T_A = 25°C$

Table 13-5 : 8080-Series MCU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-4 : 8080-series MCU parallel interface characteristics

Write cycle

Read cycle
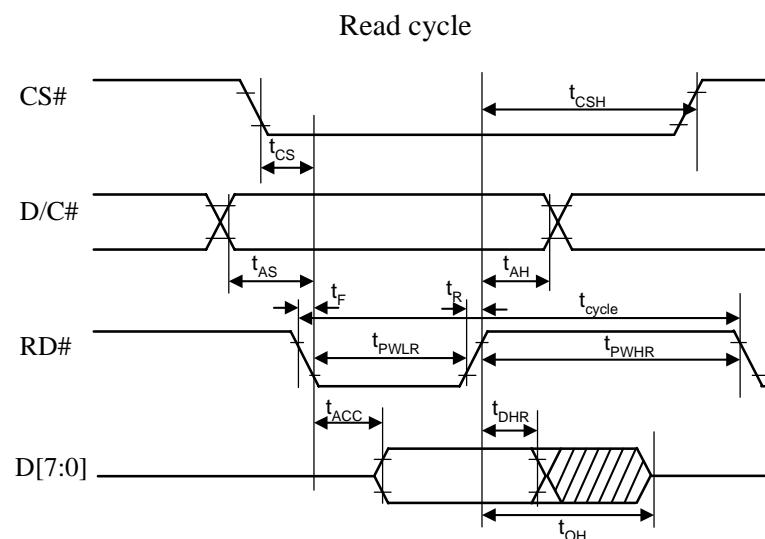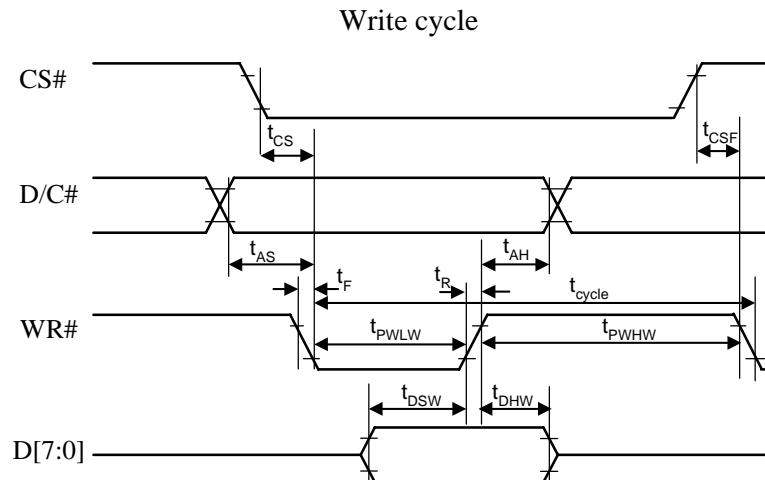
14 APPLICATION EXAMPLES

Figure 14-1 : Application Example for SSD1326U (I^{2}C interface mode)

(Condition: $V_{DD} = V_{DDIO} = 2.7V$, $V_{CC} = 12V$)

Pins connected to MCU interface   : SCL, SDA, RES#
Pin internally connected to V_{DDIO} : CLS
Pins internally connected to V_{SS} : V_{LSS}, SA0 (D/C#)
Pins internally connected together to form SDA : SDA_{IN}, SDA_{OUT}
Pin floated   : CL

C1 ~ C4: 1uF -4.7uF [1]
R1 ~ R2: 2K~10K Ω [2]
R_{REF} = (Voltage at I_{REF} pin - V_{SS})/I_{REF}
Voltage at I_{REF} = V_{CC} − 3V

Note
[1] The capacitor value is recommended value. Select appropriate value against module application.
[2] The resistor value is recommended value. Select appropriate value against module application.

15 PACKAGE INFORMATION

15.1 SSD1326U Detail Dimension

Figure 15-1 : SSD1326U Detail Dimension
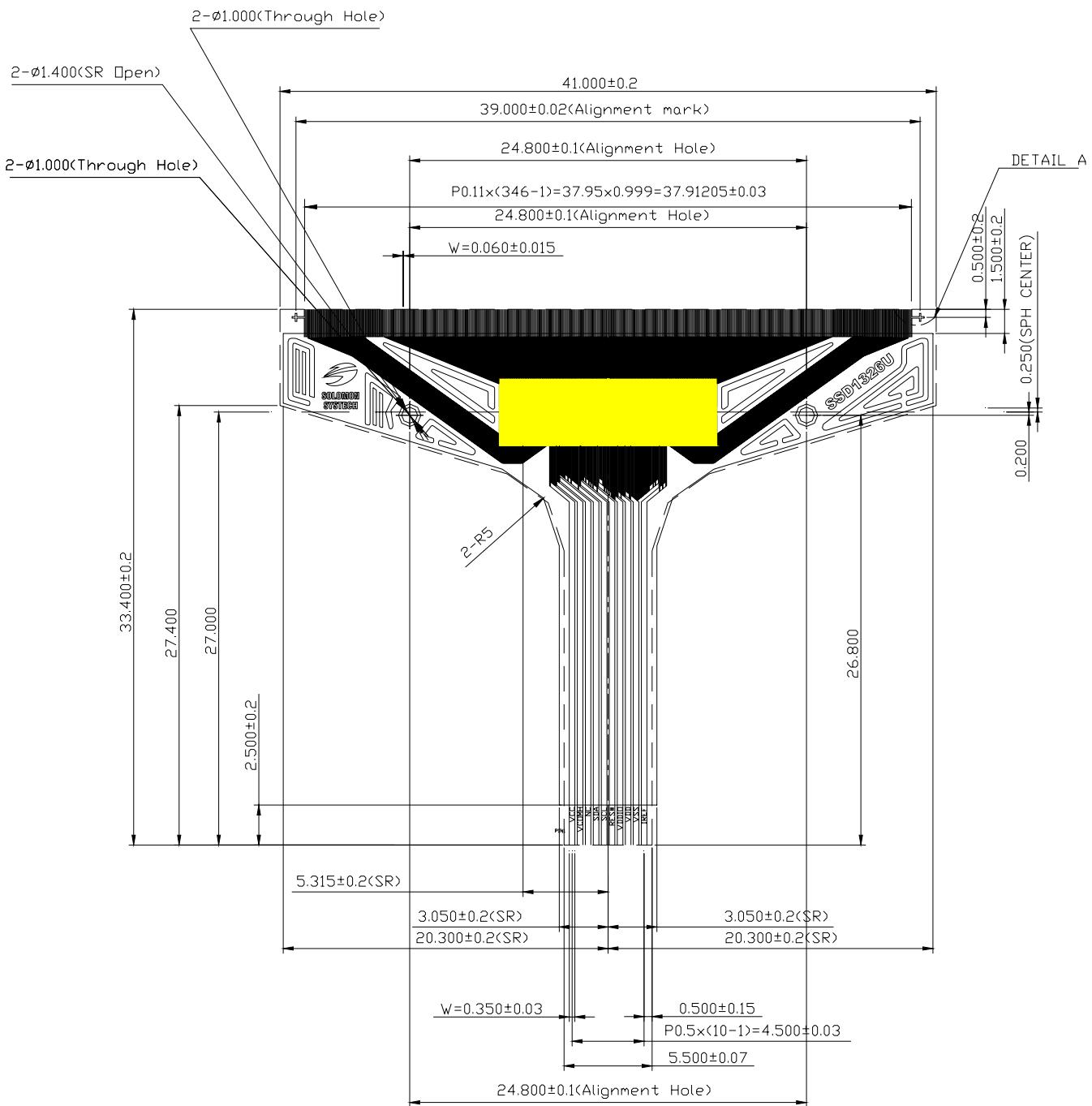
NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 10um
   OTHER GENERAL TOLERANCE±0.200mm
3. SN PLATING: 0.230±0.05um

SIDE VIEW

Contact Side
Plating: Sn

Max 1.5
(SEAL)

3.5±0.3(stiffener)

Contact Side
Plating: Sn

Stiffener(PI)

0.3±0.03

MAX 0.8

MAX 1.5mm

DIE

COPPER

KAPTON

MIRROR DESIGN

Sn-plated

W0.500

W0.500

0.500

W0.750

P1.000

W0.750

0.500

2.500

0.500

2.500

0.500
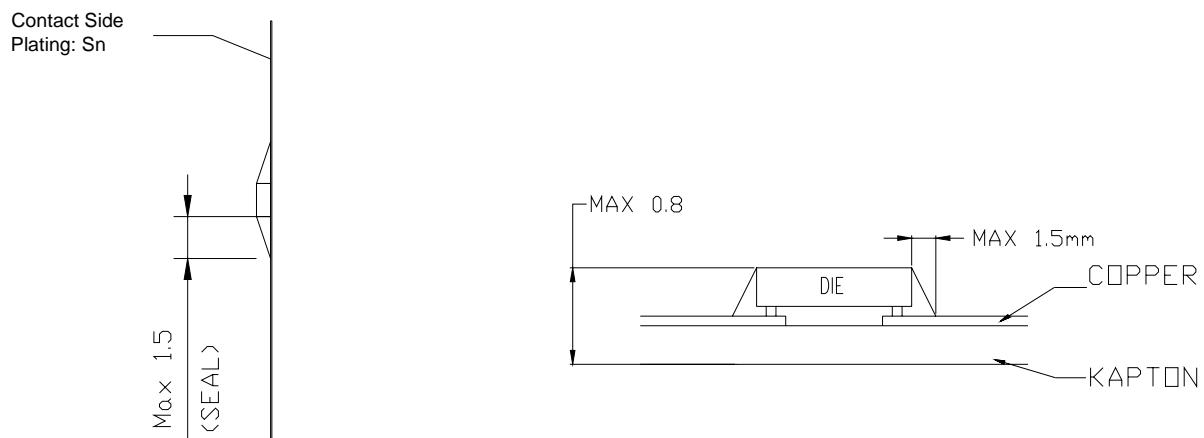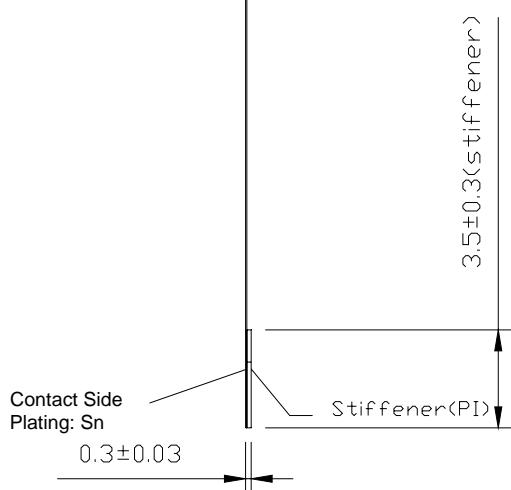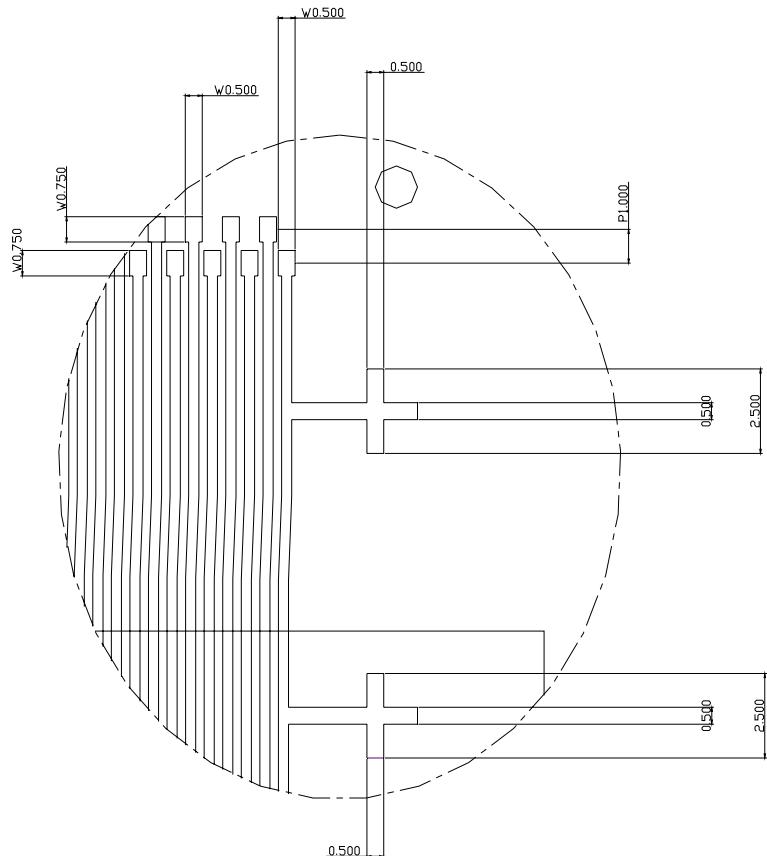
DETAIL A
SCALE: 5:1

15.2 SSD1326U1 Detail Dimension

Figure 15-2 : SSD1326U1 Detail Dimension
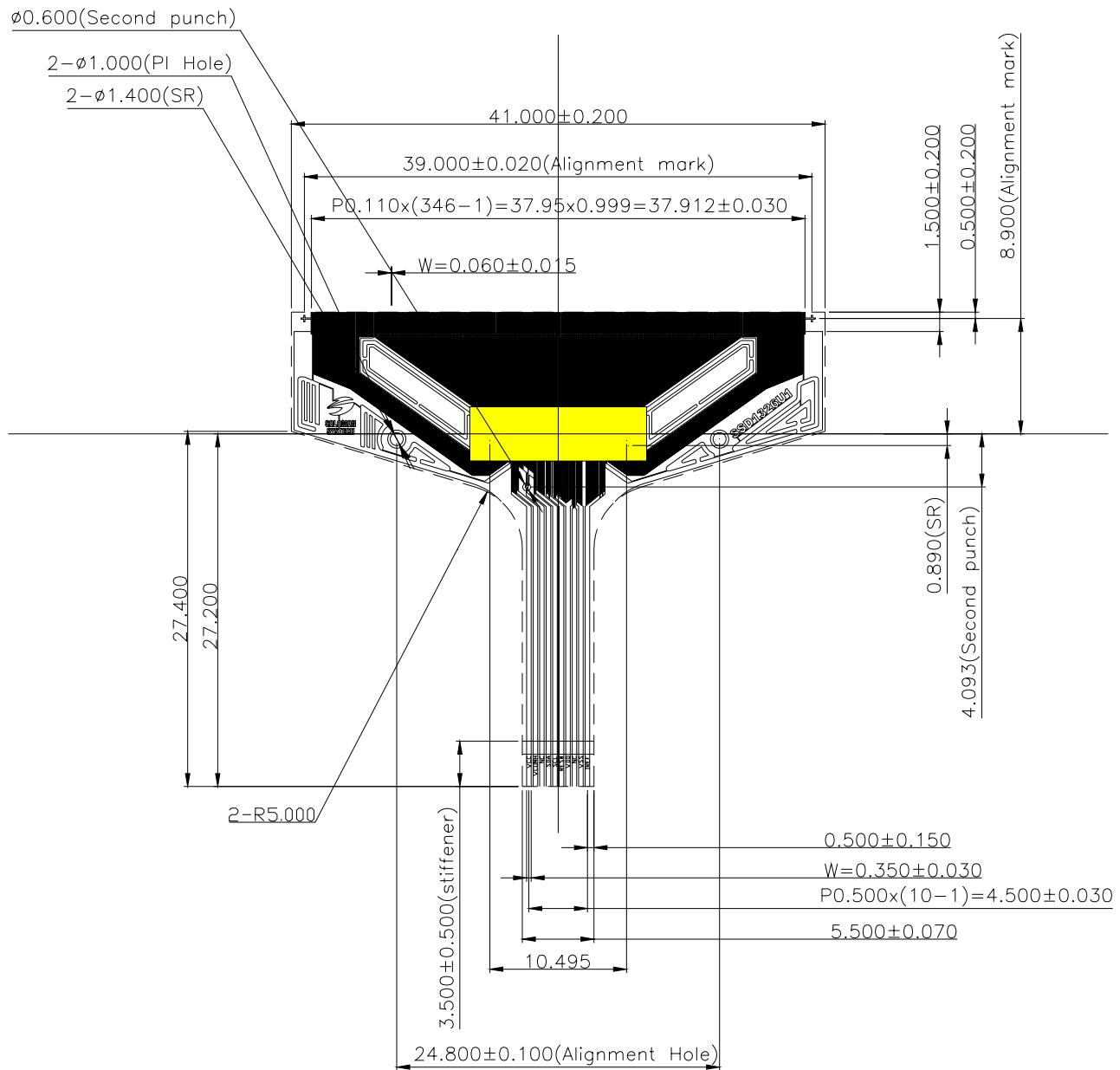
NOTE:
1. GENERAL TOLERANCE: 0.05mm
2. MATERIAL
   PI: 384um
   CU: 82um
   SR: 1510um
   (OTHER TOLERANCE: 0.200mm)
3. AU/Ni PLATING: AU 0.40.15um
                  Ni 0.50.25um

SIDE VIEW

Contact Side
Plating: Au

Max 1.5

Contact Side
Plating: Au

Stiffener (PI)

3.50.5(stiffener)

0.30.03

MAX 0.8

MAX 1.5mm

DIE

COPPER

KAPTON

MIRROR DESIGN

Au-plated

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) "Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)" and China standard "电子信息产品污染控制标识要求 (SJ/T11364-2006)" with control Marking Symbol . Hazardous Substances test report is available upon requested.

http://www.solomon-systech.com

Appendix: IC Revision history of SSD1326 Specification

Version	Content	Date
1.0	1. Add SSD1326U drawing 2. Add SSD1326U1 drawing 3. Update section 2 ordering information 4. Revise Horizontal scrolling command table and description 5. Revise section 8.8 Power ON and OFF sequence 6. Revise section 8.1.4 and Remove "CS# is serve as the data/command latch signal" part in section 8.1.4 MCU parallel 8080 series interface 7. Revise figure 13-4, table 13-5 (8080 MCU interface) 8. Revise table 11-1 Maximum ratings 9. Revise Table 12-1 and Update "TBD" and remove test condition for V_{IH}, V_{IL} on Table 12-1 10. Add a note for Fosc and Revise Fosc Typ value in table 13-1 11. Revise CL & V_{COMH} pin descriptions 12. Add key for section 6 Pin description 13. Rename LVSS into V_{LSS} in Table 5-1 14. Add TR[8:0], BGGND and V_{BREF} pin in Table 6-1 15. Add Figure 10-2 Segment current vs contrast setting 16. Add a note in Figure 14-1 about resistor value 17. Revise Die thickness to 457um from 475um 18. Add $V_{DDIO} = V_{DD}$ for Table 13-2 to13-5. 19. Revise Figure 8-10 "Segment and Common Driver Block Diagram" 20. Revise RES# timing in Table 3-1 : AC Characteristics (change to 2us from 1us) 21. Revise temperature condition for Table 13-2 (I^2C interface): (change to 25°C)	14-Sep-06
1.1	1. Revise note 2 in Section 8.8 Power ON/OFF sequence (add : "disable") 2. Revise CL pin description 3. Revise Figure 10-2 : Segment current vs Contrast setting (half current range) 4. Add light sensitive note In Section 11 – Maximum ratings	05-Dec-07
1.2	1. Add note 3-5 in Section 8.8 Power ON/OFF sequence 2. Revise CL pin description in Section 8.3 Oscillator Circuit and Display Time Generator 3. Revise Table 13-1 AC Characteristics	17-Jul-08