ST7272A

480x480 System-On-Chip Driver

for 320RGBx240 Dual Gate TFT LCD

Datasheet

Version 1.3
2019/08

Hazardous Substance Free
RoHS/ REACH Compliant

Sitronix Technology Corporation

LIST OF CONTENT

1. GENERAL DESCRIPTION

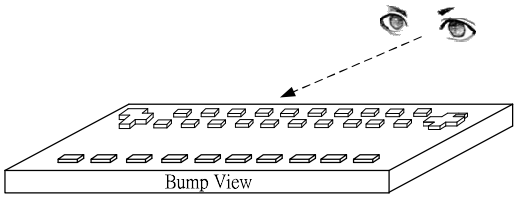
ST7272A offers all-in-one chip solution of 320RGBx240 for dual gate color TFT-LCD panel. The driver IC output ports consists of 480 source channels and 480 gate channels. This chip incorporated with digital timing generator, source and gate driver, power supply circuit and embedded serial communication interface for function setting. This chip can support parallel 24-bit RGB and serial 8-bit RGB interface. The source output support real 8-bit resolution and 256-gray scale with small output deviation are designed to support higher color resolution. The power supply circuit incorporated with step-up circuit, regulators and operational amplifiers to generate power supply voltages to drive TFT LCD.

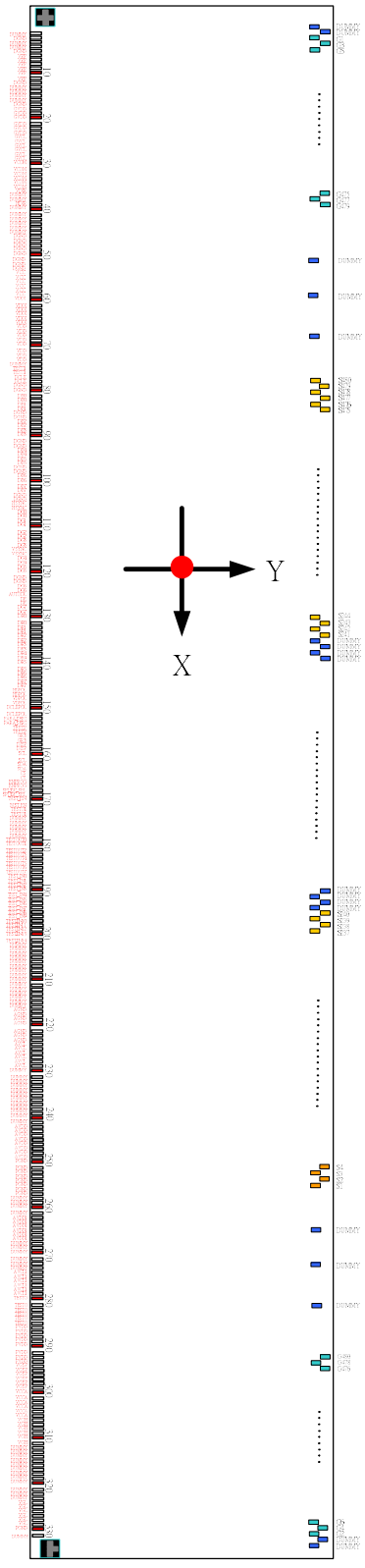
2. FEATURES

- Display Maximum Resolution:
  - support dual gate panel resolution: 320RGB * 240
- LCD Driver Output Circuits
  - source outputs: 480 channels
  - gate outputs: 480 channels
  - common electrode output
- 256 Gray Scale with True 8-bit DAC
- Microprocessor Interface
  - 8-bit and 24-bit RGB interface support: SYNC, SYNC-DE and DE mode
  - 3-wire SPI and I^2C interface
- On Chip Build-In Circuits
  - DC/DC converter
  - timing controller
- Wide Supply Voltage Range
  - I/O voltage (VDDI to DGND): 1.65V ~ 3.6V
  - analog voltage (VDD to AGND): 3.0V ~ 3.6V
  - charge pump voltage (PVDD to PGND): 3.0V ~ 3.6V
  - VDDI $\leqq$ VDD = PVDD
- On-Chip Power System
  - GVDD: 4.960V ~ 5.968V
  - GVCL: -2.960V ~ -4.480V
  - VGSP: 0.24V ~ 1.504V (VGSP = (GVDD + GVCL) / 2, the VGSP voltage is set by panel characteristics)
  - gate high level (VGH to AGND): 13V ~ 16.5V
  - gate low level (VGL to AGND): -7V ~ -10V
- Optimized Layout for COG Assembly
- Built-in OTP Programming Circuit
  - internal VPP power supply
- Multi-OTP Adjustable Parameters
  - 7-bit for VCOM offset adjustment (3 times)
  - 7-bit ID1/ ID2/ ID3 for end user use (3 times)
- **Design for Consumer Applications; Automotive Related Products are Excluded.**

3. PAD ARRANGEMENT

3.1 Output Bump Dimension



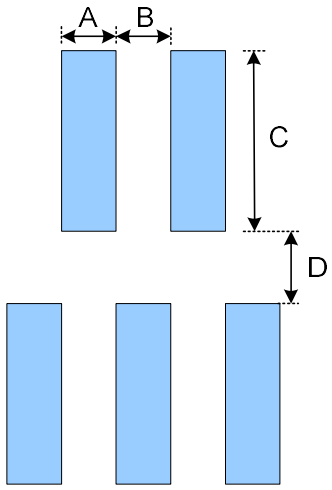


3.2 Bump Dimension

Output Pads

S1~S480、G1~G480、VCOM、DUMMY

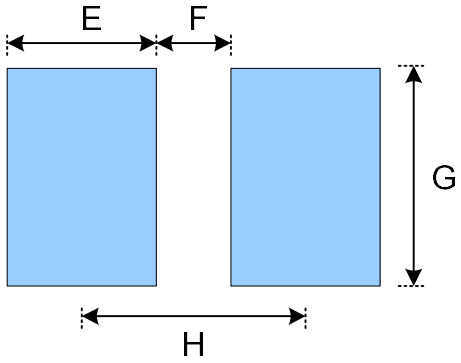
(No.332~1548)



Symbol	Item	Size
A	Bump Width	15 um
B	Bump Gap 1 (Horizontal)	15、30、75um
C	Bump Height	100 um
D	Bump Gap 2 (Vertical)	30 um

Input Pads

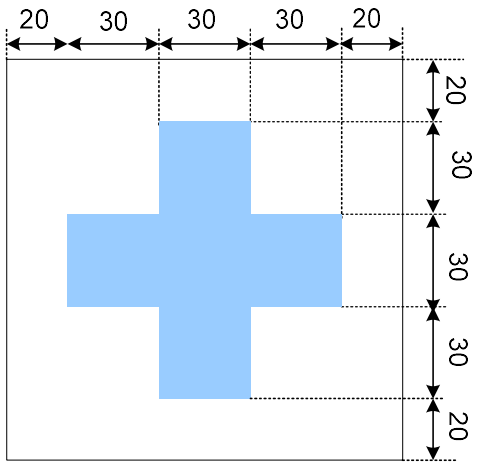
(No.1~331)



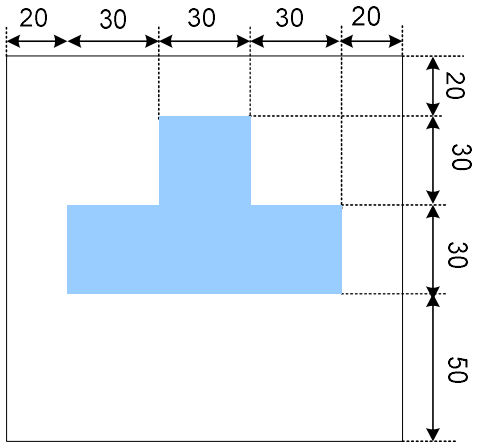
Symbol	Item	Size
E	Bump Width	35 um
F	Bump Gap	24 um
G	Bump Height	100 um
H	Bump Pitch	59 um

3.3 Alignment Mark Dimension

Alignment Mark: A1(X,Y)=(-9963,-235)



Alignment Mark: A2(X,Y)=(9963,-235)



3.4 Chip Information

Chip Size	20180um x 710um
Chip thickness	300μm
Pad Location	Pad center
Coordinate Origin	Chip center
Au bump height	9um

4. PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y
1	DUMMY	-9735	-257
2	DGND	-9676	-257
3	DUMMY	-9617	-257
4	DUMMY	-9558	-257
5	DGND	-9499	-257
6	VPP	-9440	-257
7	VPP	-9381	-257
8	VPP	-9322	-257
9	VPP	-9263	-257
10	VPP	-9204	-257
11	VPP	-9145	-257
12	DGND	-9086	-257
13	DUMMY	-9027	-257
14	DUMMY	-8968	-257
15	DUMMY	-8909	-257
16	DUMMY	-8850	-257
17	DGND	-8791	-257
18	GVDD	-8732	-257
19	GVDD	-8673	-257
20	GVDD	-8614	-257
21	GVDD	-8555	-257
22	GVDD	-8496	-257
23	GVDD	-8437	-257
24	GVCL	-8378	-257
25	GVCL	-8319	-257
26	GVCL	-8260	-257
27	GVCL	-8201	-257
28	GVCL	-8142	-257
29	GVCL	-8083	-257
30	VCOM	-8024	-257
31	VCOM	-7965	-257
32	VCOM	-7906	-257
33	VCOM	-7847	-257
34	VCOM	-7788	-257
35	VCOM	-7729	-257
36	VDIR	-7670	-257
37	DUMMY	-7611	-257
38	DUMMY	-7552	-257
39	HDIR	-7493	-257
40	DUMMY	-7434	-257
41	DUMMY	-7375	-257
42	DUMMY	-7316	-257
43	DUMMY	-7257	-257
44	DUMMY	-7198	-257
45	DUMMY	-7139	-257
46	DGND	-7080	-257
47	DGND	-7021	-257
48	DGND	-6962	-257
49	DGND	-6903	-257
50	DGND	-6844	-257
51	DGND	-6785	-257
52	DGND	-6726	-257
53	DGND	-6667	-257
54	VCC	-6608	-257
55	VCC	-6549	-257
56	VCC	-6490	-257
57	VCC	-6431	-257
58	VCC	-6372	-257
59	VCC	-6313	-257
60	VDDI	-6254	-257
61	VDDI	-6195	-257
62	VDDI	-6136	-257
63	VDDI	-6077	-257
64	VDDI	-6018	-257
65	VDDI	-5959	-257
66	VDD	-5900	-257

PAD No.	PIN Name	X	Y
67	VDD	-5841	-257
68	VDD	-5782	-257
69	VDD	-5723	-257
70	VDD	-5664	-257
71	VDD	-5605	-257
72	VDD	-5546	-257
73	VDD	-5487	-257
74	DUMMY	-5428	-257
75	TESTI1	-5369	-257
76	TESTI1	-5310	-257
77	DCLK	-5251	-257
78	DCLK	-5192	-257
79	DGND	-5133	-257
80	DGND	-5074	-257
81	DB0	-5015	-257
82	DB0	-4956	-257
83	DB1	-4897	-257
84	DB1	-4838	-257
85	DGND	-4779	-257
86	DGND	-4720	-257
87	DB2	-4661	-257
88	DB2	-4602	-257
89	DB3	-4543	-257
90	DB3	-4484	-257
91	DGND	-4425	-257
92	DGND	-4366	-257
93	DB4	-4307	-257
94	DB4	-4248	-257
95	DB5	-4189	-257
96	DB5	-4130	-257
97	DGND	-4071	-257
98	DGND	-4012	-257
99	DB6	-3953	-257
100	DB6	-3894	-257
101	DB7	-3835	-257
102	DB7	-3776	-257
103	DGND	-3717	-257
104	DGND	-3658	-257
105	HSYNC	-3599	-257
106	HSYNC	-3540	-257
107	DG0	-3481	-257
108	DG0	-3422	-257
109	DG1	-3363	-257
110	DG1	-3304	-257
111	DG2	-3245	-257
112	DG2	-3186	-257
113	DG3	-3127	-257
114	DG3	-3068	-257
115	VSYNC	-3009	-257
116	VSYNC	-2950	-257
117	DG4	-2891	-257
118	DG4	-2832	-257
119	DG5	-2773	-257
120	DG5	-2714	-257
121	DGND	-2655	-257
122	DGND	-2596	-257
123	DG6	-2537	-257
124	DG6	-2478	-257
125	AUTODL	-2419	-257
126	DE	-2360	-257
127	DE	-2301	-257
128	DG7	-2242	-257
129	DG7	-2183	-257
130	DR0	-2124	-257
131	DR0	-2065	-257
132	DR1	-2006	-257
133	DR1	-1947	-257
134	DR2	-1888	-257

PAD No.	PIN Name	X	Y
135	DR2	-1829	-257
136	DR3	-1770	-257
137	DR3	-1711	-257
138	DR4	-1652	-257
139	DR4	-1593	-257
140	DR5	-1534	-257
141	DR5	-1475	-257
142	DR6	-1416	-257
143	DR6	-1357	-257
144	DR7	-1298	-257
145	DR7	-1239	-257
146	HDPOL	-1180	-257
147	HDPOL	-1121	-257
148	VDPOL	-1062	-257
149	VDPOL	-1003	-257
150	DCLKPOL	-944	-257
151	DCLKPOL	-885	-257
152	PARA_SERI	-826	-257
153	PARA_SERI	-767	-257
154	TESTI2	-708	-257
155	TESTI2	-649	-257
156	GRB	-590	-257
157	GRB	-531	-257
158	DISP	-472	-257
159	DISP	-413	-257
160	SCL	-354	-257
161	SCL	-295	-257
162	SDA	-236	-257
163	SDA	-177	-257
164	CS	-118	-257
165	CS	-59	-257
166	ENPROG	0	-257
167	ENPROG	59	-257
168	SPI_I²C_SEL	118	-257
169	SPI_I²C_SEL	177	-257
170	BIST_EN	236	-257
171	BIST_EN	295	-257
172	TESTO1	354	-257
173	TESTO1	413	-257
174	DUMMY	472	-257
175	DUMMY	531	-257
176	DUMMY	590	-257
177	DUMMY	649	-257
178	DUMMY	708	-257
179	TESTOUT0	767	-257
180	TESTOUT1	826	-257
181	TESTOUT2	885	-257
182	TESTOUT3	944	-257
183	TESTOUT4	1003	-257
184	TESTOUT5	1062	-257
185	TESTOUT6	1121	-257
186	TESTOUT7	1180	-257
187	TEST_IN0	1239	-257
188	TEST_IN1	1298	-257
189	TEST_IN2	1357	-257
190	TEST_IN3	1416	-257
191	TEST_IN4	1475	-257
192	TEST_IN5	1534	-257
193	TEST_IN6	1593	-257
194	TEST_IN7	1652	-257
195	TEST_IN8	1711	-257
196	TEST_IN9	1770	-257
197	TEST_IN10	1829	-257
198	TEST_IN11	1888	-257
199	TEST_IN12	1947	-257
200	TEST_IN13	2006	-257
201	TEST_IN14	2065	-257
202	DUMMY	2124	-257

PAD No.	PIN Name	X	Y
203	DUMMY	2183	-257
204	DUMMY	2242	-257
205	DUMMY	2301	-257
206	DUMMY	2360	-257
207	DUMMY	2419	-257
208	DUMMY	2478	-257
209	DUMMY	2537	-257
210	DUMMY	2596	-257
211	DUMMY	2655	-257
212	DUMMY	2714	-257
213	DUMMY	2773	-257
214	DUMMY	2832	-257
215	DUMMY	2891	-257
216	DUMMY	2950	-257
217	AGND	3009	-257
218	AGND	3068	-257
219	AGND	3127	-257
220	AGND	3186	-257
221	AGND	3245	-257
222	AGND	3304	-257
223	AGND	3363	-257
224	AVCL	3422	-257
225	AVCL	3481	-257
226	AVCL	3540	-257
227	AVCL	3599	-257
228	AVCL	3658	-257
229	AVCL	3717	-257
230	DUMMY	3776	-257
231	DUMMY	3835	-257
232	DUMMY	3894	-257
233	DUMMY	3953	-257
234	DUMMY	4012	-257
235	DUMMY	4071	-257
236	DUMMY	4130	-257

PAD No.	PIN Name	X	Y
237	DUMMY	4189	-257
238	DUMMY	4248	-257
239	DUMMY	4307	-257
240	DUMMY	4366	-257
241	DUMMY	4425	-257
242	AVDD	4484	-257
243	AVDD	4543	-257
244	AVDD	4602	-257
245	AVDD	4661	-257
246	AVDD	4720	-257
247	AVDD	4779	-257
248	AVDD	4838	-257
249	AVDD	4897	-257
250	PGND	4956	-257
251	PGND	5015	-257
252	PGND	5074	-257
253	PGND	5133	-257
254	PGND	5192	-257
255	PGND	5251	-257
256	PGND	5310	-257
257	PGND	5369	-257
258	DUMMY	5428	-257
259	DUMMY	5487	-257
260	DUMMY	5546	-257
261	DUMMY	5605	-257
262	AVDD1	5664	-257
263	AVDD1	5723	-257
264	AVDD1	5782	-257
265	AVDD1	5841	-257
266	AVDD1	5900	-257
267	AVDD1	5959	-257
268	DUMMY	6018	-257
269	DUMMY	6077	-257
270	DUMMY	6136	-257

PAD No.	PIN Name	X	Y
271	DUMMY	6195	-257
272	DUMMY	6254	-257
273	DUMMY	6313	-257
274	AVCL1	6372	-257
275	AVCL1	6431	-257
276	AVCL1	6490	-257
277	AVCL1	6549	-257
278	AVCL1	6608	-257
279	AVCL1	6667	-257
280	TESTO	6726	-257
281	TESTO	6785	-257
282	TESTO	6844	-257
283	TESTO	6903	-257
284	TESTO	6962	-257
285	TESTO	7021	-257
286	PVDD	7080	-257
287	PVDD	7139	-257
288	PVDD	7198	-257
289	PVDD	7257	-257
290	PVDD	7316	-257
291	PVDD	7375	-257
292	PVDD	7434	-257
293	PVDD	7493	-257
294	VGSP	7552	-257
295	VGSP	7611	-257
296	VGSP	7670	-257
297	VGSP	7729	-257
298	VGSP	7788	-257
299	VGSP	7847	-257
300	VCCA	7906	-257
301	VCCA	7965	-257
302	VCCA	8024	-257
303	VCCA	8083	-257
304	VCCA	8142	-257

PAD No.	PIN Name	X	Y
305	VCCA	8201	-257
306	VGH	8260	-257
307	VGH	8319	-257
308	VGH	8378	-257
309	VGH	8437	-257
310	VGH	8496	-257
311	VGH	8555	-257
312	DUMMY	8614	-257
313	DUMMY	8673	-257
314	DUMMY	8732	-257
315	DUMMY	8791	-257
316	DUMMY	8850	-257
317	DUMMY	8909	-257
318	DUMMY	8968	-257
319	DUMMY	9027	-257
320	DUMMY	9086	-257
321	DUMMY	9145	-257
322	DUMMY	9204	-257
323	DUMMY	9263	-257
324	VGL	9322	-257
325	VGL	9381	-257
326	VGL	9440	-257
327	VGL	9499	-257
328	VGL	9558	-257
329	VGL	9617	-257
330	PGND	9676	-257
331	DUMMY	9735	-257
332	DUMMY	9945	127
333	DUMMY	9930	257
334	G2	9900	127
335	G4	9885	257
336	G6	9870	127
337	G8	9855	257
338	G10	9840	127

PAD No.	PIN Name	X	Y
339	G12	9825	257
340	G14	9810	127
341	G16	9795	257
342	G18	9780	127
343	G20	9765	257
344	G22	9750	127
345	G24	9735	257
346	G26	9720	127
347	G28	9705	257
348	G30	9690	127
349	G32	9675	257
350	G34	9660	127
351	G36	9645	257
352	G38	9630	127
353	G40	9615	257
354	G42	9600	127
355	G44	9585	257
356	G46	9570	127
357	G48	9555	257
358	G50	9540	127
359	G52	9525	257
360	G54	9510	127
361	G56	9495	257
362	G58	9480	127
363	G60	9465	257
364	G62	9450	127
365	G64	9435	257
366	G66	9420	127
367	G68	9405	257
368	G70	9390	127
369	G72	9375	257
370	G74	9360	127
371	G76	9345	257
372	G78	9330	127

PAD No.	PIN Name	X	Y
373	G80	9315	257
374	G82	9300	127
375	G84	9285	257
376	G86	9270	127
377	G88	9255	257
378	G90	9240	127
379	G92	9225	257
380	G94	9210	127
381	G96	9195	257
382	G98	9180	127
383	G100	9165	257
384	G102	9150	127
385	G104	9135	257
386	G106	9120	127
387	G108	9105	257
388	G110	9090	127
389	G112	9075	257
390	G114	9060	127
391	G116	9045	257
392	G118	9030	127
393	G120	9015	257
394	G122	9000	127
395	G124	8985	257
396	G126	8970	127
397	G128	8955	257
398	G130	8940	127
399	G132	8925	257
400	G134	8910	127
401	G136	8895	257
402	G138	8880	127
403	G140	8865	257
404	G142	8850	127
405	G144	8835	257
406	G146	8820	127

PAD No.	PIN Name	X	Y
407	G148	8805	257
408	G150	8790	127
409	G152	8775	257
410	G154	8760	127
411	G156	8745	257
412	G158	8730	127
413	G160	8715	257
414	G162	8700	127
415	G164	8685	257
416	G166	8670	127
417	G168	8655	257
418	G170	8640	127
419	G172	8625	257
420	G174	8610	127
421	G176	8595	257
422	G178	8580	127
423	G180	8565	257
424	G182	8550	127
425	G184	8535	257
426	G186	8520	127
427	G188	8505	257
428	G190	8490	127
429	G192	8475	257
430	G194	8460	127
431	G196	8445	257
432	G198	8430	127
433	G200	8415	257
434	G202	8400	127
435	G204	8385	257
436	G206	8370	127
437	G208	8355	257
438	G210	8340	127
439	G212	8325	257
440	G214	8310	127

PAD No.	PIN Name	X	Y
441	G216	8295	257
442	G218	8280	127
443	G220	8265	257
444	G222	8250	127
445	G224	8235	257
446	G226	8220	127
447	G228	8205	257
448	G230	8190	127
449	G232	8175	257
450	G234	8160	127
451	G236	8145	257
452	G238	8130	127
453	G240	8115	257
454	G242	8100	127
455	G244	8085	257
456	G246	8070	127
457	G248	8055	257
458	G250	8040	127
459	G252	8025	257
460	G254	8010	127
461	G256	7995	257
462	G258	7980	127
463	G260	7965	257
464	G262	7950	127
465	G264	7935	257
466	G266	7920	127
467	G268	7905	257
468	G270	7890	127
469	G272	7875	257
470	G274	7860	127
471	G276	7845	257
472	G278	7830	127
473	G280	7815	257
474	G282	7800	127

PAD No.	PIN Name	X	Y
475	G284	7785	257
476	G286	7770	127
477	G288	7755	257
478	G290	7740	127
479	G292	7725	257
480	G294	7710	127
481	G296	7695	257
482	G298	7680	127
483	G300	7665	257
484	G302	7650	127
485	G304	7635	257
486	G306	7620	127
487	G308	7605	257
488	G310	7590	127
489	G312	7575	257
490	G314	7560	127
491	G316	7545	257
492	G318	7530	127
493	G320	7515	257
494	G322	7500	127
495	G324	7485	257
496	G326	7470	127
497	G328	7455	257
498	G330	7440	127
499	G332	7425	257
500	G334	7410	127
501	G336	7395	257
502	G338	7380	127
503	G340	7365	257
504	G342	7350	127
505	G344	7335	257
506	G346	7320	127
507	G348	7305	257
508	G350	7290	127

PAD No.	PIN Name	X	Y
509	G352	7275	257
510	G354	7260	127
511	G356	7245	257
512	G358	7230	127
513	G360	7215	257
514	G362	7200	127
515	G364	7185	257
516	G366	7170	127
517	G368	7155	257
518	G370	7140	127
519	G372	7125	257
520	G374	7110	127
521	G376	7095	257
522	G378	7080	127
523	G380	7065	257
524	G382	7050	127
525	G384	7035	257
526	G386	7020	127
527	G388	7005	257
528	G390	6990	127
529	G392	6975	257
530	G394	6960	127
531	G396	6945	257
532	G398	6930	127
533	G400	6915	257
534	G402	6900	127
535	G404	6885	257
536	G406	6870	127
537	G408	6855	257
538	G410	6840	127
539	G412	6825	257
540	G414	6810	127
541	G416	6795	257
542	G418	6780	127

PAD No.	PIN Name	X	Y
543	G420	6765	257
544	G422	6750	127
545	G424	6735	257
546	G426	6720	127
547	G428	6705	257
548	G430	6690	127
549	G432	6675	257
550	G434	6660	127
551	G436	6645	257
552	G438	6630	127
553	G440	6615	257
554	G442	6600	127
555	G444	6585	257
556	G446	6570	127
557	G448	6555	257
558	G450	6540	127
559	G452	6525	257
560	G454	6510	127
561	G456	6495	257
562	G458	6480	127
563	G460	6465	257
564	G462	6450	127
565	G464	6435	257
566	G466	6420	127
567	G468	6405	257
568	G470	6390	127
569	G472	6375	257
570	G474	6360	127
571	G476	6345	257
572	G478	6330	127
573	G480	6315	257
574	DUMMY	6150	127
575	DUMMY	5970	127
576	DUMMY	5760	127

PAD No.	PIN Name	X	Y
577	S1	5610	127
578	S2	5595	257
579	S3	5580	127
580	S4	5565	257
581	S5	5550	127
582	S6	5535	257
583	S7	5520	127
584	S8	5505	257
585	S9	5490	127
586	S10	5475	257
587	S11	5460	127
588	S12	5445	257
589	S13	5430	127
590	S14	5415	257
591	S15	5400	127
592	S16	5385	257
593	S17	5370	127
594	S18	5355	257
595	S19	5340	127
596	S20	5325	257
597	S21	5310	127
598	S22	5295	257
599	S23	5280	127
600	S24	5265	257
601	S25	5250	127
602	S26	5235	257
603	S27	5220	127
604	S28	5205	257
605	S29	5190	127
606	S30	5175	257
607	S31	5160	127
608	S32	5145	257
609	S33	5130	127
610	S34	5115	257

PAD No.	PIN Name	X	Y
611	S35	5100	127
612	S36	5085	257
613	S37	5070	127
614	S38	5055	257
615	S39	5040	127
616	S40	5025	257
617	S41	5010	127
618	S42	4995	257
619	S43	4980	127
620	S44	4965	257
621	S45	4950	127
622	S46	4935	257
623	S47	4920	127
624	S48	4905	257
625	S49	4890	127
626	S50	4875	257
627	S51	4860	127
628	S52	4845	257
629	S53	4830	127
630	S54	4815	257
631	S55	4800	127
632	S56	4785	257
633	S57	4770	127
634	S58	4755	257
635	S59	4740	127
636	S60	4725	257
637	S61	4710	127
638	S62	4695	257
639	S63	4680	127
640	S64	4665	257
641	S65	4650	127
642	S66	4635	257
643	S67	4620	127
644	S68	4605	257

PAD No.	PIN Name	X	Y
645	S69	4590	127
646	S70	4575	257
647	S71	4560	127
648	S72	4545	257
649	S73	4530	127
650	S74	4515	257
651	S75	4500	127
652	S76	4485	257
653	S77	4470	127
654	S78	4455	257
655	S79	4440	127
656	S80	4425	257
657	S81	4410	127
658	S82	4395	257
659	S83	4380	127
660	S84	4365	257
661	S85	4350	127
662	S86	4335	257
663	S87	4320	127
664	S88	4305	257
665	S89	4290	127
666	S90	4275	257
667	S91	4260	127
668	S92	4245	257
669	S93	4230	127
670	S94	4215	257
671	S95	4200	127
672	S96	4185	257
673	S97	4170	127
674	S98	4155	257
675	S99	4140	127
676	S100	4125	257
677	S101	4110	127
678	S102	4095	257

PAD No.	PIN Name	X	Y
679	S103	4080	127
680	S104	4065	257
681	S105	4050	127
682	S106	4035	257
683	S107	4020	127
684	S108	4005	257
685	S109	3990	127
686	S110	3975	257
687	S111	3960	127
688	S112	3945	257
689	S113	3930	127
690	S114	3915	257
691	S115	3900	127
692	S116	3885	257
693	S117	3870	127
694	S118	3855	257
695	S119	3840	127
696	S120	3825	257
697	S121	3810	127
698	S122	3795	257
699	S123	3780	127
700	S124	3765	257
701	S125	3750	127
702	S126	3735	257
703	S127	3720	127
704	S128	3705	257
705	S129	3690	127
706	S130	3675	257
707	S131	3660	127
708	S132	3645	257
709	S133	3630	127
710	S134	3615	257
711	S135	3600	127
712	S136	3585	257

PAD No.	PIN Name	X	Y
713	S137	3570	127
714	S138	3555	257
715	S139	3540	127
716	S140	3525	257
717	S141	3510	127
718	S142	3495	257
719	S143	3480	127
720	S144	3465	257
721	S145	3450	127
722	S146	3435	257
723	S147	3420	127
724	S148	3405	257
725	S149	3390	127
726	S150	3375	257
727	S151	3360	127
728	S152	3345	257
729	S153	3330	127
730	S154	3315	257
731	S155	3300	127
732	S156	3285	257
733	S157	3270	127
734	S158	3255	257
735	S159	3240	127
736	S160	3225	257
737	S161	3210	127
738	S162	3195	257
739	S163	3180	127
740	S164	3165	257
741	S165	3150	127
742	S166	3135	257
743	S167	3120	127
744	S168	3105	257
745	S169	3090	127
746	S170	3075	257

PAD No.	PIN Name	X	Y
747	S171	3060	127
748	S172	3045	257
749	S173	3030	127
750	S174	3015	257
751	S175	3000	127
752	S176	2985	257
753	S177	2970	127
754	S178	2955	257
755	S179	2940	127
756	S180	2925	257
757	S181	2910	127
758	S182	2895	257
759	S183	2880	127
760	S184	2865	257
761	S185	2850	127
762	S186	2835	257
763	S187	2820	127
764	S188	2805	257
765	S189	2790	127
766	S190	2775	257
767	S191	2760	127
768	S192	2745	257
769	S193	2730	127
770	S194	2715	257
771	S195	2700	127
772	S196	2685	257
773	S197	2670	127
774	S198	2655	257
775	S199	2640	127
776	S200	2625	257
777	S201	2610	127
778	S202	2595	257
779	S203	2580	127
780	S204	2565	257

PAD No.	PIN Name	X	Y
781	S205	2550	127
782	S206	2535	257
783	S207	2520	127
784	S208	2505	257
785	S209	2490	127
786	S210	2475	257
787	S211	2460	127
788	S212	2445	257
789	S213	2430	127
790	S214	2415	257
791	S215	2400	127
792	S216	2385	257
793	S217	2370	127
794	S218	2355	257
795	S219	2340	127
796	S220	2325	257
797	S221	2310	127
798	S222	2295	257
799	S223	2280	127
800	S224	2265	257
801	S225	2250	127
802	S226	2235	257
803	S227	2220	127
804	S228	2205	257
805	S229	2190	127
806	S230	2175	257
807	S231	2160	127
808	S232	2145	257
809	S233	2130	127
810	S234	2115	257
811	S235	2100	127
812	S236	2085	257
813	S237	2070	127
814	S238	2055	257

PAD No.	PIN Name	X	Y
815	S239	2040	127
816	S240	2025	257
817	DUMMY	2010	127
818	DUMMY	1995	257
819	DUMMY	1980	127
820	DUMMY	1965	257
821	DUMMY	1950	127
822	DUMMY	1935	257
823	DUMMY	1920	127
824	DUMMY	1905	257
825	DUMMY	1890	127
826	DUMMY	1875	257
827	DUMMY	1860	127
828	DUMMY	1845	257
829	DUMMY	1830	127
830	DUMMY	1815	257
831	DUMMY	1800	127
832	DUMMY	1785	257
833	DUMMY	1770	127
834	DUMMY	1755	257
835	DUMMY	1740	127
836	DUMMY	1725	257
837	DUMMY	1710	127
838	DUMMY	1695	257
839	DUMMY	1680	127
840	DUMMY	1665	257
841	DUMMY	1650	127
842	DUMMY	1635	257
843	DUMMY	1620	127
844	DUMMY	1605	257
845	DUMMY	1590	127
846	DUMMY	1575	257
847	DUMMY	1560	127
848	DUMMY	1545	257

PAD No.	PIN Name	X	Y
849	DUMMY	1530	127
850	DUMMY	1515	257
851	DUMMY	1500	127
852	DUMMY	1485	257
853	DUMMY	1470	127
854	DUMMY	1455	257
855	DUMMY	1440	127
856	DUMMY	1425	257
857	DUMMY	1410	127
858	DUMMY	1395	257
859	DUMMY	1380	127
860	DUMMY	1365	257
861	DUMMY	1350	127
862	DUMMY	1335	257
863	DUMMY	1320	127
864	DUMMY	1305	257
865	DUMMY	1290	127
866	DUMMY	1275	257
867	DUMMY	1260	127
868	DUMMY	1245	257
869	DUMMY	1230	127
870	DUMMY	1215	257
871	DUMMY	1200	127
872	DUMMY	1185	257
873	DUMMY	1170	127
874	DUMMY	1155	257
875	DUMMY	1140	127
876	DUMMY	1125	257
877	DUMMY	1110	127
878	DUMMY	1095	257
879	DUMMY	1080	127
880	DUMMY	1065	257
881	DUMMY	1050	127
882	DUMMY	1035	257

PAD No.	PIN Name	X	Y
883	DUMMY	1020	127
884	DUMMY	1005	257
885	DUMMY	990	127
886	DUMMY	975	257
887	DUMMY	960	127
888	DUMMY	945	257
889	DUMMY	930	127
890	DUMMY	915	257
891	DUMMY	900	127
892	DUMMY	885	257
893	DUMMY	870	127
894	DUMMY	855	257
895	DUMMY	840	127
896	DUMMY	825	257
897	DUMMY	810	127
898	DUMMY	795	257
899	DUMMY	780	127
900	DUMMY	765	257
901	DUMMY	750	127
902	DUMMY	735	257
903	DUMMY	720	127
904	DUMMY	705	257
905	DUMMY	690	127
906	DUMMY	675	257
907	DUMMY	660	127
908	DUMMY	645	257
909	DUMMY	630	127
910	DUMMY	615	257
911	DUMMY	600	127
912	DUMMY	585	257
913	DUMMY	570	127
914	DUMMY	555	257
915	DUMMY	540	127
916	DUMMY	525	257

PAD No.	PIN Name	X	Y
917	DUMMY	510	127
918	DUMMY	495	257
919	DUMMY	480	127
920	DUMMY	465	257
921	DUMMY	450	127
922	DUMMY	435	257
923	DUMMY	420	127
924	DUMMY	405	257
925	DUMMY	390	127
926	DUMMY	375	257
927	DUMMY	360	127
928	DUMMY	345	257
929	DUMMY	330	127
930	DUMMY	315	257
931	DUMMY	300	127
932	DUMMY	285	257
933	DUMMY	270	127
934	DUMMY	255	257
935	DUMMY	240	127
936	DUMMY	225	257
937	DUMMY	150	127
938	DUMMY	135	257
939	DUMMY	120	127
940	DUMMY	105	257
941	DUMMY	90	127
942	DUMMY	75	257
943	DUMMY	60	127
944	DUMMY	-15	257
945	DUMMY	-30	127
946	DUMMY	-45	257
947	DUMMY	-60	127
948	DUMMY	-75	257
949	DUMMY	-90	127
950	DUMMY	-105	257

PAD No.	PIN Name	X	Y
951	DUMMY	-120	127
952	DUMMY	-135	257
953	DUMMY	-150	127
954	DUMMY	-165	257
955	DUMMY	-180	127
956	DUMMY	-195	257
957	DUMMY	-210	127
958	DUMMY	-225	257
959	DUMMY	-240	127
960	DUMMY	-255	257
961	DUMMY	-270	127
962	DUMMY	-285	257
963	DUMMY	-300	127
964	DUMMY	-315	257
965	DUMMY	-330	127
966	DUMMY	-345	257
967	DUMMY	-360	127
968	DUMMY	-375	257
969	DUMMY	-390	127
970	DUMMY	-405	257
971	DUMMY	-420	127
972	DUMMY	-435	257
973	DUMMY	-450	127
974	DUMMY	-465	257
975	DUMMY	-480	127
976	DUMMY	-495	257
977	DUMMY	-510	127
978	DUMMY	-525	257
979	DUMMY	-540	127
980	DUMMY	-555	257
981	DUMMY	-570	127
982	DUMMY	-585	257
983	DUMMY	-600	127
984	DUMMY	-615	257

PAD No.	PIN Name	X	Y
985	DUMMY	-630	127
986	DUMMY	-645	257
987	DUMMY	-660	127
988	DUMMY	-675	257
989	DUMMY	-690	127
990	DUMMY	-705	257
991	DUMMY	-720	127
992	DUMMY	-735	257
993	DUMMY	-750	127
994	DUMMY	-765	257
995	DUMMY	-780	127
996	DUMMY	-795	257
997	DUMMY	-810	127
998	DUMMY	-825	257
999	DUMMY	-840	127
1000	DUMMY	-855	257
1001	DUMMY	-870	127
1002	DUMMY	-885	257
1003	DUMMY	-900	127
1004	DUMMY	-915	257
1005	DUMMY	-930	127
1006	DUMMY	-945	257
1007	DUMMY	-960	127
1008	DUMMY	-975	257
1009	DUMMY	-990	127
1010	DUMMY	-1005	257
1011	DUMMY	-1020	127
1012	DUMMY	-1035	257
1013	DUMMY	-1050	127
1014	DUMMY	-1065	257
1015	DUMMY	-1080	127
1016	DUMMY	-1095	257
1017	DUMMY	-1110	127
1018	DUMMY	-1125	257

PAD No.	PIN Name	X	Y
1019	DUMMY	-1140	127
1020	DUMMY	-1155	257
1021	DUMMY	-1170	127
1022	DUMMY	-1185	257
1023	DUMMY	-1200	127
1024	DUMMY	-1215	257
1025	DUMMY	-1230	127
1026	DUMMY	-1245	257
1027	DUMMY	-1260	127
1028	DUMMY	-1275	257
1029	DUMMY	-1290	127
1030	DUMMY	-1305	257
1031	DUMMY	-1320	127
1032	DUMMY	-1335	257
1033	DUMMY	-1350	127
1034	DUMMY	-1365	257
1035	DUMMY	-1380	127
1036	DUMMY	-1395	257
1037	DUMMY	-1410	127
1038	DUMMY	-1425	257
1039	DUMMY	-1440	127
1040	DUMMY	-1455	257
1041	DUMMY	-1470	127
1042	DUMMY	-1485	257
1043	DUMMY	-1500	127
1044	DUMMY	-1515	257
1045	DUMMY	-1530	127
1046	DUMMY	-1545	257
1047	DUMMY	-1560	127
1048	DUMMY	-1575	257
1049	DUMMY	-1590	127
1050	DUMMY	-1605	257
1051	DUMMY	-1620	127
1052	DUMMY	-1635	257

PAD No.	PIN Name	X	Y
1053	DUMMY	-1650	127
1054	DUMMY	-1665	257
1055	DUMMY	-1680	127
1056	DUMMY	-1695	257
1057	DUMMY	-1710	127
1058	DUMMY	-1725	257
1059	DUMMY	-1740	127
1060	DUMMY	-1755	257
1061	DUMMY	-1770	127
1062	DUMMY	-1785	257
1063	DUMMY	-1800	127
1064	S241	-1815	257
1065	S242	-1830	127
1066	S243	-1845	257
1067	S244	-1860	127
1068	S245	-1875	257
1069	S246	-1890	127
1070	S247	-1905	257
1071	S248	-1920	127
1072	S249	-1935	257
1073	S250	-1950	127
1074	S251	-1965	257
1075	S252	-1980	127
1076	S253	-1995	257
1077	S254	-2010	127
1078	S255	-2025	257
1079	S256	-2040	127
1080	S257	-2055	257
1081	S258	-2070	127
1082	S259	-2085	257
1083	S260	-2100	127
1084	S261	-2115	257
1085	S262	-2130	127
1086	S263	-2145	257

PAD No.	PIN Name	X	Y
1087	S264	-2160	127
1088	S265	-2175	257
1089	S266	-2190	127
1090	S267	-2205	257
1091	S268	-2220	127
1092	S269	-2235	257
1093	S270	-2250	127
1094	S271	-2265	257
1095	S272	-2280	127
1096	S273	-2295	257
1097	S274	-2310	127
1098	S275	-2325	257
1099	S276	-2340	127
1100	S277	-2355	257
1101	S278	-2370	127
1102	S279	-2385	257
1103	S280	-2400	127
1104	S281	-2415	257
1105	S282	-2430	127
1106	S283	-2445	257
1107	S284	-2460	127
1108	S285	-2475	257
1109	S286	-2490	127
1110	S287	-2505	257
1111	S288	-2520	127
1112	S289	-2535	257
1113	S290	-2550	127
1114	S291	-2565	257
1115	S292	-2580	127
1116	S293	-2595	257
1117	S294	-2610	127
1118	S295	-2625	257
1119	S296	-2640	127
1120	S297	-2655	257

PAD No.	PIN Name	X	Y
1121	S298	-2670	127
1122	S299	-2685	257
1123	S300	-2700	127
1124	S301	-2715	257
1125	S302	-2730	127
1126	S303	-2745	257
1127	S304	-2760	127
1128	S305	-2775	257
1129	S306	-2790	127
1130	S307	-2805	257
1131	S308	-2820	127
1132	S309	-2835	257
1133	S310	-2850	127
1134	S311	-2865	257
1135	S312	-2880	127
1136	S313	-2895	257
1137	S314	-2910	127
1138	S315	-2925	257
1139	S316	-2940	127
1140	S317	-2955	257
1141	S318	-2970	127
1142	S319	-2985	257
1143	S320	-3000	127
1144	S321	-3015	257
1145	S322	-3030	127
1146	S323	-3045	257
1147	S324	-3060	127
1148	S325	-3075	257
1149	S326	-3090	127
1150	S327	-3105	257
1151	S328	-3120	127
1152	S329	-3135	257
1153	S330	-3150	127
1154	S331	-3165	257

PAD No.	PIN Name	X	Y
1155	S332	-3180	127
1156	S333	-3195	257
1157	S334	-3210	127
1158	S335	-3225	257
1159	S336	-3240	127
1160	S337	-3255	257
1161	S338	-3270	127
1162	S339	-3285	257
1163	S340	-3300	127
1164	S341	-3315	257
1165	S342	-3330	127
1166	S343	-3345	257
1167	S344	-3360	127
1168	S345	-3375	257
1169	S346	-3390	127
1170	S347	-3405	257
1171	S348	-3420	127
1172	S349	-3435	257
1173	S350	-3450	127
1174	S351	-3465	257
1175	S352	-3480	127
1176	S353	-3495	257
1177	S354	-3510	127
1178	S355	-3525	257
1179	S356	-3540	127
1180	S357	-3555	257
1181	S358	-3570	127
1182	S359	-3585	257
1183	S360	-3600	127
1184	S361	-3615	257
1185	S362	-3630	127
1186	S363	-3645	257
1187	S364	-3660	127
1188	S365	-3675	257

PAD No.	PIN Name	X	Y
1189	S366	-3690	127
1190	S367	-3705	257
1191	S368	-3720	127
1192	S369	-3735	257
1193	S370	-3750	127
1194	S371	-3765	257
1195	S372	-3780	127
1196	S373	-3795	257
1197	S374	-3810	127
1198	S375	-3825	257
1199	S376	-3840	127
1200	S377	-3855	257
1201	S378	-3870	127
1202	S379	-3885	257
1203	S380	-3900	127
1204	S381	-3915	257
1205	S382	-3930	127
1206	S383	-3945	257
1207	S384	-3960	127
1208	S385	-3975	257
1209	S386	-3990	127
1210	S387	-4005	257
1211	S388	-4020	127
1212	S389	-4035	257
1213	S390	-4050	127
1214	S391	-4065	257
1215	S392	-4080	127
1216	S393	-4095	257
1217	S394	-4110	127
1218	S395	-4125	257
1219	S396	-4140	127
1220	S397	-4155	257
1221	S398	-4170	127
1222	S399	-4185	257

PAD No.	PIN Name	X	Y
1223	S400	-4200	127
1224	S401	-4215	257
1225	S402	-4230	127
1226	S403	-4245	257
1227	S404	-4260	127
1228	S405	-4275	257
1229	S406	-4290	127
1230	S407	-4305	257
1231	S408	-4320	127
1232	S409	-4335	257
1233	S410	-4350	127
1234	S411	-4365	257
1235	S412	-4380	127
1236	S413	-4395	257
1237	S414	-4410	127
1238	S415	-4425	257
1239	S416	-4440	127
1240	S417	-4455	257
1241	S418	-4470	127
1242	S419	-4485	257
1243	S420	-4500	127
1244	S421	-4515	257
1245	S422	-4530	127
1246	S423	-4545	257
1247	S424	-4560	127
1248	S425	-4575	257
1249	S426	-4590	127
1250	S427	-4605	257
1251	S428	-4620	127
1252	S429	-4635	257
1253	S430	-4650	127
1254	S431	-4665	257
1255	S432	-4680	127
1256	S433	-4695	257

PAD No.	PIN Name	X	Y
1257	S434	-4710	127
1258	S435	-4725	257
1259	S436	-4740	127
1260	S437	-4755	257
1261	S438	-4770	127
1262	S439	-4785	257
1263	S440	-4800	127
1264	S441	-4815	257
1265	S442	-4830	127
1266	S443	-4845	257
1267	S444	-4860	127
1268	S445	-4875	257
1269	S446	-4890	127
1270	S447	-4905	257
1271	S448	-4920	127
1272	S449	-4935	257
1273	S450	-4950	127
1274	S451	-4965	257
1275	S452	-4980	127
1276	S453	-4995	257
1277	S454	-5010	127
1278	S455	-5025	257
1279	S456	-5040	127
1280	S457	-5055	257
1281	S458	-5070	127
1282	S459	-5085	257
1283	S460	-5100	127
1284	S461	-5115	257
1285	S462	-5130	127
1286	S463	-5145	257
1287	S464	-5160	127
1288	S465	-5175	257
1289	S466	-5190	127
1290	S467	-5205	257

PAD No.	PIN Name	X	Y
1291	S468	-5220	127
1292	S469	-5235	257
1293	S470	-5250	127
1294	S471	-5265	257
1295	S472	-5280	127
1296	S473	-5295	257
1297	S474	-5310	127
1298	S475	-5325	257
1299	S476	-5340	127
1300	S477	-5355	257
1301	S478	-5370	127
1302	S479	-5385	257
1303	S480	-5400	127
1304	DUMMY	-5700	127
1305	DUMMY	-5880	127
1306	DUMMY	-6090	127
1307	G479	-6315	257
1308	G477	-6330	127
1309	G475	-6345	257
1310	G473	-6360	127
1311	G471	-6375	257
1312	G469	-6390	127
1313	G467	-6405	257
1314	G465	-6420	127
1315	G463	-6435	257
1316	G461	-6450	127
1317	G459	-6465	257
1318	G457	-6480	127
1319	G455	-6495	257
1320	G453	-6510	127
1321	G451	-6525	257
1322	G449	-6540	127
1323	G447	-6555	257
1324	G445	-6570	127

PAD No.	PIN Name	X	Y
1325	G443	-6585	257
1326	G441	-6600	127
1327	G439	-6615	257
1328	G437	-6630	127
1329	G435	-6645	257
1330	G433	-6660	127
1331	G431	-6675	257
1332	G429	-6690	127
1333	G427	-6705	257
1334	G425	-6720	127
1335	G423	-6735	257
1336	G421	-6750	127
1337	G419	-6765	257
1338	G417	-6780	127
1339	G415	-6795	257
1340	G413	-6810	127
1341	G411	-6825	257
1342	G409	-6840	127
1343	G407	-6855	257
1344	G405	-6870	127
1345	G403	-6885	257
1346	G401	-6900	127
1347	G399	-6915	257
1348	G397	-6930	127
1349	G395	-6945	257
1350	G393	-6960	127
1351	G391	-6975	257
1352	G389	-6990	127
1353	G387	-7005	257
1354	G385	-7020	127
1355	G383	-7035	257
1356	G381	-7050	127
1357	G379	-7065	257
1358	G377	-7080	127

PAD No.	PIN Name	X	Y
1359	G375	-7095	257
1360	G373	-7110	127
1361	G371	-7125	257
1362	G369	-7140	127
1363	G367	-7155	257
1364	G365	-7170	127
1365	G363	-7185	257
1366	G361	-7200	127
1367	G359	-7215	257
1368	G357	-7230	127
1369	G355	-7245	257
1370	G353	-7260	127
1371	G351	-7275	257
1372	G349	-7290	127
1373	G347	-7305	257
1374	G345	-7320	127
1375	G343	-7335	257
1376	G341	-7350	127
1377	G339	-7365	257
1378	G337	-7380	127
1379	G335	-7395	257
1380	G333	-7410	127
1381	G331	-7425	257
1382	G329	-7440	127
1383	G327	-7455	257
1384	G325	-7470	127
1385	G323	-7485	257
1386	G321	-7500	127
1387	G319	-7515	257
1388	G317	-7530	127
1389	G315	-7545	257
1390	G313	-7560	127
1391	G311	-7575	257
1392	G309	-7590	127

PAD No.	PIN Name	X	Y
1393	G307	-7605	257
1394	G305	-7620	127
1395	G303	-7635	257
1396	G301	-7650	127
1397	G299	-7665	257
1398	G297	-7680	127
1399	G295	-7695	257
1400	G293	-7710	127
1401	G291	-7725	257
1402	G289	-7740	127
1403	G287	-7755	257
1404	G285	-7770	127
1405	G283	-7785	257
1406	G281	-7800	127
1407	G279	-7815	257
1408	G277	-7830	127
1409	G275	-7845	257
1410	G273	-7860	127
1411	G271	-7875	257
1412	G269	-7890	127
1413	G267	-7905	257
1414	G265	-7920	127
1415	G263	-7935	257
1416	G261	-7950	127
1417	G259	-7965	257
1418	G257	-7980	127
1419	G255	-7995	257
1420	G253	-8010	127
1421	G251	-8025	257
1422	G249	-8040	127
1423	G247	-8055	257
1424	G245	-8070	127
1425	G243	-8085	257
1426	G241	-8100	127

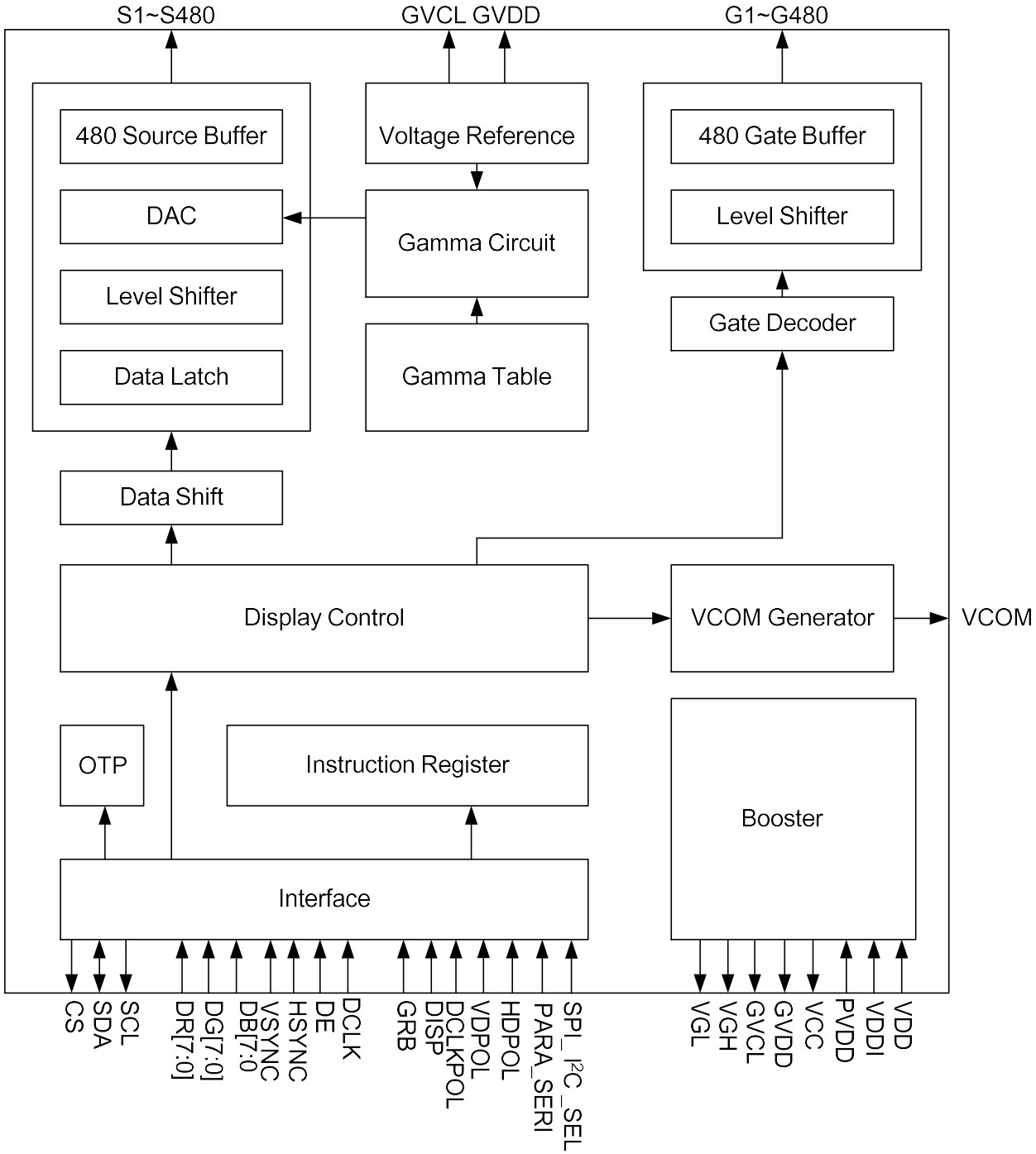
PAD No.	PIN Name	X	Y
1427	G239	-8115	257
1428	G237	-8130	127
1429	G235	-8145	257
1430	G233	-8160	127
1431	G231	-8175	257
1432	G229	-8190	127
1433	G227	-8205	257
1434	G225	-8220	127
1435	G223	-8235	257
1436	G221	-8250	127
1437	G219	-8265	257
1438	G217	-8280	127
1439	G215	-8295	257
1440	G213	-8310	127
1441	G211	-8325	257
1442	G209	-8340	127
1443	G207	-8355	257
1444	G205	-8370	127
1445	G203	-8385	257
1446	G201	-8400	127
1447	G199	-8415	257
1448	G197	-8430	127
1449	G195	-8445	257
1450	G193	-8460	127
1451	G191	-8475	257
1452	G189	-8490	127
1453	G187	-8505	257
1454	G185	-8520	127
1455	G183	-8535	257
1456	G181	-8550	127
1457	G179	-8565	257
1458	G177	-8580	127
1459	G175	-8595	257
1460	G173	-8610	127

PAD No.	PIN Name	X	Y
1461	G171	-8625	257
1462	G169	-8640	127
1463	G167	-8655	257
1464	G165	-8670	127
1465	G163	-8685	257
1466	G161	-8700	127
1467	G159	-8715	257
1468	G157	-8730	127
1469	G155	-8745	257
1470	G153	-8760	127
1471	G151	-8775	257
1472	G149	-8790	127
1473	G147	-8805	257
1474	G145	-8820	127
1475	G143	-8835	257
1476	G141	-8850	127
1477	G139	-8865	257
1478	G137	-8880	127
1479	G135	-8895	257
1480	G133	-8910	127
1481	G131	-8925	257
1482	G129	-8940	127
1483	G127	-8955	257
1484	G125	-8970	127
1485	G123	-8985	257
1486	G121	-9000	127
1487	G119	-9015	257
1488	G117	-9030	127
1489	G115	-9045	257
1490	G113	-9060	127
1491	G111	-9075	257
1492	G109	-9090	127
1493	G107	-9105	257
1494	G105	-9120	127

PAD No.	PIN Name	X	Y
1495	G103	-9135	257
1496	G101	-9150	127
1497	G99	-9165	257
1498	G97	-9180	127
1499	G95	-9195	257
1500	G93	-9210	127
1501	G91	-9225	257
1502	G89	-9240	127
1503	G87	-9255	257
1504	G85	-9270	127
1505	G83	-9285	257
1506	G81	-9300	127
1507	G79	-9315	257
1508	G77	-9330	127
1509	G75	-9345	257
1510	G73	-9360	127
1511	G71	-9375	257
1512	G69	-9390	127
1513	G67	-9405	257
1514	G65	-9420	127
1515	G63	-9435	257
1516	G61	-9450	127
1517	G59	-9465	257
1518	G57	-9480	127
1519	G55	-9495	257
1520	G53	-9510	127
1521	G51	-9525	257
1522	G49	-9540	127
1523	G47	-9555	257
1524	G45	-9570	127
1525	G43	-9585	257
1526	G41	-9600	127
1527	G39	-9615	257
1528	G37	-9630	127

PAD No.	PIN Name	X	Y
1529	G35	-9645	257
1530	G33	-9660	127
1531	G31	-9675	257
1532	G29	-9690	127
1533	G27	-9705	257
1534	G25	-9720	127
1535	G23	-9735	257
1536	G21	-9750	127
1537	G19	-9765	257
1538	G17	-9780	127
1539	G15	-9795	257
1540	G13	-9810	127
1541	G11	-9825	257
1542	G9	-9840	127
1543	G7	-9855	257
1544	G5	-9870	127
1545	G3	-9885	257
1546	G1	-9900	127
1547	DUMMY	-9930	257
1548	DUMMY	-9945	127

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 Pin Function

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="3">3-Wire SPI / I²C Interface Pins</td></tr>
<tr><td>SPI_ I²C _SEL</td><td>I</td><td>3-wire SPI and I²C interface control.
<table>
<tr><th>SPI_ I²C _SEL</th><th>Function Description</th></tr>
<tr><td>L</td><td>I²C interface</td></tr>
<tr><td>H</td><td>3-wire SPI interface</td></tr>
</table></td></tr>
<tr><td>CS</td><td>I</td><td>Serial communication chip selection.
CS is not used in I²C interface and should be connected to “H”.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Serial communication data input and output.</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial communication clock input.</td></tr>
<tr><td colspan="3">Control Pins</td></tr>
<tr><td>PARA_SERI</td><td>I</td><td>Set parallel or serial RGB interface.
<table>
<tr><th>PARA_SERI</th><th>Function Description</th></tr>
<tr><td>L</td><td>Serial 8-bit RGB interface and input through DG[7:0]</td></tr>
<tr><td>H</td><td>Parallel 24-bit RGB interface and input through DR[7:0], DB[7:0], DG[7:0]</td></tr>
</table></td></tr>
<tr><td>HDIR</td><td>I</td><td>Horizontal scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>HDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From right to left</td></tr>
<tr><td>H</td><td>From left to right</td></tr>
</table></td></tr>
<tr><td>VDIR</td><td>I</td><td>Vertical scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>VDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From down to up.</td></tr>
<tr><td>H</td><td>From up to down.</td></tr>
</table></td></tr>
<tr><td>VDPOL</td><td>I</td><td>VDPOL sets VSYNC polarity in RGB interface.
<table>
<tr><th>VDPOL</th><th>Function Description</th></tr>
<tr><td>L</td><td>VSYNC polarity: positive</td></tr>
<tr><td>H</td><td>VSYNC polarity: negative</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>HDPOL</td><td>I</td><td>HDPOL sets HSYNC polarity in RGB interface.<table><tr><th>HDPOL</th><th>Function Description</th></tr><tr><td>L</td><td>HSYNC polarity: positive</td></tr><tr><td>H</td><td>HSYNC polarity: negative</td></tr></table></td></tr>
<tr><td>DCLKPOL</td><td>I</td><td>DCLKPOL sets DCLK polarity in RGB interface.<table><tr><th>DCLKPOL</th><th>Function Description</th></tr><tr><td>L</td><td>DCLK polarity: positive</td></tr><tr><td>H</td><td>DCLK polarity: negative</td></tr></table></td></tr>
<tr><td>GRB</td><td>I</td><td>Global reset pin. When GRB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>DISP</td><td>I</td><td>DISP sets the display mode.<table><tr><th>DISP</th><th>Function Description</th></tr><tr><td>L</td><td>Standby mode</td></tr><tr><td>H</td><td>Normal display mode</td></tr></table></td></tr>
<tr><td>AUTODL</td><td>I</td><td>Auto-refresh function control pin.<table><tr><th>AUTODL</th><th>Function Description</th></tr><tr><td>L</td><td>Disable auto-refresh function</td></tr><tr><td>H</td><td>Enable auto-refresh function</td></tr></table></td></tr>
<tr><td>ENPROG</td><td>I</td><td>OTP program control pin.<table><tr><th>ENPROG</th><th>Function Description</th></tr><tr><td>L</td><td>Disable OTP program function</td></tr><tr><td>H</td><td>Enable OTP program function</td></tr></table></td></tr>
<tr><td>BIST_EN</td><td>I</td><td>BIST function control pin.<table><tr><th>BIST_EN</th><th>Function Description</th></tr><tr><td>L</td><td>Disable BIST function</td></tr><tr><td>H</td><td>Enable BIST function</td></tr></table></td></tr>
<tr><td colspan="3">Input Interface Pins</td></tr>
<tr><td>DR[7:0]
DG[7:0]
DB[7:0]</td><td>I</td><td>RGB interface data input pins.<table><tr><th colspan="2">Function Description</th></tr><tr><td>DR[7:0]</td><td>8-bit data bus display red data.DR[7:0] are not used in 8-bit RGB interface and should be connected to “L” .</td></tr><tr><td>DG[7:0]</td><td>8-bit data bus display green data. DG[7:0] are used in 8-bit RGB interface.</td></tr><tr><td>DB[7:0]</td><td>8-bit data bus display blue data. DB[7:0] are not used in 8-bit RGB interface and should be connected to “L”.</td></tr></table></td></tr>
<tr><td>DCLK</td><td>I</td><td>Pixel clock input pin.</td></tr>
</table>

Name	Type	Description
HSYNC	I	Horizontal sync signal, default is negative polarity.
VSYNC	I	Vertical sync signal, default is negative polarity.
DE	I	Data input enable. Display access is enabled when DE is “H”.
Source / Gate Driver Pins		
S1~S480	O	Source driver output signals.
G1~G480	O	Gate driver output signals.
VCOM Generator Pin		
VCOM	O	Power supply for the TFT-LCD common electrode.
Power Supply Pins		
VDD	P	Power supply for analog circuit.
VDDI	P	Power supply for digital I/O pins.
PVDD	P	Power supply for charge pump circuit.
DGND	P	Ground pin for digital circuit.
AGND	P	Ground pin for analog circuit.
PGND	P	Ground pin for charge pump circuit.
Power Circuit Pins		
AVDD	C	DC/DC converter for positive source OP-AMP .
AVCL	C	DC/DC converter for negative source OP-AMP .
VGH	C	Positive power supply for gate .
VGL	C	Negative power supply for gate .
GVDD	PO	Positive voltage output of grayscale.
GVCL	PO	Negative voltage output of grayscale.
Test Pins		
VGSP	T	Monitor pin of internal VCOM offset, please leave it open.
VCC	T	Reserved for testing only, please leave it open.
VCCA	T	Reserved for testing only, please leave it open.
AVDD1	T	Reserved for testing only, please leave it open.
AVCL1	T	Reserved for testing only, please leave it open.
VPP	T	Reserved for testing only, please leave it open.
TEST_IN[14:0]	T	Reserved for testing only, please leave these pins open.
TESTI[2:1]	T	These pins must be connected to “L”.
TESTOUT[7:0]	T	Reserved for testing only, please leave these pins open.
TESTO TESTO1	T	Reserved for testing only, please leave these pins open.

Note: 1. I: input, O: output, I/O: input/output, P: power input, PO: power out, D: dummy, T: test pin, C: capacitor pin

2. If hardware pin is not used, please fix to “H” by VDDI or “L” by DGND

6.2 Hardware Pin and Software Register Options

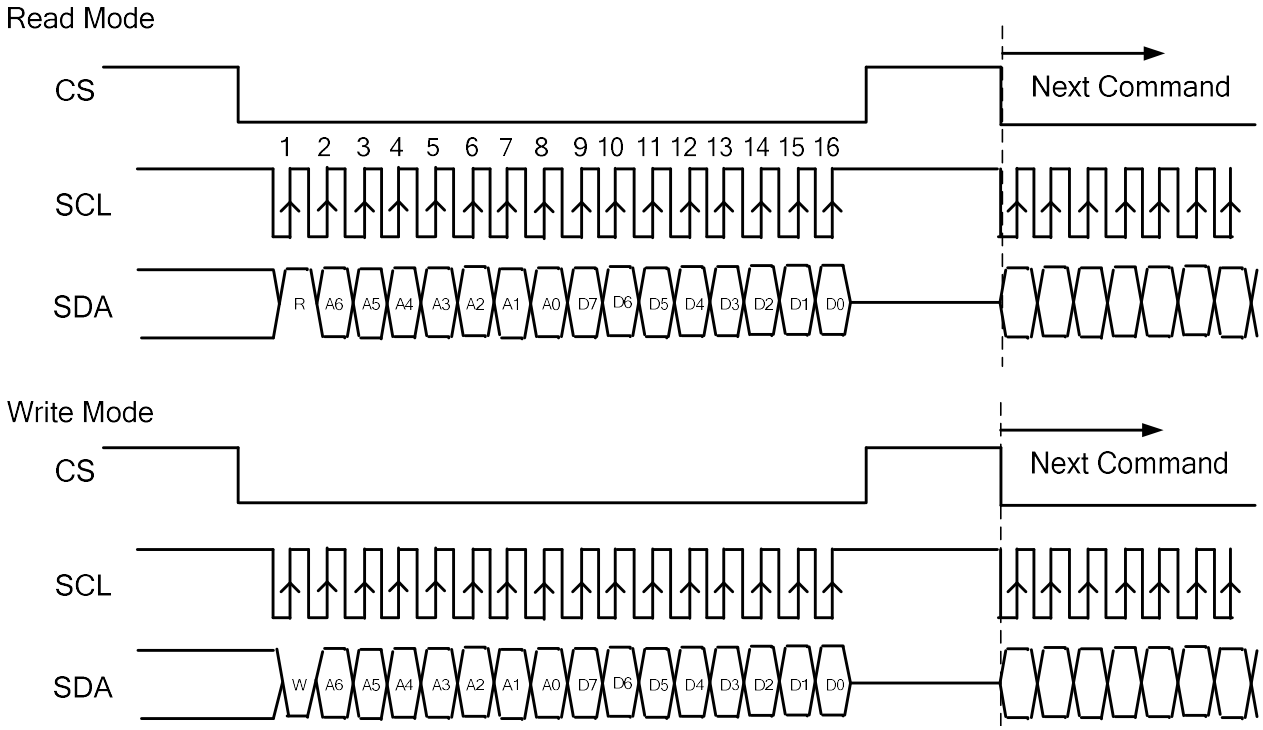
The following setting can be selected by hardware and software registers. If hardware pin and software register are set at the same time, the judgment criteria are as follows:

Hardware Pin Setting	Register Setting	Judgment Result
DISP	10h_bit[0]	DISP (Hardware Pin)
VDIR	19h_bit[6]	19h_bit[6] (Register)
HDIR	19h_bit[5]	19h_bit 5] (Register)
VDPOL	19h_bit[3]	19h_bit[3] (Register)
HDPOL	19h_bit[2]	19h_bit[2] (Register)
DCLKPOL	19h_bit[0]	19h_bit[0] (Register)
AUTODL	1Bh_bit[2]	1Bh_bit[2] (Register)

7. COMMUNICATION INTERFACE

7.1 3-wire Serial Interface

R/W: Read/Write mode control bit.
R/W=1: Read mode
R/W=0: Write mode



a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

e. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before then rising edge of CS pulse are valid data.

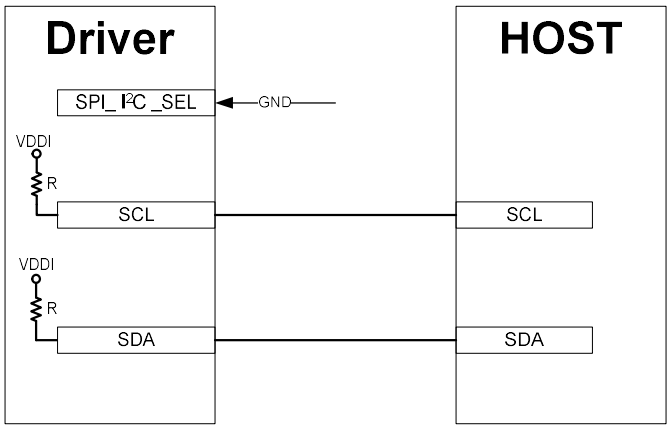
f. Serial block operates with the SCL clock

g. Serial data can be accepted in the power save mode.

h. After power on reset or GRB reset, it is required 100ms delay to begin SPI communication.

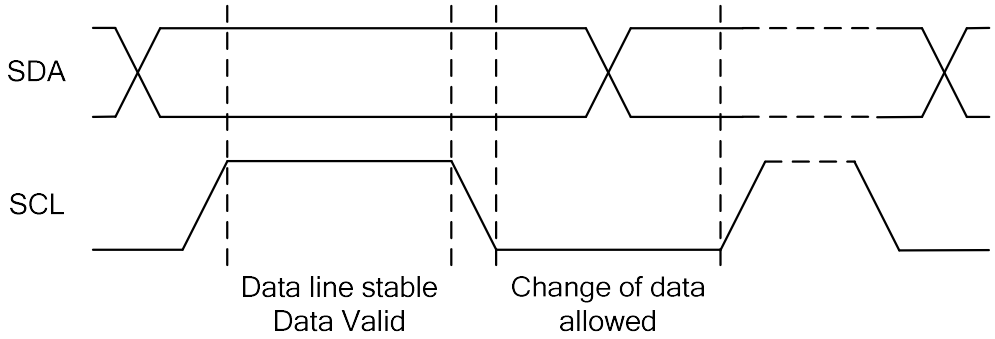
7.2 I²C Interface

The I²C Interface is bi-directional two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines have built-in pull up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.



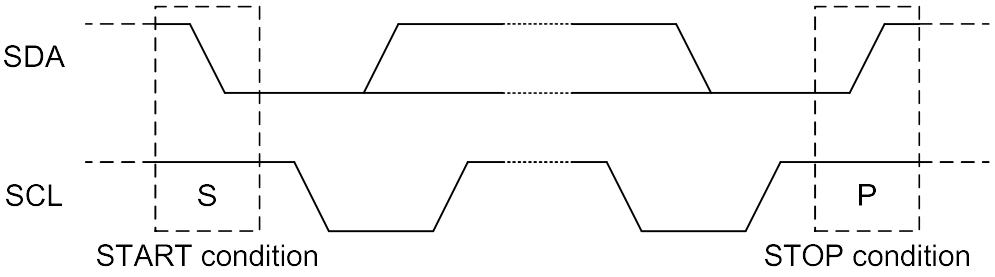
7.2.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated as follows.

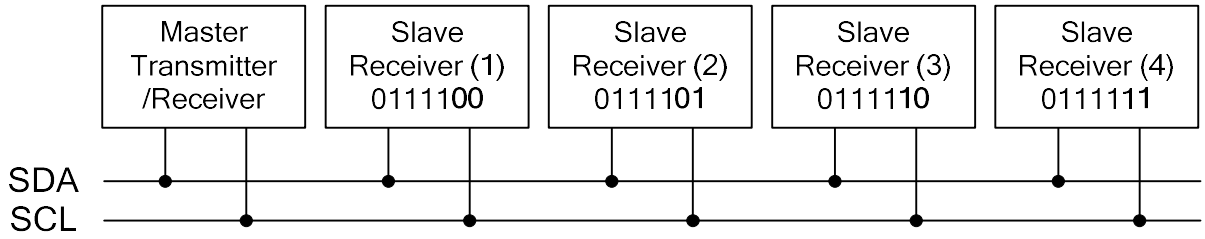


7.2.2 START and STOP Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated as follows.



7.2.3 System Configuration



The system configuration is illustrated above and some word-definitions are explained below:

a. Transmitter: the device which sends the data to the bus.

b. Receiver: the device which receives the data from the bus.

c. Master: the device which initiates a transfer generates clock signals and terminates a transfer.

d. Slave: the device which is addressed by a master.

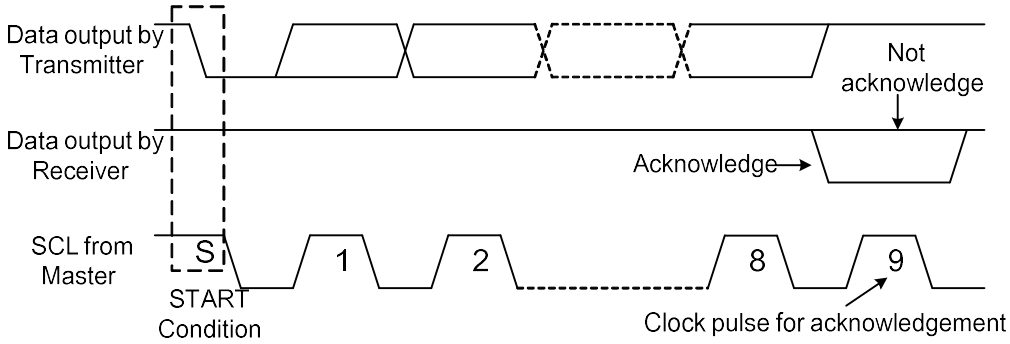
e. Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

f. Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.

g. Synchronization: procedure to synchronize the clock signals of two or more devices.

7.2.4 Acknowledgment

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated as follows.

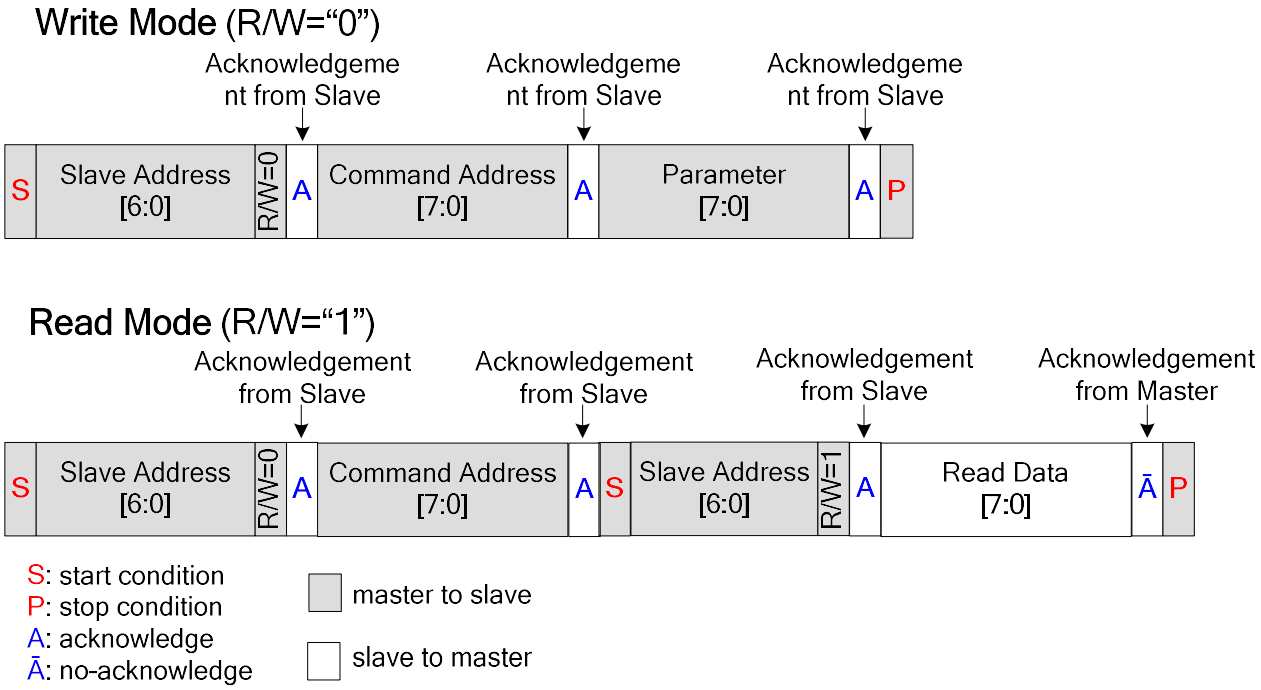


7.2.5 I²C Interface Protocol

The driver supports command/data write to addressed slaves on the bus. Before any data is transmitted on the I²C Interface, the device which should respond is addressed first. The default slave address is 0111100b and the three times I²C address could be OTP programing.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master. The register write/ read transference sequence are described as follows.



7.3 RGB Interface

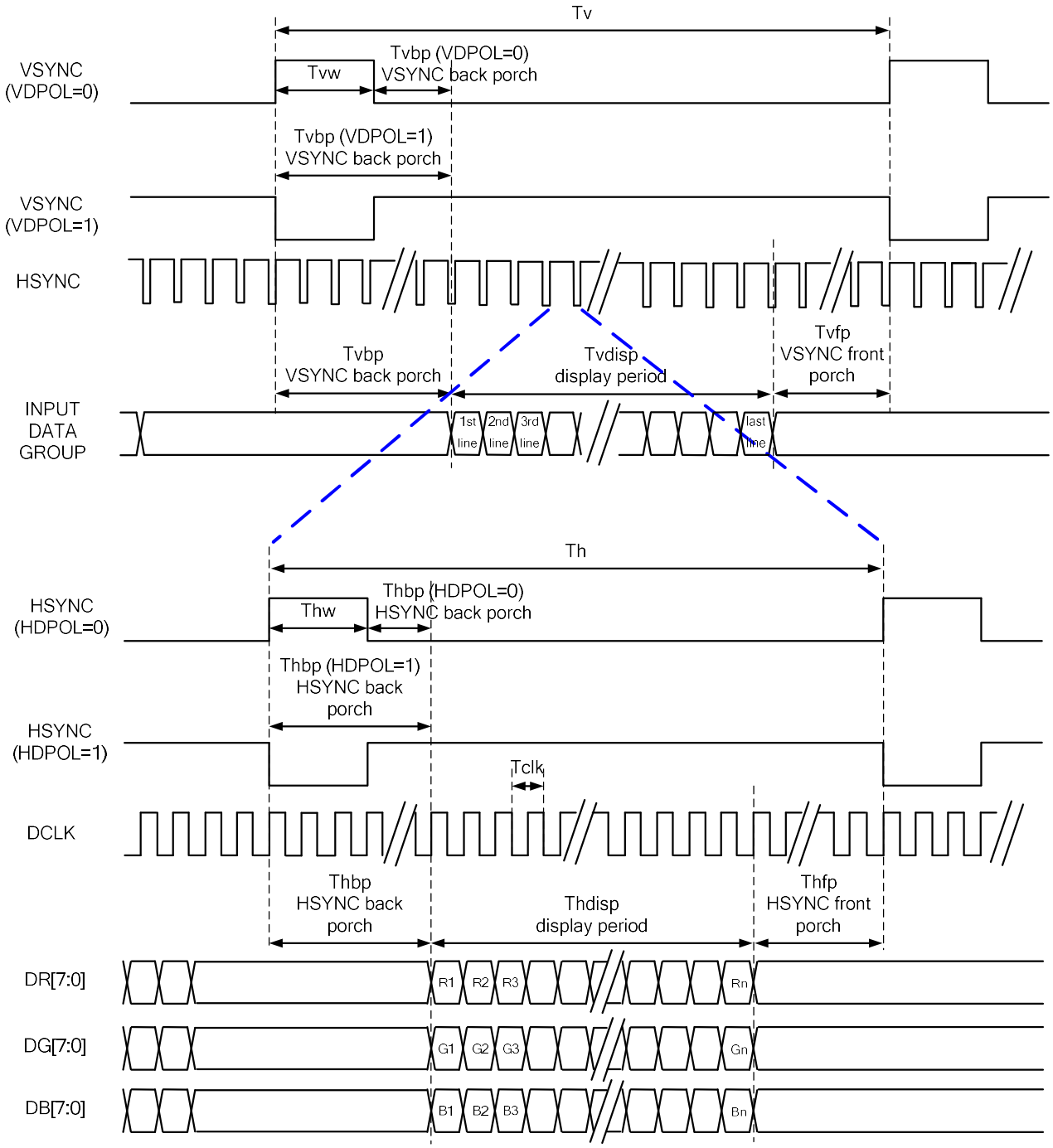
7.3.1 Pin Assignment for RGB Interface

Pin		Parallel RGB			Serial RGB		
		888	666	565	888	666	565
VSYNC	SYNC Mode	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	DE Mode	x	x	x	x	x	x
HSYNC	SYNC Mode	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	DE Mode	x	x	x	x	x	x
DE	SYNC Mode	x	x	x	x	x	x
	DE Mode	DE	DE	DE	DE	DE	DE
CLK		CLK	CLK	CLK	CLK	CLK	CLK
DR0		R0	x	x	x	x	x
DR1		R1	x	x	x	x	x
DR2		R2	R0	x	x	x	x
DR3		R3	R1	R0	x	x	x
DR4		R4	R2	R1	x	x	x
DR5		R5	R3	R2	x	x	x
DR6		R6	R4	R3	x	x	x
DR7		R7	R5	R4	x	x	x
DG0		G0	x	x	D0	x	x
DG1		G1	x	x	D1	x	x
DG2		G2	G0	G0	D2	D0	D0
DG3		G3	G1	G1	D3	D1	D1
DG4		G4	G2	G2	D4	D2	D2
DG5		G5	G3	G3	D5	D3	D3
DG6		G6	G4	G4	D6	D4	D4
DG7		G7	G5	G5	D7	D5	D5
DB0		B0	x	x	x	x	x
DB1		B1	x	x	x	x	x
DB2		B2	B0	x	x	x	x
DB3		B3	B1	B0	x	x	x
DB4		B4	B2	B1	x	x	x
DB5		B5	B3	B2	x	x	x
DB6		B6	B4	B3	x	x	x
DB7		B7	B5	B4	x	x	x

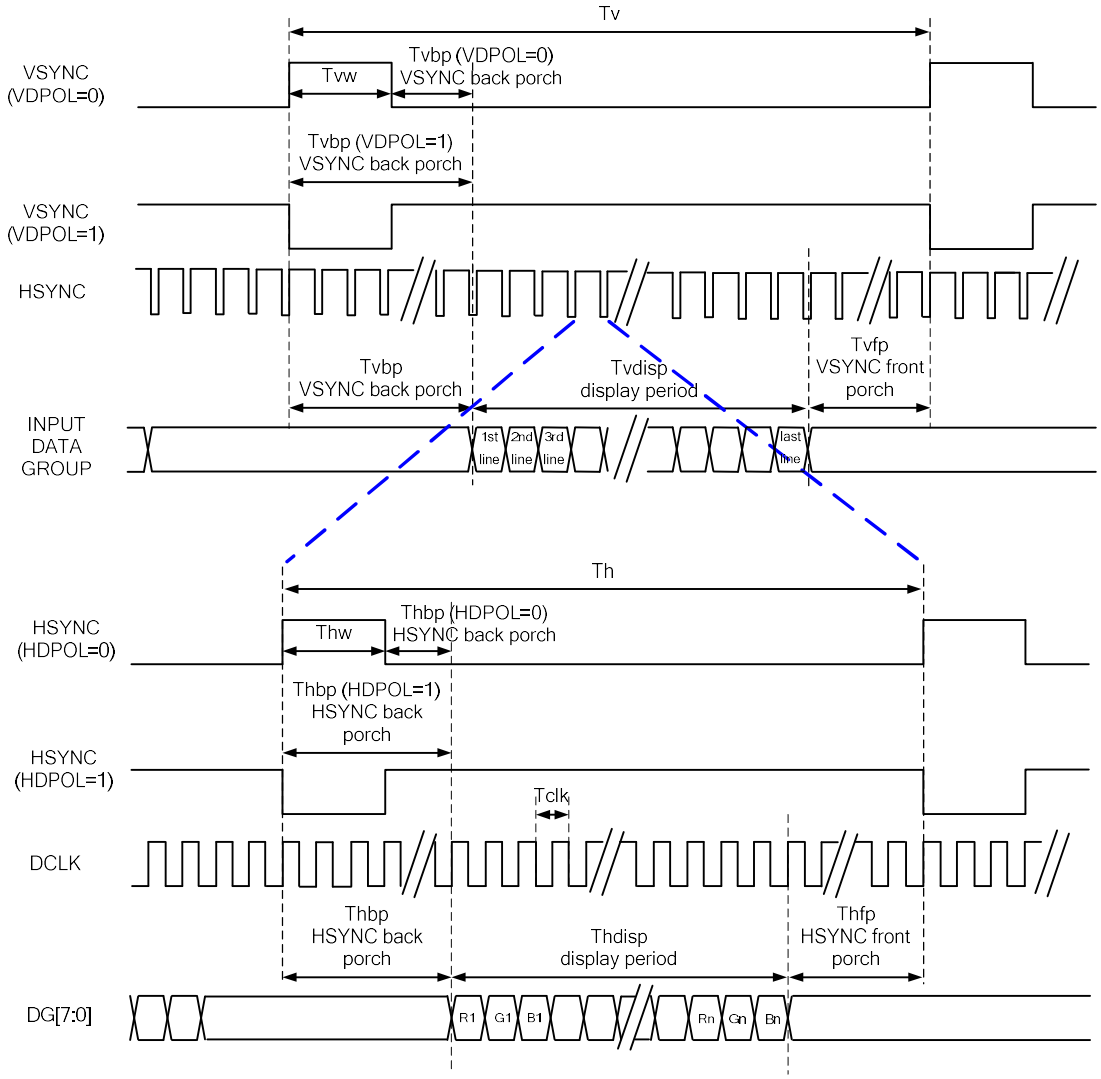
RGB Mode Selection Table	DCLK	HSYNC	VSYNC	DE
SYNC – DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input

Note: "Input" means these signals are driven by host side

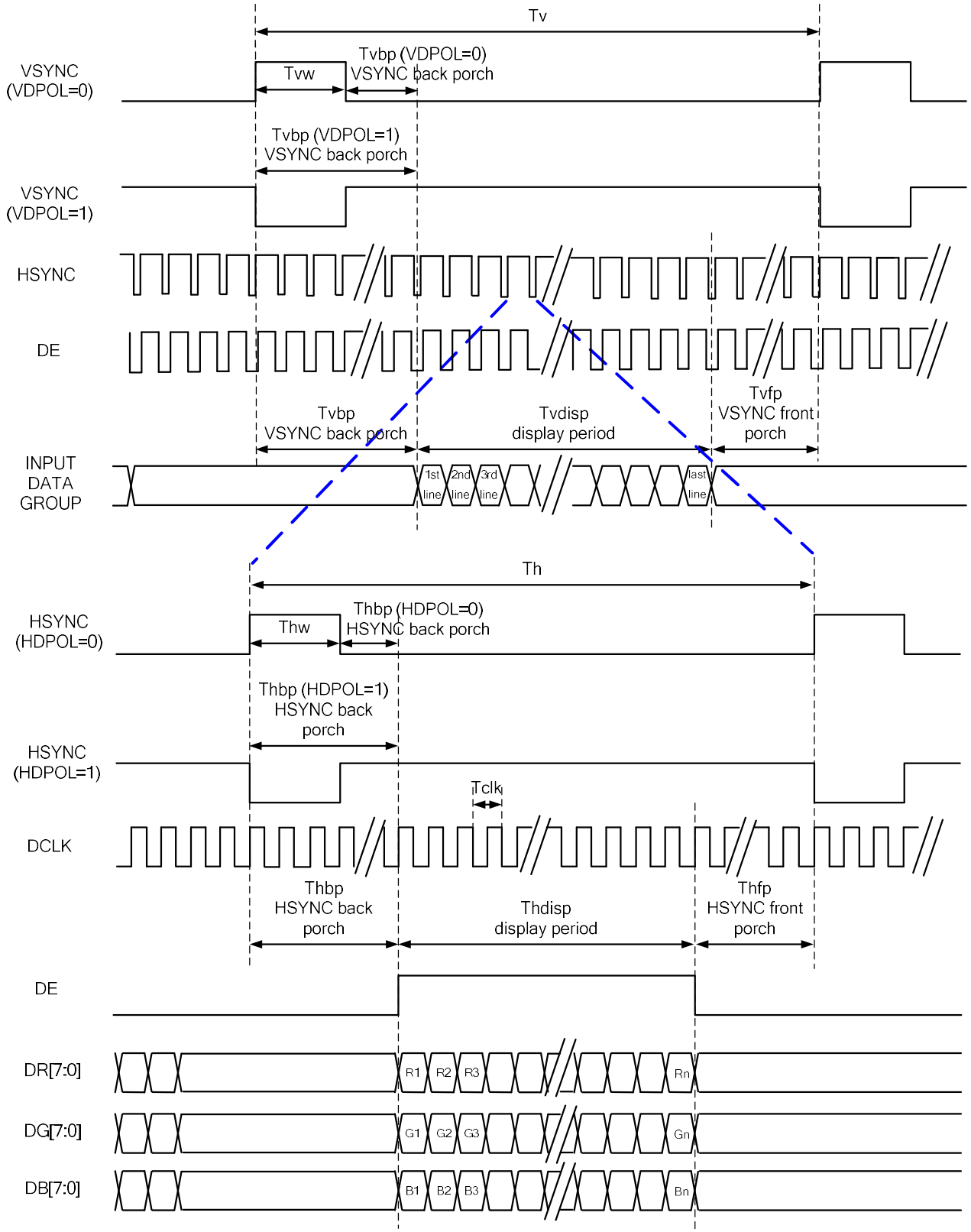
7.3.2 Parallel RGB SYNC Mode



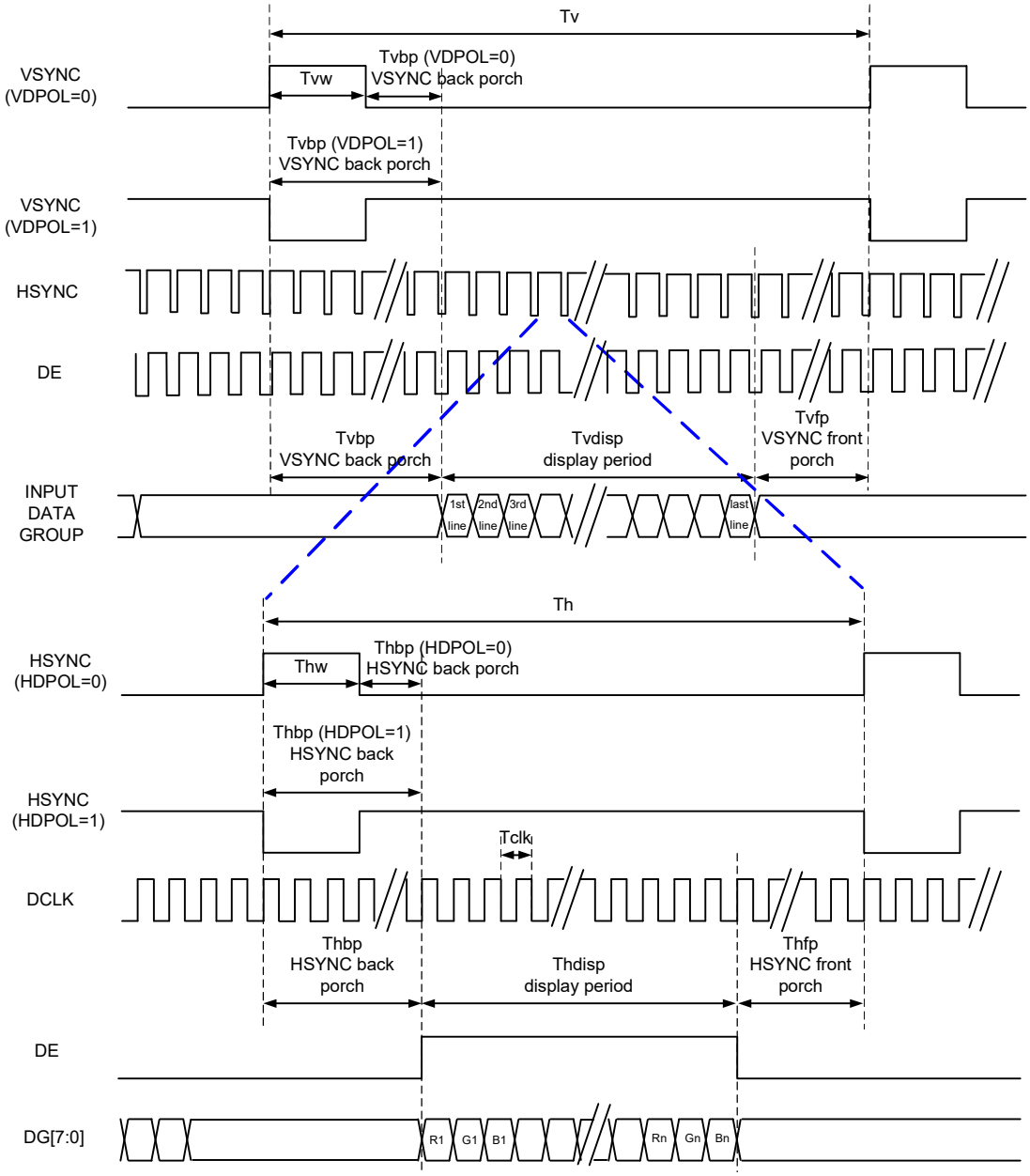
7.3.3 Serial RGB SYNC Mode



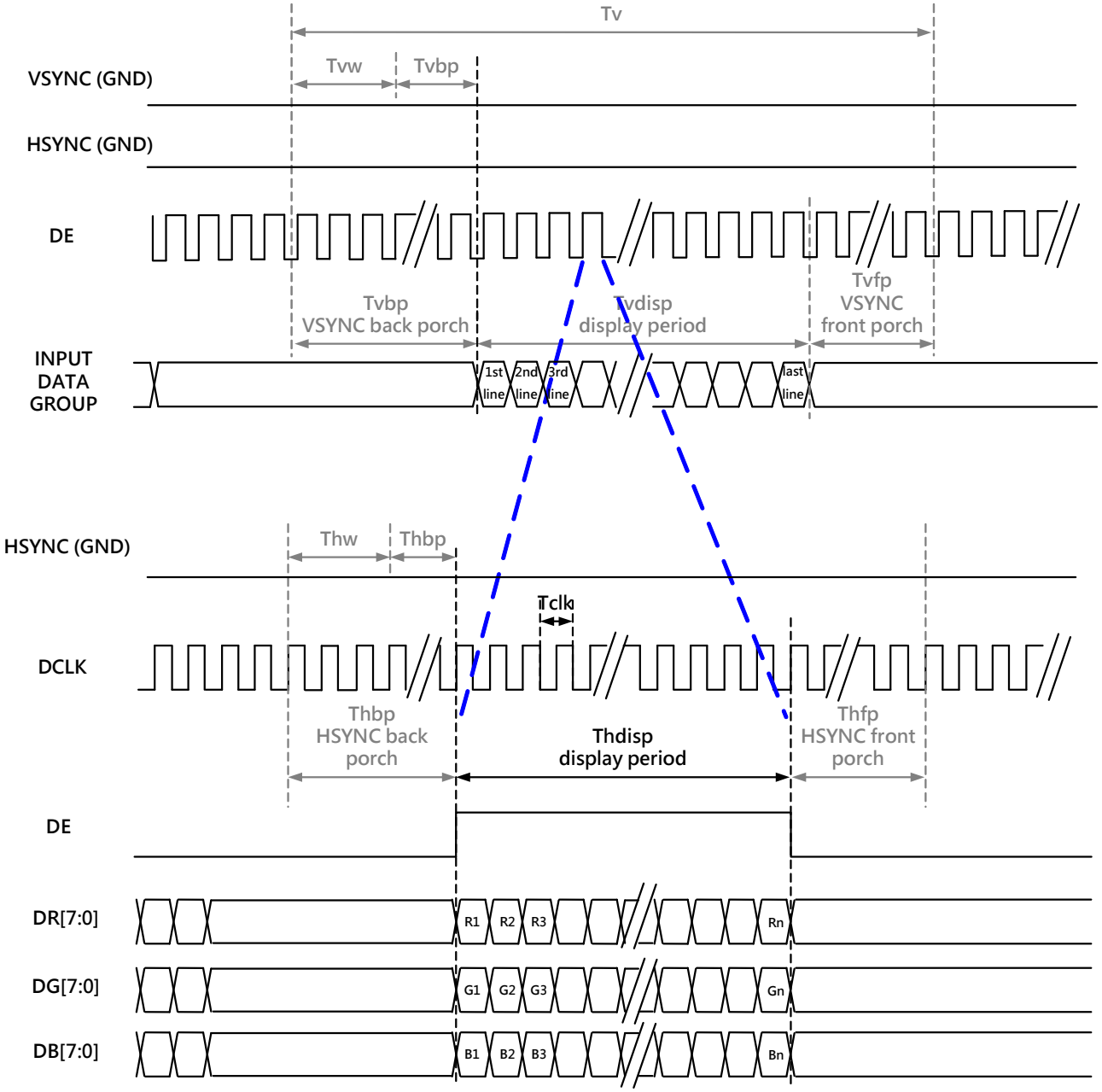
7.3.4 Parallel RGB SYNC-DE Mode



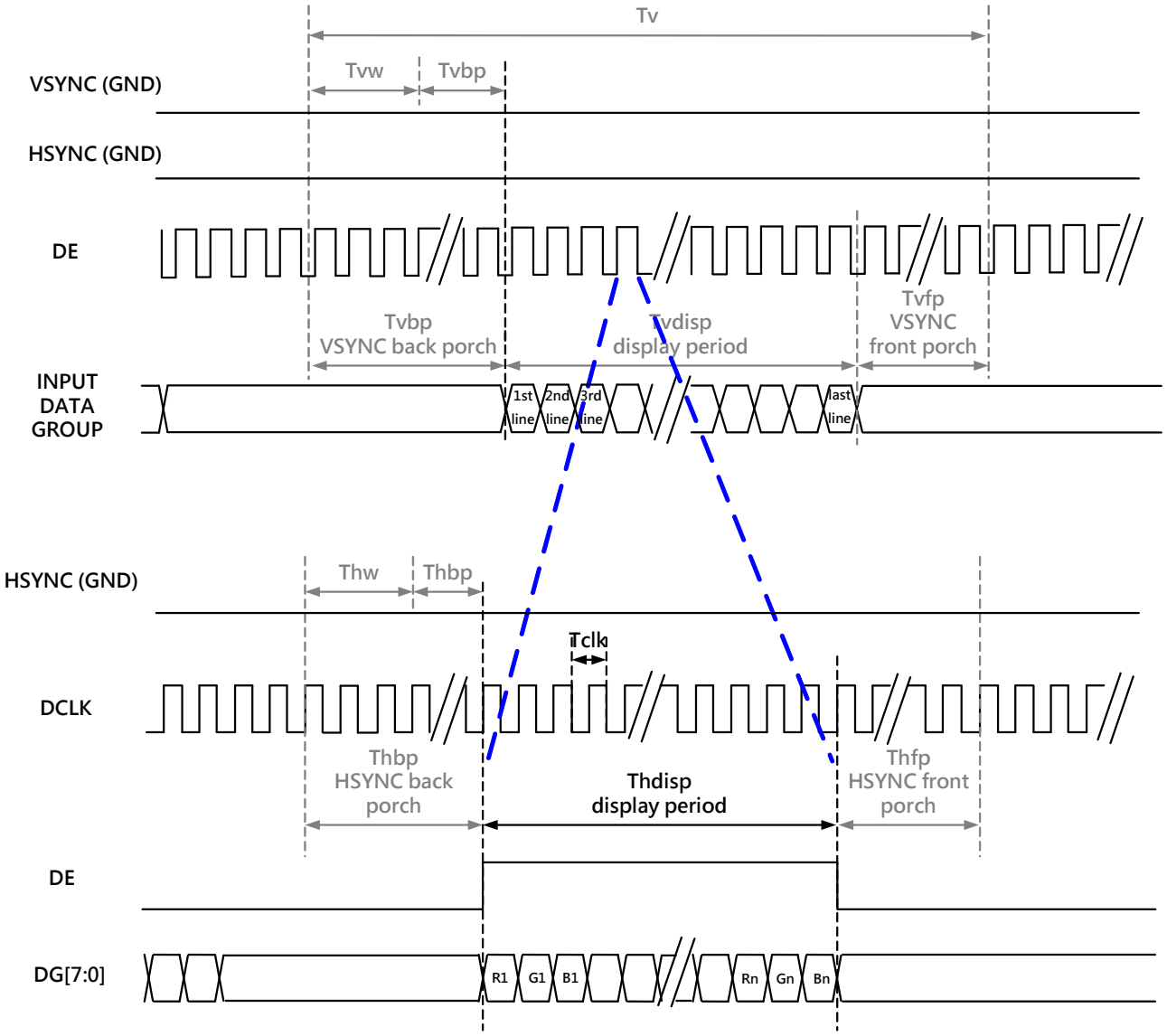
7.3.5 Serial RGB SYNC-DE Mode



7.3.6 Parallel RGB DE Mode



7.3.7 Serial RGB DE Mode



7.3.8 Parallel RGB Input Timing Table

Parallel 24-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Parallel 24-bit RGB Input Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
DCLK Frequency		Fclk	5	6	8	MHz	
DCLK Period		Tclk	125	167	200	ns	
HSYNC	Period Time	Th	325	371	438	DCLK	
	Display Period	Thdisp	-	320	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	SYNC mode back porch control by H_BLANKING[7:0] setting Thbp= H_BLANKING[7:0]
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	244	260	289	HSYNC	
	Display Period	Tvdisp	-	240	-	HSYNC	
	Back Porch	Tvbp	2	12	12	HSYNC	SYNC mode back porch control by V_BLANKING[7:0] setting Tvbp= V_BLANKING[7:0]
	Front Porch	Tvfp	2	8	37	HSYNC	
	Pulse Width	Tvw	2	4	12	HSYNC	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

7.3.9 Serial RGB Input Timing Table

Serial 8-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Serial 8-bit RGB Input Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	15	18	21	MHz	
DCLK Period		Tclk	47	55	66	ns	
HSYNC	Period Time	Th	965	1011	1078	DCLK	
	Display Period	Thdisp	-	960	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	SYNC mode back porch control by H_BLANKING[7:0] setting Thbp= H_BLANKING[7:0]
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	244	260	289	HSYNC	
	Display Period	Tvdisp	-	240	-	HSYNC	
	Back Porch	Tvbp	2	12	12	HSYNC	SYNC mode back porch control by V_BLANKING[7:0] setting Tvbp= V_BLANKING[7:0]
	Front Porch	Tvfp	2	8	37	HSYNC	
	Pulse Width	Tvw	2	4	12	HSYNC	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

8. REGISTER LIST

8.1 Register Summary

COMMAND TABLE 1									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	0	0	0	0	GRB	0	0	DISP	08h
11h	CONTRAST[7:0]								40h
12h	0	SUB_CONTRAST_R[6:0]							40h
13h	0	SUB_CONTRAST_B[6:0]							40h
14h	BRIGHTNESS[7:0]								40h
15h	0	SUB_BRIGHTNESS_R[6:0]							40h
16h	0	SUB_BRIGHTNESS_B[6:0]							40h
17h	H_BLANKING[7:0]								2Bh
18h	V_BLANKING[7:0]								0Ch
19h	MVA_TN	VDIR	HDIR	SBGR	VDPOL	HDPOL	DEPOL	DCLKPOL	--
1Bh	0	0	0	0	1	AUTODL	0	0	--
1Ch	0	0	PICSEC[1:0]		AUTOBIST	PICSEL [2:0]			38h
COMMAND TABLE 2									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	0	1	VRHP[5:0]						--
41h	0	VRHN[6:0]							--
44h	0	1	0	0	AVCLS[1:0]		AVDDS[1:0]		--
45h	0	0	0	0	VGLSEL[1:0]		VGHSEL[1:0]		--
46h	T4T[1:0]		T3T[1:0]		T2T[1:0]		T1T[1:0]		--
47h	0	0	0	0	0	SOURCE_AP[2:0]			--
49h	0	NO[2:0]			0	1	0	0	--
4Ah	0	PRGB_GWIDTH[2:0]			0	SRGB_GWIDTH[2:0]			--

Note:

1. When GRB is "Low", all registers reset to default values.

2. Symbol "–" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

GAMMA COMMAND TABLE									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	0	-	-	VRF0P[4:0]					--
21h	0	-	-	VOS0P[4:0]					--
22h	PFP0[2:0]			PKP0[4:0]					--
23h	PFP1[2:0]			PKP1[4:0]					--
24h	PFP2[2:0]			PKP2[4:0]					--
25h	PFP3[2:0]			PKP3[4:0]					--
26h	PFP4[2:0]			PKP4[4:0]					--
27h	PFP5[2:0]			PKP5[4:0]					--
28h	PFP6[2:0]			PKP6[4:0]					--
29h	0	0	0	PKP7[4:0]					--
30h	0	-	-	VRF0N[4:0]					--
31h	0	-	-	VOS0N[4:0]					--
32h	PFN0[2:0]			PKN0[4:0]					--
33h	PFN1[2:0]			PKN1[4:0]					--
34h	PFN2[2:0]			PKN2[4:0]					--
35h	PFN3[2:0]			PKN3[4:0]					--
36h	PFN4[2:0]			PKN4[4:0]					--
37h	PFN5[2:0]			PKN5[4:0]					--
38h	PFN6[2:0]			PKN6[4:0]					--
39h	0	0	0	PKN7[4:0]					--

Note:

1. When GRB is “Low”, all registers reset to default values.

2. Symbol ”-” means this value is don’t care.

2. Symbol “–” means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

OTP COMMAND TABLE									
Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	0	ID1[6:0]							--
02h	0	ID2[6:0]							--
03h	0	ID3[6:0]							--
04h	0	I^2CID[6:0]							78h
05h	0	VMF[6:0]							40h
60h	0	1	0	0	0	1	OTPEN	0	44h
65h	OTPACK[7:0]								00h
66h	0	0	0	0	0	VMF OTP TIME[2:0]			--
67h	0	0	0	0	0	CMD2 OTP TIME[2:0]			--
68h	0	0	0	0	0	GAMMA OTP TIME[2:0]			--
69h	0	0	0	0	0	ID1 OTP TIME[2:0]			--
6Ah	0	0	0	0	0	ID2 OTP TIME[2:0]			--
6Bh	0	0	0	0	0	ID3 OTP TIME[2:0]			--
6Ch	0	0	0	0	0	I^2CID OTP TIME[2:0]			--

Note:

1. When GRB is "Low", all registers reset to default values.

2. Symbol "–" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

8.2 Command Table1 Register Description

8.2.1 GRB、DISP CONTROL (10h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	W	0	0	0	0	GRB	0	0	DISP	08h

Designation	Description
GRB	Reset register setting GRB=0: reset all registers to default value GRB=1: normal operation
DISP	Standby (power saving) mode setting DISP=0: standby mode DISP=1: normal mode

8.2.2 CONTRAST (11h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
11h	W	CONTRAST[7:0]								40h

Designation	Description
CONTRAST[7:0]	Set RGB contrast level, the range of gain is 0~3.984 CONTRAST=00h: contrast gain=0 CONTRAST=40h: contrast gain=1 CONTRAST=FFh: contrast gain=3.984

8.2.3 SUB_CONTRAST_R (12h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	W	0	SUB_CONTRAST_R[6:0]							40h

Designation	Description
SUB_CONTRAST_R[6:0]	Set red color sub-contrast level, the range of gain is 0.75~1.246 SUB_CONTRAST_R=00h: contrast gain=0.75 SUB_CONTRAST_R=40h: contrast gain=1 SUB_CONTRAST_R=7Fh: contrast gain=1.246

8.2.4 SUB_CONTRAST_B (13h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
13h	W	0	SUB_CONTRAST_B[6:0]							40h

Designation	Description
SUB_CONTRAST_B[6:0]	Set blue color sub-contrast level, the range of gain is 0.75~1.246 SUB_CONTRAST_B=00h: contrast gain=0.75 SUB_CONTRAST_B=40h: contrast gain=1 SUB_CONTRAST_B=7Fh: contrast gain=1.246

8.2.5 BRIGHTNESS (14h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	W	BRIGHTNESS[7:0]								40h

Designation	Description
BRIGHTNESS[7:0]	Set RGB brightness level, the range of brightness is -64~+191 BRIGHTNESS=00h: -64 BRIGHTNESS=40h: 0 BRIGHTNESS=FFh: +191

8.2.6 SUB-BRIGHTNESS_R (15h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
15h	W	0	SUB_BRIGHTNESS_R[6:0]							40h

Designation	Description
SUB_BRIGHTNESS_R [6:0]	Set red color sub-brightness level, the range of brightness is -64~+63 SUB_BRIGHTNESS_R=00h: -64 SUB_BRIGHTNESS_R=40h: 0 SUB_BRIGHTNESS_R=7Fh: +63

8.2.7 SUB-BRIGHTNESS_B (16h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	W	0	SUB_BRIGHTNESS_B[6:0]							40h

Designation	Description
SUB_BRIGHTNESS_B [6:0]	Set blue color sub-brightness level, the range of brightness is -64~+63 SUB_BRIGHTNESS_B=00h: -64 SUB_BRIGHTNESS_B=40h: 0 SUB_BRIGHTNESS_B=7Fh: +63

8.2.8 H_BLANKING (17h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
17h	W	H_BLANKING[7:0]								2Bh

Designation	Description
H_BLANKING[7:0]	The HSYNC back porch setting of RGB interface

8.2.9 V_BLANKING (18h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	W	V_BLANKING[7:0]								0Ch

Designation	Description
V_BLANKING[7:0]	The VSYNC back porch setting of RGB interface

8.2.10 DISPLAY MODE SETTING (19h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
19h	W	MVA_TN	VDIR	HDIR	SBGR	VDPOL	HDPOL	DEPOL	DCLKPOL	--

Designation	Description
MVA_TN	MVA_TN=0: TN mode for panel display. MVA_TN=1: VA mode for panel display.
VDIR	Vertical scan direction setting VDIR= 0: from bottom to top, L(n)(first line) → L(n-1) →…→ L2 → L1(last line) VDIR= 1: from top to bottom, L1(first line) → L2 →…→ L(n-1) → L(n)(last line)
HDIR	Horizontal scan direction setting HDIR= 0: from right to left, Y(n)(first data) → Y(n-1) →…→ Y2 → Y1(last data) HDIR= 1: from left to right, Y1(first data) → Y2 →…→ Y(n-1) → Y(n)(last data)
SBGR	Data of red and blue exchange SBGR= 0: normal, DR[7:0]→DR[7:0] and DB[7:0]→DB[7:0] SBGR= 1: exchange, DR[7:0]→DB[7:0] and DB[7:0]→DR[7:0]
VDPOL	VSYNC polarity setting VDPOL= 0: positive polarity VDPOL= 1: negative polarity
HDPOL	HSYNC polarity setting HDPOL= 0: positive polarity HDPOL= 1: negative polarity
DEPOL	DE polarity setting DEPOL= 0: positive polarity DEPOL= 1: negative polarity
DCLKPOL	DCLK polarity setting DCLKPOL= 0: positive polarity DCLKPOL= 1: negative polarity

Note: The default setting of register (19h) can refer to the relevant hardware pin setting.

8.2.11 AUTO-REFRESH CONTROL (1Bh)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Bh	W	0	0	0	0	1	AUTODL	0	0	--

Designation	Description
AUTODL	Auto-refresh function control AUTODL= 0: disable auto-refresh function AUTODL= 1: enable auto-refresh function

8.2.12 BIST FUNCTION SETTING (1Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	W	0	0	PICSEC[1:0]		AUTOBIST	PICSEL[2:0]			38h

Designation	Description
PICSEC[1:0]	The time interval of test pattern in the BIST mode PICSEC[1:0] / Time(sec): 00 / 0.5; 01 / 1; 10 / 1.5; 11 / 2
AUTOBIST	Auto display pattern control in the BIST mode AUTOBIST=0: Disable auto display mode AUTOBIST=1: Enable auto display mode
PICSEL[2:0]	BIST pattern selection PICSEL [2:0] / Display Pattern: 000 / Black; 001 / White; 010 / Red; 011 / Green; 100 / Blue; 101 / Black; 110 / Black; 111 / Black

8.3 Command Table2 Register Description

8.3.1 GVDD SETTING (40h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	R/W	0	1	VRHP[5:0]						--

Designation	Description
VRHP[5:0]	GVDD level setting

VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD
000000	5.9680	010000	5.7120	100000	5.4560	110000	5.2000
000001	5.9520	010001	5.6960	100001	5.4400	110001	5.1840
000010	5.9360	010010	5.6800	100010	5.4240	110010	5.1680
000011	5.9200	010011	5.6640	100011	5.4080	110011	5.1520
000100	5.9040	010100	5.6480	100100	5.3920	110100	5.1360
000101	5.8880	010101	5.6320	100101	5.3760	110101	5.1200
000110	5.8720	010110	5.6160	100110	5.3600	110110	5.1040
000111	5.8560	010111	5.6000	100111	5.3440	110111	5.0880
001000	5.8400	011000	5.5840	101000	5.3280	111000	5.0720
001001	5.8240	011001	5.5680	101001	5.3120	111001	5.0560
001010	5.8080	011010	5.5520	101010	5.2960	111010	5.0400
001011	5.7920	011011	5.5360	101011	5.2800	111011	5.0240
001100	5.7760	011100	5.5200	101100	5.2640	111100	5.0080
001101	5.7600	011101	5.5040	101101	5.2480	111101	4.9920
001110	5.7440	011110	5.4880	101110	5.2320	111110	4.9760
001111	5.7280	011111	5.4720	101111	5.2160	111111	4.9600

8.3.2 GVCL SETTING (41h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
41h	R/W	0	VRHN[6:0]							--

Designation	Description
VRHN[6:0]	GVCL level setting

VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL
0100000	-4.4800	0111000	-4.0960	1010000	-3.7120	1101000	-3.3280
0100001	-4.4640	0111001	-4.0800	1010001	-3.6960	1101001	-3.3120
0100010	-4.448	0111010	-4.0640	1010010	-3.6800	1101010	-3.2960
0100011	-4.4320	0111011	-4.0480	1010011	-3.6640	1101011	-3.2800
0100100	-4.4160	0111100	-4.0320	1010100	-3.6480	1101100	-3.2640
0100101	-4.4000	0111101	-4.0160	1010101	-3.6320	1101101	-3.2480
0100110	-4.3840	0111110	-4.0000	1010110	-3.6160	1101110	-3.2320
0100111	-4.3680	0111111	-3.9840	1010111	-3.6000	1101111	-3.2160
0101000	-4.3520	1000000	-3.9680	1011000	-3.5840	1110000	-3.2000
0101001	-4.3360	1000001	-3.9520	1011001	-3.5680	1110001	-3.1840
0101010	-4.3200	1000010	-3.9360	1011010	-3.5520	1110010	-3.1680
0101011	-4.3040	1000011	-3.9200	1011011	-3.5360	1110011	-3.1520
0101100	-4.2880	1000100	-3.9040	1011100	-3.5200	1110100	-3.1360
0101101	-4.2720	1000101	-3.8880	1011101	-3.5040	1110101	-3.1200
0101110	-4.2560	1000110	-3.8720	1011110	-3.4880	1110110	-3.1040
0101111	-4.2400	1000111	-3.8560	1011111	-3.4720	1110111	-3.0880
0110000	-4.2240	1001000	-3.8400	1100000	-3.4560	1111000	-3.0720
0110001	-4.2080	1001001	-3.8240	1100001	-3.4400	1111001	-3.0560
0110010	-4.1920	1001010	-3.8080	1100010	-3.4240	1111010	-3.0400
0110011	-4.1760	1001011	-3.7920	1100011	-3.4080	1111011	-3.0240
0110100	-4.1600	1001100	-3.7760	1100100	-3.3920	1111100	-3.0080
0110101	-4.1440	1001101	-3.7600	1100101	-3.3760	1111101	-2.9920
0110110	-4.1280	1001110	-3.7440	1100110	-3.3600	1111110	-2.9760
0110111	-4.1120	1001111	-3.7280	1100111	-3.3440	1111111	-2.9600

8.3.3 AVDD, AVCL SETTING (44h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
44h	R/W	0	1	0	0	AVCLS[1:0]		AVDDS[1:0]		--

Designation	Description
AVCLS[1:0]	AVCL level setting AVCLS[1:0] / AVCL (V) 00 / -4.2 01 / -4.6 10 / Reserved 11 / Reserved
AVDDS[1:0]	AVDD level setting AVDDS[1:0] / AVDD (V) 00 / 6.2 01 / 6.4 10 / Reserved 11 / Reserved

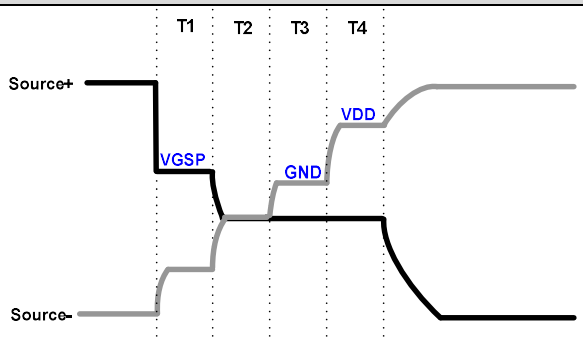
8.3.4 VGH, VGL SETTING (45h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
45h	R/W	0	0	0	0	VGLSEL[1:0]		VGHSEL[1:0]		--

Designation	Description
VGLSEL[1:0]	VGL level setting VGLSEL[1:0] / VGL (V) 00 / -7 01 / -8 10 / -10 11 / Reserved
VGHSEL[1:0]	VGH level setting VGHSEL[1:0] / VGH (V) 00 / 13 01 / 15 10 / 16 11 / 16.5

8.3.5 SOURCE EQUALIZE TIME SETTING (46h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
46h	R/W	T4T[1:0]		T3T[1:0]		T2T[1:0]		T1T[1:0]		--

Designation	Description
T4T[1:0] T3T[1:0] T2T[1:0] T1T[1:0]	

Source equalizing T4 timing setting

T4T[1:0]	T4 (DCLK)
00	2
01	5
10	10
11	20

Source equalizing T3 timing setting

T3T[1:0]	T3 (DCLK)
00	1
01	5
10	10
11	20

Source equalizing T2 timing setting

T2T[1:0]	T2 (DCLK)
00	1
01	5
10	10
11	20

Source equalizing T1 timing setting

T1T[1:0]	T1 (DCLK)
00	OFF
01	1
10	2
11	5

8.3.6 SOURCE OP-AMP POWER SETTING (47h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
47h	R/W	0	0	0	0	0	SOURCE_AP[2:0]			--

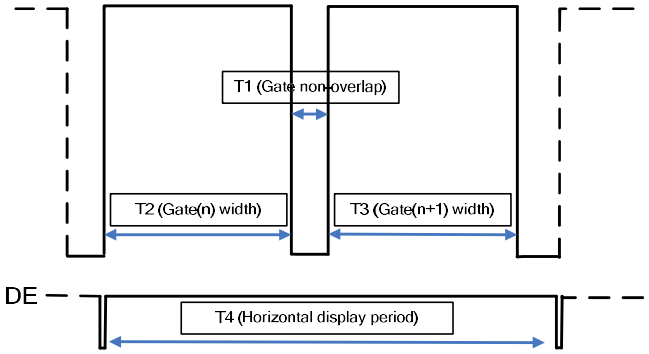
Designation	Description
SOURCE_AP[2:0]	Source driving ability setting. When value is higher, the source output current will increase.

SOURCE_AP[2:0]	Source Power
000	Level 1 (lowest)
001	Level 2 (minimal)
010	Level 3 (minimal to medium)
011	Level 4 (medium)
100	Level 5 (medium to large)
101	Level 6 (large)
110	Level 7 (large to highest)
111	Level 8 (highest)

Note: The setting value needs to be adjusted according to the display performance.

8.3.7 GATE TIMING SETTING 1 (49h)

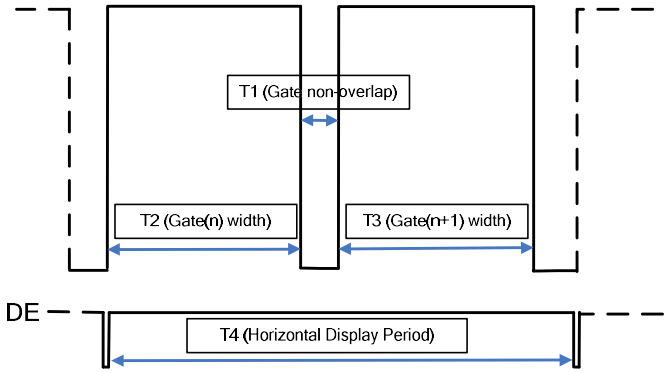
Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
49h	R/W	0	NO[2:0]			0	1	0	0	--

Designation	Description
NO[2:0]	 Gate (n) and Gate (n+1) non-overlap T1 timing setting

NO[2:0]	T1 non-overlap (DCLK)
000	4
001	8
010	16
011	24
100	32
101	40
110	60
111	80

8.3.8 GATE TIMING SETTING 2 (4Ah)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Ah	R/W	0	PRGB_GWIDTH[2:0]			0	SRGB _GWIDTH[2:0]			--

Designation	Description
PRGB_GWIDTH[2:0] SRGB_GWIDTH[2:0]	

Set gate pulse width of parallel RGB interface.

PRGB _GWIDTH[2:0]	T2 Gate (n) width (DCLK)	T3 Gate (n+1) width (DCLK)
000	GT1	GT2
001	GT1 + 4	GT2 – 4
010	GT1 + 8	GT2 – 8
011	GT1 + 12	GT2 – 12
100	GT1 + 16	GT2 – 16
101	GT1 + 20	GT2 – 20
110	GT1 + 30	GT2 – 30
111	GT1 +40	GT2 – 40

Set gate pulse width of serial RGB interface.

SRGB_GWIDTH[2:0]	T2 Gate (n) width (DCLK)	T3 Gate (n+1) width (DCLK)
000	GT1	GT2
001	GT1 + 4	GT2 – 4
010	GT1 + 8	GT2 – 8
011	GT1 + 12	GT2 – 12
100	GT1 + 16	GT2 – 16
101	GT1 + 20	GT2 – 20
110	GT1 + 30	GT2 – 30
111	GT1 +40	GT2 – 40

8.4 Gamma Table Register Description

8.4.1 GAMMA SETTING (20h~29h, 30h~39h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	R/W	0	-	-	VRF0P[4:0]					--
21h	R/W	0	-	-	VOS0P[4:0]					--
22h	R/W	PFP0[2:0]			PKP0[4:0]					--
23h	R/W	PFP1[2:0]			PKP1[4:0]					--
24h	R/W	PFP2[2:0]			PKP2[4:0]					--
25h	R/W	PFP3[2:0]			PKP3[4:0]					--
26h	R/W	PFP4[2:0]			PKP4[4:0]					--
27h	R/W	PFP5[2:0]			PKP5[4:0]					--
28h	R/W	PFP6[2:0]			PKP6[4:0]					--
29h	R/W	0	0	0	PKP7[4:0]					--
30h	R/W	0	-	-	VRF0N[4:0]					--
31h	R/W	0	-	-	VOS0N[4:0]					--
32h	R/W	PFN0[2:0]			PKN0[4:0]					--
33h	R/W	PFN1[2:0]			PKN1[4:0]					--
34h	R/W	PFN2[2:0]			PKN2[4:0]					--
35h	R/W	PFN3[2:0]			PKN3[4:0]					--
36h	R/W	PFN4[2:0]			PKN4[4:0]					--
37h	R/W	PFN5[2:0]			PKN5[4:0]					--
38h	R/W	PFN6[2:0]			PKN6[4:0]					--
39h	R/W	0	0	0	PKN7[4:0]					--

Designation	Description
PKP0[4:0]	V16 gamma selection
PKN0[4:0]	
PKP1[4:0]	V32 gamma selection
PKN1[4:0]	
PKP2[4:0]	V48 gamma selection
PKN2[4:0]	
PKP3[4:0]	V80 gamma selection
PKN3[4:0]	
PKP4[4:0]	V176 gamma selection
PKN4[4:0]	
PKP5[4:0]	V208 gamma selection
PKN5[4:0]	

PKP6[4:0]	V224 gamma selection
PKN6[4:0]	
PKP7[4:0]	V240 gamma selection
PKN7[4:0]	
VRF0P[4:0]	V8 gamma selection
VRF0N[4:0]	
VOS0P[4:0]	V248 gamma selection
VOS0N[4:0]	
PFP0[2:0]	V12 gamma selection
PFN0[2:0]	
PFP1[2:0]	V64 gamma selection
PFN1[2:0]	
PFP2[2:0]	V104 gamma selection
PFN2[2:0]	
PFP3[2:0]	V128 gamma selection
PFN3[2:0]	
PFP4[2:0]	V152 gamma selection
PFN4[2:0]	
PFP5[2:0]	V192 gamma selection
PFN5[2:0]	
PFP6[2:0]	V244 gamma selection
PFN6[2:0]	

8.5 OTP Table Register Description

8.5.1 ID1 SETTING (01h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	R/W	0	ID1[6:0]							--

Designation	Description
ID1[6:0]	Built-in OTP for ID1 setting. The OTP supports 3 times programming

8.5.2 ID2 SETTING (02h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	R/W	0	ID2[6:0]							--

Designation	Description
ID2[6:0]	Built-in OTP for ID2 setting. The OTP supports 3 times programming

8.5.3 ID3 SETTING (03h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
03h	R/W	0	ID3[6:0]							--

Designation	Description
ID3[6:0]	Built-in OTP for ID3 setting. The OTP supports 3 times programming

8.5.4 I2C ID CODE SETTING (04h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	R/W	0	I^2CID[6:0]							78h

Designation	Description
I^2CID[6:0]	Built-in OTP for I^2C interface ID setting. The OTP supports 3 times programming

8.5.5 VCOM OFFSET SETTING (05h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
05h	R/W	0	VMF[6:0]							40h

Designation	Description
VMF[6:0]	VCOM offset setting

VMF[6]	VMF[5:0]	VGSP	GVDD	GVCL
0	000000	VCOMS[6:0]+64d	VRHP[6:0]+64d	VRHN[6:0]+64d
0	000001	VCOMS[6:0]+63d	VRHP[6:0]+63d	VRHN[6:0]+63d
0	000010	VCOMS[6:0]+62d	VRHP[6:0]+62d	VRHN[6:0]+62d
0	|	|	|	|
0	111110	VCOMS[6:0]+2d	VRHP[6:0]+2d	VRHN[6:0]+2d
0	111111	VCOMS[6:0]+1d	VRHP[6:0]+1d	VRHN[6:0]+1d
1	000000	VCOMS[6:0]	VRHP[6:0]	VRHN[6:0]
1	000001	VCOMS[6:0]-1d	VRHP[6:0]-1d	VRHN[6:0]-1d
1	000010	VCOMS[6:0]-2d	VRHP[6:0]-2d	VRHN[6:0]-2d
1	|	|	|	|
1	111110	VCOMS[6:0]-62d	VRHP[6:0]-62d	VRHN[6:0]-62d
1	111111	VCOMS[6:0]-63d	VRHP[6:0]-63d	VRHN[6:0]-63d

Note: d=16mV

8.5.6 OTP FUNCTION CONTROL (60h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	W	0	1	0	0	0	1	OTPEN	0	44h

Designation	Description
OTPEN	OTP function control OTPEN = 0: disable OTP function OTPEN = 1: enable OTP function

8.5.7 OTP ACKNOWLEDGEMENT CONTROL (65h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
65h	W	OTPACK[7:0]								00h

Designation	Description
OTPACK[7:0]	OTP active selection OTPACK[7:0] / Description 31h: ID1 program 32h: ID2 program 33h: ID3 program 34h: I²C I/F ID program 3Ah: VCOM offset program 4Bh: Command 2 program 5Ch: Gamma program

8.5.8 VCOM OFFSET OTP PROGRAM TIMES (66h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
66h	R	0	0	0	0	0	VMF OTP TIME[2:0]			--

Designation	Description
VMF OTP TIME[2:0]	Read VCOM offset remaining programmable times

8.5.9 COMMAND 2 PROGRAM TIMES (67h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
67h	R	0	0	0	0	0	CMD2 OTP TIME[2:0]			--

Designation	Description
CMD2 OTP TIME[2:0]	Read COMMAND 2 remaining programmable times

8.5.10 GAMMA OTP PROGRAM TIMES (68h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
68h	R	0	0	0	0	0	GAMMA OTP TIME[2:0]			--

Designation	Description
GAMMA OTP TIME[2:0]	Read GAMMA remaining programmable times

8.5.11 ID1 OTP PROGRAM TIMES (69h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
69h	R	0	0	0	0	0	ID1 OTP TIME[2:0]			--

Designation	Description
ID1 OTP TIME[2:0]	Read ID1 remaining programmable times

8.5.12 ID2 OTP PROGRAM TIMES (6Ah)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ah	R	0	0	0	0	0	ID2 OTP TIME[2:0]			--

Designation	Description
ID2 OTP TIME[2:0]	Read ID2 remaining programmable times

8.5.13 ID3 OTP PROGRAM TIMES (6Bh)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Bh	R	0	0	0	0	0	ID3 OTP TIME[2:0]			--

Designation	Description
ID3 OTP TIME[2:0]	Read ID3 remaining programmable times

8.5.14 I^2C ID OTP PROGRAM TIMES (6Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ch	R	0	0	0	0	0	I^2CID OTP TIME[2:0]			--

Designation	Description
I^2CID OTP TIME[2:0]	Read I^2CID remaining programmable times

9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	VDD	- 0.3 ~ +4.0	V
IO Supply Voltage	VDDI	- 0.3 ~ +4.0	V
Charge Pump Supply Voltage	PVDD	- 0.3 ~ +4.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VOUT	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Note:

1. That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/AC Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.

2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

3. Insure the voltage levels of VDDI, VDD, PVDD always matches the correct relation:

$1.65V \leqq VDDI \leqq VDD = PVDD \leqq 3.6V$

4. VIN should be less than or equal to 3.6V. ($VIN \leq 3.6V$)

9.2 DC Characteristics

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

9.2.1 Recommended Operating Range

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VDD	3.0	3.3	3.6	V	
IO Supply Voltage	VDDI	1.65	-	3.6	V	
Charge Pump Supply Voltage	PVDD	3.0	3.3	3.6	V	

9.2.2 DC Characteristics for Digital Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	
Logic-Low Input Voltage	Vil	DGND	-	0.3VDDI	V	
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	

9.2.3 DC Characteristics for Analog Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-Voltage Power	VGH	13	15	16.5	V	No Load@ FR=60Hz
Negative High-Voltage Power	VGL	-7	-10	-10	V	
Output Voltage Deviation	Vod	-	±35	±45	mV	
Standby Current	Isc	-	-	50	uA	
Operation Current	Ioc	-	20	-	mA	

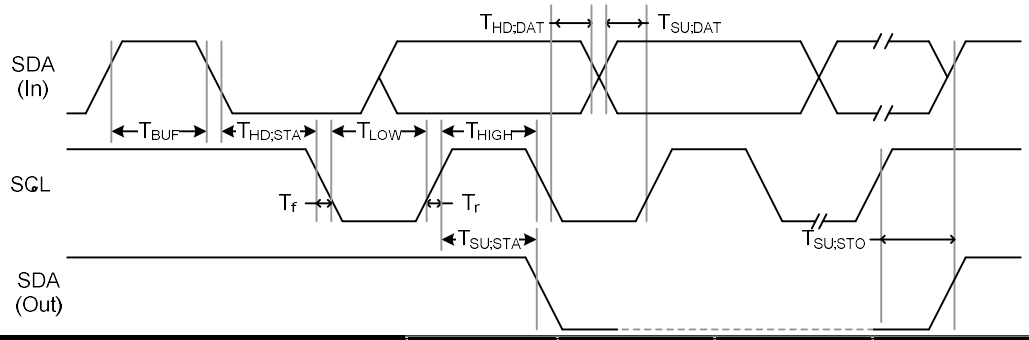
9.3 AC Characteristics

AC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

9.3.1 System Operation AC Characteristics

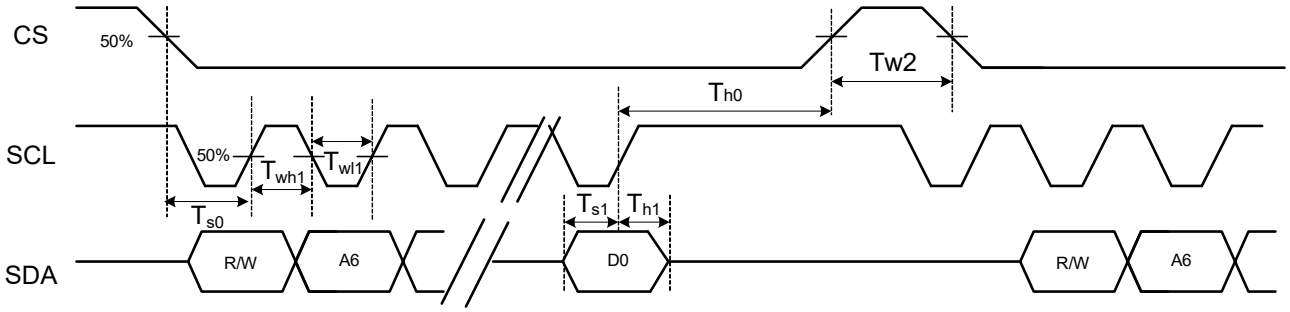
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power Source Slew Time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB Pulse Width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
SD Output Stable Time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD Output Rise and Fall Time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF

9.3.2 System Bus Timing for I²C Interface



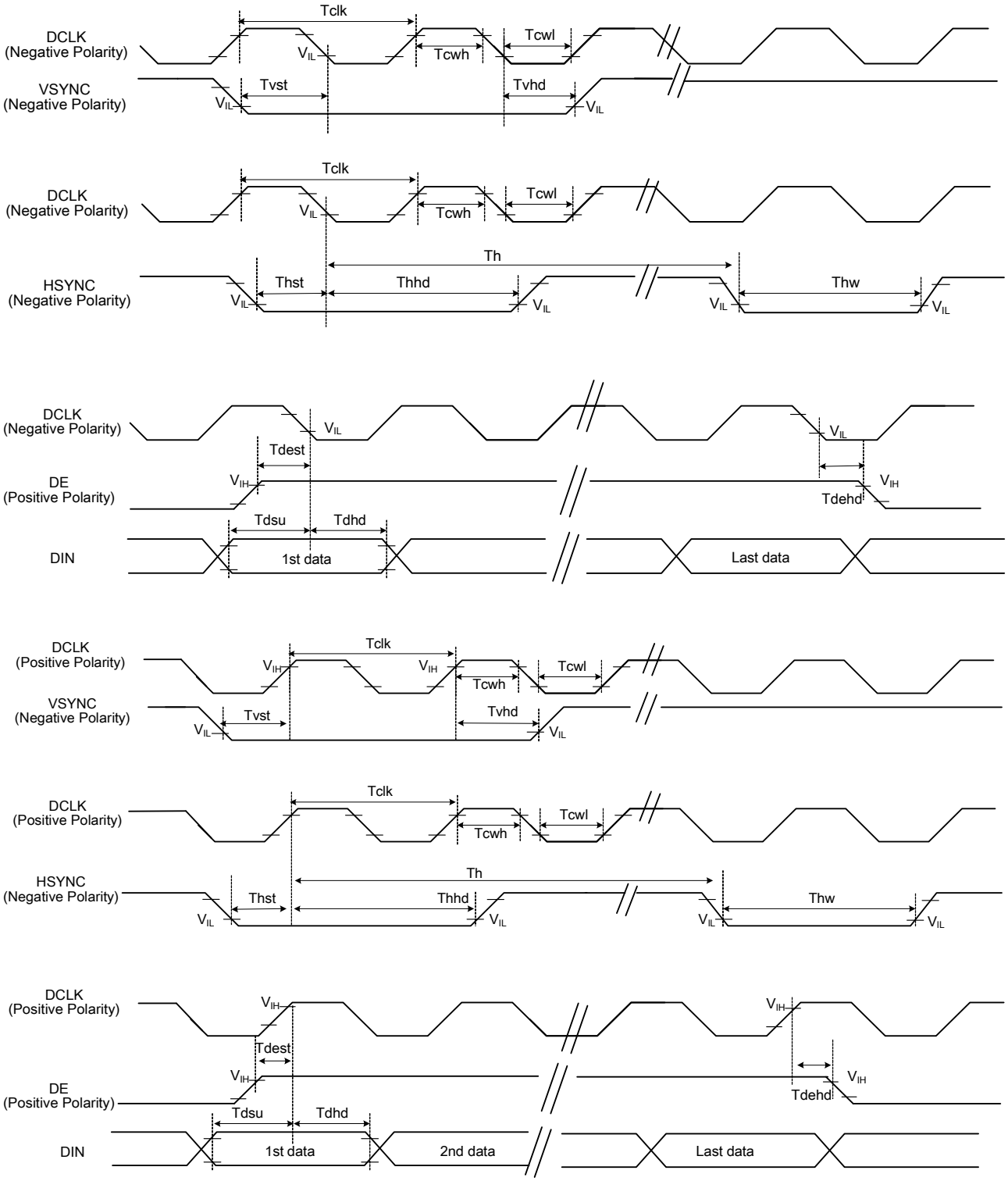
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCL Clock Frequency	FSCL	-	-	400	KHz	
SCL Clock Low Period	TLOW	1300	-	-	ns	
SCL Clock High Period	THIGH	600	-	-	ns	
Signal Rise Time	Tr	20+0.1Cb	-	300	ns	
Signal Fall Time	Tf	20+0.1Cb	-	300	ns	
Start Condition Setup Time	TSU;STA	600	-	-	ns	
Start Condition Hold Time	THD;STA	600	-	-	ns	
Data Setup Time	TSU;DAT	100	-	-	ns	
Data Hold Time	THD;DAT	0	-	900	ns	
Setup Time for STOP Condition	TSU;STO	600	-	-	ns	
Bus Free Time Between a STOP and START	TBUF	100	-	-	ns	
Capacitive load represented by each bus line	Cb	-	-	400	pF	
Tolerable Spike Width on Bus	TSW	-	-	50	ns	

9.3.3 System Bus Timing for 3-Wire SPI Interface



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CS Input Setup Time	Ts0	50	-	-	ns	
Serial Data Input Setup Time	Ts1	50	-	-	ns	
CS Input Hold Time	Th0	50	-	-	ns	
Serial Data Input Hold Time	Th1	50	-	-	ns	
SCL Write Pulse High Width	Twh1	50	-	-	ns	
SCL Write Pulse Low Width	Twl1	50	-	-	ns	
SCL Read Pulse High Width	Trh1	300			ns	
SCL Read Pulse Low Width	Trl1	300			ns	
CS Pulse High Width	Tw2	400	-	-	ns	

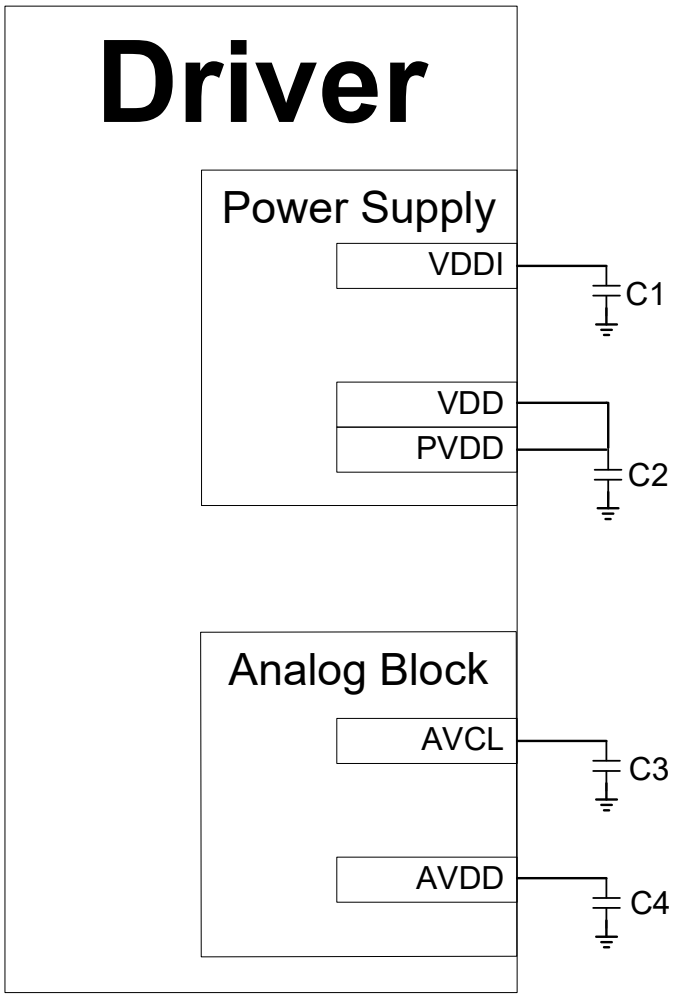
9.3.4 System Bus Timing for RGB Interface



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Pulse Duty	Tclk	40	50	60	%	
HSYNC Width	Thw	2	-	-	DCLK	
VSYNC Setup Time	Tvst	12	-	-	ns	
VSYNC Hold Time	Tvhd	12	-	-	ns	
HSYNC Setup Time	Thst	12	-	-	ns	
HSYNC Hold Time	Thhd	12	-	-	ns	
Data Setup Time	Tdsu	12	-	-	ns	
Data Hold Time	Tdhd	12	-	-	ns	
DE Setup Time	Tdest	12	-	-	ns	
DE Hold Time	Tdehd	12	-	-	ns	

10. APPLICATION CIRCUIT

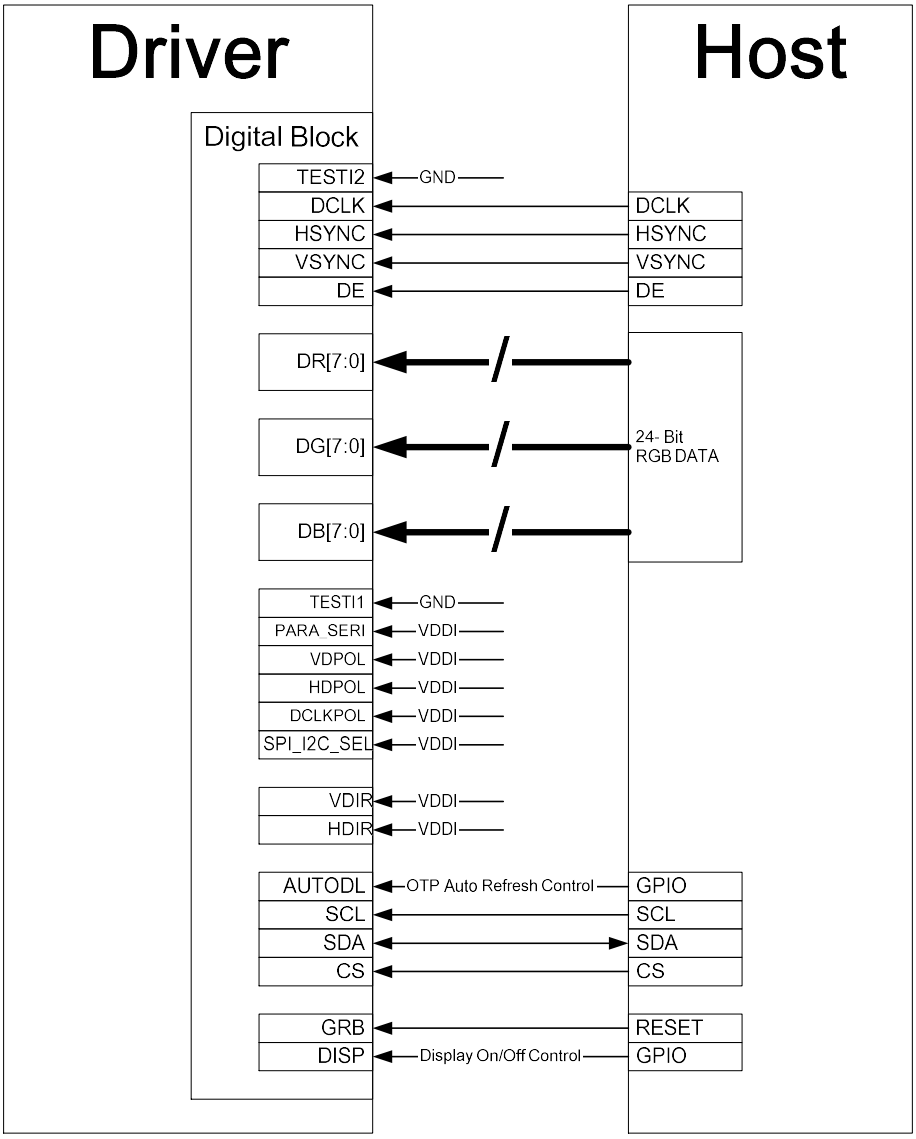
10.1 External Component of Power Circuit



Symbol	Capacitance (uF)	Working Voltage (V)	Note
C1	1	6	Default NC
C2	1	6	Default NC
C3	1	10	Default NC
C4	1	10	Default NC

Note: Default NC, the components would be needed depend on the system power, panel loading and display quality

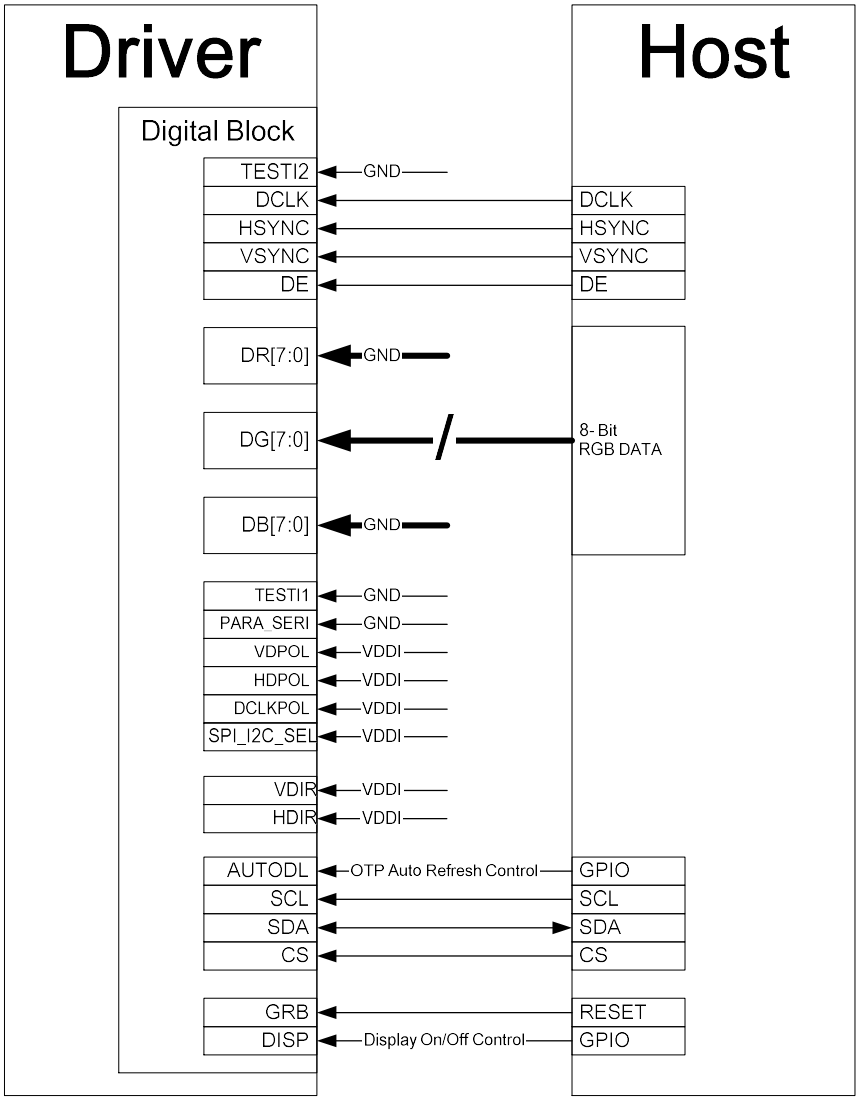
10.2 Parallel 24-bit RGB with 3-wire SPI



Pin Connection	Description
TESTI [2:1]	Those pins connect to “L”.
PARA_SERI= “H”	Parallel 24-bit RGB interface
VDPOL= “H”	VSYNC negative polarity
HDPOL= “H”	HSYNC negative polarity
DCLKPOL= “H”	DCLK negative polarity
SPI_I²C_SEL= “H”	3-Wire SPI
VDIR= “H”	Vertical scan direction= L1->L2->..... ->L(last line)
HDIR= “H”	Horizontal scan direction= Y1->Y2->.....->Y(last data)

Note: For detailed pin description please refer to section 6.1 PIN DESCRIPTION.

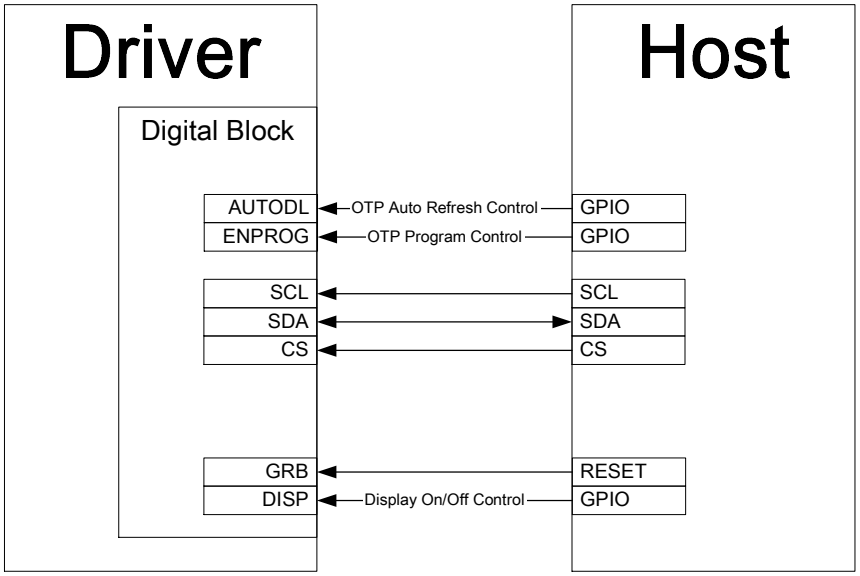
10.3 Serial 8-bit RGB with 3-wire SPI



Pin Connection	Description
TESTI [2:1]	Those pins connect to “L”.
PARA_SERI = “L”	Serial 8-bit RGB interface
VDPOL= “H”	VSYNC negative polarity
HDPOL= “H”	HSYNC negative polarity
DCLKPOL= “H”	DCLK negative polarity
SPI_I^{2}C_SEL= “H”	3-Wire SPI
VDIR= “H”	Vertical scan direction= L1->L2->.....->L(last line)
HDIR= “H”	Horizontal scan direction= Y1->Y2->.....->Y(last data)

Note: For detailed pin description please refer to section 6.1 PIN DESCRIPTION.

10.4 OTP Operation

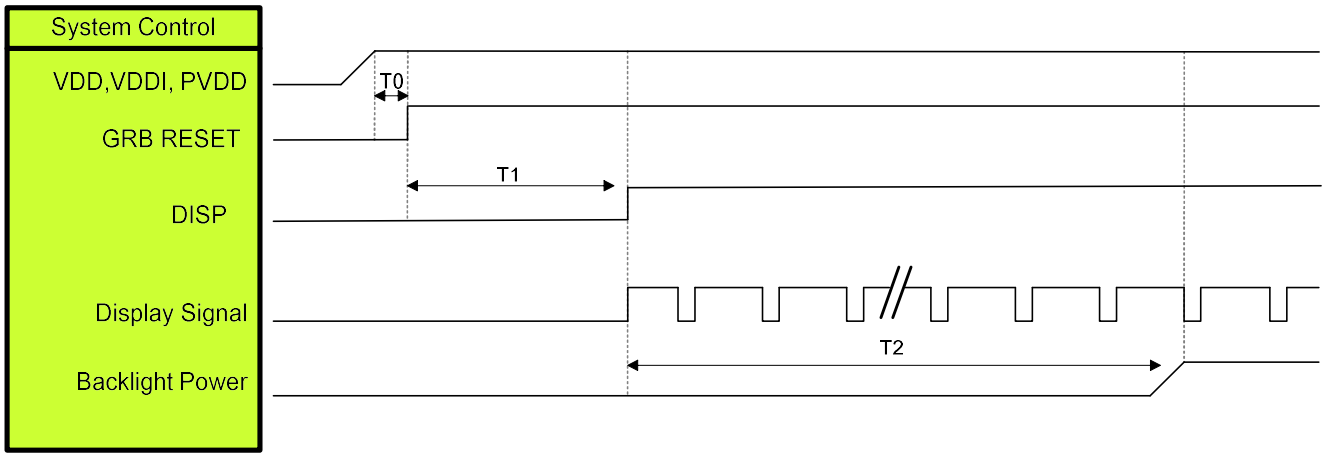


Pin Connection	Description
AUTODL	OTP auto-refresh function control
ENPROG	OTP program function control

Note: For detailed pin description please refer to section 6.1 PIN DESCRIPTION.

11. POWER ON/OFF SEQUENCE

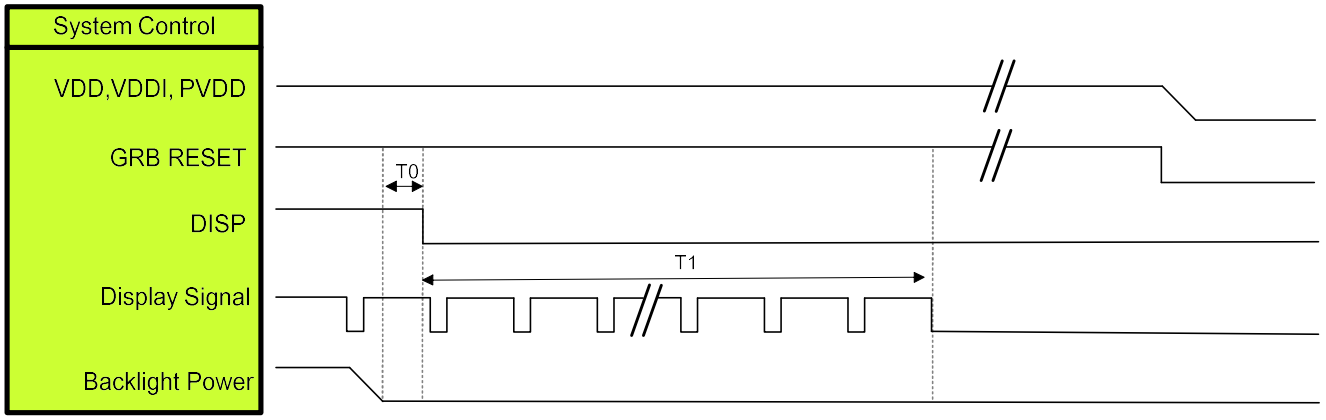
11.1 Power On Sequence



Symbol	Description	Min. Time	Unit
T0	System power stability to GRB RESET signal	0	ms
T1	GRB RESET= “High” to DISP=”High”	10	ms
T2	Display Signal output to Backlight Power on	250	ms

Note: Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0]

11.2 Power Off Sequence



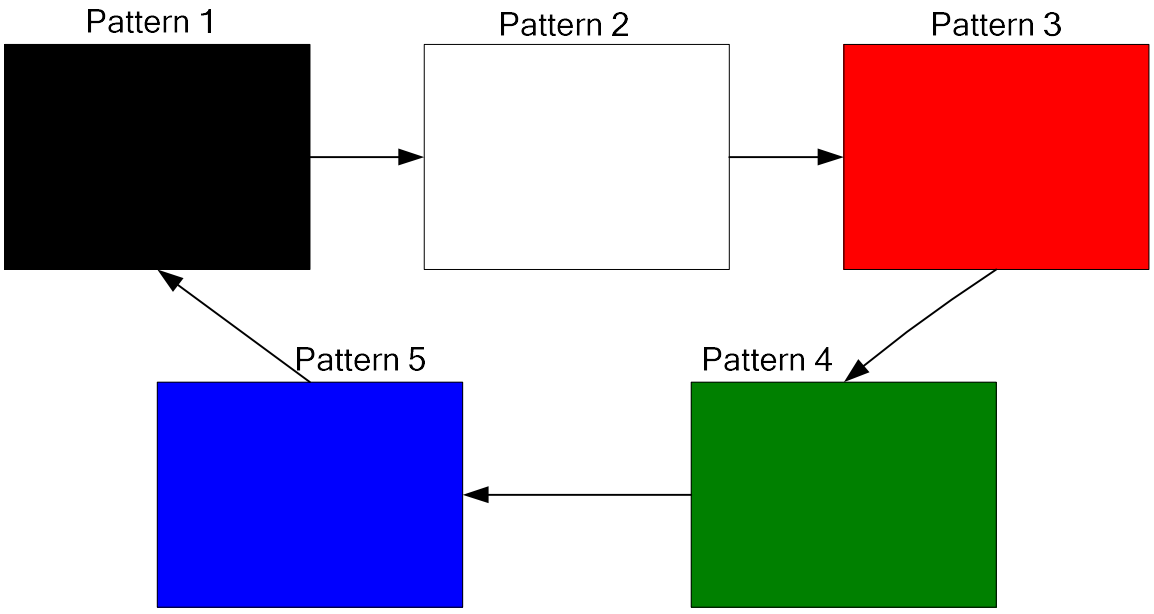
Symbol	Description	Min. Time	Unit
T0	Backlight Power off to DISP=”Low”	5	ms
T1	DISP=”Low” to IC internal voltage discharge complete	80	ms

Note: Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0]

12. BIST FUNCTION

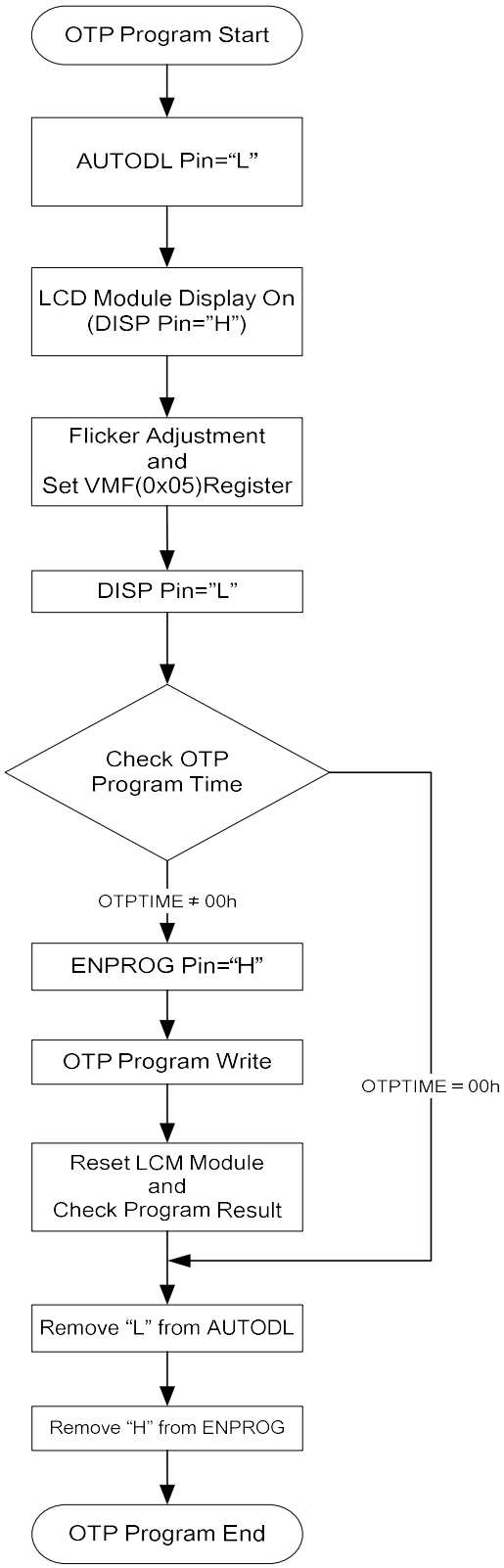
When “BIST_EN” pin sets to “H”, the BIST function is enabled. The BIST pattern will automatically display BIST pattern in the BIST mode as follows.

12.1 BIST Pattern



13. OTP PROGRAM FLOW

13.1 VCOM Offset OTP Flow



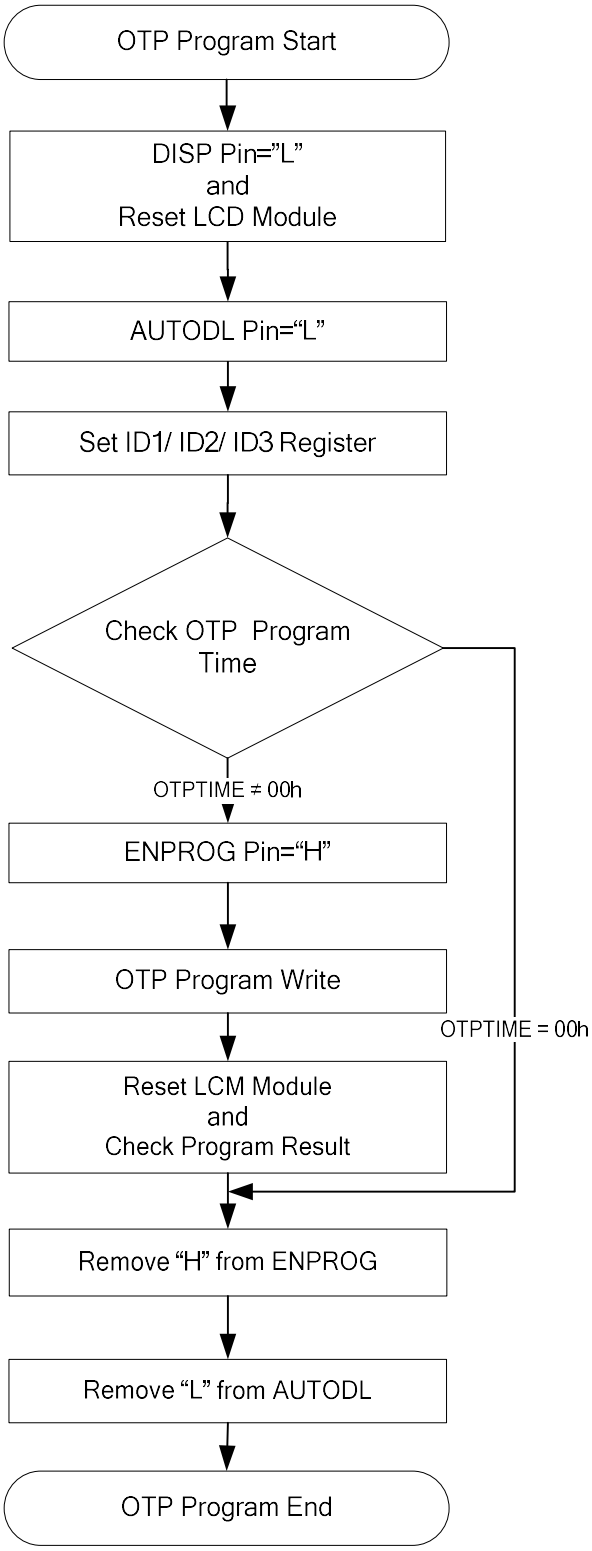
```
void Set_VMF_Register ()
{
    Write(Command,0x05);                    //Flicker adjustment and VMF[6:0] register setting
    Write(Data, VMF);
}

void Check_OTP_Program_Time()
{
    Write(Command,0x66);                    //VMF OTPTIME register address
    Read(Data, VMFOTPTIME);
}

void OTP_Program_Write()
{
    Write(Command,0x60);                    //OTP write function enable
    Write(Data,0x46);
    Delay_ms(10);
    Write(Command,0x65);                    //OTP ACK= 0x3A
    Write(Data,0x3A);
    Delay_ms(100);
}

void Check_Program_Result()
{
    Write(Command,0x05);                    //Read VMF[6:0] register setting
    Read(Data, VMF);
}
```

13.2 Custom Application ID Code OTP Flow



```
void Set_OTP_Register ()
{
    Write(Command,0x01);              //The parameter should be adjusted by the customer
    Write(Data, ID);                  //ID1= 0x01, ID2= 0x02, ID3= 0x03
}

void Check_OTP_Program_Time()
{
    Write(Command,0x69);              //The parameter should be adjusted by the customer;
    Read(Data, IDOTPTIME);            //ID1 OTPTIME= 0x69, ID2 OTPTIME= 0x6A
}                                     //ID3 OTPTIME= 0x6B

void OTP_Program_Write()
{
    Write(Command,0x60);              //OTP write function enable
    Write(Data,0x46);
    Delay_ms(10);
    Write(Command,0x65);              // The parameter should be adjusted by the customer;
    Write(Data,0x31);                 // ID1 ACK= 0x31, ID2 ACK= 0x32, ID3 ACK= 0x33
    Delay_ms(100);
}

void Check_Program_Result ()
{
    Write(Command,0x01);              // The parameter should be adjusted by the customer
    Read(Data, ID);                   // ID1= 0x01, ID2= 0x02, ID3= 0x03
}
```

14. RECOMMENDED PANEL ROUTING RESISTANCE

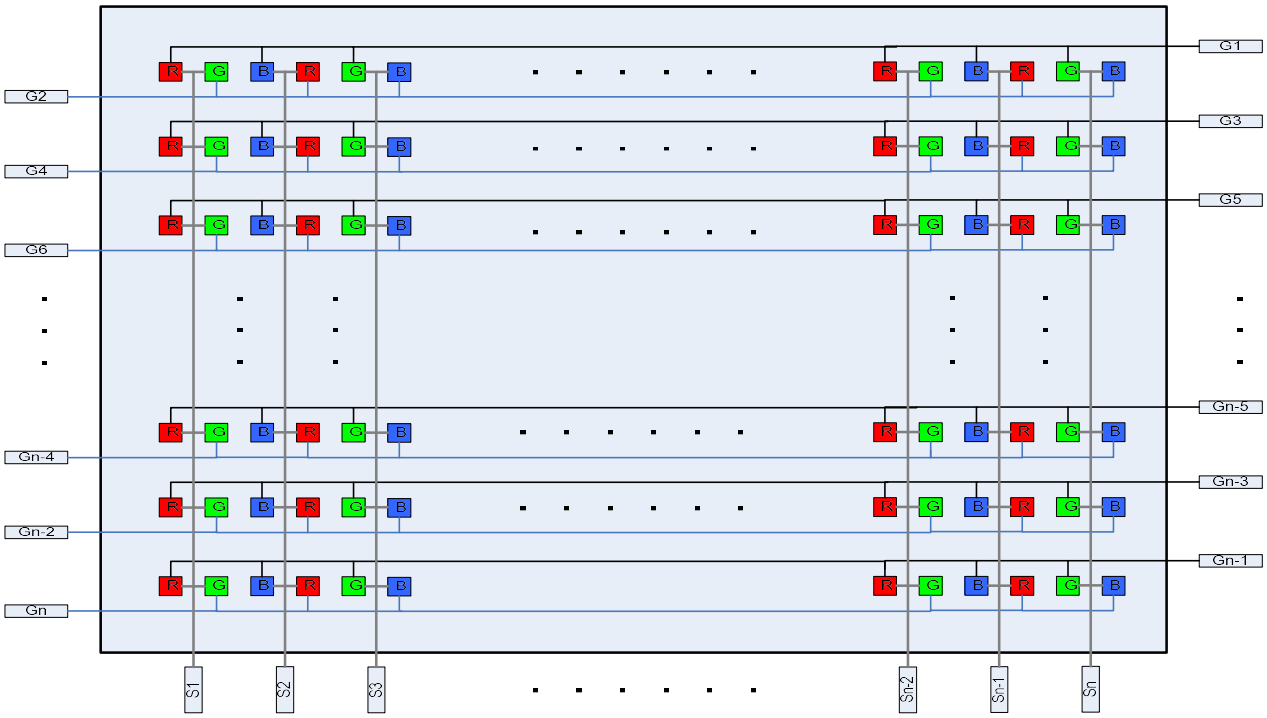
The wiring resistance values will affect the current capability of the power supply. Please design the wiring resistance according to the following table.

No.	Pin Name	Unit: ohm
1	VPP	<3
2	GVDD	<50
3	GVCL	<50
4	VCOM	<3
5	DGND	<3
6	VCC	<50
7	VDDI	<3
8	VDD	<3
9	VSYNC	<50
10	HSYNC	<50
11	DCLK	<50
12	VDPOL	<50
13	HDPOL	<50
14	DCLKPOL	<50
15	ENPROG	<50
16	DE	<50
17	PARA_SERI	<50
18	AUTODL	<50
19	HDIR	<50
20	AGND	<3

No.	Pin Name	Unit: ohm
21	CS	<50
22	SDA	<50
23	SCL	<50
24	DISP	<50
25	GRB	<50
26	BIST_EN	<50
27	DR7-DR0	<50
28	DG7-DG0	<50
29	DB7-DB0	<50
30	AGND	<3
31	SPI_I2C_SEL	<50
32	AVCL	<50
33	AVCL1	<50
34	AVDD	<50
35	AVDD1	<50
36	VGSP	<50
37	PGND	<3
38	PVDD	<3
39	VGH	<50
40	VGL	<50

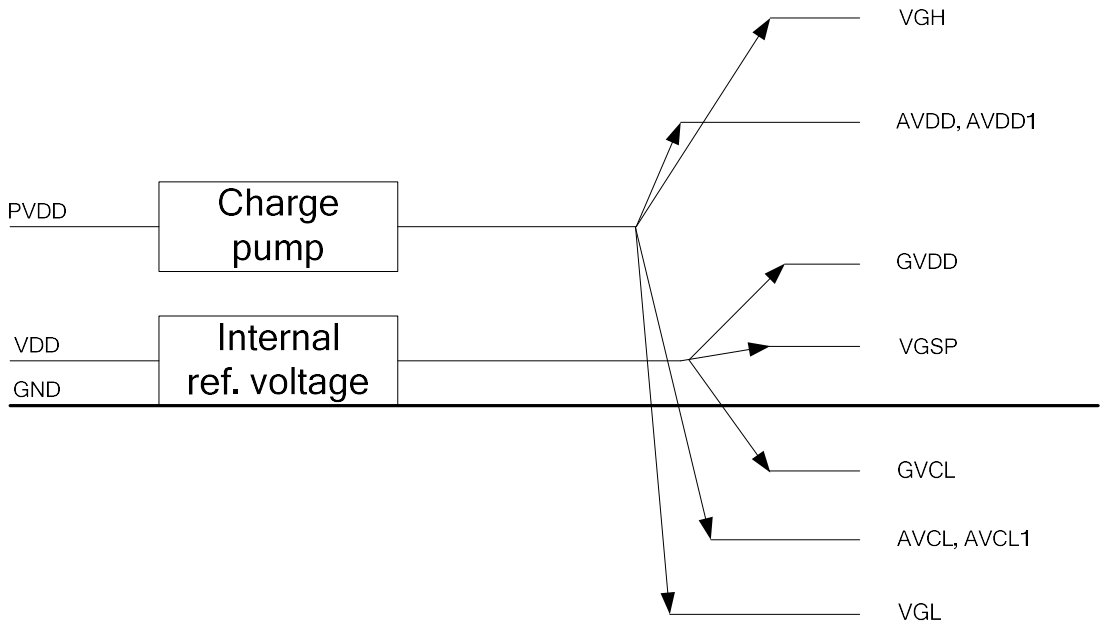
15. COLOR FILTER ARRANGEMENT

The IC supports the stripe color filter of dual-gate application. The color filter arrangement on panel is shown below.



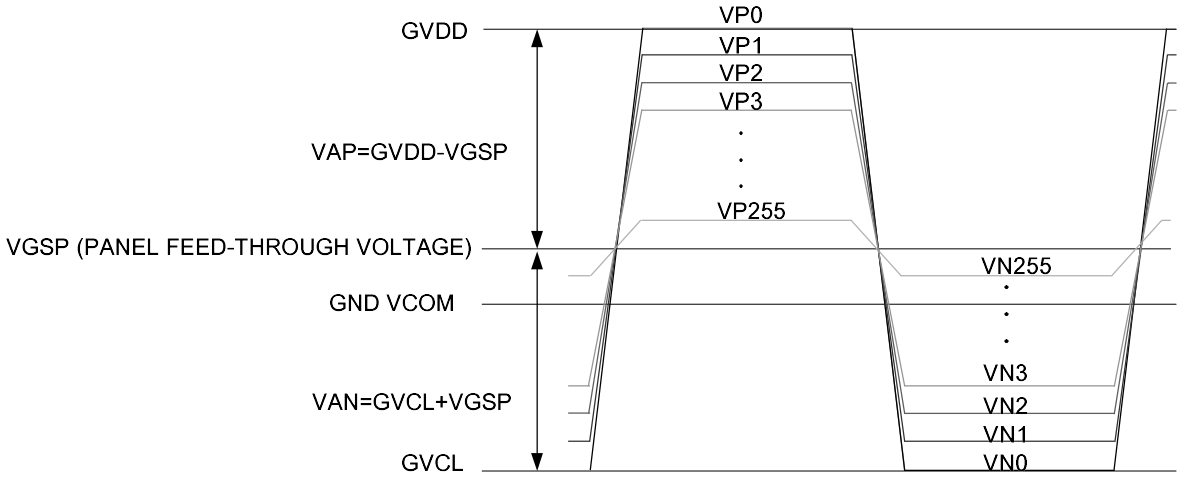
16. POWER STRUCTURE

16.1 Voltage Generation



16.2 Source Voltage Relations

The relations between VCOM and source voltage is shown as below:

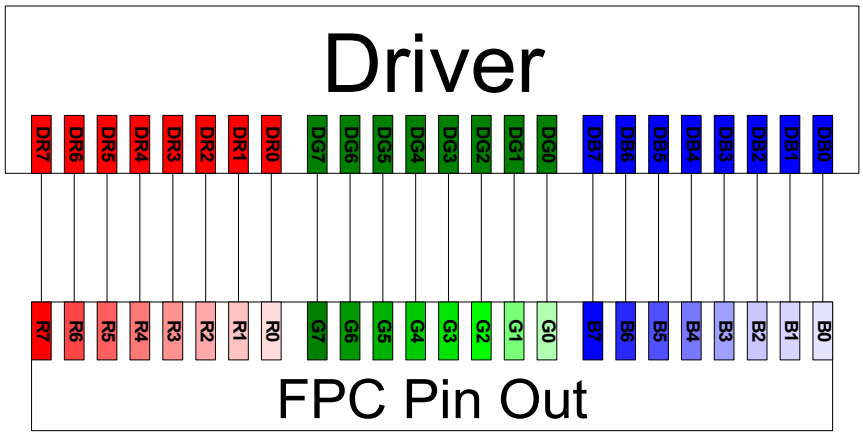


Note: The IC source support maximum LC driving voltage VAP (VAN): 5.224V [(GVDD-VGSP)=(VGSP-GVCL)=(GVDD-GVCL)/ 2].

The driver compensates the panel feed-through voltage = VGSP

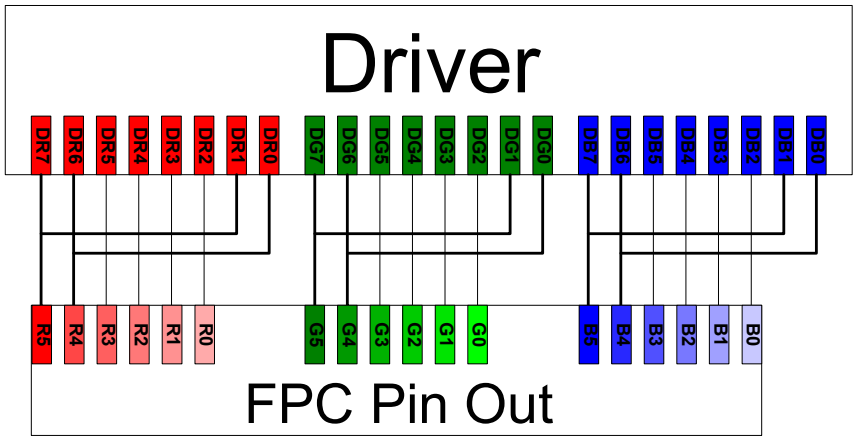
17. COLOR FORMAT INPUT PIN APPLICATION CIRCIT

17.1 16.7M Color Format Input Pin Connection



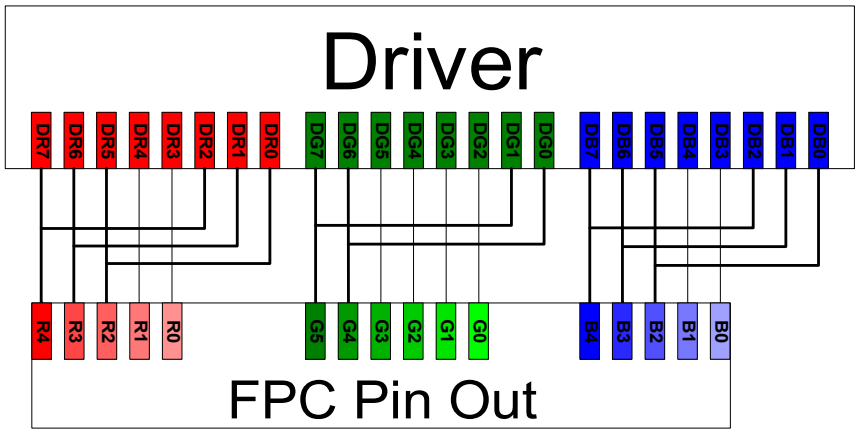
Driver	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
FPC Pin Out	R7	R6	R5	R4	R3	R2	R1	R0
Driver	DG7	DG6	DG5	DG4	DG3	DG2	DG1	DG0
FPC Pin Out	G7	G6	G5	G4	G3	G2	G1	G0
Driver	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
FPC Pin Out	B7	B6	B5	B4	B3	B2	B1	B0

17.2 262K Color Format Input Pin Connection



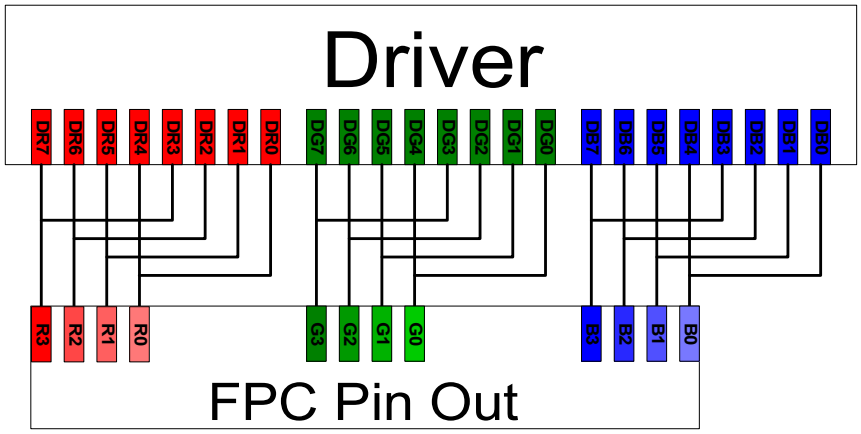
Driver	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
FPC Pin Out	R5	R4	R3	R2	R1	R0	R5	R4
Driver	DG7	DG6	DG5	DG4	DG3	DG2	DG1	DG0
FPC Pin Out	G5	G4	G3	G2	G1	G0	G5	G4
Driver	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
FPC Pin Out	B5	B4	B3	B2	B1	B0	B5	B4

17.3 65K Color Format Input Pin Connection



Driver	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
FPC Pin Out	R4	R3	R2	R1	R0	R4	R3	R2
Driver	DG7	DG6	DG5	DG4	DG3	DG2	DG1	DG0
FPC Pin Out	G5	G4	G3	G2	G1	G0	G5	G4
Driver	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
FPC Pin Out	B4	B3	B2	B1	B0	B4	B3	B2

17.4 4K Color Format Input Pin Connection



Driver	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
FPC Pin Out	R3	R2	R1	R0	R3	R2	R1	R0
Driver	DG7	DG6	DG5	DG4	DG3	DG2	DG1	DG0
FPC Pin Out	G3	G2	G1	G0	G3	G2	G1	G0
Driver	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
FPC Pin Out	B3	B2	B1	B0	B3	B2	B1	B0

18. REVISION HISTORY

Revision	Description	Date
V 1.0	Official Release	2018/08
V1.1	1. Add the relationship between VDDI, VDD, PVDD 2. Modify Pin Name Error in the Output Bum Dimension Figure 3. Modify Typing Error	2018/11
V1.2	1. Modify register(19h) description	2019/03
V1.3	1. Add Chip Size 2. Modify Application Range of VDDI 3. Modify Registers 20h, 21h, 30h, 31h	2019/08