Sitronix

ST7541

4 Gray Scale Dot Matrix LCD Controller/Driver

INTRODUCTION

ST7541 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. This chip can connect directly to a microprocessor which supports: Serial Peripheral Interface (SPI), IIC or 8-bit parallel interface. Display data stores in an on-chip display data RAM of 128 x 129 x 2 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

4-level Gray Scale

– Display with PWM and FRC Methods

DDRAM Data [2n:2n+1]		Gray Scale
2n	2n + 1	
0	0	White
0	1	Light gray
1	0	Dark gray
1	1	Black

(Accessible column address, n = 0~127)

Driver Output Circuits

128 segment outputs / 128+1 common outputs

Applicable Duty Ratios

– Various partial display

– Partial window moving & data scrolling

On-chip Display Data RAM

– Capacity: 128 × 129 × 2= 33,024 bits

Microprocessor Interface

– 8-bit bi-directional parallel interface supports 6800-series or 8080-series MPU

– 4-line serial interface (4-Line SPI)

– 3-line serial interface (3-Line 8-bit SPI)

– IIC serial interface

On-chip Low Power Analog Circuit

– On-chip oscillator circuit

– Voltage booster (x3, x4, x5 or x6)

– Voltage regulator (temperature coefficient: -0.144%/˚C, or external input)

– On-chip electronic contrast control function (64 steps X 8)

– Voltage follower (LCD bias : 1/5 to 1/12)

Operating Voltage Range

– Supply voltage (VDD): 1.8 to 3.3V

– Supply voltage (VDD2): 2.4 to 3.3V

– LCD driving voltage (VLCD = V0 - VSS): 3.5 to 15.0 V

Package Type

– Application for COG

ST7541	**6800 , 8080 , 4-Line , 3-Line interface (without IIC interface)**	ST
ST7541i	**IIC interface**	I²C BUS

ST7541 Pad Arrangement (COG)

Chip Size: 12,575 um × 1,220 um

Bump Pitch:

PAD NO 1 ~ 229, 353 ~ 385: 55 um (COM/SEG), PAD NO 230 ~ 338: 75 um (I/O) ,PAD NO 339 ~ 352: 75 um (I/O) , PAD 338 ~ 339 : 81um

Bump Size:

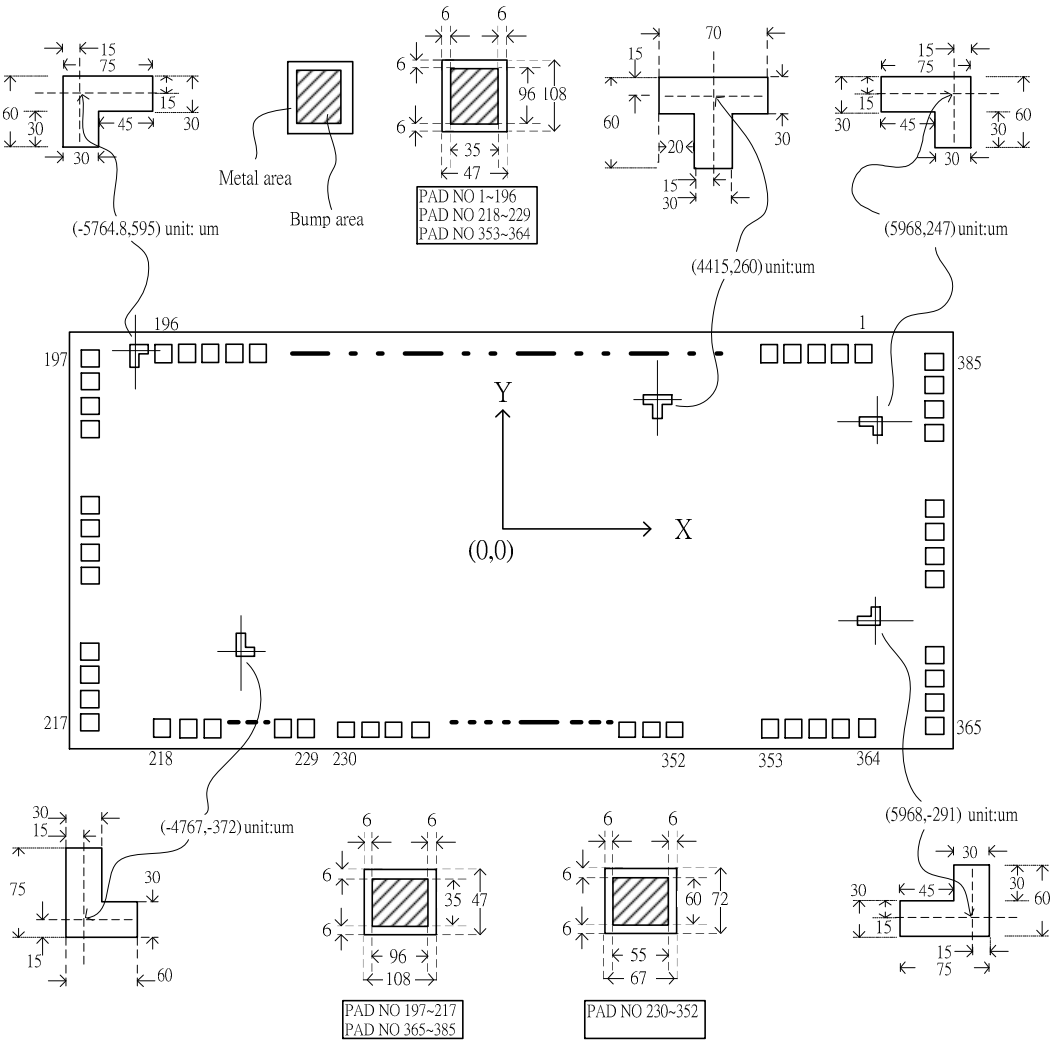
PAD NO 1 ~ 196, 218 ~ 229, 353 ~ 364 : 35(x) um ×96(y) um PAD NO 197 ~ 217, 365 ~ 385 : 96(x) um ×35(y) um

PAD NO 230 ~ 352 : 55(x)um ×60(y) um

Bump Height: 17 um (Typ)

Chip Thickness:

Part Number	Thickness
ST7541-G	635 um (default)
ST7541-G2	480 um
ST7541-G4	300 um



Pad Center Coordinates

PAD No.	Pin Name	X	Y
1	COM30	5096	556
2	COM29	5041	556
3	COM28	4986	556
4	COM27	4931	556
5	COM26	4876	556
6	COM25	4821	556
7	COM24	4766	556
8	COM23	4711	556
9	COM22	4656	556
10	COM21	4601	556
11	COM20	4546	556
12	COM19	4491	556
13	COM18	4436	556
14	COM17	4381	556
15	COM16	4326	556
16	COM15	4271	556
17	COM14	4216	556
18	COM13	4161	556
19	COM12	4106	556
20	COM11	4051	556
21	COM10	3996	556
22	COM9	3941	556
23	COM8	3886	556
24	COM7	3831	556
25	COM6	3776	556
26	COM5	3721	556
27	COM4	3666	556
28	COM3	3611	556
29	COM2	3556	556
30	COM1	3501	556
31	COM0	3446	556
32	COMS1	3391	556
33	SEG0	3336	556
34	SEG1	3281	556
35	SEG2	3226	556

PAD No.	Pin Name	X	Y
36	SEG3	3171	556
37	SEG4	3116	556
38	SEG5	3061	556
39	SEG6	3006	556
40	SEG7	2951	556
41	SEG8	2896	556
42	SEG9	2841	556
43	SEG10	2786	556
44	SEG11	2731	556
45	SEG12	2676	556
46	SEG13	2621	556
47	SEG14	2566	556
48	SEG15	2511	556
49	SEG16	2456	556
50	SEG17	2401	556
51	SEG18	2346	556
52	SEG19	2291	556
53	SEG20	2236	556
54	SEG21	2181	556
55	SEG22	2126	556
56	SEG23	2071	556
57	SEG24	2016	556
58	SEG25	1961	556
59	SEG26	1906	556
60	SEG27	1851	556
61	SEG28	1796	556
62	SEG29	1741	556
63	SEG30	1686	556
64	SEG31	1631	556
65	SEG32	1576	556
66	SEG33	1521	556
67	SEG34	1466	556
68	SEG35	1411	556
69	SEG36	1356	556
70	SEG37	1301	556

PAD No.	Pin Name	X	Y
71	SEG38	1246	556
72	SEG39	1191	556
73	SEG40	1136	556
74	SEG41	1081	556
75	SEG42	1026	556
76	SEG43	971	556
77	SEG44	916	556
78	SEG45	861	556
79	SEG46	806	556
80	SEG47	751	556
81	SEG48	696	556
82	SEG49	641	556
83	SEG50	586	556
84	SEG51	531	556
85	SEG52	476	556
86	SEG53	421	556
87	SEG54	366	556
88	SEG55	311	556
89	SEG56	256	556
90	SEG57	201	556
91	SEG58	146	556
92	SEG59	91	556
93	SEG60	36	556
94	SEG61	-19	556
95	SEG62	-74	556
96	SEG63	-129	556
97	SEG64	-184	556
98	SEG65	-239	556
99	SEG66	-294	556
100	SEG67	-349	556
101	SEG68	-404	556
102	SEG69	-459	556
103	SEG70	-514	556
104	SEG71	-569	556
105	SEG72	-624	556

PAD No.	Pin Name	X	Y
106	SEG73	-679	556
107	SEG74	-734	556
108	SEG75	-789	556
109	SEG76	-844	556
110	SEG77	-899	556
111	SEG78	-954	556
112	SEG79	-1009	556
113	SEG80	-1064	556
114	SEG81	-1119	556
115	SEG82	-1174	556
116	SEG83	-1229	556
117	SEG84	-1284	556
118	SEG85	-1339	556
119	SEG86	-1394	556
120	SEG87	-1449	556
121	SEG88	-1504	556
122	SEG89	-1559	556
123	SEG90	-1614	556
124	SEG91	-1669	556
125	SEG92	-1724	556
126	SEG93	-1779	556
127	SEG94	-1834	556
128	SEG95	-1889	556
129	SEG96	-1944	556
130	SEG97	-1999	556
131	SEG98	-2054	556
132	SEG99	-2109	556
133	SEG100	-2164	556
134	SEG101	-2219	556
135	SEG102	-2274	556
136	SEG103	-2329	556
137	SEG104	-2384	556
138	SEG105	-2439	556
139	SEG106	-2494	556
140	SEG107	-2549	556

PAD No.	Pin Name	X	Y
141	SEG108	-2604	556
142	SEG109	-2659	556
143	SEG110	-2714	556
144	SEG111	-2769	556
145	SEG112	-2824	556
146	SEG113	-2879	556
147	SEG114	-2934	556
148	SEG115	-2989	556
149	SEG116	-3044	556
150	SEG117	-3099	556
151	SEG118	-3154	556
152	SEG119	-3209	556
153	SEG120	-3264	556
154	SEG121	-3319	556
155	SEG122	-3374	556
156	SEG123	-3429	556
157	SEG124	-3484	556
158	SEG125	-3539	556
159	SEG126	-3594	556
160	SEG127	-3649	556
161	Reserve	-3704	556
162	Reserve	-3759	556
163	Reserve	-3814	556
164	Reserve	-3869	556
165	COM64	-3924	556
166	COM65	-3979	556
167	COM66	-4034	556
168	COM67	-4089	556
169	COM68	-4144	556
170	COM69	-4199	556
171	COM70	-4254	556
172	COM71	-4309	556
173	COM72	-4364	556
174	COM73	-4419	556
175	COM74	-4474	556

PAD No.	Pin Name	X	Y
176	COM75	-4529	556
177	COM76	-4584	556
178	COM77	-4639	556
179	COM78	-4694	556
180	COM79	-4749	556
181	COM80	-4804	556
182	COM81	-4859	556
183	COM82	-4914	556
184	COM83	-4969	556
185	COM84	-5024	556
186	COM85	-5079	556
187	COM86	-5134	556
188	COM87	-5189	556
189	COM88	-5244	556
190	COM89	-5299	556
191	COM90	-5354	556
192	COM91	-5409	556
193	COM92	-5464	556
194	COM93	-5519	556
195	COM94	-5574	556
196	COM95	-5629	556
197	COM96	-6234	550
198	COM97	-6234	495
199	COM98	-6234	440
200	COM99	-6234	385
201	COM100	-6234	330
202	COM101	-6234	275
203	COM102	-6234	220
204	COM103	-6234	165
205	COM104	-6234	110
206	COM105	-6234	55
207	COM106	-6234	0
208	COM107	-6234	-55
209	COM108	-6234	-110
210	COM109	-6234	-165

PAD No.	Pin Name	X	Y
211	COM110	-6234	-220
212	COM111	-6234	-275
213	COM112	-6234	-330
214	COM113	-6234	-385
215	COM114	-6234	-440
216	COM115	-6234	-495
217	COM116	-6234	-550
218	COM117	-5418	-556
219	COM118	-5363	-556
220	COM119	-5308	-556
221	COM120	-5253	-556
222	COM121	-5198	-556
223	COM122	-5143	-556
224	COM123	-5088	-556
225	COM124	-5033	-556
226	COM125	-4978	-556
227	COM126	-4923	-556
228	COM127	-4868	-556
229	COMS2	-4813	-556
230	T9	-4729	-574
231	VDD	-4654	-574
232	PS0	-4579	-574
233	PS1	-4504	-574
234	PS2	-4429	-574
235	VSS	-4354	-574
236	CSB	-4279	-574
237	CSB	-4204	-574
238	RST	-4129	-574
239	RST	-4054	-574
240	A0	-3979	-574
241	A0	-3904	-574
242	RW_WR	-3829	-574
243	RW_WR	-3754	-574
244	E_RD	-3679	-574
245	E_RD	-3604	-574

PAD No.	Pin Name	X	Y
246	D0	-3529	-574
247	D0	-3454	-574
248	D1	-3379	-574
249	D1	-3304	-574
250	D2	-3229	-574
251	D2	-3154	-574
252	D3	-3079	-574
253	D3	-3004	-574
254	D4	-2929	-574
255	D4	-2854	-574
256	D5	-2779	-574
257	D5	-2704	-574
258	D6	-2629	-574
259	D6	-2554	-574
260	D7	-2479	-574
261	D7	-2404	-574
262	VDD	-2329	-574
263	VDD	-2254	-574
264	VDD	-2179	-574
265	VDD	-2104	-574
266	VDD	-2029	-574
267	VDD	-1954	-574
268	VDD2	-1879	-574
269	VDD2	-1804	-574
270	VDD2	-1729	-574
271	VDD2	-1654	-574
272	VDD2	-1579	-574
273	VDD2	-1504	-574
274	VDD2	-1429	-574
275	VDD2	-1354	-574
276	VDD2	-1279	-574
277	VDD2	-1204	-574
278	VDD2	-1129	-574
279	VDD2	-1054	-574
280	VDD2	-979	-574

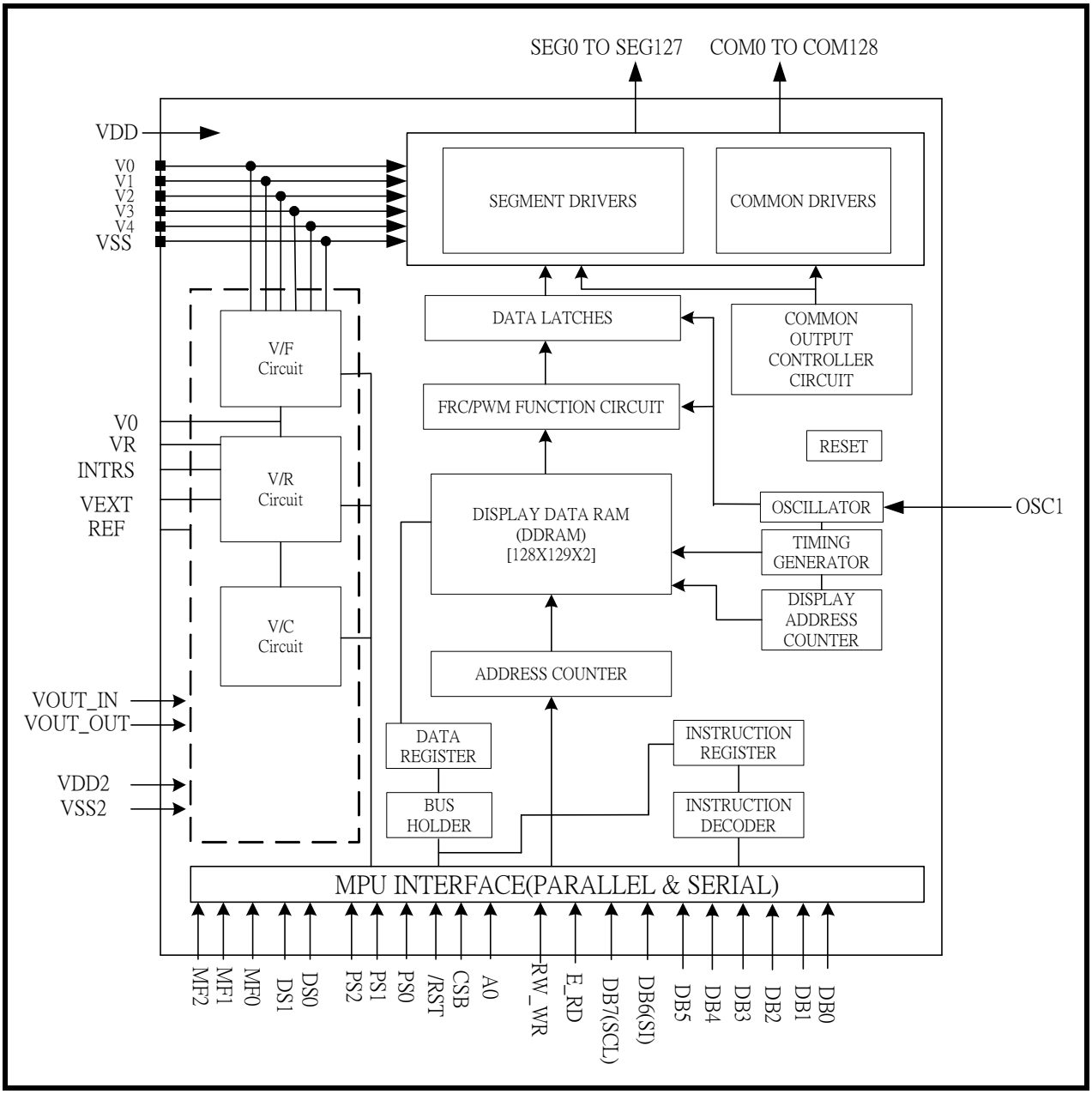
PAD No.	Pin Name	X	Y
281	VDD2	-904	-574
282	VDD2	-829	-574
283	VDD2	-754	-574
284	VSS2	-679	-574
285	VSS2	-604	-574
286	VSS2	-529	-574
287	VSS2	-454	-574
288	VSS2	-379	-574
289	VSS2	-304	-574
290	VSS2	-229	-574
291	VSS2	-154	-574
292	VSS2	-79	-574
293	VSS2	-4	-574
294	VSS2	71	-574
295	VSS2	146	-574
296	VSS2	221	-574
297	VSS2	296	-574
298	VSS2	371	-574
299	VSS2	446	-574
300	VSS	521	-574
301	VSS	596	-574
302	VSS	671	-574
303	VSS	746	-574
304	VSS	821	-574
305	VSS	896	-574
306	TA	971	-574
307	TB	1046	-574
308	MF2	1121	-574
309	MF1	1196	-574
310	MF0	1271	-574
311	DS0	1346	-574
312	DS1	1421	-574
313	VDD	1496	-574
314	VOUT_OUT	1571	-574
315	VOUT_OUT	1646	-574

PAD No.	Pin Name	X	Y
316	VOUT_OUT	1721	-574
317	VOUT_OUT	1796	-574
318	VOUT_OUT	1871	-574
319	VOUT_OUT	1946	-574
320	VOUT_IN	2021	-574
321	VOUT_IN	2096	-574
322	VOUT_IN	2171	-574
323	VOUT_IN	2246	-574
324	VOUT_IN	2321	-574
325	VOUT_IN	2396	-574
326	T[8]	2471	-574
327	T[7]	2546	-574
328	T[6]	2621	-574
329	T[5]	2696	-574
330	T[4]	2771	-574
331	T[3]	2846	-574
332	T[2]	2921	-574
333	T[1]	2996	-574
334	T[0]	3071	-574
335	VDD	3146	-574
336	REF	3221	-574
337	VSS	3296	-574
338	VEXT	3371	-574
339	VDD	3452	-574
340	INTRS	3527	-574
341	VSS	3602	-574
342	OSC1	3677	-574
343	OSC1	3752	-574
344	VDD	3827	-574
345	VR	3902	-574
346	VR	3977	-574
347	V4	4052	-574
348	V3	4127	-574
349	V2	4202	-574
350	V1	4277	-574

PAD No.	Pin Name	X	Y
351	V0	4352	-574
352	V0	4427	-574
353	COM63	5340	-556
354	COM62	5395	-556
355	COM61	5450	-556
356	COM60	5505	-556
357	COM59	5560	-556
358	COM58	5615	-556
359	COM57	5670	-556
360	COM56	5725	-556
361	COM55	5780	-556
362	COM54	5835	-556
363	COM53	5890	-556
364	COM52	5945	-556
365	COM51	6234	-550
366	COM50	6234	-495
367	COM49	6234	-440
368	COM48	6234	-385

PAD No.	Pin Name	X	Y
369	COM47	6234	-330
370	COM46	6234	-275
371	COM45	6234	-220
372	COM44	6234	-165
373	COM43	6234	-110
374	COM42	6234	-55
375	COM41	6234	0
376	COM40	6234	55
377	COM39	6234	110
378	COM38	6234	165
379	COM37	6234	220
380	COM36	6234	275
381	COM35	6234	330
382	COM34	6234	385
383	COM33	6234	440
384	COM32	6234	495
385	COM31	6234	550

BLOCK DIAGRAM



PIN DESCRIPTION

POWER SUPPLY

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>VDD</td><td>Power</td><td>Digital Power supply</td></tr>
<tr><td>VSS</td><td>Power</td><td>Ground</td></tr>
<tr><td>VDD2</td><td>Power</td><td>Analog Power supply</td></tr>
<tr><td>VSS2</td><td>Power</td><td>Ground</td></tr>
<tr><td>VOUT_OUT</td><td>Power</td><td>Internal booster output. Left these pads open when using external power supply.
Short VOUT_OUT with VOUT_IN when using internal booster.</td></tr>
<tr><td>VOUT_IN</td><td>Power</td><td>The power supply pads of internal regulator. Apply high voltage here for internal regulator.
If using external booster, VOUT_OUT must be open with internal booster programmed OFF (set register VC=0).
If using internal booster, short VOUT_OUT with VOUT_IN together.</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>Power</td><td>LCD driver supply voltages. V1, V2, V3, V4 need the capacitor between with VSS.
Voltages should have the following relationship:
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
NOTE: N = 5 to 12</td></tr>
</table>

LCD DRIVER SUPPLY

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjustment pin
It is valid only when on-chip resistors are not used (INTRS = "L")
When using internal resistors (INTRS = "H"), open this pin</td></tr>
<tr><td>REF</td><td>I</td><td>Selects the external VREF voltage via the VEXT pin
REF = “H”: using the internal VREF
REF = “L”: using the external VREF</td></tr>
<tr><td>VEXT</td><td>I</td><td>Externally input reference voltage (VREF) for the internal voltage regulator
It is valid only when REF is "L"
When using internal voltage regulator, this pin must be open</td></tr>
<tr><td>OSC1</td><td>I</td><td>External OSC input pin, when using internal clock oscillator, connect OSC1 to VDD.</td></tr>
</table>

SYSTEM CONTROL

Name	Type	Description
INTRS	I	Internal resistor select pin. This pin selects the resistors for adjusting V0 voltage level. INTRS = "H": use the internal resistors. INTRS = "L": use the external resistors. VR pin and external resistive divider control V0 voltage
T[0] ~ T[9]	Test	Test pins. Don' t use these pins. Please Open these pins.
Reserve	X	This pin must be OPEN
MF[2:0]	I	Manufacturer ID code for reference, suggest set to [MF2.MF1.MF0 = 0.0.0]
DS[1:0]	I	Display size ID code for reference, suggest set to [DS1.DS0 = 0.0]
TA, TB	I	Test pins TA and TB must connect to Vss.

MICROPROCESSOR INTERFACE

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin. When RST is “L”, initialization is executed.</td></tr>
<tr><td>PS[2:0]</td><td>I</td><td>Microprocessor interface select input pin
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>Interface mode</th><th>A0</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Parallel 80</td><td>A0</td><td>DB[7:0]</td><td>/RD, /WR</td><td>-</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Parallel 68</td><td>A0</td><td>DB[7:0]</td><td>E, R/W</td><td>-</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>3Line Serial</td><td>-</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>4Line Serial</td><td>A0</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>IIC Serial</td><td>-</td><td>SDA</td><td>Read/Write</td><td>SCL</td></tr>
</table>
NOTE:
*1. Reading of data or status is not available in serial interface modes (4-Line, 3-Line and IIC).
*2. In 3-Line or 4-Line interface: DB[5:0], E_RD and RW_WR must be fixed to “H” or “L”.
*3. In IIC and 3-Line interface: A0 must be fixed to “H” or “L”.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input. Data/instruction I/O is enabled only when CSB is "L".
When chip select is non-active, DB[7:0] will be high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register selection input.
A0 = "H": DB[7:0] are display data.
A0 = "L": DB[7:0] are control instruction.</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>PS1</th><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>R/W</td><td>Read / Write control input pin.
R/W = “H” : read;
R/W = “L” : write.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin.
The data on DB[7:0] are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
</table>

MICROPROCESSOR INTERFACE (continued)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>PS1</th><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin.
R/W = “H”: When E is “H”, DB[7:0] are in an output status;
R/W = “L”: DB[7:0] are latched at the falling edge of this signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin.
When /RD is “L”, DB[7:0] are in output status.</td></tr>
</table></td></tr>
<tr><td rowspan="3">DB[7:0]</td><td rowspan="3">I/O</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When chip select is not active (CSB=H), DB[7:0] will be high impedance.</td></tr>
<tr><td>When the 3-Line/4-Line serial interface is selected (PS[2:0] = "000" or “010”):
DB[0:5]: high impedance (connect to “H” or “L”);
DB6: serial input clock (SCLK);
DB7: serial input data (SID).
When chip select is not active, DB[7:0] is high impedance.</td></tr>
<tr><td>When the IIC serial interface is selected (PS[2:0] = "100"):
DB7: serial clock input (SCL);
DB[6:4]: serial data input (SDA_IN);
DB[3:2]: serial data output (SDA_OUT). For acknowledge signal output in IIC interface;
DB[1:0]: Is slave address (SA) bit1, 0, must connect to Vdd or Vss.
*DB[6:2]: must be connected together as SDA signal of IIC interface.</td></tr>
</table>

Note:

1. By connecting SDA_IN and SDA_OUT externally, the SDA line becomes fully IIC interface compatible. Separating acknowledge-output from serial data input is advantageous for chip-on-glass (COG) applications. In COG applications, the ITO resistance and the pull-up resistor will form a voltage divider which affects acknowledge-signal level. Larger ITO resistance will raise the acknowledge-signal level and system cannot recognize this level as a valid logic “0” level. By separating SDA_IN from SDA_OUT, the IC can be used in a mode which ignores the acknowledge-bit. For applications which check acknowledge-bit, it is necessary to minimize the ITO resistance of the SDA_OUT trace to guarantee a valid low level.
2. After VDD is turned ON, any MPU interface pins cannot be left floating.

LCD DRIVER OUTPUTS

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG127</td><td>O</td><td>LCD segment driver outputs.
The display data and frame signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">Frame</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>-</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>+</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>-</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF, Power Saving</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM127</td><td>O</td><td>LCD common driver outputs.
The scan signal and frame signal control the output voltage of common driver.
<table>
<tr><th>Scan Data</th><th>Frame</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>+</td><td>VSS</td></tr>
<tr><td>H</td><td>-</td><td>V0</td></tr>
<tr><td>L</td><td>+</td><td>V1</td></tr>
<tr><td>L</td><td>-</td><td>V4</td></tr>
<tr><td colspan="2">Display OFF, Power Saving</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS
(COMS1,2)</td><td>O</td><td>Common output for the icons.
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

Recommend ITO Resistance

PIN Name	ITO Resistance
PS[2:0], REF, OCS1, INTRS, TA, TB	No Limitation
T[9:0], VR, VEXT	Floating
Vdd, Vdd2, Vss, Vss2 , VOUT_IN , VOUT_OUT	<100Ω
SDA (SDA_IN & SDA_OUT)*1	<300Ω
CSB , E , R/W , A0 , DB[7:0]*1	<1KΩ
V0, V1 , V2 , V3 , V4	<500Ω
RST	<10KΩ

Note:

1. If using IIC interface mode, the resistance of SDA signal should be lower than 300Ω (if the system pull up resistor is 4.7KΩ).
2. The option setting to be “H” should connect to VDD.
3. The option setting to be “L” should connect to VSS.

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The ST7541 can interface with an MPU when CSB is "L". When these pins are set to any other combination, A0, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

ST7541 has five types of interface with an MPU, which are three serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table 1.

Table 1 Parallel / Serial Interface Mode

Type	PS2	PS1	PS0	CSB	Interface mode
Parallel	L	H	H	CSB	6800-series MPU mode
	L	L			8080-series MPU mode
Serial	L	L	L	CSB	3-Line SPI mode
	L	H		CSB	4-Line SPI mode
	H	L		CSB	IIC SPI mode

Parallel Interface (PS0 = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in Table 2. The type of data transfer is determined by signals at A0, E_RD and RW_WR as shown in Table **3**.

Table 2 Microprocessor Selection for Parallel Interface

PS1	CSB	A0	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CSB	A0	E	R/W	DB0 to DB7	6800-series
L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E_RD (E)	RW_WR (R/W)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When E_RD pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0, RW_WR as in case of 6800-series mode.

Serial Interface

Serial mode	PS0	PS1	PS2	CSB	A0
3-Line SPI mode	L	L	L	CSB	No used
4-Line SPI mode	L	H	L	CSB	Used
IIC SPI mode	L	L	H	CSB	No Used

If A0 is not used it must be fixed either “H” or “L”

3-Line / 4-Line (PS[2:0] = "000" or “010”)

3-Line and 4-Line serial interface are similar except the display data/command indication is controlled by commands (3-Line SPI mode) or by the register selection pin (A0, 4-Line SPI mode).

When ST7541 is active (CSB=“L”), serial data (DB7) and serial clock (DB6) inputs are enabled. When ST7541 is not active (CSB=“H”), the internal 8-bit shift register and 3-bit counter are reset. The read operation is not supported in these modes. Serial data on SID is latched at the rising edge of serial clock on SCL. After the 8th serial clock, the serial input data on SID will be processed as 8-bit parallel data/command. When writing sequential display data, the DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

4-Line SPI Mode (PS0 = "L", PS1 = "H", PS2 = "L")

This mode uses A0 pin to indicate the input serial data on SID is display data (A0=“H”) or command (A0=“L”).

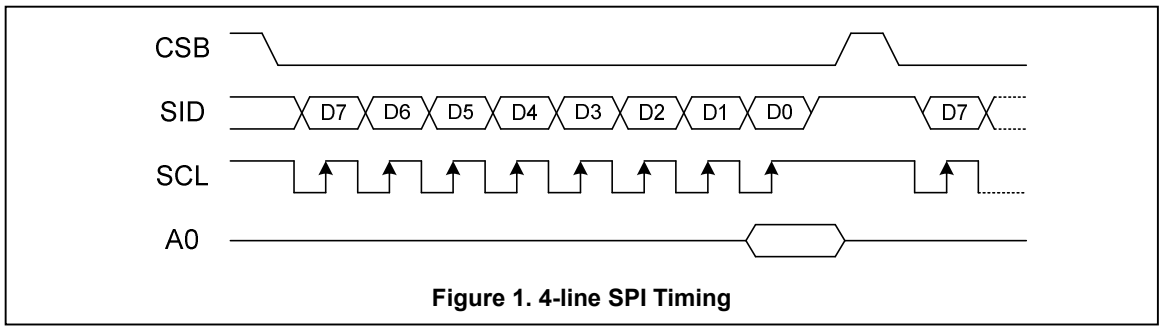


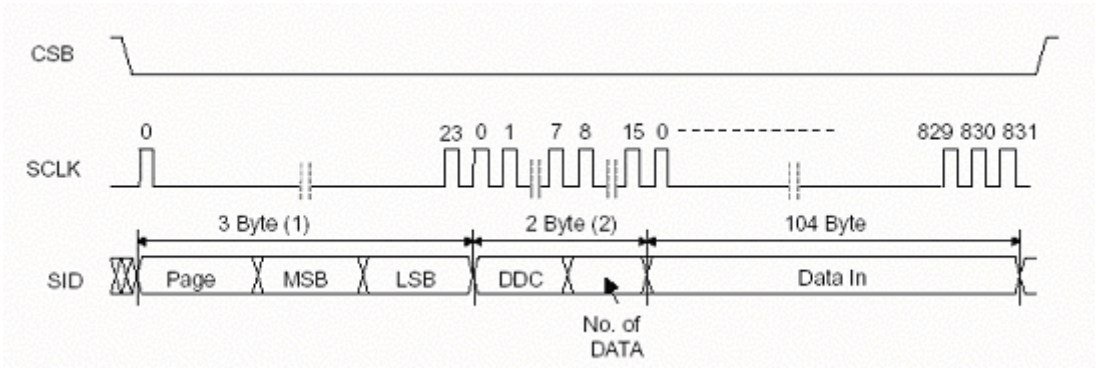
Figure 1. 4-line SPI Timing

3-Line SPI Mode (PS0 = "L", PS1 = "L" ,PS2= "L")

This mode does not have an A0 pin to indicate the input serial data on SID is display data or command. The default input from MCU is command. The display data/command indication is controlled via software. The MCU send 2-byte command (**Set Data Direction & Display Data Length**) before the display data(s). These 2 commands are only used in 3-Line SPI mode.

The first command “Set Data Direction” (11101000b) indicates MCU wants to transfer display data. The second command “Display Data Length” informs LCD driver the number of input data bytes. After receiving these two continuous commands, the following messages will be treated as display data rather than command. After the display data string is sent over, the following bytes are treated as commands (unless receiving another pair of **Set Data Direction & Display Data Length** commands). If data transfer is stopped during transmitting, it is not valid data. New data will be transferred serially with most significant bit first.

NOTE: In spite of transmission of data, if CSB is disabled, the state will be terminated abnormally and next state is initialized.



(1) Set Page and Column Address:

Action	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set **Page** Address	1	0	1	1	P3	P2	P1	P0
Set Column Address **MSB**	0	0	0	1	0	Y7	Y6	Y5
Set Column Address **LSB**	0	0	0	0	Y4	Y3	Y2	Y1

(2) Set Data Direction and Set Display Data Length:

Action	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set Data Direction (**DDC**) (3-Line SPI mode Only)	1	1	1	0	1	0	0	0
Set Display Data Length (**No. of DATA**)	D7	D6	D5	D4	D3	D2	D1	D0

(3) This figure is example for 104 Data bytes to be transferred.

Figure 2. 3-Line SPI Timing (A0 is not used)

IIC Interface (PS0 = "L", PS1 = "L", PS2= "H")

IIC Interface uses two signals (Serial Data: SDA and Serial Clock: SCL) to communicate with MPU and other ICs or modules. It receives the command and data sent by MPU through SDA and SCL. Both SDA and SCL must connect to VDD by a pull-up resistor which drives SDA and SCL to “HIGH” when the bus is not busy. Data transfer can be initiated only when the bus is not busy. This interface supports writing command/data and reading acknowledge-bit.

[BIT TRANSFER]

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes on SDA while SCL is “HIGH” will be interpreted as START or STOP. Bit transfer is illustrated in Figure 3.

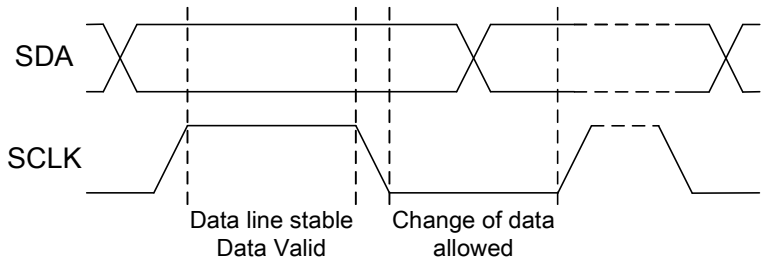


Figure 3. Bit transfer

[START AND STOP CONDITIONS]

When the bus is not busy, both SDA and SCL lines remain HIGH. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 4.

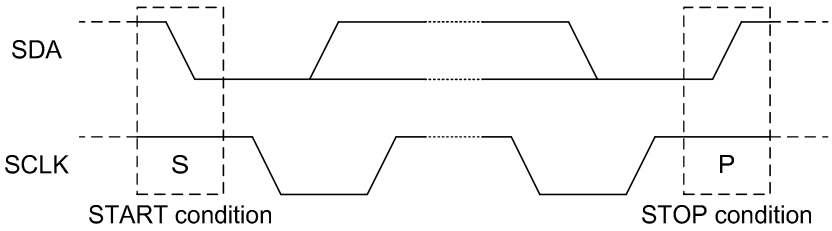


Figure 4. Definition of START and STOP conditions

[SYSTEM CONFIGURATION]

The system configuration is illustrated in Figure 5 and some word-definitions are explained below:

- Transmitter: the device, which sends the data to the bus.
- Receiver: the device, which receives the data from the bus.
- Master: the device, which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

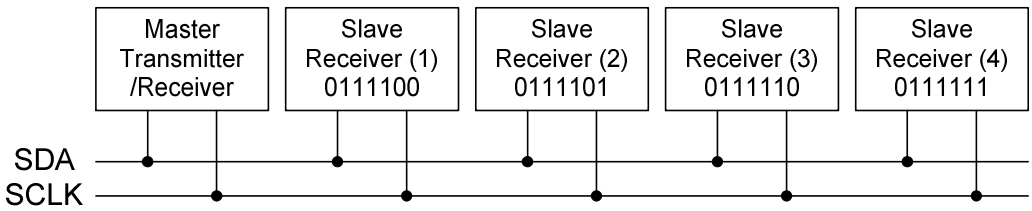


Figure 5. System configuration

[ACKNOWLEDGE]

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit, after the reception of each byte. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). Acknowledgement on the IIC Interface is illustrated in Figure 6.

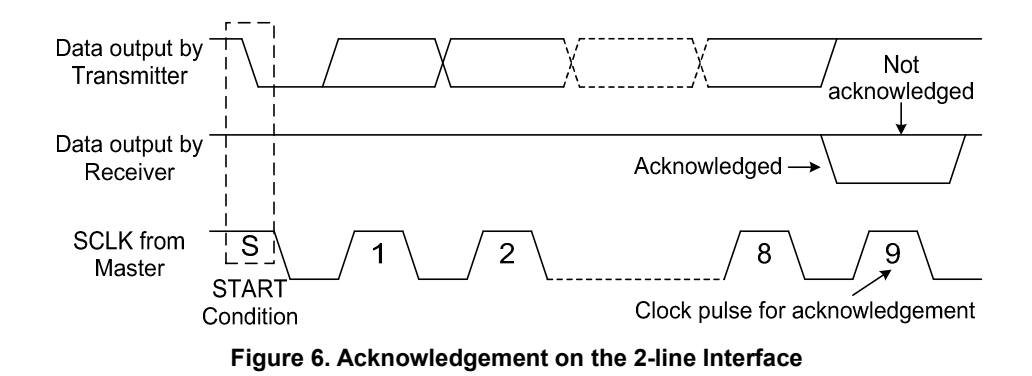


Figure 6. Acknowledgement on the 2-line Interface

[IIC INTERFACE PROTOCOL]

The IIC interface of ST7541 supports writing command/data to the addressed slaves on the bus. Before transferring any data on the bus, the target device(s) should be addressed first. Four slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for ST7541. The least significant 2 bits of the slave address is configured by connecting the inputs SA1 and SA0 to either logic 0 (VSS) or logic 1 (VDD). The IIC Interface protocol is illustrated in Figure 7.

The IIC communication sequence is initiated with a START condition (S) set by the master, and then followed by a slave address. All slaves with the same specified address should acknowledge in parallel, all the others will ignore the bus transfer. After the acknowledgement of the slave address, one or more command words are followed. The command word(s) define the status of the addressed slaves. A command word consists of a control byte (which defines Co and A0) and a data byte. The last control byte is tagged with a cleared most significant bit (i.e. Co=0), and is followed by data byte(s) only. The A0 bit in the control byte defines whether the data byte(s) will be interpreted as command or as RAM data. Therefore, after the last control byte, either a series of display data bytes or a series of command data bytes may follow (depends on the A0 bit). If the A0 bit is set to 0, the command bytes will be decoded and execute. If the A0 bit of the last control byte is set to 1, the series of display data bytes will be stored in DDRAM. The data pointer is automatically increased by 1 after writing each byte of display data into DDRAM. The addressed slave makes the acknowledgement after receiving each byte of command or display data. At the end of transmission the bus master issues a STOP condition (P).

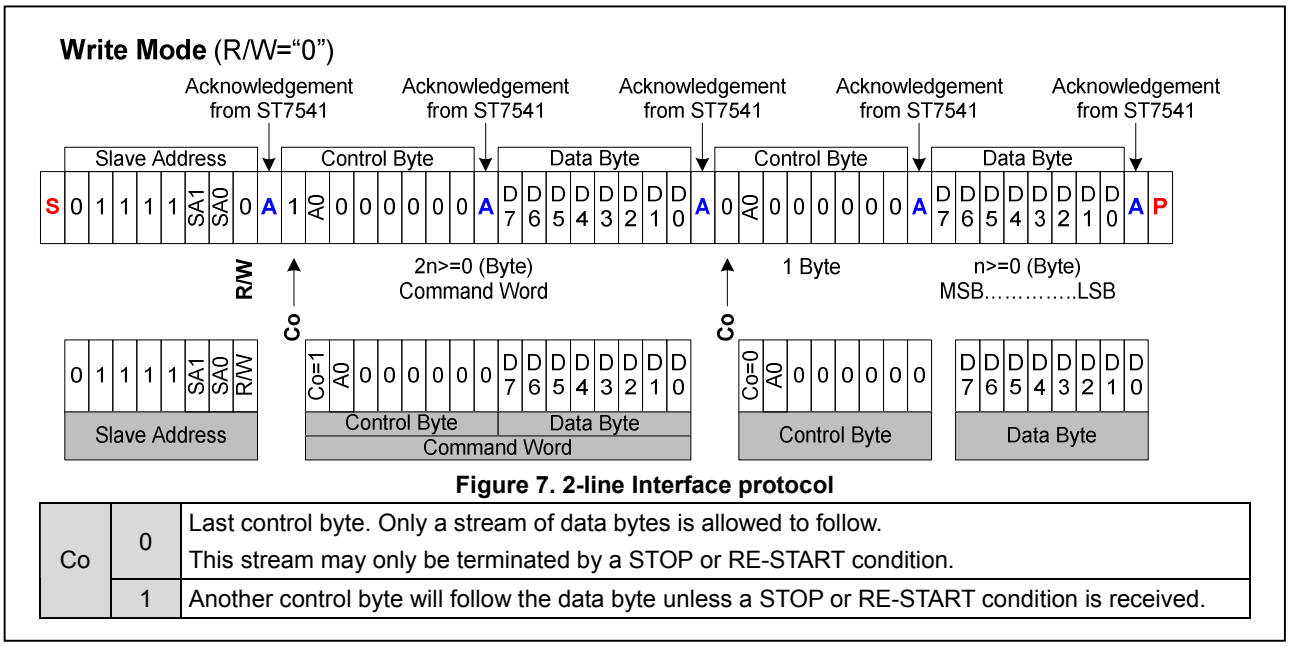


Figure 7. 2-line Interface protocol

Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

BUSY FLAG

The Busy Flag indicates whether the ST7541 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

DATA TRANSFER

The ST7541 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 8. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 9. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

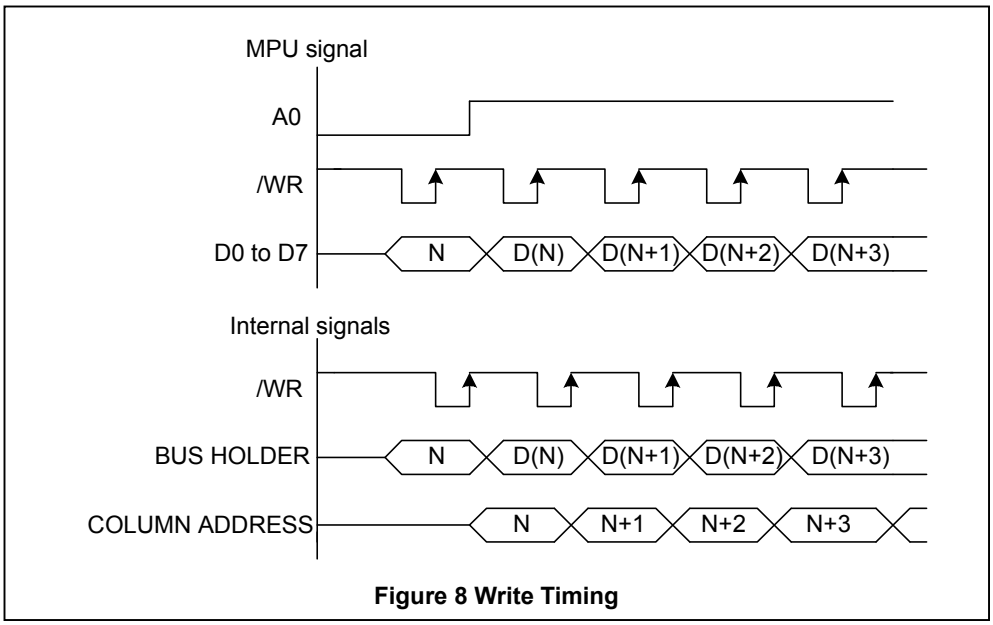


Figure 8 Write Timing

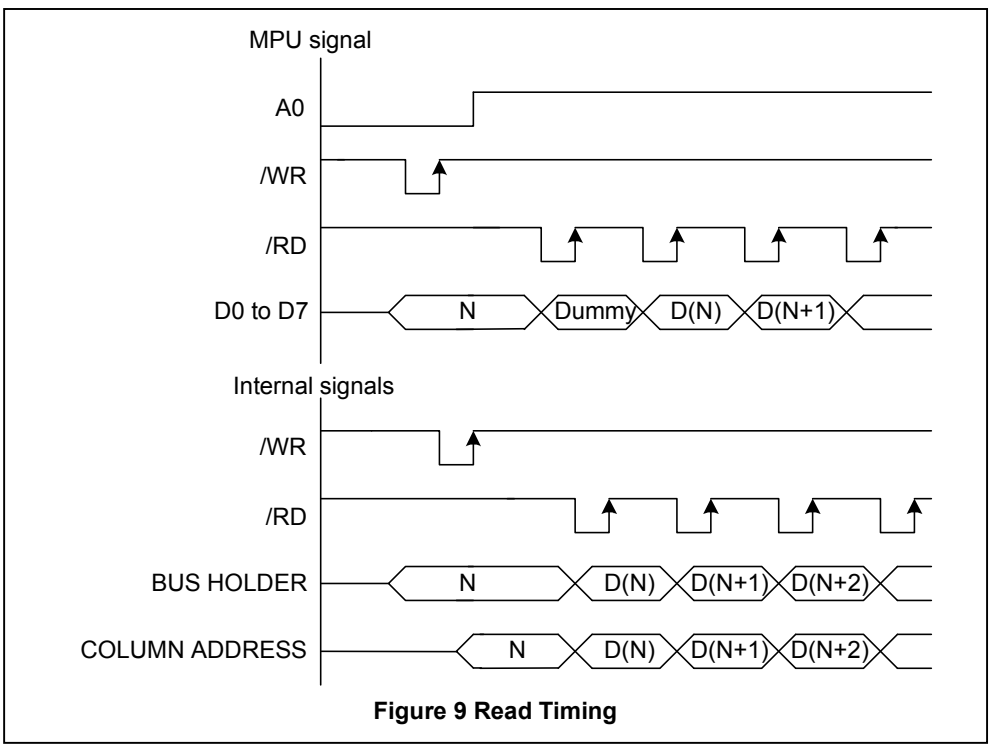


Figure 9 Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 129-row (17 pages by 8 bits) by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 15, and Page 16 is for Icon page.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Segment Control Circuit

This circuit controls the display data scan circuit. It allows the display data related commands (such as: Display ON/OFF, Reverse Display ON/OFF and Entire Display ON/OFF) without changing the data in the DDRAM.

Column Address Circuit

Command “Set Column Address MSB / LSB” will set 7-bit ([Y7:Y1]) of the internal column address and Y0 is set to “0”. The internal column address (Y[7:0]) is increased by 1 after accessing (read or write) each byte of display data (refer to Figure 10). After the 2nd access (read or write), the Column Address will point to the next column)

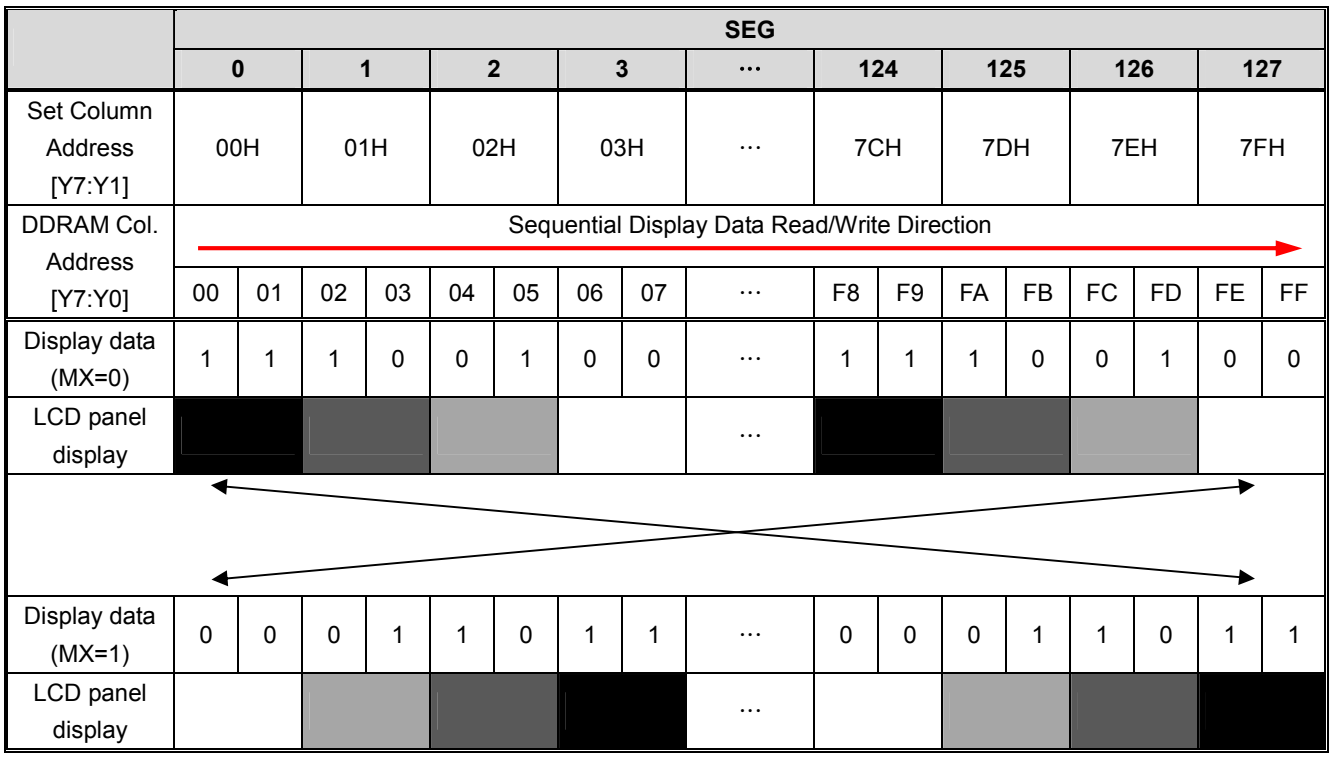


Figure 10 The Relationship between the Column Address and The Segment Outputs

LCD DISPLAY CIRCUITS

FRC (Frame Rate Control) and PWM (Pulse Width Modulation) Function Circuit

ST7541 incorporates FRC function and PWM circuits to display a 4-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. ST7541 provides palette-registers to assign the desired gray level. These registers are set by the instructions and the RST.

4FRC & 3FRC vs. 9PWM, 12PWM, 15PWM

– Gray Scale Table of 4 FRC (Frame Rate Control)

Gray scale level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)

– Gray Scale Table of 3 FRC (Frame Rate Control)

Gray scale level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	XXXX	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	XXXX	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	XXXX	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	XXXX	3rd FR (FR3)

– Gray Scale Table of PWM (Pulse Width Modulation)

Frame Parameter (FRn)			15-PWM		12-PWM		9-PWM	
Dec	Hex	4-bit	PWM width	Note	PWM width	Note	PWM width	Note
0	00	0000	0(0/15)	Brighter	0(0/12)	Brighter	0(0/9)	Brighter
1	01	0001	1/15	↑	1/12	↑	1/9	↑
2	02	0010	2/15		2/12		2/9	
3	03	0011	3/15		3/12		3/9	
4	04	0100	4/15		4/12		4/9	
5	05	0101	5/15		5/12		5/9	
6	06	0110	6/15		6/12		6/9	
7	07	0111	7/15		7/12		7/9	
8	08	1000	8/15		8/12		8/9	↓
9	09	1001	9/15		9/12		1(9/9)	Darker
10	0A	1010	10/15		10/12		0/9	This field is OFF level
11	0B	1011	11/15		11/12	↓		
12	0C	1100	12/15		1(12/12)	Darker		
13	0D	1101	13/15	↓	0/12	This field is OFF level		
14	0E	1110	14/15					
15	0F	1111	1(15/15)	Darker				

Oscillator

This is on-chip Oscillator without external resistor. When the internal oscillator is used, this pin must connect to VDD; when the external oscillator is used, this pin could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 11.

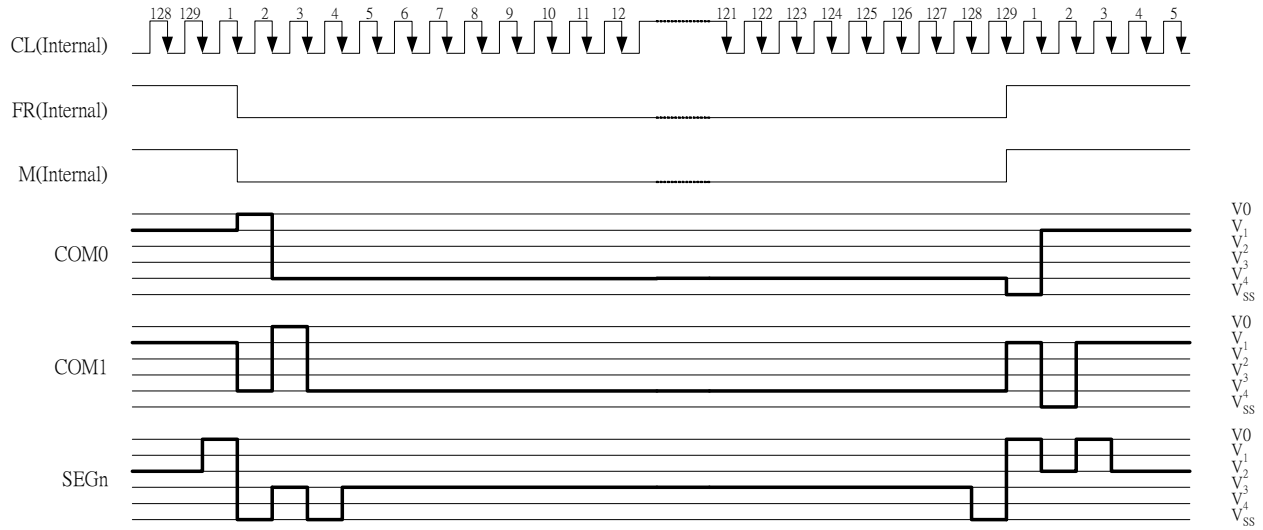


Figure 11 2-frame AC Driving Waveform (Duty Ratio: 1/129)

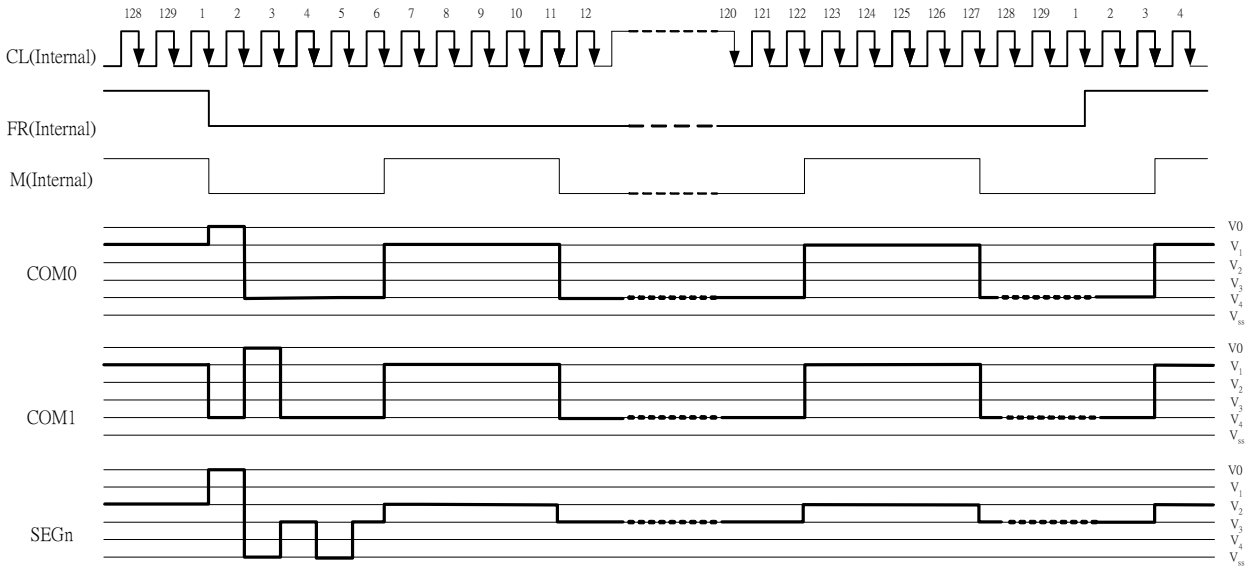
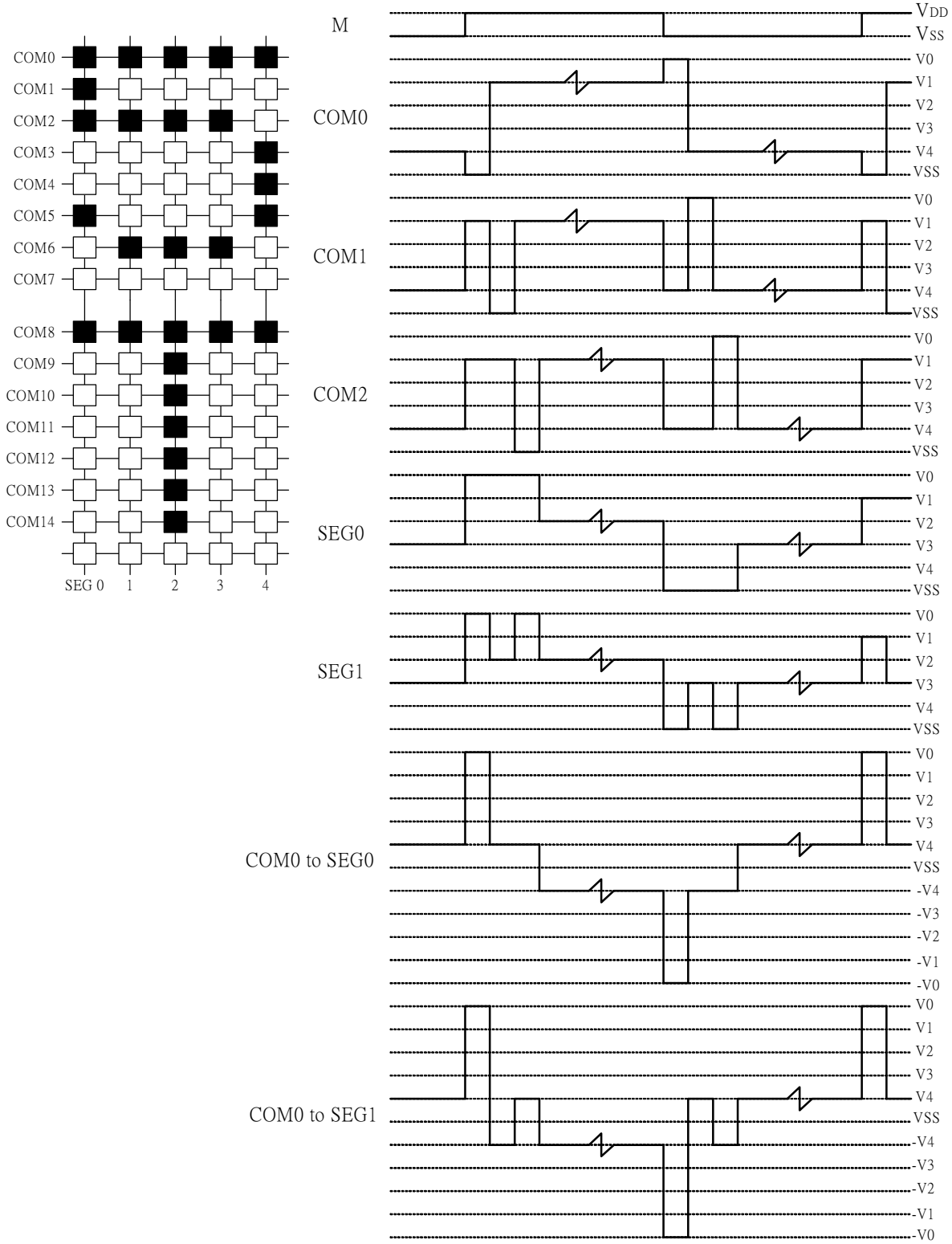


Figure 12 N-Line Inversion Driving Waveform (N=5,Duty Ratio=1/129)

LCD DRIVER CIRCUIT

This driver circuit is configured by 129-channel common drivers and 128-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.



Partial Display on LCD

ST7541 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages. The partial display duty ratio could be set from 16 ~ 128.

If the partial display region is out of the Max. Display range, it would be no operation.

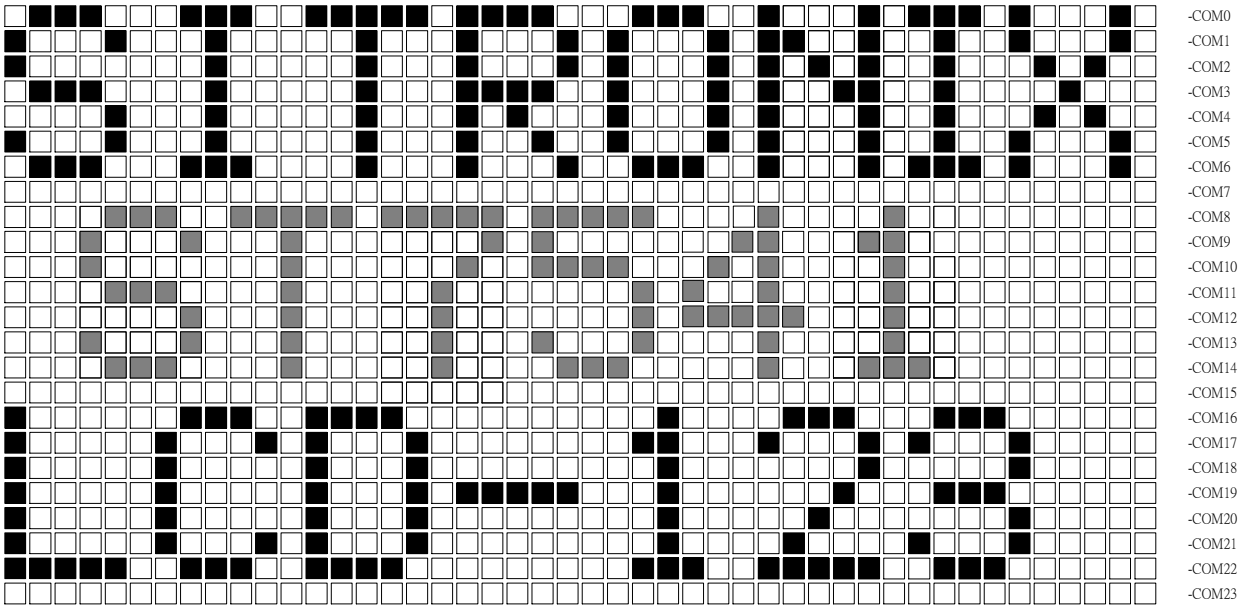


Figure 13 Reference Example for Partial Display

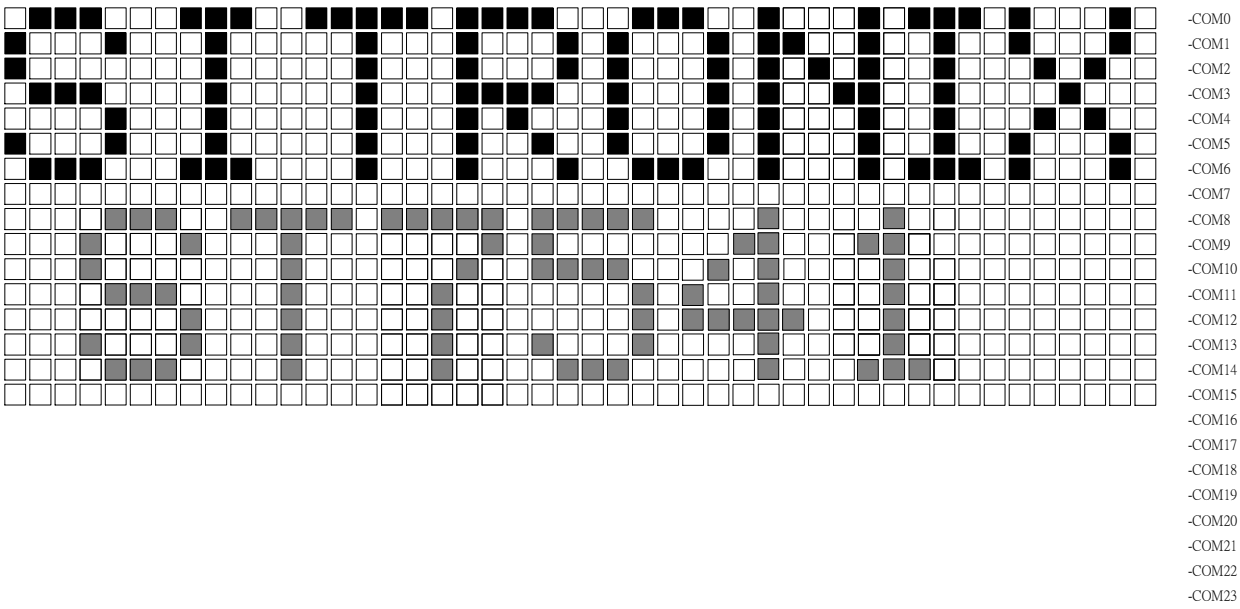


Figure 14 Partial Display (Partial Display Duty=16,initial COM0=0)

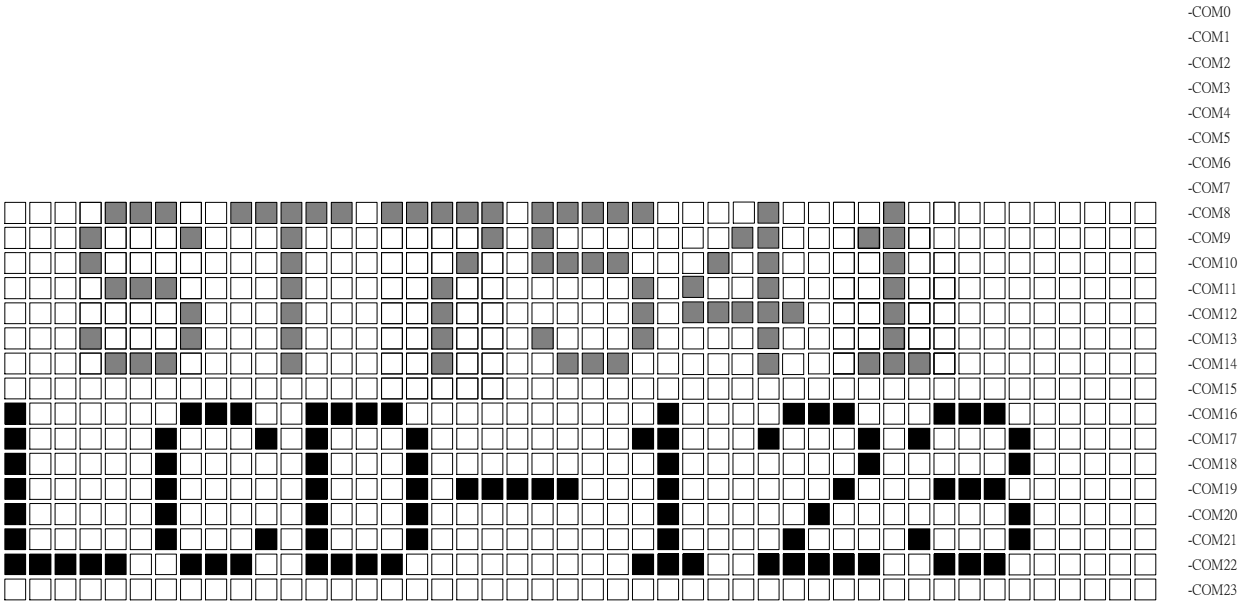


Figure 15 Moving Display (Partial Display Duty=16,Initial COM0=8)

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 4 shows the referenced combinations in using Power Supply circuits.

Table 4 Recommended Power Supply Combinations

Customer Power System	Power Control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT_IN	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Internal	Without capacitor	With capacitor
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Without capacitor	With capacitor
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	OPEN	External input	With capacitor
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	OPEN	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VDD2 and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by “Set DC-DC Step-up” instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

Note: we would like to recommend to use the external VOUT when the panel is large than 1.8 inch

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in Figure 16, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and VEV. The Ra and Rb are connected internally or externally by INTRS pin. And VEV called the voltage of electronic volume is determined by Eq. 2, where the parameter ˛ is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. VREF voltage at Ta= 25˚C is shown in Table 5.

$$V0 = (1 + Rb / Ra) \times VEV \quad [V] \ldots\ldots\ldots\ldots\ldots \text{(Eq. 1)}$$

$$VEV = (1 - (63 - \alpha) / 210) \times VREF \quad [V] \ldots\ldots\ldots\ldots\ldots \text{(Eq. 2)}$$

Table 5 VREF Voltage at Ta = 25°C

REF	Temp. coefficient	VREF [V]
1	-0.144% / ˚C	2.1
0	External input	VEXT

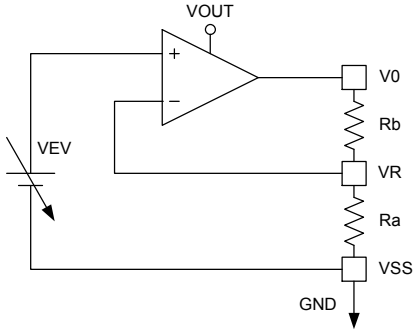


Figure 16 Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = “H”)

When INTRS pin is "H", resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 6 Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1 + (Rb / Ra)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Figure 17 Shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25°C.

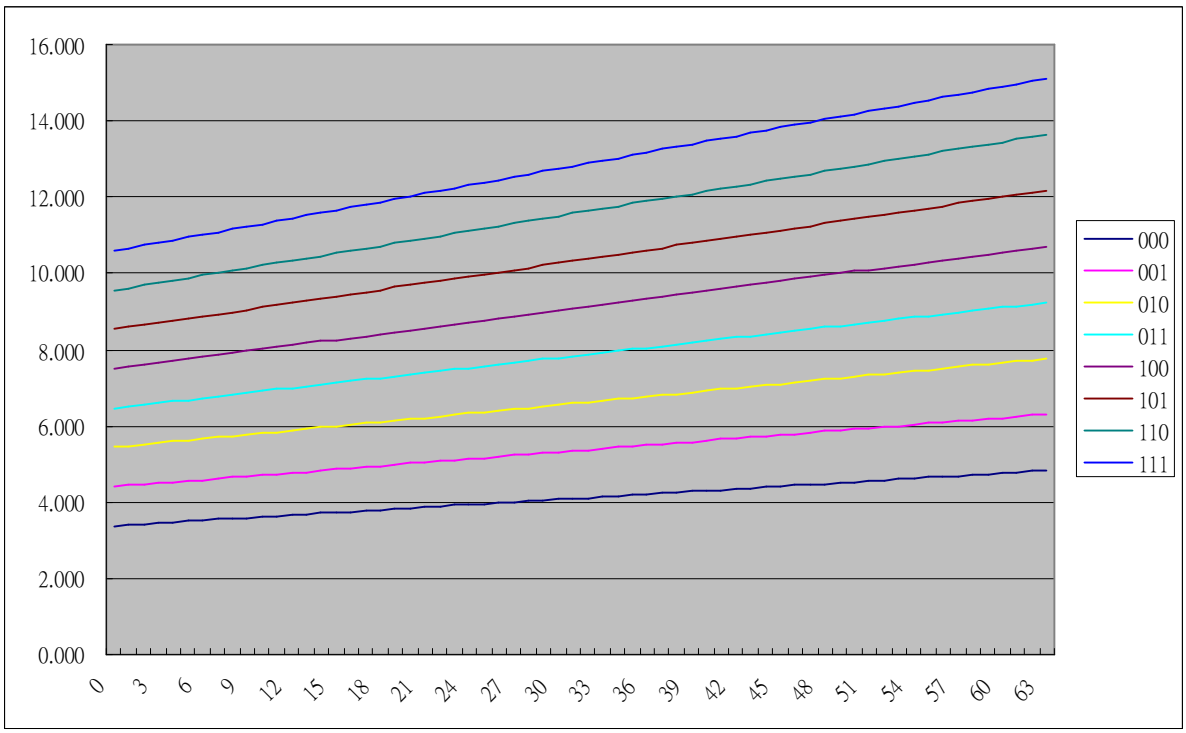


Figure 17 Electronic Volume Level (Temp. Coefficient = -0.144% / °C)

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1:

$$10 = (1 + Rb / Ra) \times VEV \quad [V] \ldots\ldots\ldots\ldots\ldots \text{(Eq. 3)}$$

From Eq. 2:

$$VEV = (1 - (63 - 32) / 210) \times 2.1 = 1.79 \quad [V] \ldots\ldots\ldots\ldots\ldots \text{(Eq. 4)}$$

From Requirement-3:

$$10 / (Ra + Rb) = 1 \quad [uA] \ldots\ldots\ldots\ldots\ldots \text{(Eq. 5)}$$

From Eq. 3~5:

$$Ra = 1.79 \quad [M\Omega]$$
$$Rb = 8.21 \quad [M\Omega]$$

Table 7 Shows the Range of V0 depending on the above Requirements.

Table 7 The Range of V0

	Electronic volume level				
	0	.....	32	.....	63
V0	8.21	.....	10.00	.....	11.73

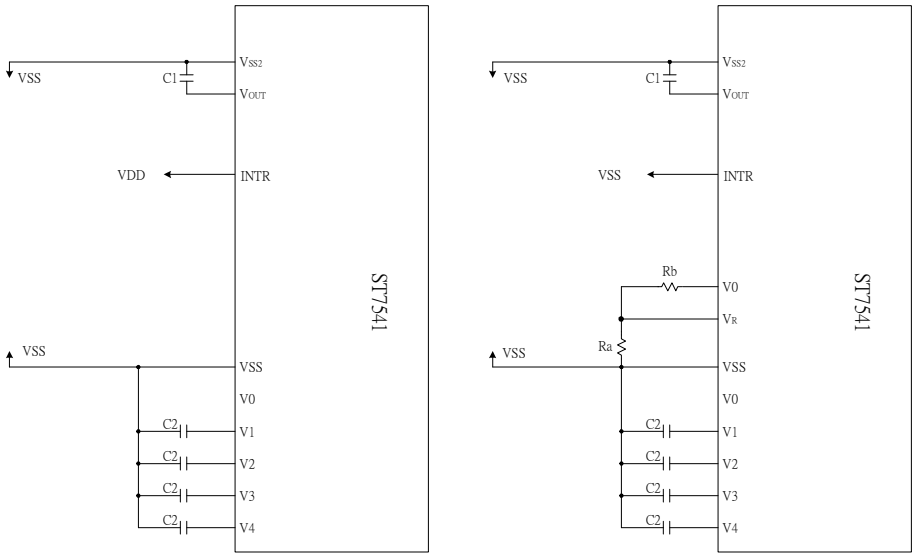
Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 8 shows the relationship between V1 to V4 level and each duty ratio.

Table 8 The Relationship between V1 to V4 Level and Each Duty Ratio

LCD bias	V1	V2	V3	V4	Remarks
1/N	(N-1)/N x V0	(N-2)/N x V0	2/N x V0	1/N x V0	N = 5 to 12

Follower Voltage Reference Circuit (Internal Booster & Regulator)

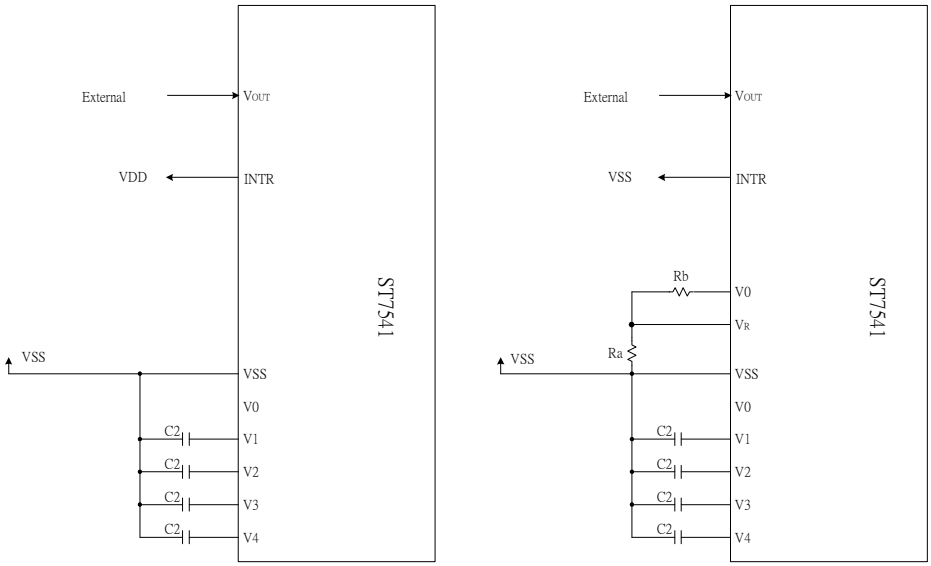


Left is using internal Resister

Right is using External Resister

C1= 1u F ~ 4.7u F , C2 = 0.1u F ~ 1u F (suggestion value: C1=1uF , C2=0.1uF)

Follower voltage reference circuit (External Vout & Internal Regulator)



Left is using internal Resister

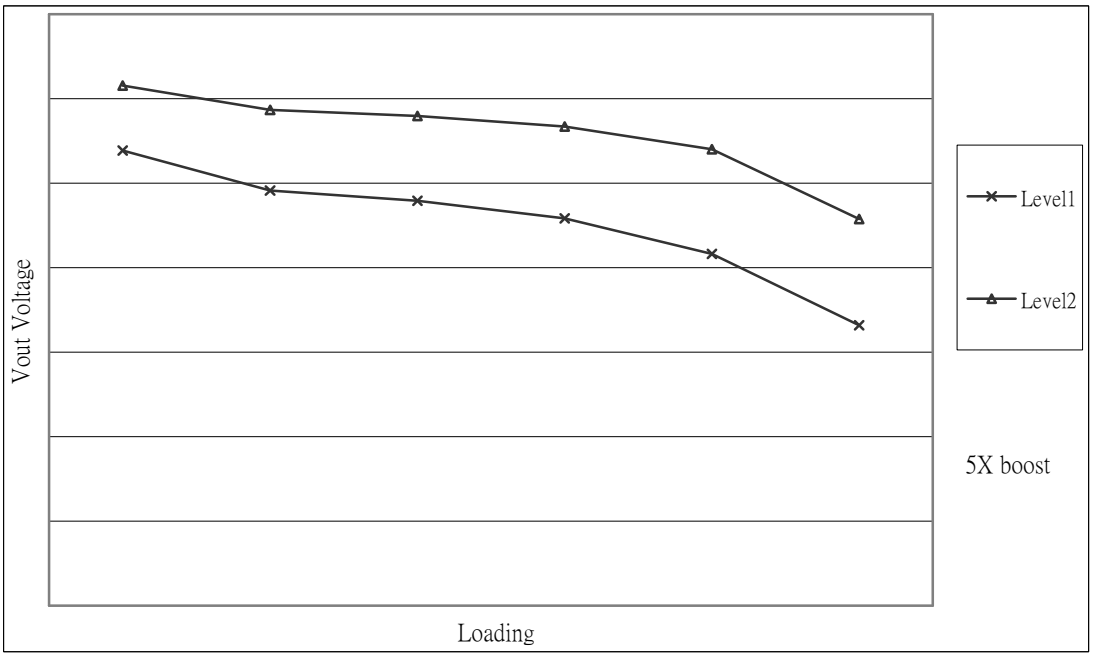
Right is using External Resister

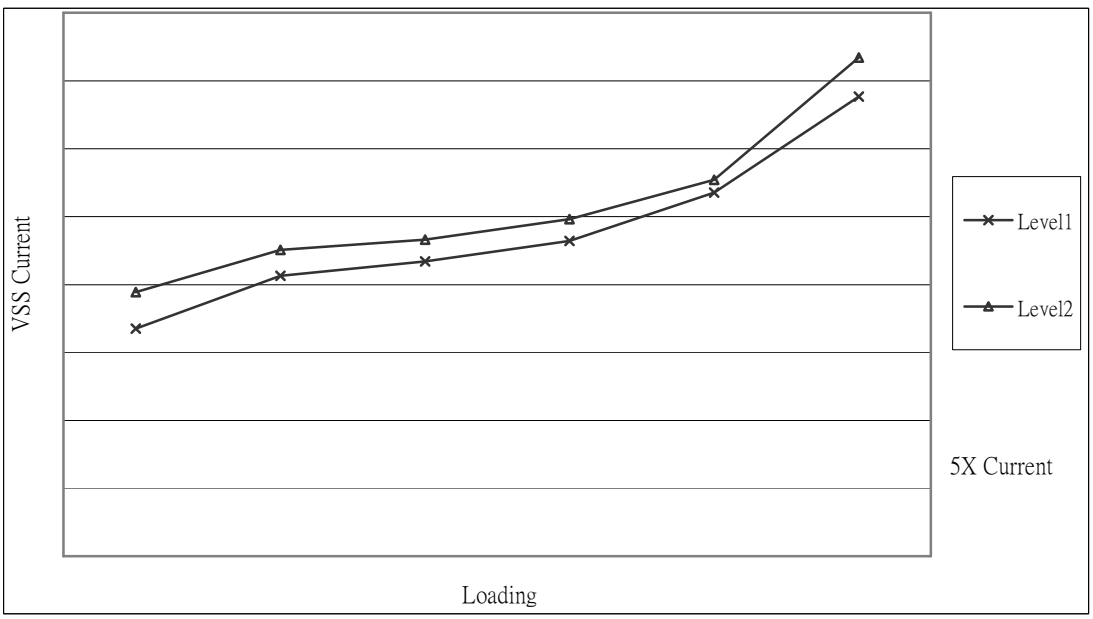
C1= 1u F ~ 4.7u F , C2 = 0.1u F ~ 1u F (suggestion value: C1=1uF , C2=0.1uF)

Booster Efficiency

By Booster Stages (3X, 4X, 5X, 6X) and Booster Efficiency (Level1~2) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level2 is higher than level1), The Boost Efficiency is better than lower level, and it just need few more power consumption current. It could be applied to each multiple voltage Condition.

When the LCD Panel loading is heavier, then the Performance of Booster will be not in a good working condition. We could set the BE level to be higher. We do not need to change to higher Booster Stage, and just need few more current. The Booster Efficiency Command could be used together with Booster Stage Command to choose one best Boost output condition. We could see the Boost Stage Command as a large scale operation, and see the Booster Efficiency Command as a small scale operation. These commands are very convenient for using.





RESET CIRCUIT

Setting RST to “L” can initialize internal function. RST pin must connect to the reset pin of MPU and initialization by RST pin is essential before operating. Please note the hardware reset is not same as the software reset. When RST becomes “L”, the hardware reset procedure will start. When RESET instruction is executed, the software reset procedure will start. The procedure is listed below:

Procedure	Hardware Reset	Software Reset
Oscillator OFF	V	X
Power Save Mode: P=0	V	X
Power Control OFF: VC=0, VR=0, VF=0	V	X
Booster Step: DC[1:0]=0	V	X
Booster Efficiency: BE=1	V	X
Frame Rate: 77Hz, FR[3:0]=0	V	X
LCD Bias: 1/12 Bias, BS[2:0]=(1,1,1)	V	X
Display OFF: D=0, all SEGs/COMs output at VSS	V	X
Normal Display: REV=0, EON=0	V	X
SEG Normal Direction: ADC=0	V	X
COM Normal Direction: SHL=0	V	X
ICON Control: OFF, ICON=0	V	X
Partial Display Duty: L[7:0]=0	V	X
N-Line Inversion: OFF, N[4:0]=0	V	X
Initial COM0: C[6:0]=0	V	X
Initial Display Line: S[6:0]=0	V	V
Read-modify-Write: Released	V	V
Display Data Length (if using 3-Line SPI Interface): D[7:0]=0	V	V
FRC/PWM Mode: 4-FRC, 9-PWM	V	V
Column Address Y[7:1]=0	V	V
Page Address P[3:0]=0	V	V
V0 Regulator Resistor: R[2:0]=(0,0,0)	V	V
EV[5:0]=(1,0,0,0,0,0)	V	V
Gray Scale Setting: [White Mode] OFF White Palette: WA[3:0]=0, WB[3:0]=0, WC[3:0]=0, WD[3:0]=0 [Light Gray Mode] OFF Light Gray Palette: LA[3:0]=0, LB[3:0]=0, LC[3:0]=0, LD[3:0]=0 [Dark Gray Mode] OFF Dark Gray Palette: DA[3:0]=0, DB[3:0]=0, DC[3:0]=0, DD[3:0]=0 [Black Mode] OFF Black Palette: BA[3:0]=0, BB[3:0]=0, BC[3:0]=0, BD[3:0]=0	V	V

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON. Besides, the power is not stable at the time that the power is just turned ON. A hardware reset is needed to initialize those internal registers after the power is stable.

COMMAND TABLE

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Mode Set	0	0	0	0	1	1	1	0	0	0	2-byte command Set FR (Frame Rate) and BE (Booster Efficiency)
	0	0	FR3	FR2	FR1	FR0	0	BE	x'	0	
Read display data	1	1	Read data								Read data into DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0	Read the internal status
ICON control ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable ICON=1: ICON enable & set page address to 16
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB
Set Read-modify-Write	0	0	1	1	1	0	0	0	0	0	DDRAM address control: Read: No change Write: column address +1
Reset Read-modify-Write	0	0	1	1	1	0	1	1	1	0	Release read-modify-write
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON
Set Initial Display Line	0	0	0	1	0	0	0	0	x'	x'	2-byte command Specify the initial display line to realize vertical scrolling
	0	0	x'	S6	S5	S4	S3	S2	S1	S0	
Set Initial COM0	0	0	0	1	0	0	0	1	x'	x'	2-byte command Specify the first COM0 to move display window
	0	0	x'	C6	C5	C4	C3	C2	C1	C0	
Set Partial Display Duty	0	0	0	1	0	0	1	0	x'	x'	2-byte command Set partial display line number
	0	0	L7	L6	L5	L4	L3	L2	L1	L0	
Set N-line Inversion	0	0	0	1	0	0	1	1	x'	x'	2-byte command Set N-line inversion register
	0	0	x'	x'	x'	N4	N3	N2	N1	N0	
Release N-line Inversion	0	0	1	1	1	0	0	1	0	0	Exit N-line inversion mode
Reverse Display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display REV=1: reverse display
Entire Display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display EON=1: entire display ON

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power Control	0	0	0	0	1	0	1	VC	VR	VF	Set power circuits ON/OFF
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select built-in booster step
Select Regulator Register	0	0	0	0	1	0	0	R2	R1	R0	Select the internal resistance ratio of the regulator resistor
Select Electronic Volume	0	0	1	0	0	0	0	0	0	1	2-byte command
	0	0	x'	x'	EV5	EV4	EV3	EV2	EV1	EV0	Adjust contrast level
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
High Power Mode	0	0	1	1	1	1	0	1	1	1	2-byte command
	0	0	0	0	0	1	1	0	1	0	Enable High Power Mode
High Power Mode Control	0	0	1	1	1	1	0	0	1	1	2-byte command
	0	0	0	0	0	0	1	1	0	1	Controls high driving mode
SHL select	0	0	1	1	0	0	SHL	x'	x'	x'	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-direction selection ADC=0: normal direction ADC=1: reverse direction
Oscillator ON	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
RESET	0	0	1	1	1	0	0	0	1	0	Software reset Refer to RESET CIRCUIT
Set display data length (DDL)	x'	x'	1	1	1	0	1	0	0	0	2-byte command
	x'	x'	D7	D6	D5	D4	D3	D2	D1	D0	Specify the number of data bytes. (3-Line SPI only)
Set FRC/PWM mode	0	0	1	0	0	1	0	FRC	PWM1	PWM0	FRC: 1=3FRC, 0=4FRC PWM[1:0]: (0,0)=(0,1)=9PWM (1,0)=12PWM (1,1)=15PWM
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Test Instruction	0	0	1	1	1	1	x'	x'	x'	x'	Don't use this instruction

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
White palette ($1^{st}/2^{nd}$ frame)	0	0	1	0	0	0	1	0	0	0	Set white mode palette
set PWM pulse width	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0	$1^{st}/2^{nd}$ frame
White palette ($3^{rd}/4^{th}$ frame)	0	0	1	0	0	0	1	0	0	1	Set white mode palette
set PWM pulse width	0	0	WD3	WD2	WD1	WD0	WC3	WC2	WC1	WC0	$3^{rd}/4^{th}$ frame
Light palette ($1^{st}/2^{nd}$ frame)	0	0	1	0	0	0	1	0	1	0	Set light gray mode palette
set PWM pulse width	0	0	LB3	LB2	LB1	LB0	LA3	LA2	LA1	LA0	$1^{st}/2^{nd}$ frame
Light palette ($3^{rd}/4^{th}$ frame)	0	0	1	0	0	0	1	0	1	1	Set light gray mode palette
set PWM pulse width	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0	$3^{rd}/4^{th}$ frame
Dark palette ($1^{st}/2^{nd}$ frame)	0	0	1	0	0	0	1	1	0	0	Set dark gray mode palette
set PWM pulse width	0	0	DB3	DB2	DB1	DB0	DA3	DA2	DA1	DA0	$1^{st}/2^{nd}$ frame
Dark palette ($3^{rd}/4^{th}$ frame)	0	0	1	0	0	0	1	1	0	1	Set dark gray mode palette
set PWM pulse width	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0	$3^{rd}/4^{th}$ frame
Black palette ($1^{st}/2^{nd}$ frame)	0	0	1	0	0	0	1	1	1	0	Set black mode palette
set PWM pulse width	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0	$1^{st}/2^{nd}$ frame
Black palette ($3^{rd}/4^{th}$ frame)	0	0	1	0	0	0	1	1	1	1	Set black mode palette
set PWM pulse width	0	0	BD3	BD2	BD1	BD0	BC3	BC2	BC1	BC0	$3^{rd}/4^{th}$ frame

COMMAND DESCRIPTION

Mode Set

2-byte instruction to set FR (Frame frequency control) and BE (Booster efficiency control)

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	FR3	FR2	FR1	FR0	0	BE	x'	0

Frame Rate

This command is used to set the frame frequency.

FR_3	FR_2	FR_1	FR_0	FR frequency
0	0	0	0	77 Hz (default)
0	0	0	1	51 Hz
0	0	1	0	55 Hz
0	0	1	1	58 Hz
0	1	0	0	63 Hz
0	1	0	1	67 Hz
0	1	1	0	68 Hz
0	1	1	1	70 Hz
1	0	0	0	73 Hz
1	0	0	1	75 Hz
1	0	1	0	80 Hz
1	0	1	1	85 Hz
1	1	0	0	91 Hz
1	1	0	1	102 Hz
1	1	1	0	113 Hz
1	1	1	1	123 Hz

Booster Efficiency

The ST7541 incorporates software configurable Booster Efficiency Command. It could be used with Voltage multiplier to get the suitable Vout and Power consumption. Default setting is Level 2.

Flag	Description	
BE	0	Booster Efficiency Level 1
	1	Booster Efficiency Level 2

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Write data							

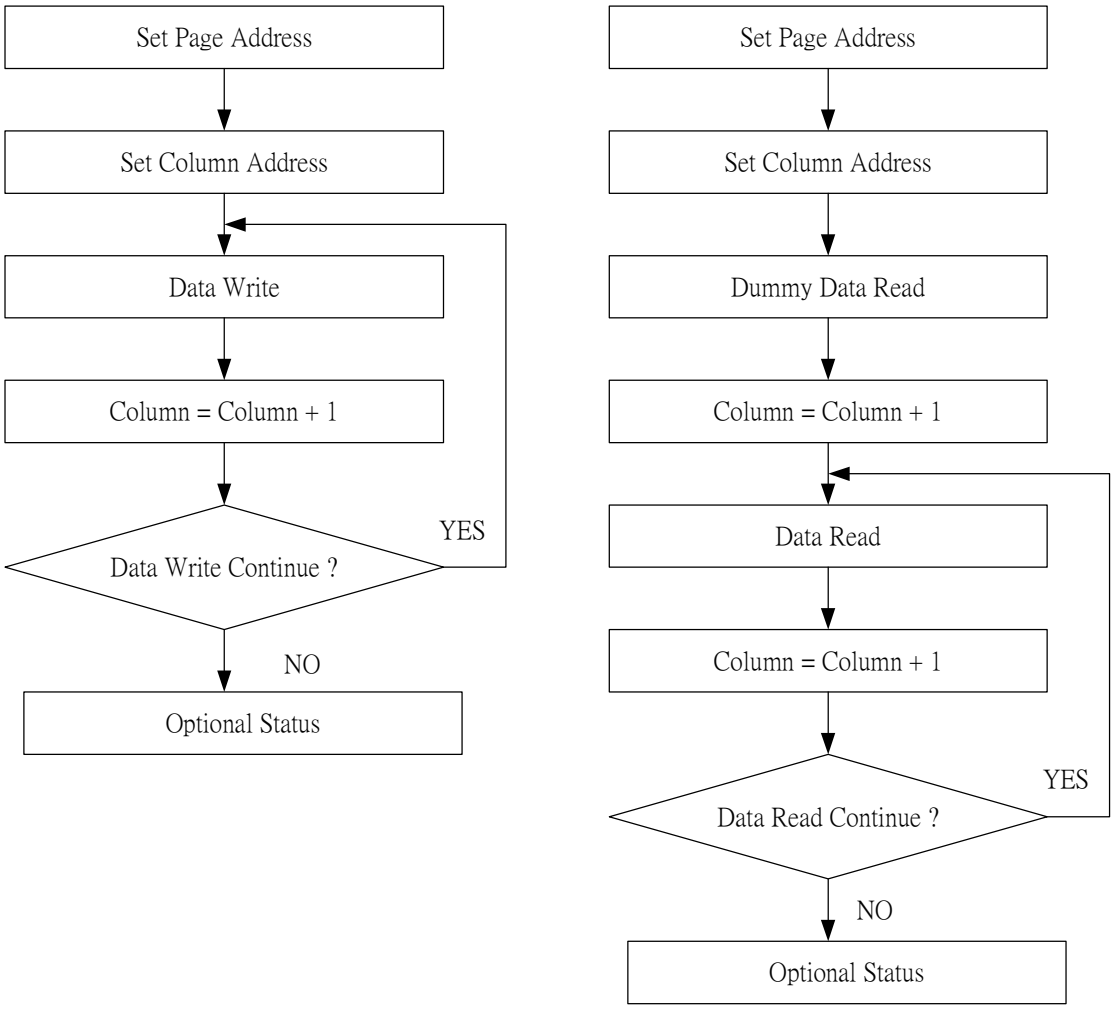


Figure 18 Sequence for Writing Display Data (Left) and Sequence for Reading Display Data (Right)

Read Status

Indicates the internal status of the ST7541

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	D	RES	MF2	MF1	MF0	DS1	DS0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
D	Indicates display ON / OFF status 0: display OFF, 1: display ON
RES	Indicates the initialization is in progress by RST signal or RESET instruction. 0: chip is active, 1: chip is being reset
MF	Manufacturer ID; recommended value: MF2 MF1 MF0 = [0 0 0] The value of MF2, MF1 and MF0 will follow the hardware selection.
DS	Display size ID; recommended value: DS1 DS0 = [0 0] The value of DS1 and DS2 will follow the hardware selection.

ICON Control ON/OFF

This instruction makes ICON enable or disable. By default, ICON display is disabled (ICON= 0). When ICON control register is set to “1”, ICON display is enabled and page address is set to “16”. Then user can write data for icons. It is impossible to set the page address to “16” by Set Page Address instruction. Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to “16”. When ICON control register is set to “0”, ICON display is disabled.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	ICON

ICON=0: ICON disable (default)

ICON=1: ICON enable & set the page address to 16

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't affect the display status. Set Page Address instruction can not be used to set the page address to “16”. Use ICON control register ON/OFF instruction to set the page address to “16”.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data.

When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y7	Y6	Y5

Set Column Address LSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y4	Y3	Y2	Y1

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Set Read-modify-Write

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Read-modify-Write instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Read-modify-Write

This instruction releases the Read-modify-Write mode, and makes the column address return to its initial value just before the set Read-modify-Write instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

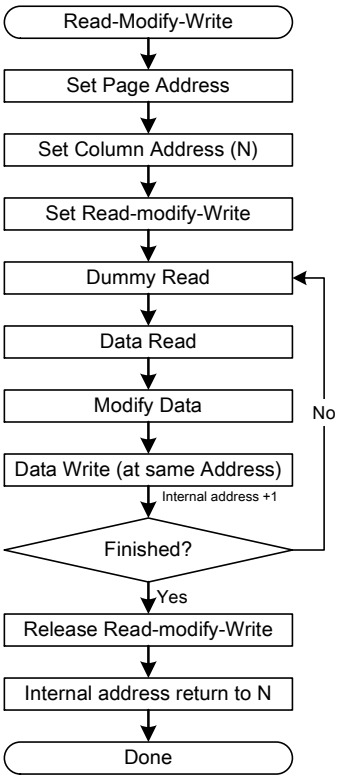
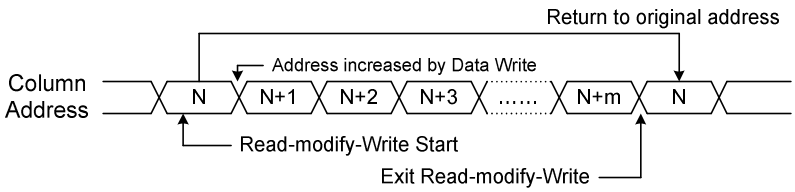


Figure 19 Sequence for Read-modify-Write



Display ON / OFF

Turns the display ON or OFF. This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON

DON = 0: display OFF

Set Initial Display Line

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row(COM0) of LCD panel.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

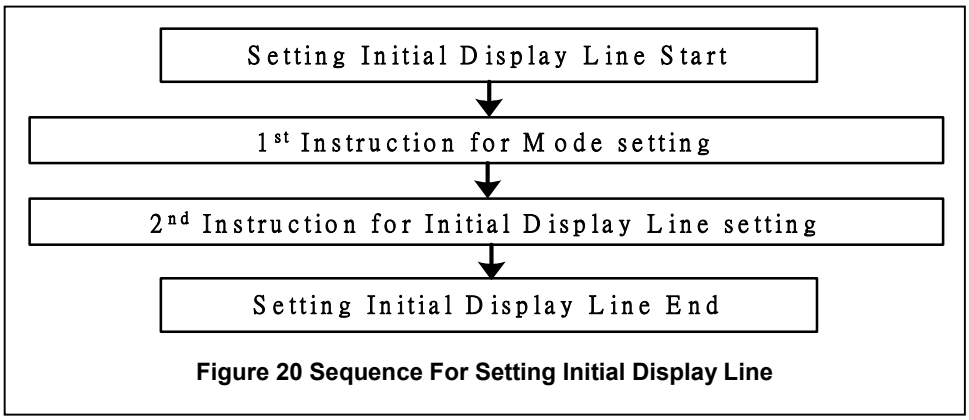


Figure 20 Sequence For Setting Initial Display Line

Set Initial COM0

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM124
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127

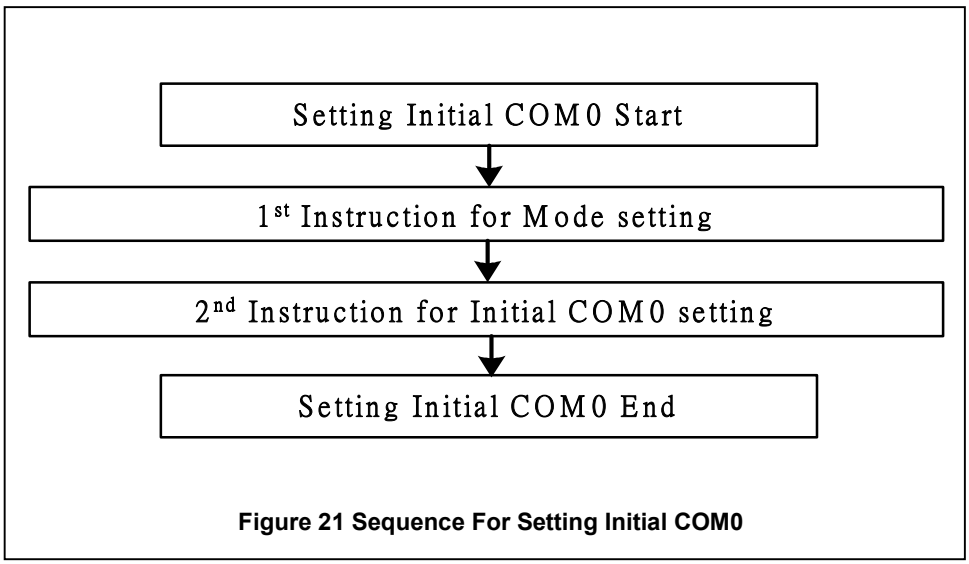


Figure 21 Sequence For Setting Initial COM0

Set Partial Display Duty

Sets the duty within range of 16 ~ 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	L7	L6	L5	L4	L3	L2	L1	L0

D7	D6	D5	D4	D3	D2	D1	D0	Valid Display Lines (ICON disabled)	Valid Display Lines (ICON enabled)
0	0	0	0	0	0	0	0	No operation	No operation
:	:	:	:	:	:	:	:		
0	0	0	0	1	1	1	1		
0	0	0	1	0	0	0	0	16 lines	16+1 lines
0	0	0	1	0	0	0	1	17 lines	17+1 lines
:	:	:	:	:	:	:	:	:	:
0	1	1	0	0	1	0	0	100 lines	100+1 lines
:	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	127 lines	127+1 lines
1	0	0	0	0	0	0	0	128 lines	128+1 lines
1	0	0	0	0	0	0	1	No Operation	No Operation
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1		

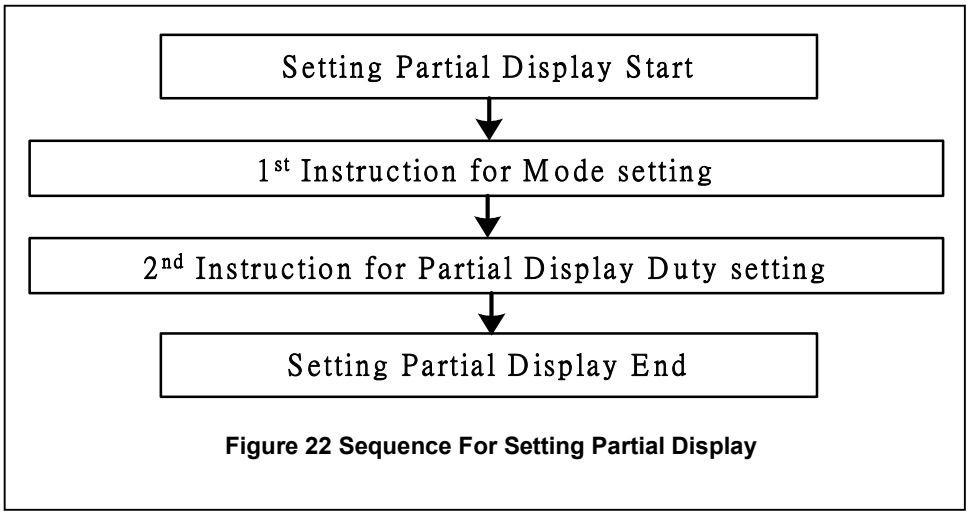


Figure 22 Sequence For Setting Partial Display

Set N-line Inversion

Sets the inverted line number within range of 3 to 33 to improve the display quality. It controls the phase of the internal LCD frame signal. To get better performance, the display duty (L) should not be complete divide by N-line setting (N). If “L” can be complete divide by “N” (assume K = L / N), the factor (K) should not be even number.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	0	0	0	0	0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

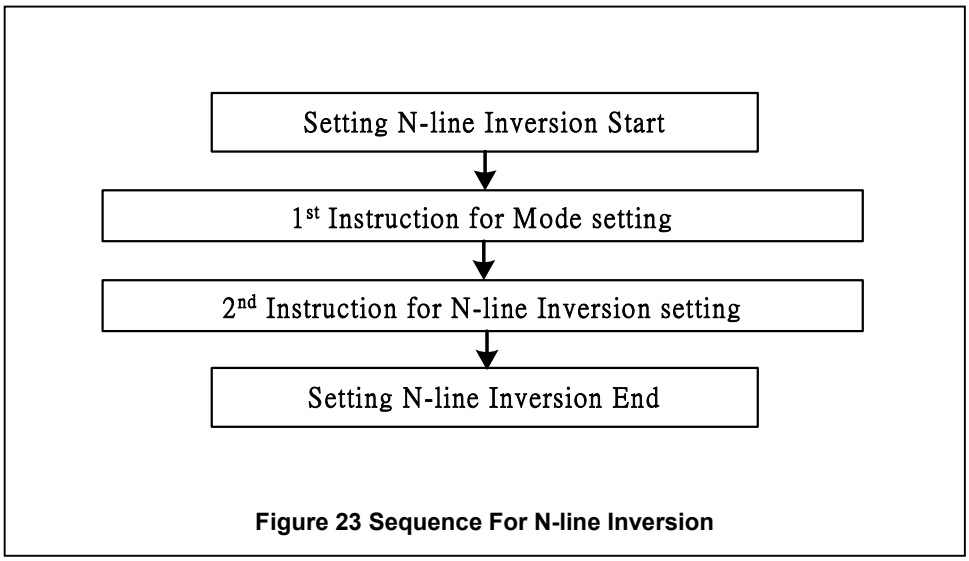


Figure 23 Sequence For N-line Inversion

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	DDRAM data = “00”	DDRAM data = “01”	DDRAM data = “10”	DDRAM data = “11”
0 (Normal)	White (“00”)	Light gray (“01”)	Dark gray (“10”)	Black (“11”)
1 (Reverse)	Black (“11”)	Dark gray (“10”)	Light gray (“01”)	White (“00”)

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	DDRAM data = “00”	DDRAM data = “01”	DDRAM data = “10”	DDRAM data = “11”
0 (Normal)	White (“00”)	Light gray (“01”)	Dark gray (“10”)	Black (“11”)
1 (Entire)	Black (“11”)	Black (“11”)	Black (“11”)	Black (“11”)

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0	–	–	Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
–	0	–	Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
–	–	0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

Select DC-DC Step-up

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ (Rb / Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

Set Electronic Volume

Consist of 2-byte Instructions. The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, Reference Voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

High Power Mode Enable

This 2-byte Instruction enables the high power mode. The high power mode control command is valid after this 2-byte Instruction.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	1

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	1	0

High Power Mode Control

This double command controls the high power mode. The driving strength is enhanced and the current consumption will be larger.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	0	1

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	x	x	x

SHL = 0: normal direction (COM0 → COM127)

SHL = 1: reverse direction (COM127 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG127)

ADC = 1: reverse direction (SEG127 → SEG0)

Oscillator ON

This instruction enables the built-in oscillator circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Power Save

The ST7541 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode , P = 1: sleep mode

Release Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

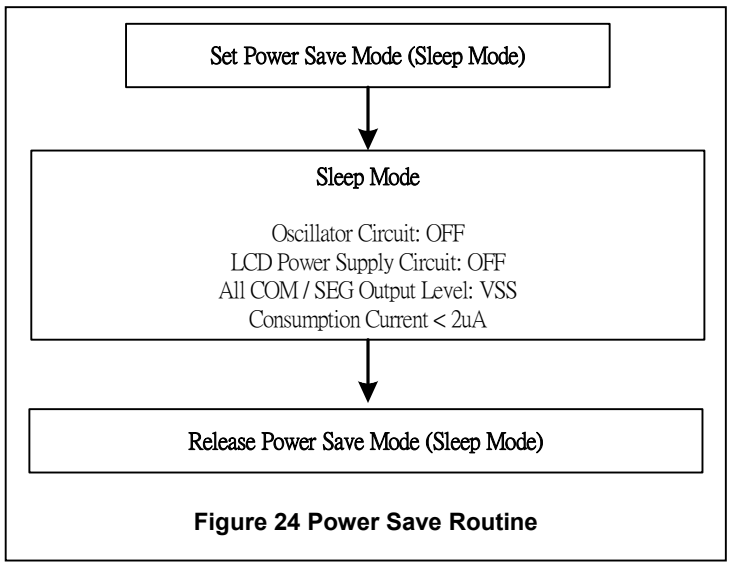


Figure 24 Power Save Routine

RESET

RESET instruction initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RST pin.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Set Display Data Length (3-Line SPI Mode)

Consists of 2 bytes instruction.

This command is used in 3-Line SPI mode only(PS0 = ”L” and PS1 = ”L”). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When A0 is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

Set PWM & FRC mode

Selects 3/4 FRC and 9 / 12 / 15 PWM

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	FRC	PWM1	PWM0

FRC	PWM1	PWM0	Status of PWM & FRC
0	–	–	4FRC
1			3FRC
–	0	0 or 1	9PWM
	1	0	12PWM
	1	1	15PWM

NOP

No operation

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

This instruction is for testing IC. Please do not use it.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	x	x	x	x

Set Gray Scale Mode & Register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

– **Set Gray Scale Mode**

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	GM2	GM1	GM0

GM_2	GM_1	GM_0	Description
0	0	0	In case of setting whit mode and 1st / 2nd frame
0	0	1	In case of setting whit mode and 3rd / 4th frame
0	1	0	In case of setting light gray mode and 1st / 2nd frame
0	1	1	In case of setting light gray mode and 3rd / 4th frame
1	0	0	In case of setting dark gray mode and 1st / 2nd frame
1	0	1	In case of setting dark gray mode and 3rd / 4th frame
1	1	0	In case of setting black mode and 1st / 2nd frame
1	1	1	In case of setting black mode and 3rd / 4th frame

--Set Gray Scale Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	GB3	GB2	GB1	GB0	GA3	GA2	GA1	GA0
0	0	GD3	GD2	GD1	GD0	GC3	GC2	GC1	GC0

GA3, GB3, GC3, GD3	GA2, GB2, GC2, GD2	GA1, GB1, GC1, GD1	GA0, GB0, GC0, GD0	Pulse width (9 PWM)	Pulse width (12 PWM)	Pulse width (15 PWM)
0	0	0	0	0/9	0/12	0/15
0	0	0	1	1/9	1/12	1/15
:	:	:	:	:	:	:
1	0	0	1	9/9	9/12	9/15
1	0	1	0	0/9	10/12	10/15
1	0	1	0	0/9	11/12	11/15
1	1	0	0	0/9	12/12	12/15
1	1	0	1	0/9	0/12	13/15
1	1	1	0	0/9	0/12	14/15
1	1	1	1	0/9	0/12	15/15

* GA3=WA3, LA3, DA3, BA3 GA2=WA2, LA2, DA2, BA2 GA1=WA1, LA1, DA1, BA1 GA0=WA0, LA0, DA0, BA0
GB3=WB3, LB3, DB3, BB3 GA2=WB2, LB2, DB2, BB2 GA1=WB1, LB1, DB1, BB1 GA0=WB0, LB0, DB0, BB0
GC3=WC3, LC3, DC3, BC3 GA2=WC2, LC2, DC2, BC2 GA1=WC1, LC1, DC1, BC1 GA0=WC0, LC0, DC0, BC0
GD3=WD3, LD3, DD3, BD3 GA2=WD2, LD2, DD2, BD2 GA1=WD1, LD1, DD1, BD1 GA0=WD0, LD0, DD0, BD0

COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

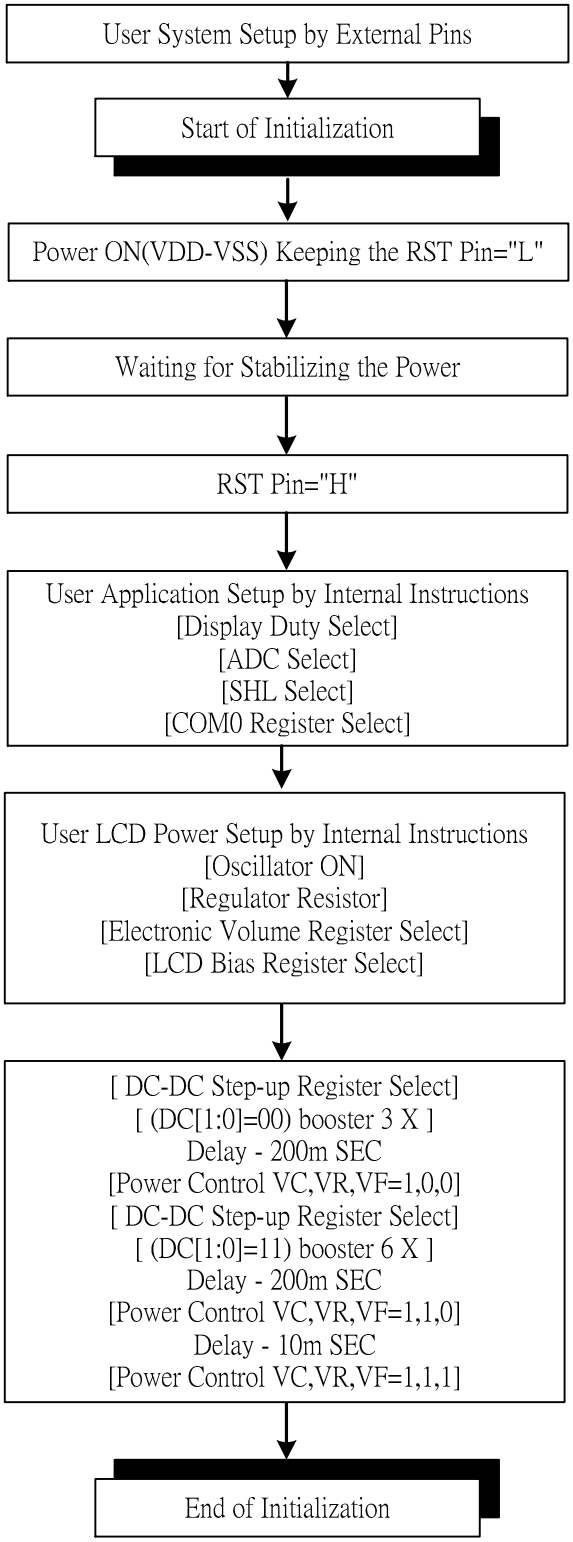


Figure 25 Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the built-in Power Supply Circuits

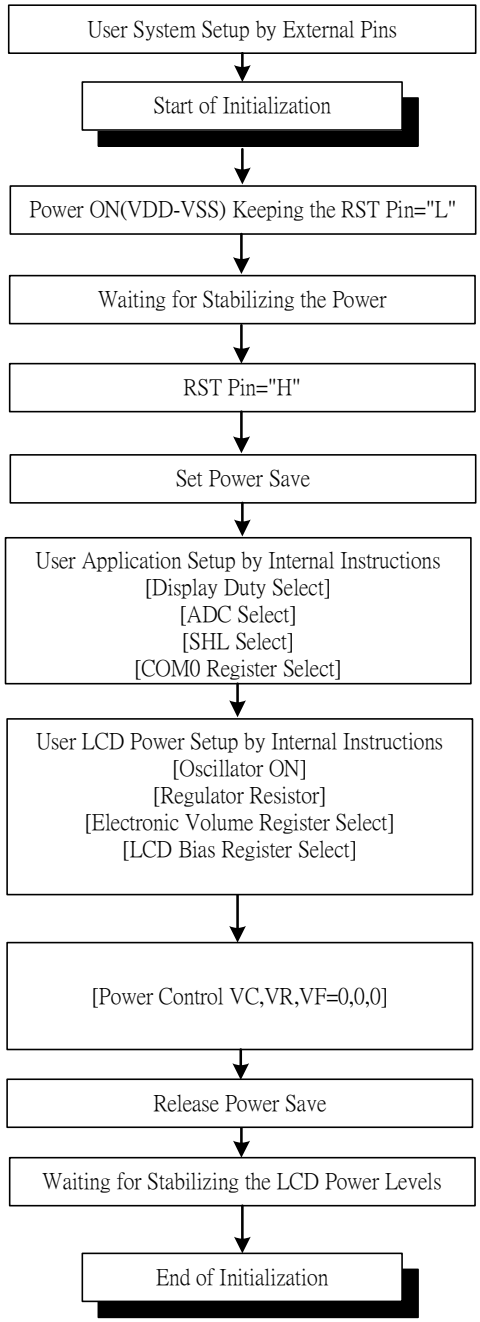


Figure 26 Initializing without Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying

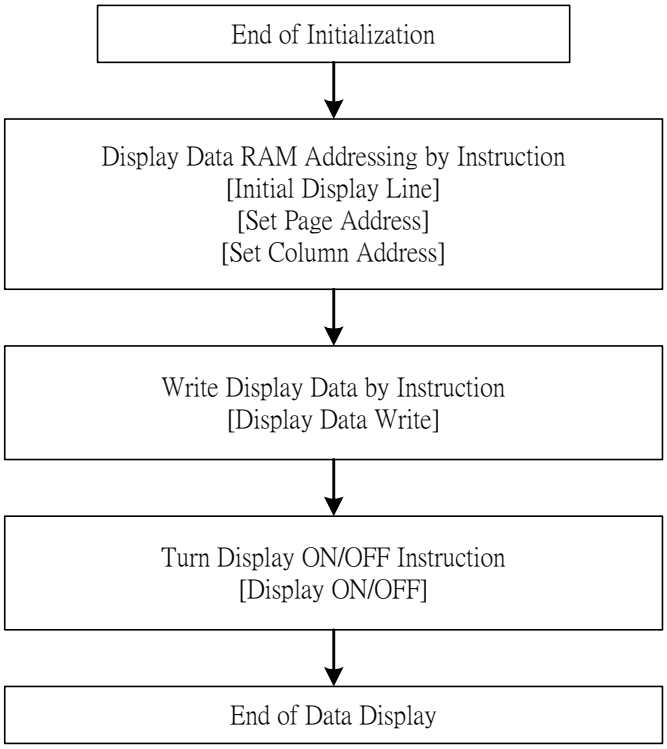


Figure 27 Data Displaying

Referential Instruction Setup Flow: Power OFF

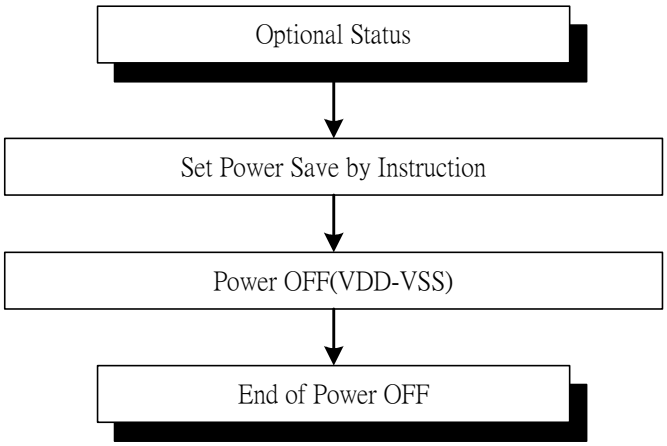
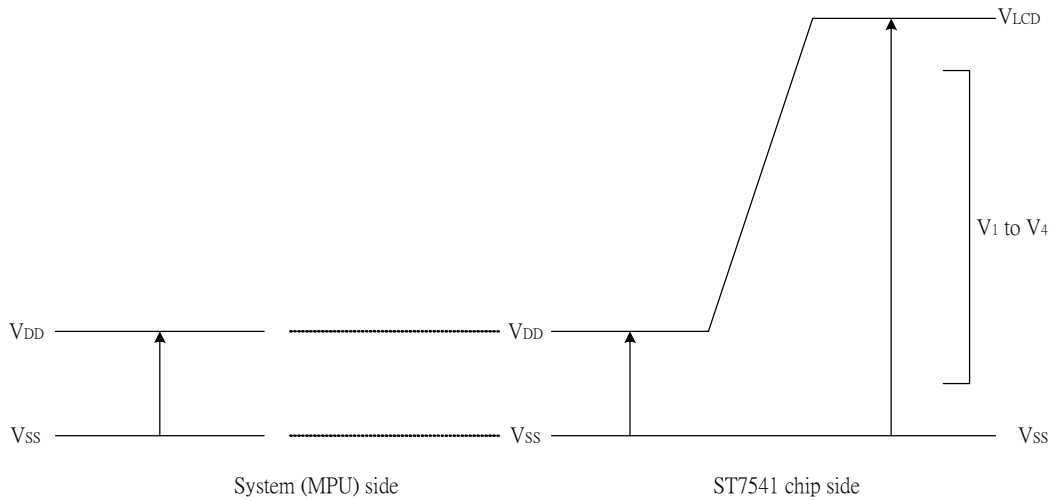


Figure 28 Power OFF

LIMITING VALUES

In accordance with the Absolutely Maximum Rating System, please refer to note 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD	–0.3 ~ +3.6	V
Power supply voltage	VDD2	1.7 ~ 3.3	V
Power supply voltage	V0	3.5 ~ 15	V
Power supply voltage	VOUT_IN	–0.5 ~ +20	V
Power supply voltage	V1, V2, V3, V4	0.3 to VOUT_IN	V
Input voltage	VIN	–0.5 to VDD+0.5	V
Output voltage	VO	–0.5 to VDD+0.5	V
Operating temperature	TOPR	–30 to +85	°C
Storage temperature	TSTR	–65 to +150	°C



Note:

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that
   VOUT_IN ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ Vss

DC CHARACTERISTICS

VDD = 1.8 V to 3.3V; VSS = 0 V; VLCD = 3.5 to 15.0V; Tamb=–30~+85°C; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD			1.8	—	3.3	V	VDD*1
Operating Voltage (2)		VDD2			2.4	—	3.3	V	VDD2
High-level Input Voltage		VIHC			0.7 x VDD	—	VDD	V	*2
Low-level Input Voltage		VILC			VSS	—	0.3 x VDD	V	*2
High-level Output Voltage		VOHC			0.7 x VDD	—	VDD	V	*3
Low-level Output Voltage		VOLC			VSS	—	0.3 x VDD	V	*3
Input leakage current		ILI	VIN = VDD or VSS		–1.0	—	1.0	μA	*4
Output leakage current		ILO	VIN = VDD or VSS		–3.0	—	3.0	μA	*5
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C	VOUT_IN = 15.0 V	—	2.0	3.5	KΩ	SEGn COMn *6
				VOUT_IN = 8.0 V	—	3.2	5.4		
Oscillator Frequency	Internal Oscillator	fOSC	1/128 duty	Ta = 25°C 9 PWM	—	443.5	462.5	kHz	*7
	External Input	fCL			—	88.7	92.5	kHz	OSC
	Frame Rate	fFRAME			—	77	85	Hz	

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Step-up Circuit output voltage	VOUT_OUT		—	—	15	V	VOUT_OUT
Voltage regulator operating Voltage	VOUT_IN		—	—	15	V	VOUT_IN

Bare Dice Consumption Current : During Display, with the Internal Power Supply, Current consumed by total ICs when an external power supply(VDD,VDD2) is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	ISS	VDD = 3.3 V, V0 – VSS = 10.7 V 5X booster 1/11 bias	—	550	650	μA	*8
Power Down	ISS	Ta = 25°C	—	0.01	2	μA	*9

Notes to the DC characteristics

1. The maximum possible VOUT voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. Power-down mode. During power down all static currents are switched off.
4. If external VLCD, the display load current is not transmitted to IDD.
5. VOUT external voltage applied to VOUT_IN pin; VOUT_IN disconnected from VOUT_OUT

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RST ,and MODE terminals.

*3 The D0 to D7, and OSC terminals.

*4 The A0,/RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RST ,and MODE terminals.

*5 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.

*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.

RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*7 The relationship between the oscillator frequency and the frame rate frequency.

*8,9 It indicates the current consumed on IC alone when the internal oscillator circuit and display are turned on.

TIMING CHARACTERISTICS

System Bus Read/Write Characteristics (For the 8080 Series MPU)

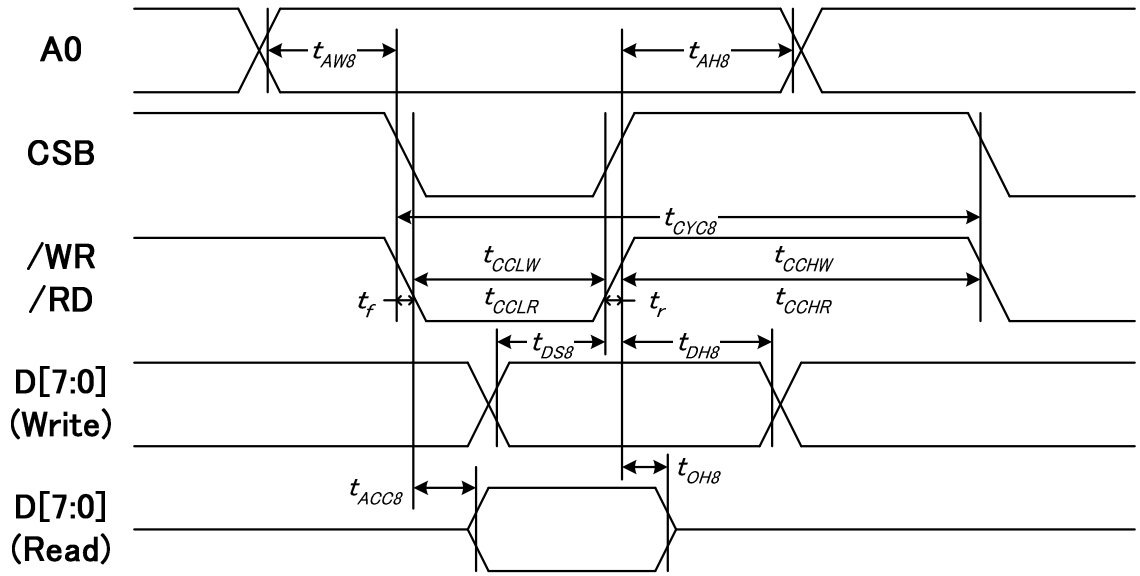


Figure 29

(VDD = 3.3V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Write L pulse width	/WR	tCCLW		80	—	
Write H pulse width		tCCHW		80	—	
Read L pulse width	/RD	tCCLR		140	—	
Read H pulse width		tCCHR		80		
Data setup time (Write)	D0 to D7	tDS8		40	—	
Write Data hold time (Write)		tDH8		10	—	
Data access time (Read)		tACC8	CL = 100 pF	—	70	
Output disable time (Read)		tOH8	CL = 100 pF	5	50	

(VDD = 2.7V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Write L pulse width	/WR	tCCLW		220	—	
Write H pulse width		tCCHW		180	—	
Read L pulse width	/RD	tCCLR		220	—	
Read H pulse width		tCCHR		180	—	
Data setup time (Write)	D0 to D7	tDS8		40	—	
Write Data hold time (Write)		tDH8		15	—	
Data access time (Read)		tACC8	CL = 100 pF	—	140	
Output disable time (Read)		tOH8	CL = 100 pF	10	100	

(VDD = 1.8V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Write L pulse width	/WR	tCCLW		360	—	
Write H pulse width		tCCHW		280	—	
Read L pulse width	/RD	tCCLR		360	—	
Read H pulse width		tCCHR		280		
Data setup time (Write)	D0 to D7	tDS8		80	—	
Write Data hold time (Write)		tDH8		30	—	
Data access time (Read)		tACC8	CL = 100 pF	—	240	
Output disable time (Read)		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics (For the 6800 Series MPU)

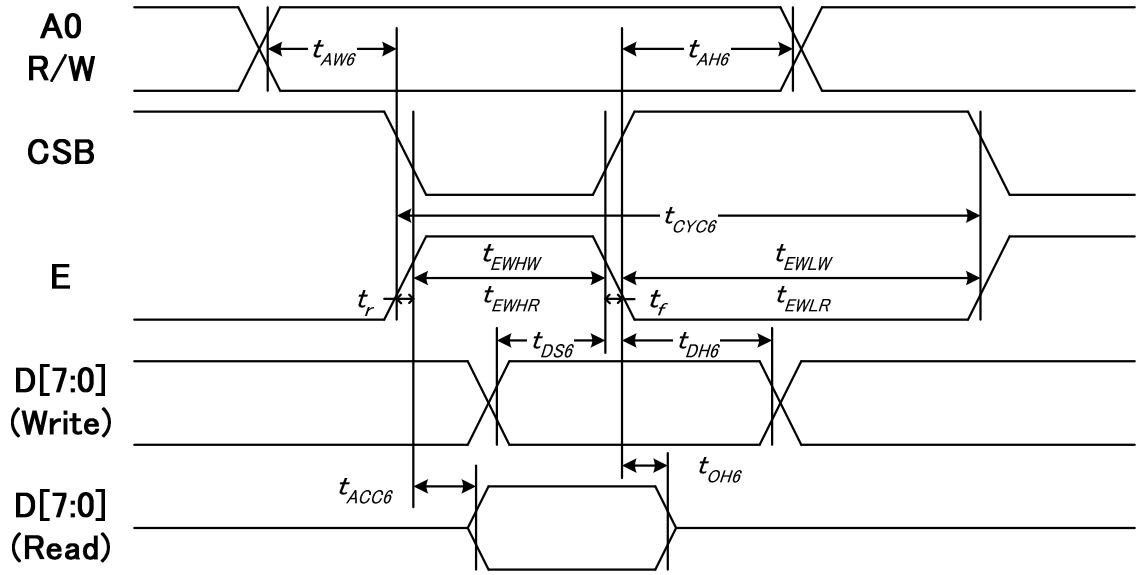


Figure 30

(VDD = 3.3 V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0, R/W	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	E	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)		tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

(VDD = 2.7V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0, R/W	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	E	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)		tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		15	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

(VDD =1.8V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0, R/W	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	E	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)		tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Data hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

Serial Interface (4-Line Interface)

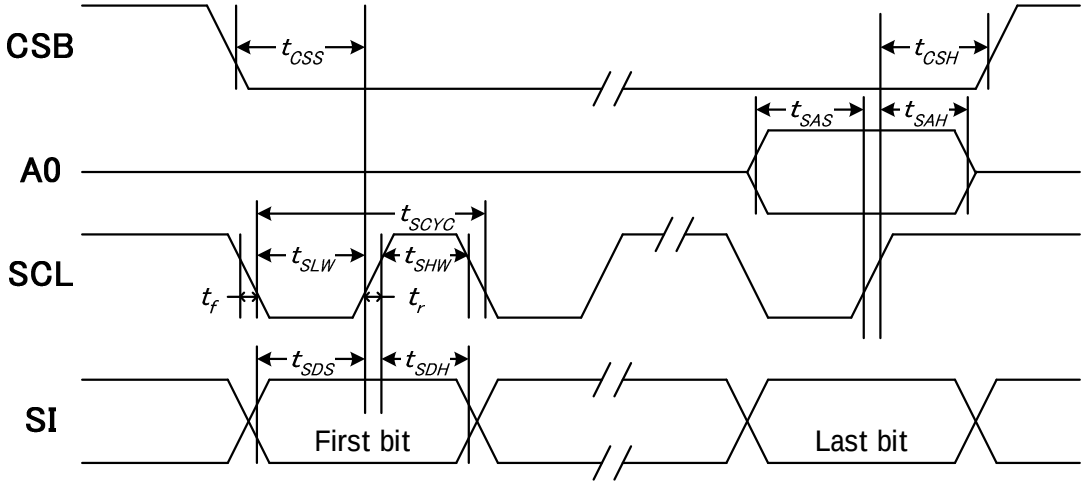


Figure 31

(VDD=3.3V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		40	—	

(VDD=2.7V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

(VDD=1.8V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

Serial Interface (3-Line Interface)

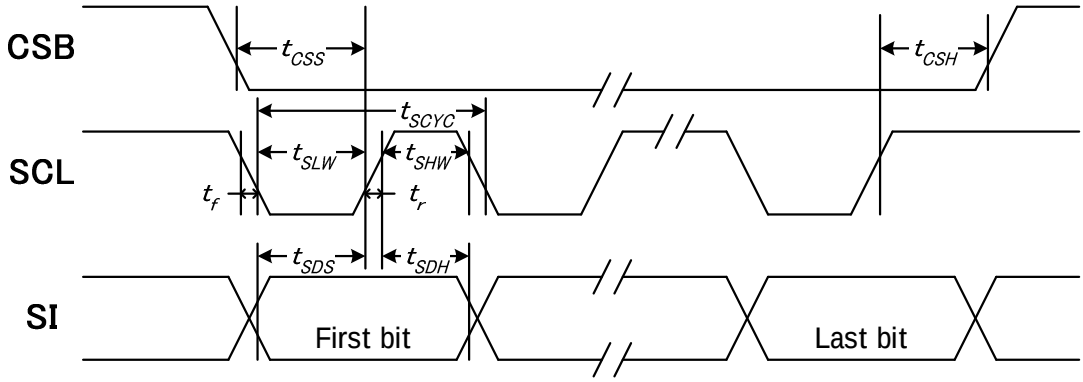


Figure 32

(VDD=3.3V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		40	—	

(VDD=2.7V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

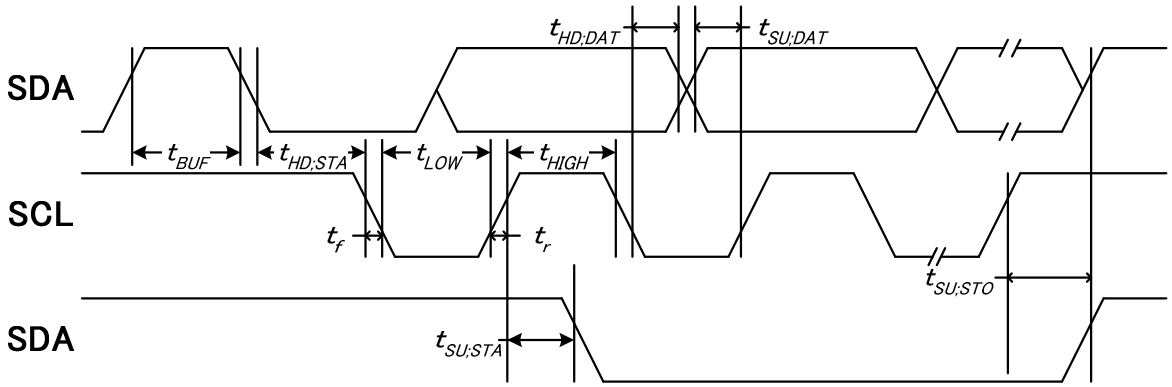
(VDD=1.8V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

Serial Interface (IIC Interface)



(VDD=3.3V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SI	TSU;Data		100	-	ns
Data hold time	SI	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SI	TSU;SUA		0.6	-	us
Start condition hold time	SI	THD;STA		0.6	-	us
Setup time for STOP ondition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and StART condition	SCL	TBUF		1.3		us

RESET TIMING

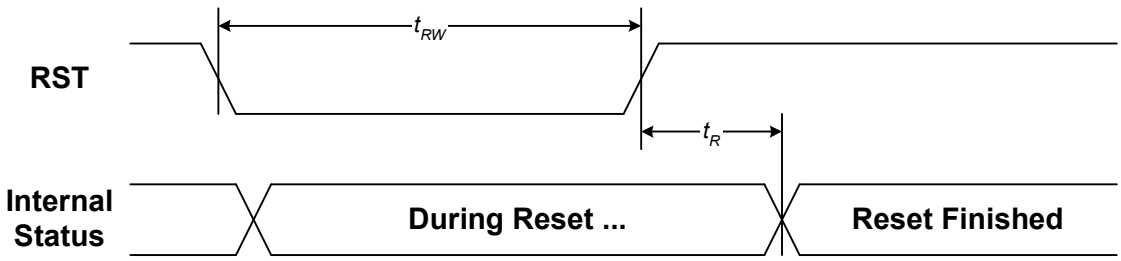


Figure 33

(VDD = 3.3V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset “L” pulse width	RST	tRW		1	—	—	us

(VDD = 2.7V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset “L” pulse width	RST	tRW		1.5	—	—	us

(VDD = 1.8V, Ta=–30~85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RST	tRW		2.0	—	—	us

POWER PAD CONNECT

The pinning of the ST7541 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 129 X 128 pixels.

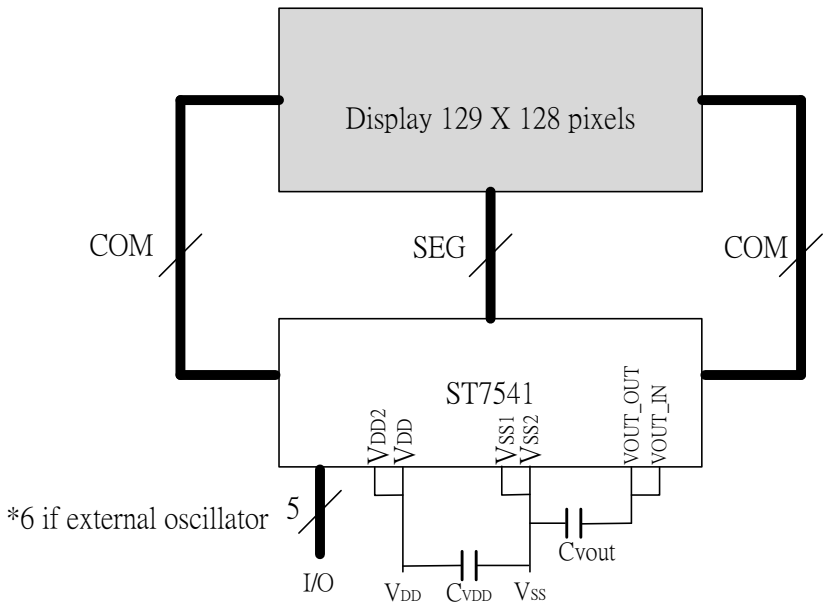


Figure 34 Application diagram: internal charge pump is used and s single VDD

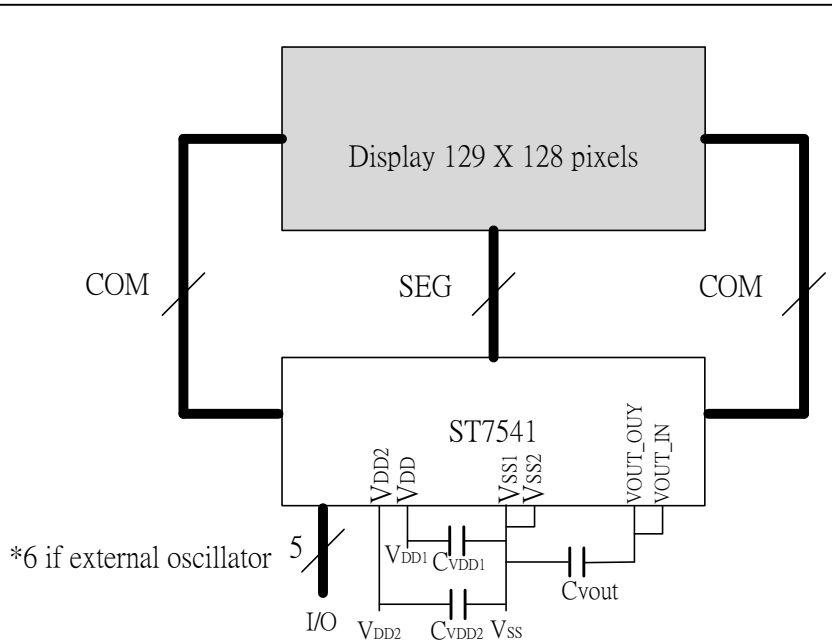


Figure 35 Application diagram: Internal charge pump is used and two separate VDD(VDD2)

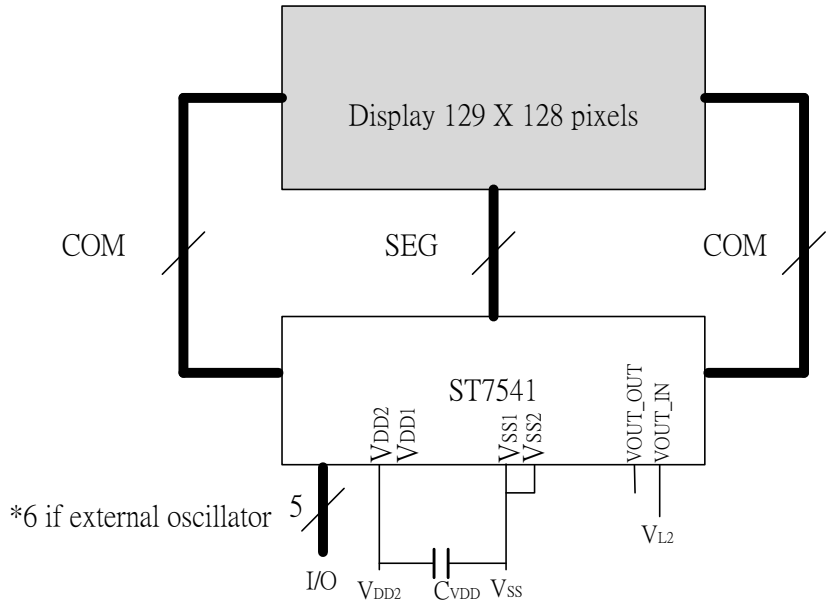


Figure 36 application diagram: External high voltage generation is used

The required minimum value for the external capacitors in an application with the ST7541 are: C_{VLCD} = min. 100nF $C_{VDD,2}$= min. 1.0 μF

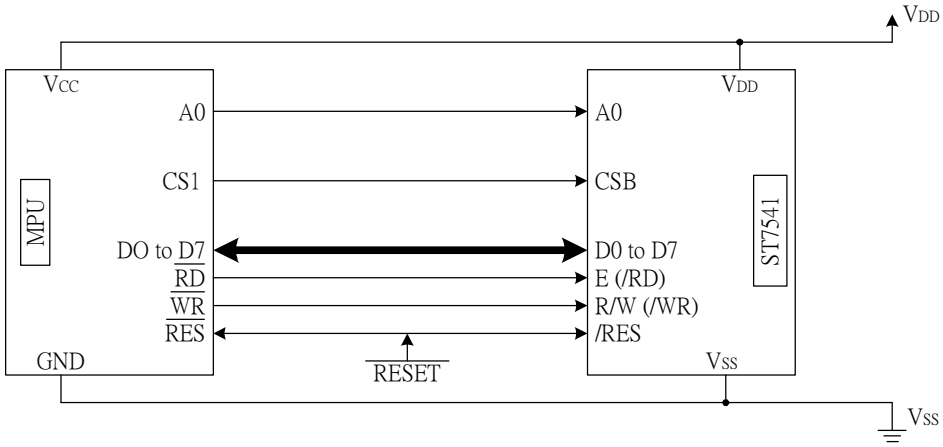
Higher capacitor values are recommended for ripple reduction.

THE MPU INTERFACE (REFERENCE EXAMPLES)

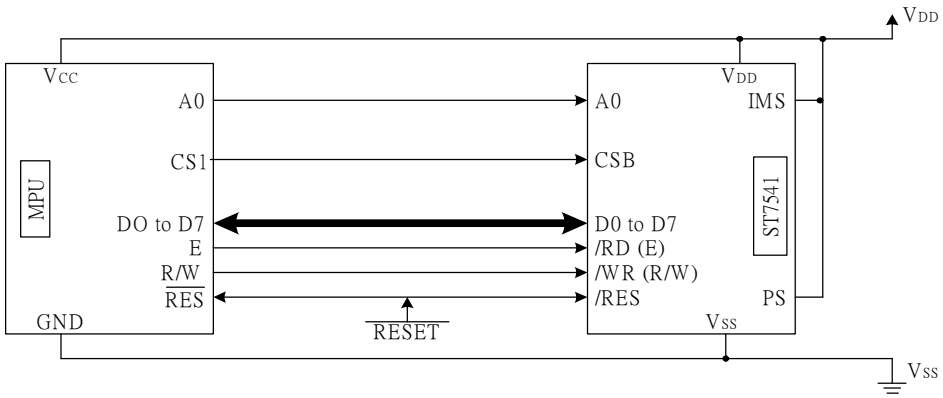
The ST7541 Series can be connected to either60X86 Series MPUs or to 6800Swries MPUs. Moreover, using the serial interface it is possible to operate the ST7541 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7541 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

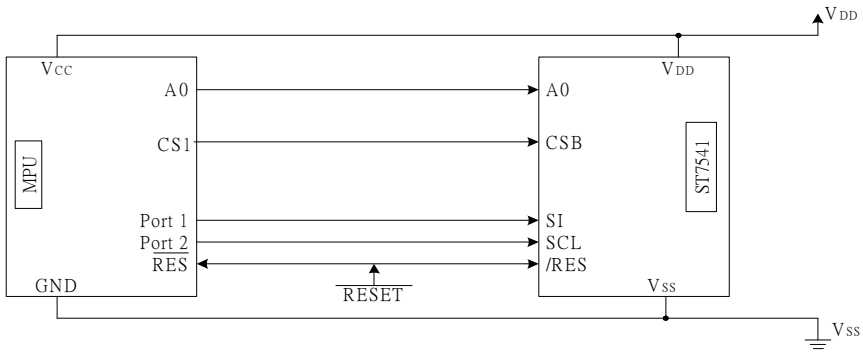
(1) 8080 Series MPUs



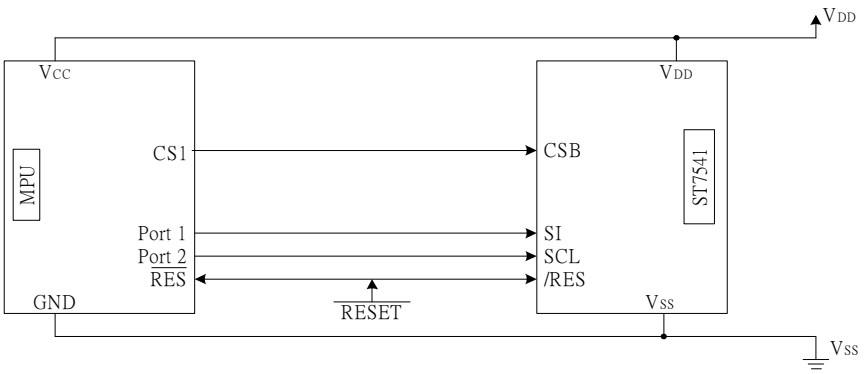
(2) 6800 Series MPUs



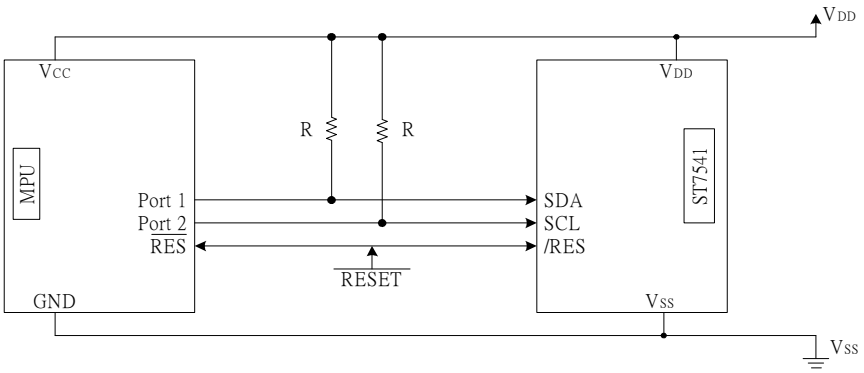
(3) Using the Serial Interface (4-line interface)



(4) Using the Serial Interface (3-line interface)

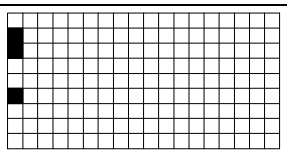
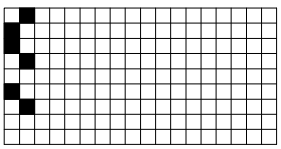
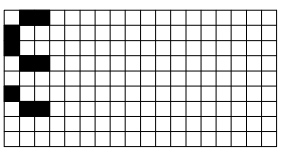
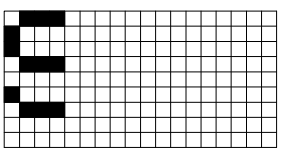


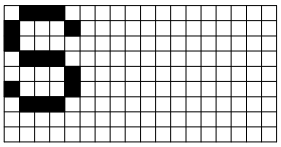
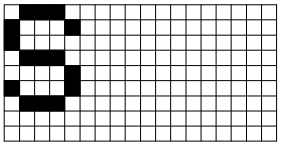
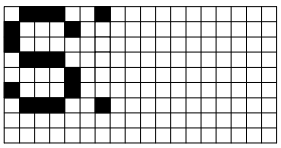
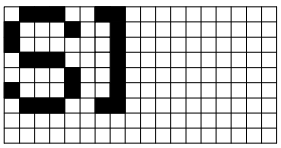
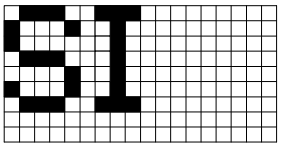
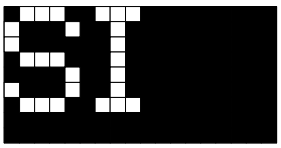
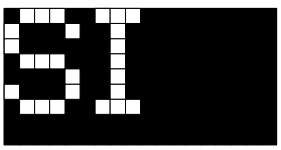
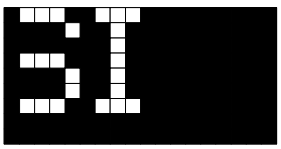
(5) Using the Serial Interface (IIC interface)



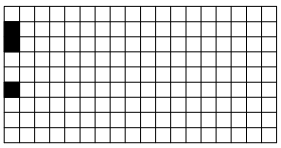
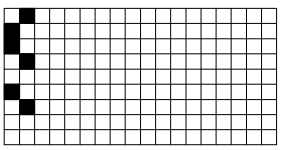
APPLICATION Program Example

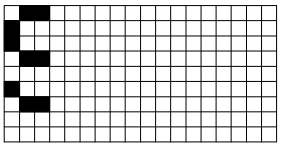
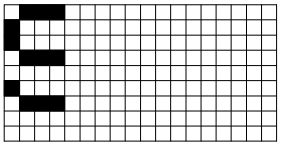
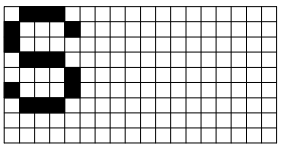
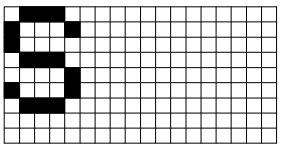
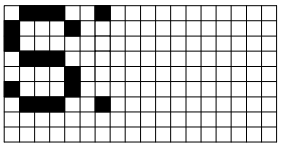
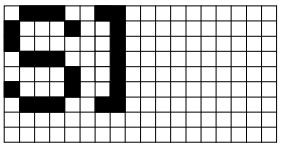
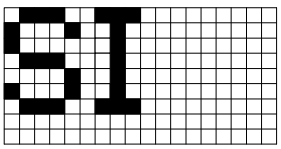
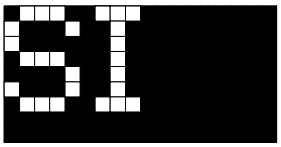
4-Gray programming example for ST7541

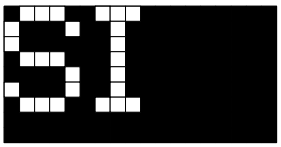
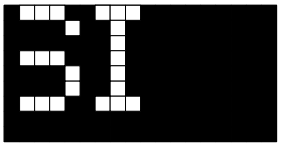
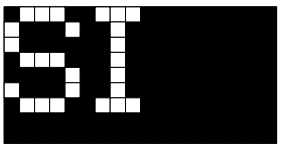
SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
0	Start		CSB IS going low.
1	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 x' 0		Mode Set. FR[3:0] = 0000 BE= 1
2	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 1 0 1 1		OSC ON
3.a	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 0 0 1 DC1 DC0		Set DC-DC Step up Set Vout
3.b	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 R2 R1 R0		Set Ra/Rb Set R[2:0]
3.c	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0 1 0 x' x' Ev5 Ev4 Ev3 Ev2 Ev1 Ev0		Set EV Set Ev[5:0]
3.d	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 1 0 B2 B1 B0		Set Bias Set B[2:0]
4.a	SET pulse width of Gray scale		Gray-Scale Setting
4.b	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 x' 0		Mode Set.
5.a	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 1 1 1 1		SET Power Control Booster ON Regulator ON Follower ON
5.b	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 1 1 1 1		Display control. Display on
6	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here…
7	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
8	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
9	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.

10	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 1 0 0 1 0 1 0 0 1 1 0 0 1 0		Data Write.
11	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.
12	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
13	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1		Data Write.
14	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
15	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 0 1 1 1		Display Control. Set Reverse display mode REV=1
16	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0		Set column address of RAM. Set address to “00000000”. Y[7:0]=00000000 (Y0 default is 0)
17	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.

programming example for ST7541(Use IIC Interface)

SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
1	IIC INTERFACE Start		
2	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
3	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0
4	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 0 0 0 0 0 0 0 1 0 x' 0		Mode Set. FR[3:0] = 0000 BE= 1
5	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 1 0 1 1		OSC ON
6.a	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 1 0 0 1 DC1 DC0		Set DC-DC Step up Set Vout
6.b	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 R2 R1 R0		Set Ra/Rb Set R[2:0]
6.c	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 1 x' x' Ev5 Ev4 Ev3 Ev2 Ev1 Ev0		Set EV Set Ev[5:0]
6.d	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 B2 B1 B0		Set Bias Set B[2:0]
7.a	SET pulse width of Gray scale		Gray-Scale Setting
7.b	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 0 0 0 0 0 0 0 0 1 x' 0		Mode Set.
8.a	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 1 1 1 1		SET Power Control Booster ON Regulator ON Follower ON
8.b	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 1 1 1 1		Display control. Display on
9	IIC INTERFACE Start		restart
10	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
11	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0		Control byte with clear Co bit and A0 set to logic 1
12	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 1 1 0 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here…
13	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.

14	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
15	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
16	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 0 0 1 0 0 0 1 1 0 0 1 0		Data Write.
17	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Data Write.
18	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1		Data Write.
19	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1		Data Write.
20	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1		Data Write.
21	IIC INTERFACE start		restart
22	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
23	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0
24	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 1 1		Display Control. Set Reverse display mode REV=1
25	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0

26	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0		Set column address of RAM. Set address to “00000000”. Y[7:0]=00000000 (Y0 default is 00)
27	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 1 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 1
28	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Data Write.
29	IIC INTERFACE start		restart
30	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
31	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0
32	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Set X address of RAM. Set address to “0000000”.
33	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0

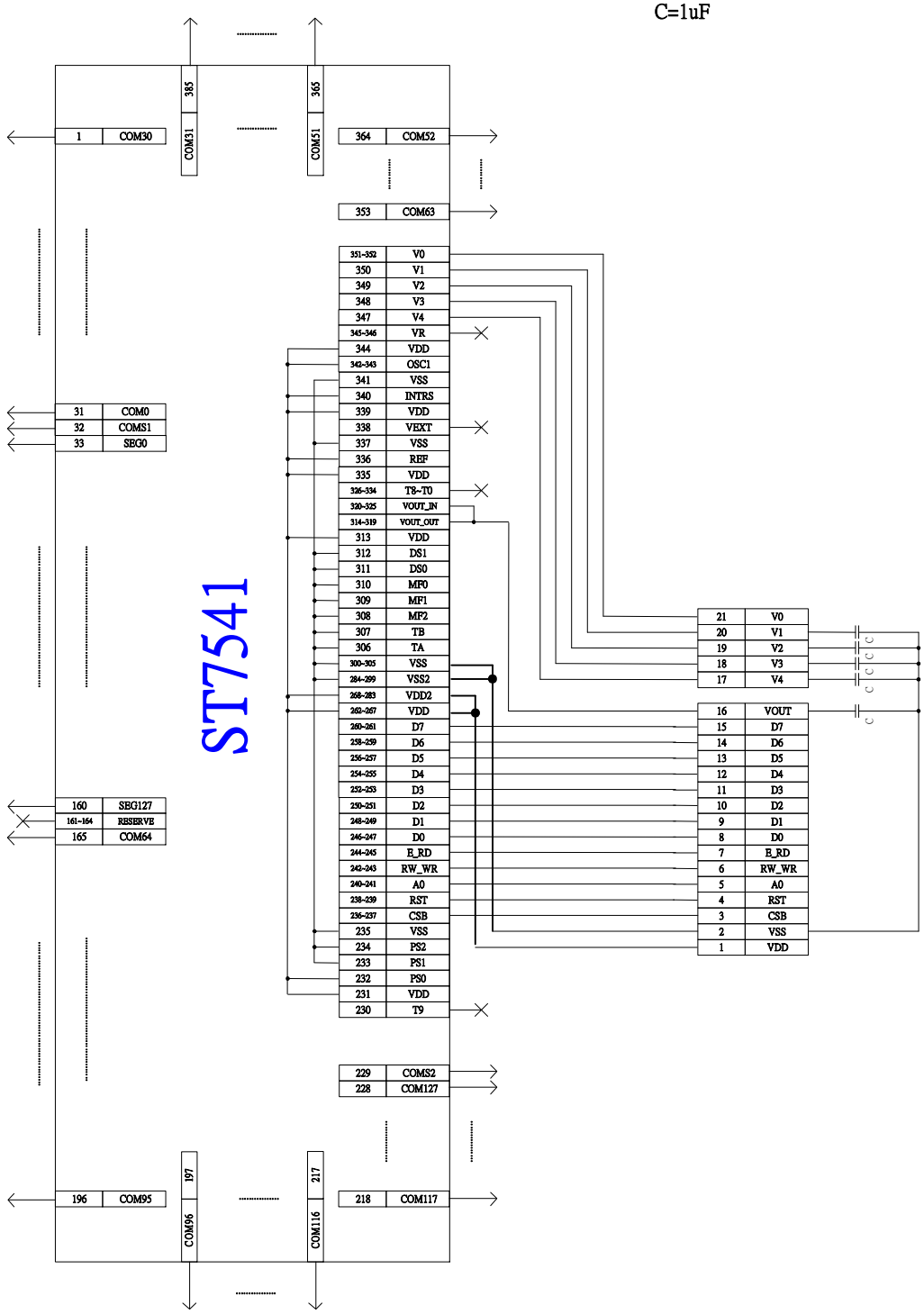
ST7541 APPICATION NOTE

ST7541

Internal analog circuit
Resolution : 129(128COM+ICOM)*128(SEG)
Interface:8080 series
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)

PS0:VDD
PS1:VSS
PS2:VSS
TA:VSS
TB:VSS
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(0,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF

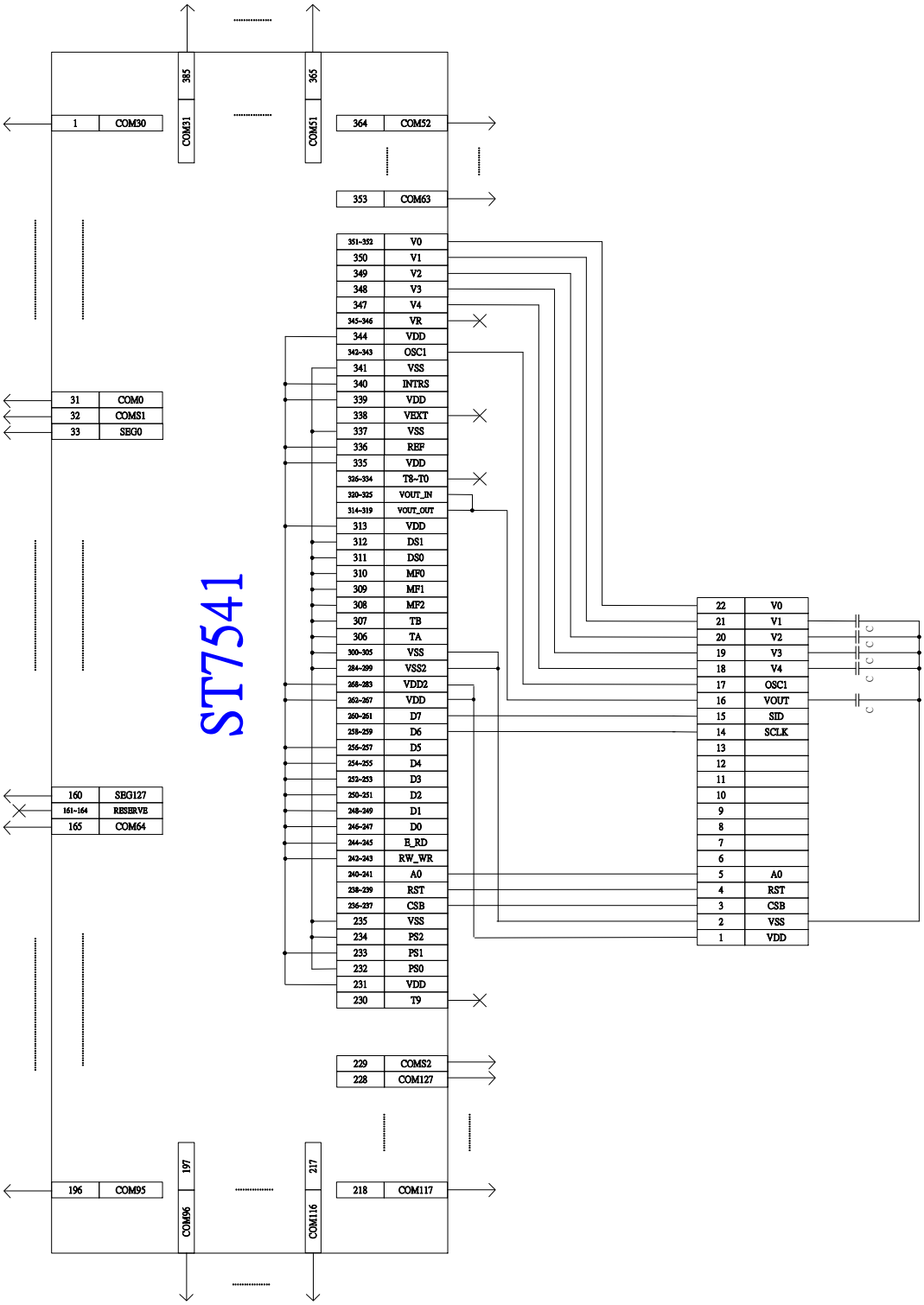


ST7541

Internal analog circuit
Resolution : 129(128COM+ICOM)*128(SEG)
Interface : 4 SPI
OSC1:External for input
(if use internal oscillator,OSC1 must be fixed to VDD)
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0))

PS0:VSS
PS1:VDD
PS2:VSS
TA:VSS
TB:VSS
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(0,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF

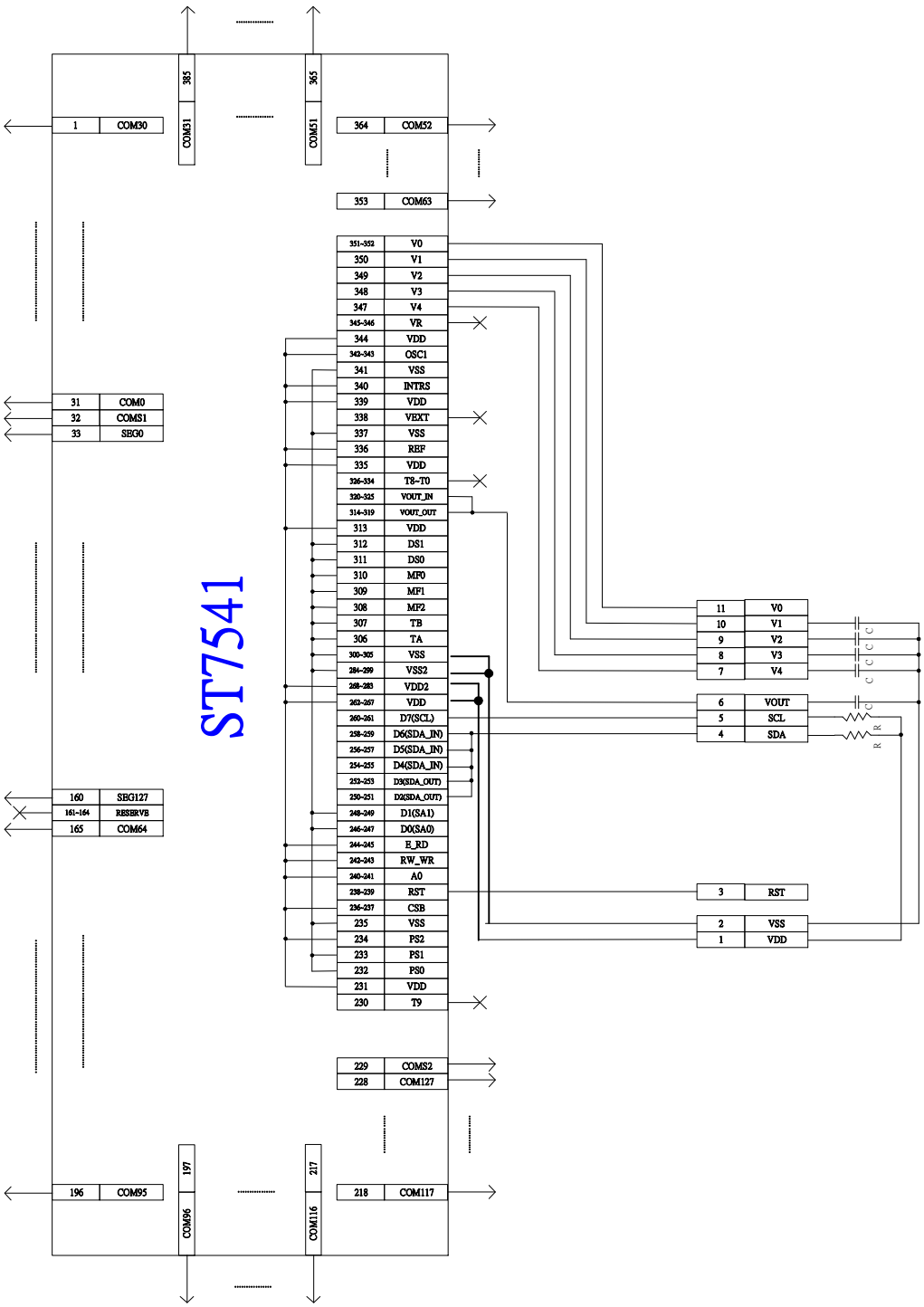


ST7541

Internal analog circuit
Resolution : 129(128COM+ICOM)*128(SEG)
Interface : I2C
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)
SA[1:0]:VDD OR VSS=(0,0)
(SA[1:0] are Slave address of I2C)

PS0:VSS
PS1:VSS
PS2:VDD
TA:VSS
TB:VSS
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(0,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF ; R=10K歐姆



ST7541

Internal analog circuit
Resolution : 129(128COM+ICOM)*128(SEG)
Interface : 3 SPI
OSC1:External for input
(the same pin shoud be connected together,
for example,pin246(D0) connect to pin247(D0)
exclude power pin)

PS0:VSS
PS1:VDD
PS2:VSS
TA:VSS
TB:VSS
REF:VDD
INTRS:VDD

VR:OPEN
VEXT:OPEN
T0~T9:OPEN
MF[2:0]:VDD OR VSS=(0,0,0)
DS[1:0]:VDD OR VSS=(0,0)
(MF[2:0]&DS[1:0] is ID of this IC,
these pins cannot be left open)
C=1uF