



Sitronix

ST7571

4 Gray Scale Dot Matrix LCD Controller/Driver

1. INTRODUCTION

ST7571 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI), I²C or 8-bit parallel display data and stores in an on-chip display data RAM of 128 x 129 x 2 bits. It performs display data RAM write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

4-level (White, Light Gray, Dark Gray, Black) Gray Scale Display with PWM Method

DDRAM Data [2n : 2n+1]		Gray Scale
2n	2n + 1	
0	0	White
0	1	Light gray
1	0	Dark gray
1	1	Black

(Accessible column address, n = 0, 1, 2,, 125, 126, 127)

Driver Output Circuits

128 segment outputs / 128+1 common outputs

Applicable Duty Ratios

- Various partial display
- Partial window moving & data scrolling

On-chip Display Data RAM

- Capacity: 128 x 129 x 2 = 33,024 bits

Microprocessor Interface

- 8-bit parallel interface with 6800-series or 8080-series
- 4-line serial interface (4-line-SPI)
- 3-line serial interface (3-line 8 bits SPI)
- I²C serial interface

On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Build-in Voltage converter (x8)
- Voltage regulator (temperature gradient: -0.13%/°C)
- On-chip contrast control function (64 steps x 8)
- Voltage follower (LCD bias : 1/5 to 1/12)

Operating Voltage Range

- Supply voltage (VDD1): 1.8 to 3.3V
- Supply voltage (VDD2, VDD3): 2.4 to 3.3V

Package Type

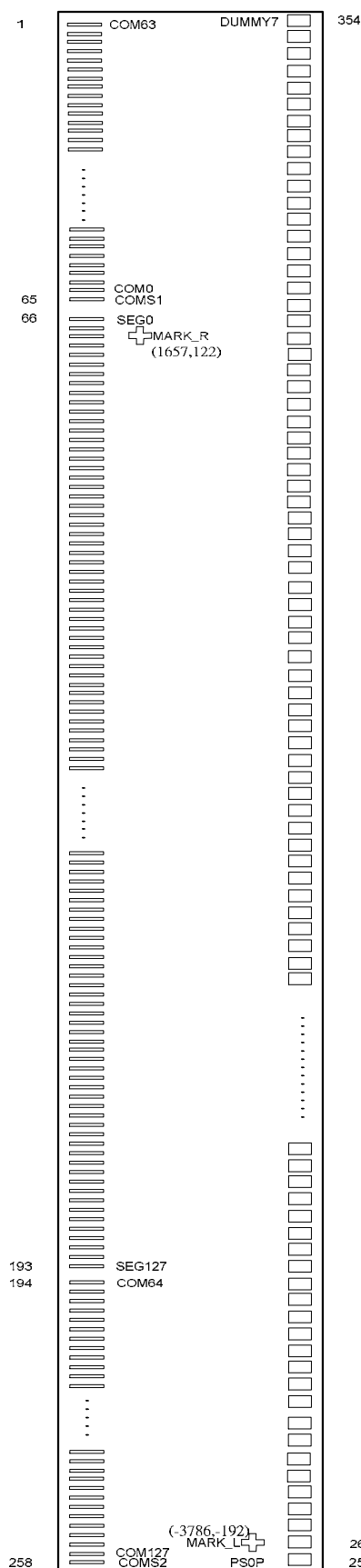
- Application for COG

Built-in EEPROM

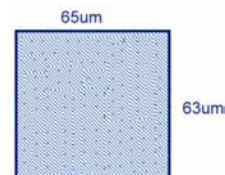
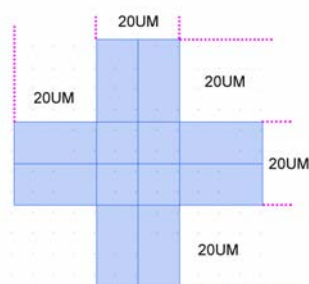
- Store contrast adjustment value for best display

ST7571	6800 , 8080 , 4-Line , 3-Line interface (without I ² C interface)	
ST7571i	I ² C interface	

3. ST7571 PAD ARRANGEMENT (COG)



- | Chip Size : 7956um X 780um
- | Bump Pitch :
I/O PAD : 80um
COM PAD : 33um
SEG PAD : 27um
- | Bump Size :
I/O PAD : 65um X 63 um
COM/SEG PAD : 14um X 128um
- | Bump Height : 15um
- | Chip Thickness : 300 um



I/O Pad



COM/SEG Pad

Fig. 1 ST7571 pad arrangement diagram

4. PAD CENTER COORDINATES

PAD No.	Pin Name	X	Y
1	COM[126]	3896.50	283.00
2	COM[124]	3863.50	283.00
3	COM[122]	3830.50	283.00
4	COM[120]	3797.50	283.00
5	COM[118]	3764.50	283.00
6	COM[116]	3731.50	283.00
7	COM[114]	3698.50	283.00
8	COM[112]	3665.50	283.00
9	COM[110]	3632.50	283.00
10	COM[108]	3599.50	283.00
11	COM[106]	3566.50	283.00
12	COM[104]	3533.50	283.00
13	COM[102]	3500.50	283.00
14	COM[100]	3467.50	283.00
15	COM[98]	3434.50	283.00
16	COM[96]	3401.50	283.00
17	COM[94]	3368.50	283.00
18	COM[92]	3335.50	283.00
19	COM[90]	3302.50	283.00
20	COM[88]	3269.50	283.00
21	COM[86]	3236.50	283.00
22	COM[84]	3203.50	283.00
23	COM[82]	3170.50	283.00
24	COM[80]	3137.50	283.00
25	COM[78]	3104.50	283.00
26	COM[76]	3071.50	283.00
27	COM[74]	3038.50	283.00
28	COM[72]	3005.50	283.00
29	COM[70]	2972.50	283.00
30	COM[68]	2939.50	283.00
31	COM[66]	2906.50	283.00
32	COM[64]	2873.50	283.00
33	COM[62]	2840.50	283.00
34	COM[60]	2807.50	283.00
35	COM[58]	2774.50	283.00

PAD No.	Pin Name	X	Y
36	COM[56]	2741.50	283.00
37	COM[54]	2708.50	283.00
38	COM[52]	2675.50	283.00
39	COM[50]	2642.50	283.00
40	COM[48]	2609.50	283.00
41	COM[46]	2576.50	283.00
42	COM[44]	2543.50	283.00
43	COM[42]	2510.50	283.00
44	COM[40]	2477.50	283.00
45	COM[38]	2444.50	283.00
46	COM[36]	2411.50	283.00
47	COM[34]	2378.50	283.00
48	COM[32]	2345.50	283.00
49	COM[30]	2312.50	283.00
50	COM[28]	2279.50	283.00
51	COM[26]	2246.50	283.00
52	COM[24]	2213.50	283.00
53	COM[22]	2180.50	283.00
54	COM[20]	2147.50	283.00
55	COM[18]	2114.50	283.00
56	COM[16]	2081.50	283.00
57	COM[14]	2048.50	283.00
58	COM[12]	2015.50	283.00
59	COM[10]	1982.50	283.00
60	COM[8]	1949.50	283.00
61	COM[6]	1916.50	283.00
62	COM[4]	1883.50	283.00
63	COM[2]	1850.50	283.00
64	COM[0]	1817.50	283.00
65	COMS1	1784.50	283.00
66	SEG[0]	1714.50	283.00
67	SEG[1]	1687.50	283.00
68	SEG[2]	1660.50	283.00
69	SEG[3]	1633.50	283.00
70	SEG[4]	1606.50	283.00

PAD No.	Pin Name	X	Y
71	SEG[5]	1579.50	283.00
72	SEG[6]	1552.50	283.00
73	SEG[7]	1525.50	283.00
74	SEG[8]	1498.50	283.00
75	SEG[9]	1471.50	283.00
76	SEG[10]	1444.50	283.00
77	SEG[11]	1417.50	283.00
78	SEG[12]	1390.50	283.00
79	SEG[13]	1363.50	283.00
80	SEG[14]	1336.50	283.00
81	SEG[15]	1309.50	283.00
82	SEG[16]	1282.50	283.00
83	SEG[17]	1255.50	283.00
84	SEG[18]	1228.50	283.00
85	SEG[19]	1201.50	283.00
86	SEG[20]	1174.50	283.00
87	SEG[21]	1147.50	283.00
88	SEG[22]	1120.50	283.00
89	SEG[23]	1093.50	283.00
90	SEG[24]	1066.50	283.00
91	SEG[25]	1039.50	283.00
92	SEG[26]	1012.50	283.00
93	SEG[27]	985.50	283.00
94	SEG[28]	958.50	283.00
95	SEG[29]	931.50	283.00
96	SEG[30]	904.50	283.00
97	SEG[31]	877.50	283.00
98	SEG[32]	850.50	283.00
99	SEG[33]	823.50	283.00
100	SEG[34]	796.50	283.00
101	SEG[35]	769.50	283.00
102	SEG[36]	742.50	283.00
103	SEG[37]	715.50	283.00
104	SEG[38]	688.50	283.00
105	SEG[39]	661.50	283.00

PAD No.	Pin Name	X	Y
106	SEG[40]	634.50	283.00
107	SEG[41]	607.50	283.00
108	SEG[42]	580.50	283.00
109	SEG[43]	553.50	283.00
110	SEG[44]	526.50	283.00
111	SEG[45]	499.50	283.00
112	SEG[46]	472.50	283.00
113	SEG[47]	445.50	283.00
114	SEG[48]	418.50	283.00
115	SEG[49]	391.50	283.00
116	SEG[50]	364.50	283.00
117	SEG[51]	337.50	283.00
118	SEG[52]	310.50	283.00
119	SEG[53]	283.50	283.00
120	SEG[54]	256.50	283.00
121	SEG[55]	229.50	283.00
122	SEG[56]	202.50	283.00
123	SEG[57]	175.50	283.00
124	SEG[58]	148.50	283.00
125	SEG[59]	121.50	283.00
126	SEG[60]	94.50	283.00
127	SEG[61]	67.50	283.00
128	SEG[62]	40.50	283.00
129	SEG[63]	13.50	283.00
130	SEG[64]	-13.50	283.00
131	SEG[65]	-40.50	283.00
132	SEG[66]	-67.50	283.00
133	SEG[67]	-94.50	283.00
134	SEG[68]	-121.50	283.00
135	SEG[69]	-148.50	283.00
136	SEG[70]	-175.50	283.00
137	SEG[71]	-202.50	283.00
138	SEG[72]	-229.50	283.00
139	SEG[73]	-256.50	283.00
140	SEG[74]	-283.50	283.00

PAD No.	Pin Name	X	Y
141	SEG[75]	-310.50	283.00
142	SEG[76]	-337.50	283.00
143	SEG[77]	-364.50	283.00
144	SEG[78]	-391.50	283.00
145	SEG[79]	-418.50	283.00
146	SEG[80]	-445.50	283.00
147	SEG[81]	-472.50	283.00
148	SEG[82]	-499.50	283.00
149	SEG[83]	-526.50	283.00
150	SEG[84]	-553.50	283.00
151	SEG[85]	-580.50	283.00
152	SEG[86]	-607.50	283.00
153	SEG[87]	-634.50	283.00
154	SEG[88]	-661.50	283.00
155	SEG[89]	-688.50	283.00
156	SEG[90]	-715.50	283.00
157	SEG[91]	-742.50	283.00
158	SEG[92]	-769.50	283.00
159	SEG[93]	-796.50	283.00
160	SEG[94]	-823.50	283.00
161	SEG[95]	-850.50	283.00
162	SEG[96]	-877.50	283.00
163	SEG[97]	-904.50	283.00
164	SEG[98]	-931.50	283.00
165	SEG[99]	-958.50	283.00
166	SEG[100]	-985.50	283.00
167	SEG[101]	-1012.50	283.00
168	SEG[102]	-1039.50	283.00
169	SEG[103]	-1066.50	283.00
170	SEG[104]	-1093.50	283.00
171	SEG[105]	-1120.50	283.00
172	SEG[106]	-1147.50	283.00
173	SEG[107]	-1174.50	283.00
174	SEG[108]	-1201.50	283.00
175	SEG[109]	-1228.50	283.00

PAD No.	Pin Name	X	Y
176	SEG[110]	-1255.50	283.00
177	SEG[111]	-1282.50	283.00
178	SEG[112]	-1309.50	283.00
179	SEG[113]	-1336.50	283.00
180	SEG[114]	-1363.50	283.00
181	SEG[115]	-1390.50	283.00
182	SEG[116]	-1417.50	283.00
183	SEG[117]	-1444.50	283.00
184	SEG[118]	-1471.50	283.00
185	SEG[119]	-1498.50	283.00
186	SEG[120]	-1525.50	283.00
187	SEG[121]	-1552.50	283.00
188	SEG[122]	-1579.50	283.00
189	SEG[123]	-1606.50	283.00
190	SEG[124]	-1633.50	283.00
191	SEG[125]	-1660.50	283.00
192	SEG[126]	-1687.50	283.00
193	SEG[127]	-1714.50	283.00
194	COM[1]	-1784.50	283.00
195	COM[3]	-1817.50	283.00
196	COM[5]	-1850.50	283.00
197	COM[7]	-1883.50	283.00
198	COM[9]	-1916.50	283.00
199	COM[11]	-1949.50	283.00
200	COM[13]	-1982.50	283.00
201	COM[15]	-2015.50	283.00
202	COM[17]	-2048.50	283.00
203	COM[19]	-2081.50	283.00
204	COM[21]	-2114.50	283.00
205	COM[23]	-2147.50	283.00
206	COM[25]	-2180.50	283.00
207	COM[27]	-2213.50	283.00
208	COM[29]	-2246.50	283.00
209	COM[31]	-2279.50	283.00
210	COM[33]	-2312.50	283.00

PAD No.	Pin Name	X	Y
211	COM[35]	-2345.50	283.00
212	COM[37]	-2378.50	283.00
213	COM[39]	-2411.50	283.00
214	COM[41]	-2444.50	283.00
215	COM[43]	-2477.50	283.00
216	COM[45]	-2510.50	283.00
217	COM[47]	-2543.50	283.00
218	COM[49]	-2576.50	283.00
219	COM[51]	-2609.50	283.00
220	COM[53]	-2642.50	283.00
221	COM[55]	-2675.50	283.00
222	COM[57]	-2708.50	283.00
223	COM[59]	-2741.50	283.00
224	COM[61]	-2774.50	283.00
225	COM[63]	-2807.50	283.00
226	COM[65]	-2840.50	283.00
227	COM[67]	-2873.50	283.00
228	COM[69]	-2906.50	283.00
229	COM[71]	-2939.50	283.00
230	COM[73]	-2972.50	283.00
231	COM[75]	-3005.50	283.00
232	COM[77]	-3038.50	283.00
233	COM[79]	-3071.50	283.00
234	COM[81]	-3104.50	283.00
235	COM[83]	-3137.50	283.00
236	COM[85]	-3170.50	283.00
237	COM[87]	-3203.50	283.00
238	COM[89]	-3236.50	283.00
239	COM[91]	-3269.50	283.00
240	COM[93]	-3302.50	283.00
241	COM[95]	-3335.50	283.00
242	COM[97]	-3368.50	283.00
243	COM[99]	-3401.50	283.00
244	COM[101]	-3434.50	283.00
245	COM[103]	-3467.50	283.00

PAD No.	Pin Name	X	Y
246	COM[105]	-3500.50	283.00
247	COM[107]	-3533.50	283.00
248	COM[109]	-3566.50	283.00
249	COM[111]	-3599.50	283.00
250	COM[113]	-3632.50	283.00
251	COM[115]	-3665.50	283.00
252	COM[117]	-3698.50	283.00
253	COM[119]	-3731.50	283.00
254	COM[121]	-3764.50	283.00
255	COM[123]	-3797.50	283.00
256	COM[125]	-3830.50	283.00
257	COM[127]	-3863.50	283.00
258	COMS2	-3896.50	283.00
259	PS0	-3858.00	-315.50
260	VSS1	-3778.00	-315.50
261	PS1	-3698.00	-315.50
262	VDD1	-3618.00	-315.50
263	PS2	-3538.00	-315.50
264	VSS1	-3458.00	-315.50
265	CSB	-3378.00	-315.50
266	RST	-3298.00	-315.50
267	A0	-3218.00	-315.50
268	EWR	-3138.00	-315.50
269	ERD	-3058.00	-315.50
270	D0	-2978.00	-315.50
271	D1	-2898.00	-315.50
272	D2	-2818.00	-315.50
273	D3	-2738.00	-315.50
274	D4	-2658.00	-315.50
275	D5	-2578.00	-315.50
276	D6	-2498.00	-315.50
277	D7	-2418.00	-315.50
278	RST	-2338.00	-315.50
279	CSB	-2258.00	-315.50
280	VDD1	-2178.00	-315.50

PAD No.	Pin Name	X	Y
281	VDD1	-2098.00	-315.50
282	VDD1	-2018.00	-315.50
283	VDD2	-1938.00	-315.50
284	VDD2	-1858.00	-315.50
285	VDD2	-1778.00	-315.50
286	VDD2	-1698.00	-315.50
287	VDD3	-1618.00	-315.50
288	VDD3	-1538.00	-315.50
289	VSS3	-1458.00	-315.50
290	VSS3	-1378.00	-315.50
291	VSS2	-1298.00	-315.50
292	VSS2	-1218.00	-315.50
293	VSS2	-1138.00	-315.50
294	VSS2	-1058.00	-315.50
295	VSS1	-978.00	-315.50
296	VSS1	-898.00	-315.50
297	VSS1	-818.00	-315.50
298	VSS1	-738.00	-315.50
299	VDD2	-658.00	-315.50
300	VDD2	-578.00	-315.50
301	VDD2	-498.00	-315.50
302	VDD2	-418.00	-315.50
303	VDD3	-338.00	-315.50
304	VDD3	-258.00	-315.50
305	MF2	-178.00	-315.50
306	MF1	-98.00	-315.50
307	MF0	-18.00	-315.50
308	DS0	62.00	-315.50
309	DS1	142.00	-315.50
310	VMO	222.00	-315.50
311	VMO	302.00	-315.50
312	VMO	382.00	-315.50
313	VSS2	462.00	-315.50
314	V0I	542.00	-315.50
315	V0I	622.00	-315.50

PAD No.	Pin Name	X	Y
316	V0I	702.00	-315.50
317	V0I	782.00	-315.50
318	V0S	862.00	-315.50
319	V0O	942.00	-315.50
320	V0O	1022.00	-315.50
321	XV0O	1102.00	-315.50
322	XV0O	1182.00	-315.50
323	XV0S	1262.00	-315.50
324	XV0I	1385.00	-315.50
325	XV0I	1465.00	-315.50
326	XV0I	1545.00	-315.50
327	XV0I	1625.00	-315.50
328	VDD1	1705.00	-315.50
329	VEXT	1785.00	-315.50
330	OSC1	1865.00	-315.50
331	DCPS	1945.00	-315.50
332	VSS1	2025.00	-315.50
333	CSEL	2105.00	-315.50
334	VD1I	2185.00	-315.50
335	VD1I	2265.00	-315.50
336	VD1O	2345.00	-315.50
337	VGO	2425.00	-315.50
338	VGO	2505.00	-315.50
339	VGS	2585.00	-315.50
340	VGI	2665.00	-315.50
341	VGI	2745.00	-315.50
342	VGI	2825.00	-315.50
343	VGI	2905.00	-315.50
344	VPP	2985.00	-315.50
345	VPP	3065.00	-315.50
346	VPP	3145.00	-315.50
347	VE	3225.00	-315.50
348	DUMMY1	3341.00	-315.50
349	DUMMY2	3421.00	-315.50
350	DUMMY3	3501.00	-315.50

PAD No.	Pin Name	X	Y
351	DUMMY4	3581.00	-315.50
352	DUMMY5	3661.00	-315.50
353	DUMMY6	3741.00	-315.50
354	DUMMY7	3821.00	-315.50

Note:

1. CSEL=H.
2. Unit: um.

5. BLOCK DIAGRAM

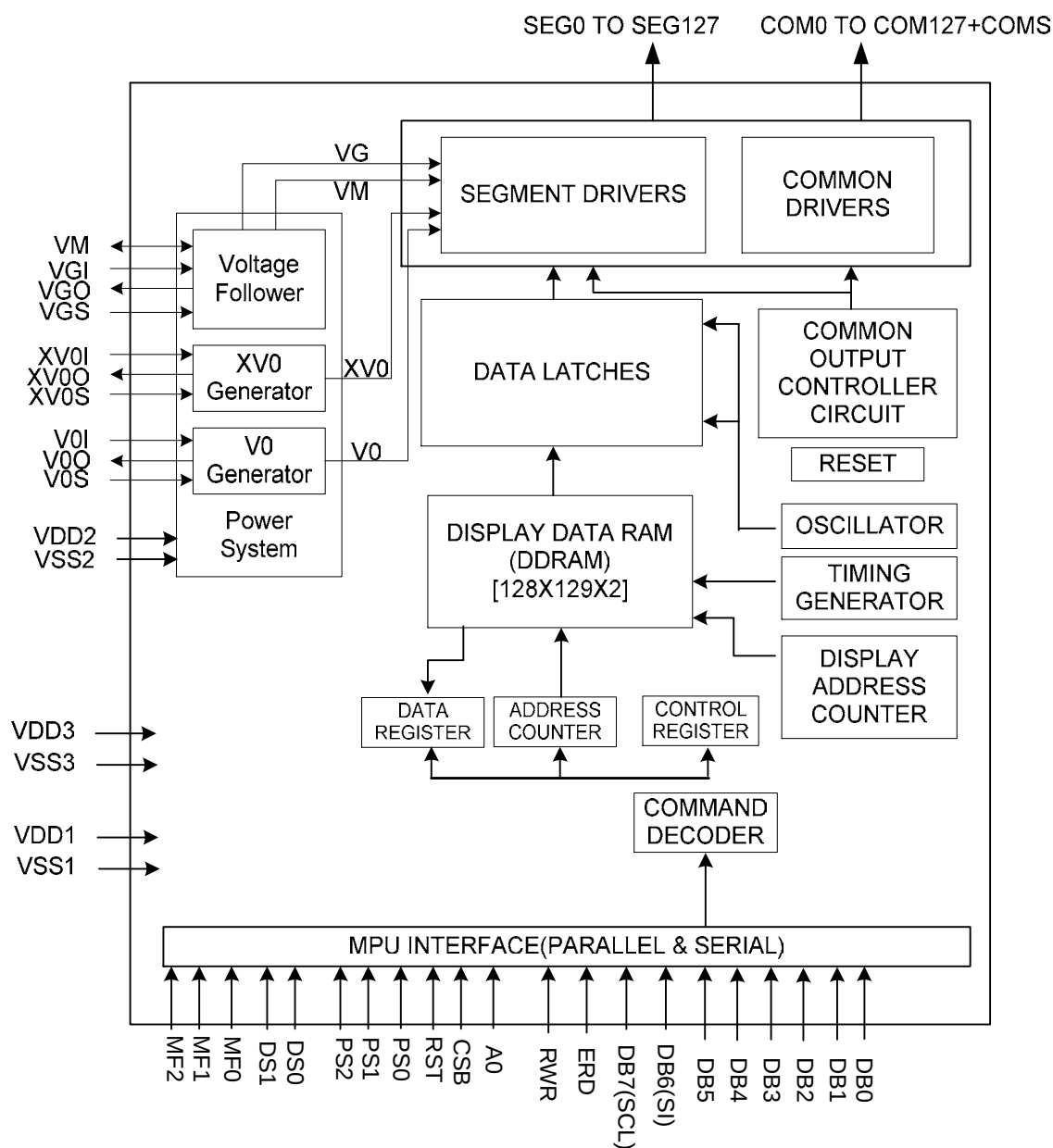


Fig.2 Block diagram

6. PIN DESCRIPTION

6.1 POWER SUPPLY

Power Supply Pin Description

Name	I/O	Description
VDD1	Power	Power supply for digital circuit. If VDD1 is the same level as VDD2, they can be connected together by FPC.
VDD2	Power	Power supply for analog circuit (booster).
VDD3	Power	Power supply for sensitive circuit (internal Vref regulator). VDD3 is the same level as VDD2, and they should be connected together by FPC.
VSS1	Power	Ground for digital circuit. VSS1, VSS2 & VSS3 should be connected together by FPC.
VSS2	Power	Ground for analog circuit (booster), it should be connected together by FPC.
VSS3	Power	Ground for sensitive circuit (Vref regulator), it should be connected together by FPC.

6.2 LCD DRIVER SUPPLY

LCD Driver Supply Pin Description

Name	I/O	Description						
V0O V0I V0S	Power	V0 is the LCD driving voltage for common circuits at negative frame. V0O is the output of V0 regulator. V0S is the feedback of V0 regulator. V0I is the V0 input of common circuits. Be sure that: $V0 \geq VG > VM > VSS \geq XV0$ (under operation). V0O, V0I & V0S should be connected together by FPC.						
XV0O XV0I XV0S	Power	XV0 is the LCD driving voltage for common circuits at positive frame. XV0O is the output of XV0 regulator. XV0S is the feedback of XV0 regulator. XV0I is the XV0 input of common circuits. XV0O, XV0I & XV0S should be connected together by FPC.						
VGO VGI VGS	Power	VG is the LCD driving voltage for segment circuits. A storage capacitor on FPC or system for VG is required. VGO is the output of VG regulator. VGS is the feedback of VG regulator. VGI is the VG input of segment circuits. VGO, VGI & VGS should be connected together by FPC. Be aware that: $1.8V \leq VG < VDD2$.						
VMO	Power	VMO is the output of VM, which is the LCD driving voltage for common circuits. A storage capacitor on FPC or system for VM is required. Be aware that: $0.7V < VM < VDD2$. When the internal power circuit is active, the VG and VM are generated according to the bias setting as shown below: <table border="1" data-bbox="416 1664 1042 1749"> <tr> <td>LCD bias</td><td>VG</td><td>VM</td></tr> <tr> <td>1/N bias</td><td>$(2/N) \times V0$</td><td>$(1/N) \times V0$</td></tr> </table> NOTE: N = 5 to 12	LCD bias	VG	VM	1/N bias	$(2/N) \times V0$	$(1/N) \times V0$
LCD bias	VG	VM						
1/N bias	$(2/N) \times V0$	$(1/N) \times V0$						

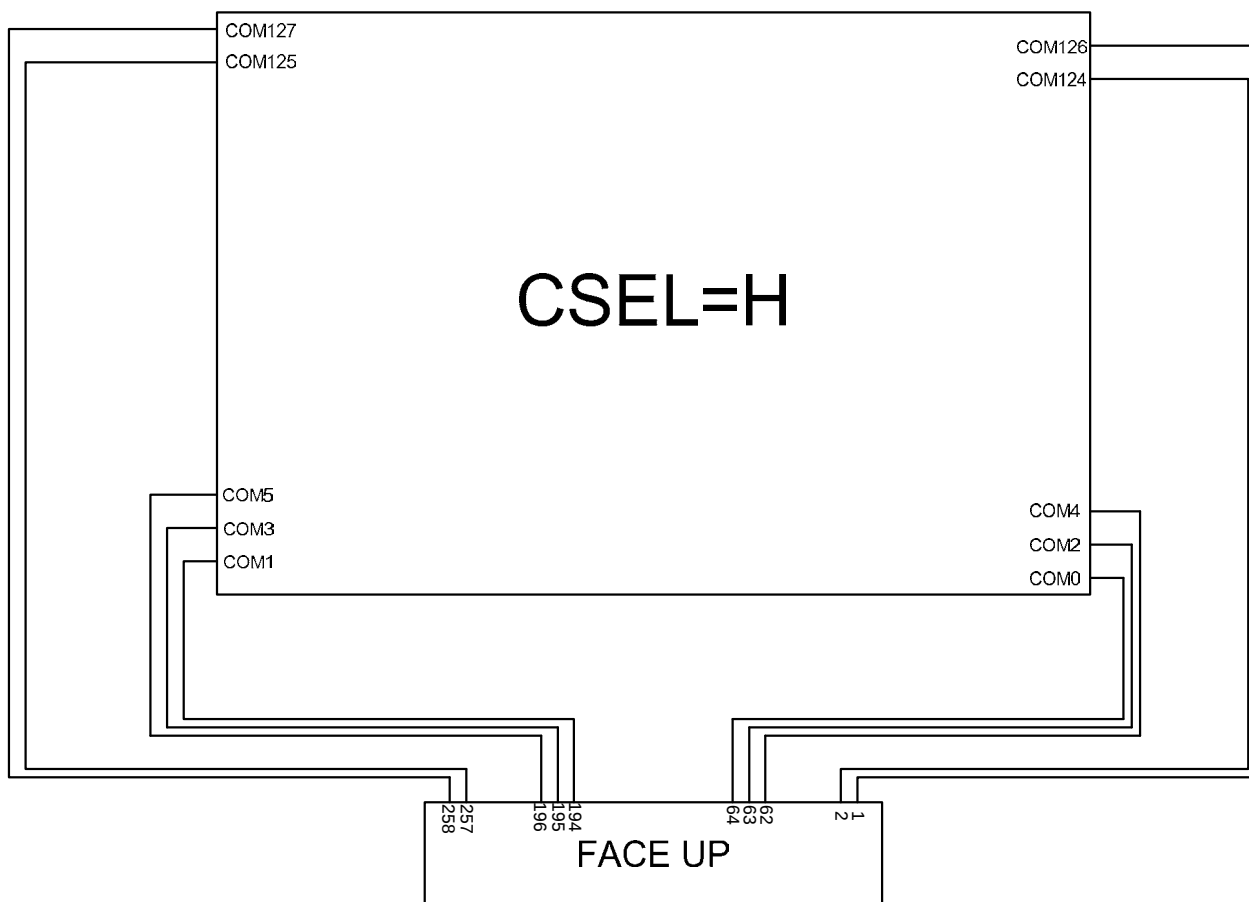
6.3 SYSTEM CONTROL

System Control Pin Description

Name	I/O	Description
VEXT	O	Reserved for testing, must set with floating.
OSC1	I	Connect OSC1 to VDD1.
DCPS	I	This pin selects the supply voltage source of the digital circuit. If system VDD1 is 3V or 3.3V, set DCPS=L to select Internal Regulator as digital circuit power. If system VDD1 is 1.8V or 2.8V (Max=3.0V), set DCPS=H to select VDD1 as digital circuit power.
CSEL	I	Select COM output sequence. Fix CSEL=H to enable “Interlace” mode (recommended). In interlace mode, COM2n (even number) is in the one side, COM(2n+1) (odd number) is in the opposite side.
VD1I VD1O	O	When DCPS=L, output voltage=2.4V. When DCPS=H, output voltage=VDD1.
VE	I	When writing EEPROM, VE should be pull-high externally.
VPP	I	When writing EEPROM, it needs external power supply voltage.
MF[2:0]	I	Reserve for testing only, recommend setting to [MF2,MF1,MF0 = 0,0,0].
DS[1:0]	I	Reserve for testing only, recommend setting to [DS1,DS0 = 0,0].

Notes:

1. When system control pin set to “H”, it should be connected to VDD1.
2. When system control pin set to “L”, it should be connected to VSS1.
3. CSEL function is illustrated as the figure below:



6.4 MICROPROCESSOR INTERFACE

Microprocessor Interface Pin Description

Name	I/O	Description																								
RST	I	Reset input pin. When RST is “L”, initialization is executed.																								
PS[2:0]	I	PS[2:0] select the microprocessor interface: <table><tr><td>PS2</td><td>PS1</td><td>PS0</td><td>Selected Interface Mode</td></tr><tr><td>L</td><td>L</td><td>H</td><td>Parallel 8080 MPU Interface</td></tr><tr><td>L</td><td>H</td><td>H</td><td>Parallel 6800 MPU Interface</td></tr><tr><td>L</td><td>L</td><td>L</td><td>Serial 3-Line Interface</td></tr><tr><td>L</td><td>H</td><td>L</td><td>Serial 4-Line Interface</td></tr><tr><td>H</td><td>L</td><td>L</td><td>Serial I²C Interface</td></tr></table> * NOTE: It is impossible to read data from the on-chip DDRAM. For detailed interface connection, please refer to Section 7.1 and Application Circuits.	PS2	PS1	PS0	Selected Interface Mode	L	L	H	Parallel 8080 MPU Interface	L	H	H	Parallel 6800 MPU Interface	L	L	L	Serial 3-Line Interface	L	H	L	Serial 4-Line Interface	H	L	L	Serial I ² C Interface
PS2	PS1	PS0	Selected Interface Mode																							
L	L	H	Parallel 8080 MPU Interface																							
L	H	H	Parallel 6800 MPU Interface																							
L	L	L	Serial 3-Line Interface																							
L	H	L	Serial 4-Line Interface																							
H	L	L	Serial I ² C Interface																							
CSB	I	Chip select input pin. The interface is enabled only when CSB is "L" (except I ² C Interface). When CSB is non-active, DB[7:0] are high impedance. CSB is not used in I ² C interface; it is recommended to fix CSB at “H” by VDD1.																								
A0	I	Register select input pin. A0 = “H”: DB0 to DB7 are display data. A0 = “L”: DB0 to DB7 are control command. A0 is not used in serial 3-Line and I ² C interface; it is recommended to fix A0 at “H” by VDD1.																								
RWR	I	Write execution control pin. <table><tr><td>PS2</td><td>PS1</td><td>PS0</td><td>MPU Type</td><td>RWR</td><td>Description</td></tr><tr><td>L</td><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>Write control input pin. Keep this pin at “L” level.</td></tr><tr><td>L</td><td>L</td><td>H</td><td>8080-series</td><td>/WR</td><td>The data on DB[7:0] are latched at the rising edge of the /WR signal.</td></tr></table>	PS2	PS1	PS0	MPU Type	RWR	Description	L	H	H	6800-series	R/W	Write control input pin. Keep this pin at “L” level.	L	L	H	8080-series	/WR	The data on DB[7:0] are latched at the rising edge of the /WR signal.						
PS2	PS1	PS0	MPU Type	RWR	Description																					
L	H	H	6800-series	R/W	Write control input pin. Keep this pin at “L” level.																					
L	L	H	8080-series	/WR	The data on DB[7:0] are latched at the rising edge of the /WR signal.																					
ERD	I	Read / Write execution control pin. <table><tr><td>PS2</td><td>PS1</td><td>PS0</td><td>MPU Type</td><td>ERD</td><td>Description</td></tr><tr><td>L</td><td>H</td><td>H</td><td>6800-series</td><td>E</td><td>The data on DB[7:0] are latched at the falling edge of the E signal.</td></tr><tr><td>L</td><td>L</td><td>H</td><td>8080-series</td><td>/RD</td><td>Keep this pin at “H” level.</td></tr></table>	PS2	PS1	PS0	MPU Type	ERD	Description	L	H	H	6800-series	E	The data on DB[7:0] are latched at the falling edge of the E signal.	L	L	H	8080-series	/RD	Keep this pin at “H” level.						
PS2	PS1	PS0	MPU Type	ERD	Description																					
L	H	H	6800-series	E	The data on DB[7:0] are latched at the falling edge of the E signal.																					
L	L	H	8080-series	/RD	Keep this pin at “H” level.																					

Name	I/O	Description
DB[7:0]	I	When using parallel interface: DB[7:0] are 8-bit data bus. DB[7:0] are connected to the 8-bit data bus of a standard microprocessor. When chip select is not active (CSB=H), DB[7:0] are high impedance.
	I	When using 3-Line/4-Line serial interface: DB7: serial input data (SID). DB6: serial input clock (SCLK). DB[5:0] are high impedance and must be fixed to "H". When chip select is not active (CSB=H), DB[7:0] are high impedance.
	I/O	When using I²C interface: DB7: SCL, serial clock input. DB[6:4]: SDA_IN, serial input data. DB[3:2]: SDA_OUT, output the acknowledge signal of the I ² C interface protocol. <u>DB[6:2] must be connected together (SDA).</u> ^{*1} DB[1:0]: SA[1:0], I ² C slave address bits of ST7571. Must connect to VDD1 or VSS1.

1. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I²C interface compatible. Separating acknowledge-output from serial data input is advantageous for chip-on-glass (COG) applications. In COG applications, the ITO resistance and the pull-up resistor will form a voltage divider, which affects acknowledge-signal level. Larger ITO resistance will raise the acknowledged-signal level and system cannot recognize this level as a valid logic "0" level. By separating SDA_IN from SDA_OUT, the IC can be used in a mode that ignores the acknowledge-bit. For applications which check acknowledge-bit, it is necessary to minimize the ITO resistance of the SDA_OUT trace to guarantee a valid low level.
2. After VDD1 is turned ON, any MPU interface pins cannot be left floating.

6.5 LCD DRIVER OUTPUTS**LCD Driver Output Pin Description**

Name	I/O	Description			
SEG0 to SEG127	O	LCD segment driver outputs The display data and the M signal control the output voltage of segment driver.			
		Display Data	Frame	Segment Driver Output Voltage	
				Normal Display	Reverse Display
		H	Positive	VG	VSS
		H	Negative	VSS	VG
		L	Positive	VSS	VG
		L	Negative	VG	VSS
		Display off / Power save mode		VSS	VSS
COM0 to COM127	O	LCD common driver outputs The internal scanning data and M signal control the output voltage of common driver.			
		Scan Data	Frame	Common Driver Output Voltage	
		H	Positive	XV0	
		H	Negative	V0	
		L	Positive	VM	
		L	Negative	VM	
		Display off / Power save mode		VSS	
COMS2 COMS1	O	Common output for the icons The output signals of two pins are same. When not used, these pins should be left open.			

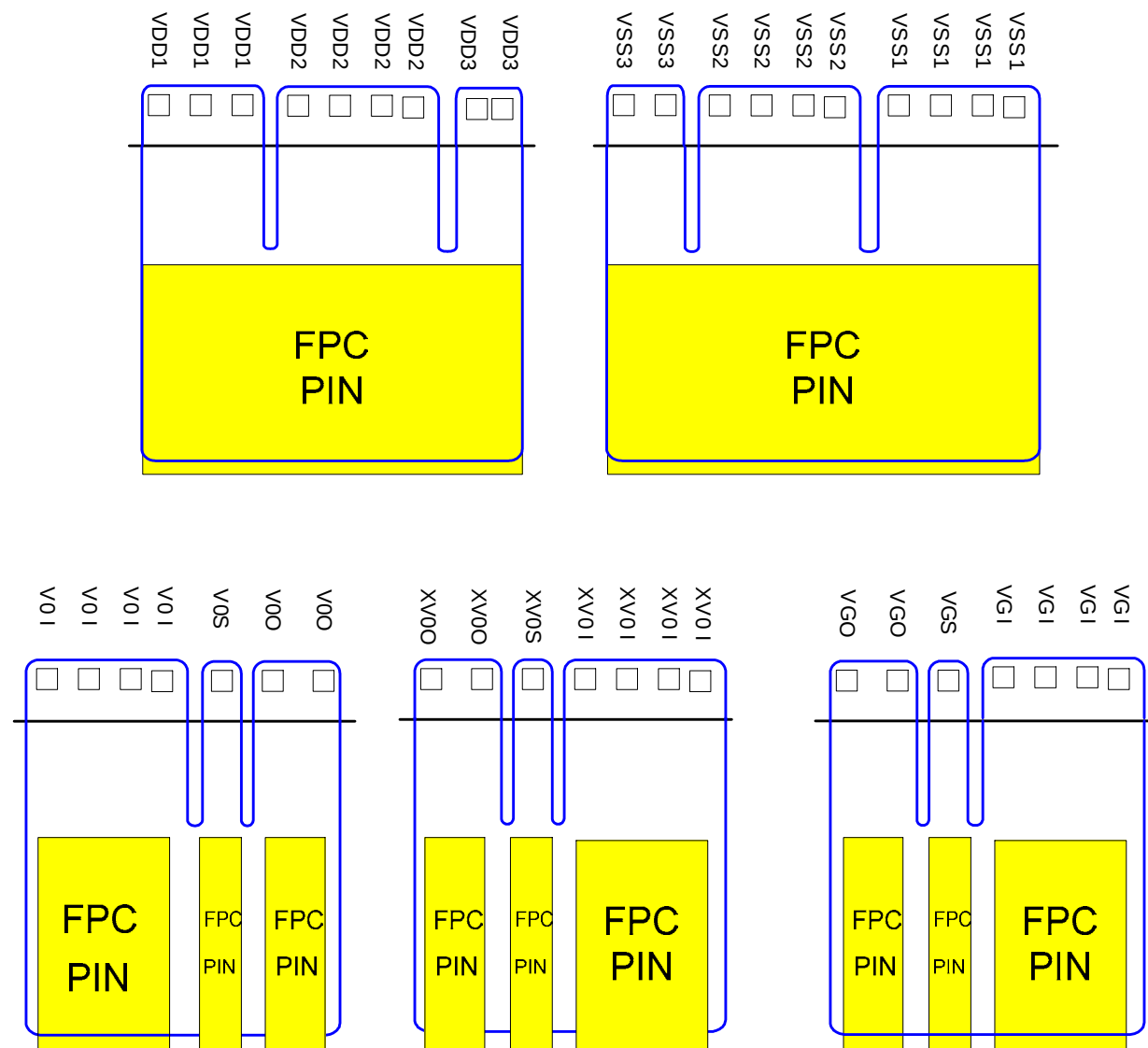
Recommend I/O Resistance

PIN Name	ITO Resister
PS[2:0], OCS1, VEXT, DCPS, MF[2:0], DS[1:0]	<5k Ω
VDD1, VDD2, VDD3, VSS1, VSS2, VSS3, VPP, VD1I, VD1O	<100 Ω
CSB, ERD, RWR, A0, DB[7:0], VE	<1K Ω
V0, VG, VM, XV0, VD1	<500 Ω
RST	<10K Ω

Note:

- These Limitations include the bottleneck of ITO layout.
- Keep the ITO resistance of COM0 ~ COM127 be equal, and so it is of SEG0 ~ SEG127.
- To avoid the noise in different power system affect other power system, please separate different power source on ITO layout. Please refer to the ITO Layout Reference.
- The V0, XV0 and Vg power circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC.

ITO Layout Reference



7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

CSB pin is used for chip selection. ST7571 can interface with an MPU when CSB is "L". When CSB is "H", the inputs of A0, ERD and RWR with any combination will be ignored and DB[7:0] are high impedance. In 3-Line and 4-Line serial interface, the internal shift register and serial counter are reset when CSB is "H".

Parallel / Serial Interface

ST7571 has types of interface for kinds of MPU. The MPU interface is selected by PS[2:0] pins as shown in Table 1. The read-function is not available.

Table 1 Parallel / Serial Interface Mode

PS2	PS1	PS0	Type	CSB	A0	ERD	RWR	MPU Interface
L	L	H	Parallel	CSB	A0	/RD	/WR	8080-series parallel interface
L	H	H				E	R/W	6800-series parallel interface
L	L	L	Serial	CSB	---	---	---	3-Line SPI interface
L	H	L			A0	---	---	4-Line SPI interface
H	L	L		---	---	---	---	I ² C Interface

* The un-used pins are marked as "---" and should be fixed to "H" by VDD1.

Parallel Interface (PS2 = "L" & PS0 = "H")

The 8-bit data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in Table 2. The type of data transfer is determined by signals at A0, ERD and RWR as shown in Table 3.

Table 2 Microprocessor Selection for Parallel Interface

PS1	CSB	A0	ERD	RWR	DB[7:0]	MPU bus
L	CSB	A0	/RD	/WR	DB[7:0]	8080-series
H	CSB	A0	E	R/W	DB[7:0]	6800-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	ERD (E)	RWR (R/W)	ERD (/RD)	RWR (/WR)	
L	H	L	H	L	Writes to internal register (instruction)
H	H	L	H	L	Display data write

Serial Interface Selection

By setting PS[2:0], one of the Serial Interfaces can be selected.

Serial mode	PS2	PS1	PS0	CSB	A0	ERD	RWR	DB[7:0]
3-Line SPI mode	L	L	L	CSB	--	--	--	DB7=SID, DB6=SCLK
4-Line SPI mode	L	H	L	CSB	A0	--	--	DB[5:0]= --
I ² C SPI mode	H	L	L	--	--	--	--	Refer to I ² C Interface. DB7=SCL, DB[6:4]=SDA_IN, DB[3:2]=SDA_OUT, DB[1:0]=SA[1:0]

* The un-used pins are marked as "--" and should be fixed to "H" by VDD1.

Note:

1. The pin setting to be "H" should connect to VDD1.
2. The pin setting to be "L" should connect to VSS1.

4-Line SPI Mode (PS0 = "L", PS1 = "H", PS2 = "L")

When ST7571 is active (CSB="L"), serial data (SDA) and serial clock (SCLK) inputs are enabled. When ST7571 is not active (CSB="H"), the internal 8-bit shift register and 3-bit counter are reset. The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. The read feature is not supported. Serial data on SDA is latched at the rising edge of serial clock on SCLK. After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

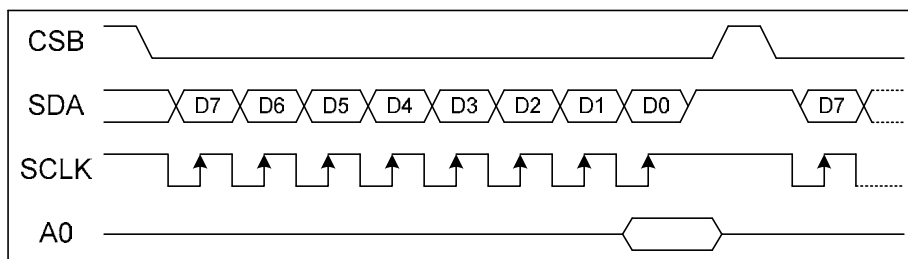


Fig. 3 4-line SPI Timing

3-Line SPI Mode (PS0 = "L", PS1 = "L", PS2 = "L")

In 3-Line mode, default message from MCU is command. The Display Data Length command (2 bytes command) must be set before writing display data into Display Data RAM, after the display data is sent over, the next message is turned to be command. Signals on SID are latched at the rising edge of SCLK. After receiving 8-bit display data, the column address pointer of DDRAM will be increased by one automatically.

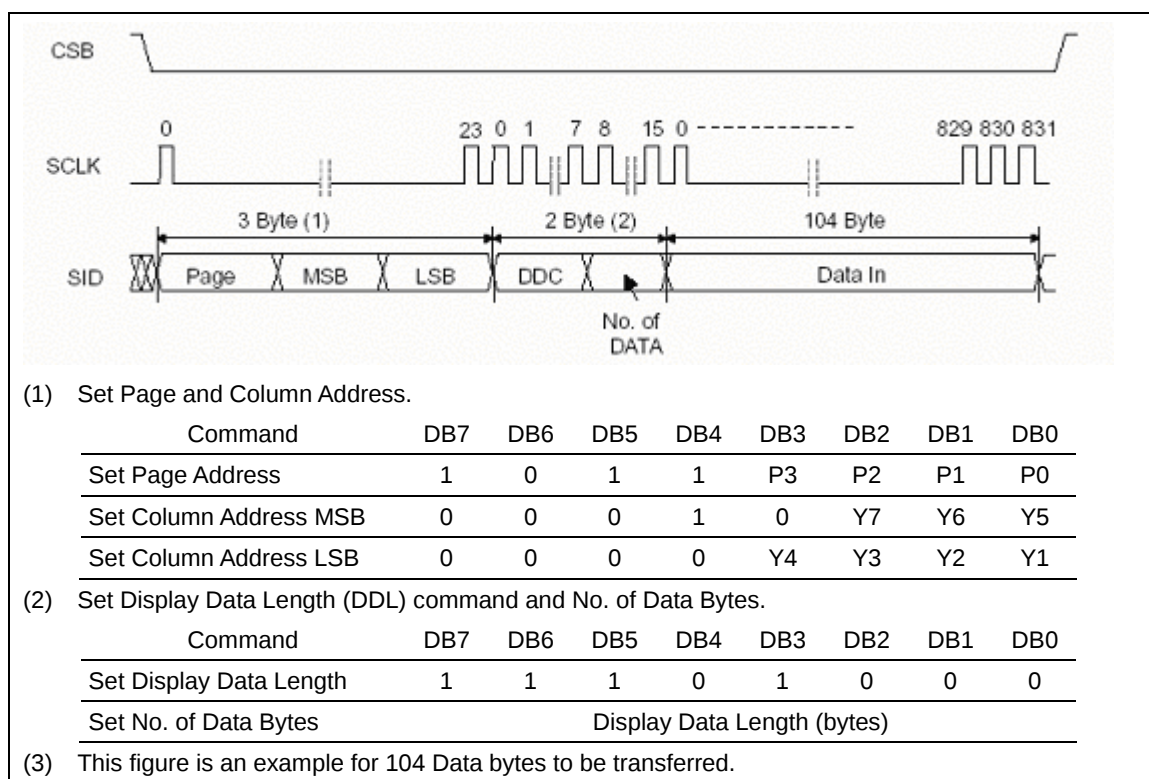


Fig. 4 3-Line SPI Timing (A0 is not used)

Use this command in 3-Line SPI mode only. It is two continuous commands: the first one informs the LCD driver and the second one is the number of input data (in bytes). After these two commands, the following messages will be data, till the data counter is cleared. If data is stopped during transmitting, it is not valid data. A new data should be transferred with most significant bit first.

NOTE: If CSB is disabled before the end of a transmission, it stops this transfer and the next access should be re-initialized.

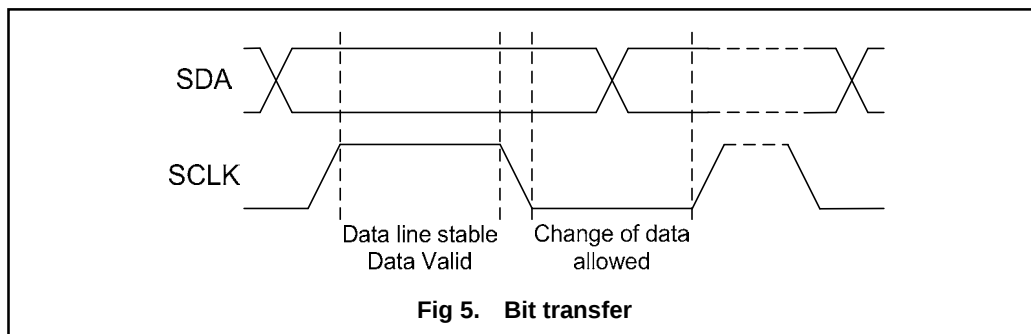
I²C Interface (PS0= "L", PS1= "L", PS2= "H")

The I²C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCLK). Both lines must be connected with a pull-up resistor which drives SDA and SCLK to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

The I²C interface of ST7571 supports write access and read of acknowledge-bit. The I²C interface receives and executes the commands sent via the I²C Interface. It also receives RAM data and sends it to the Display RAM.

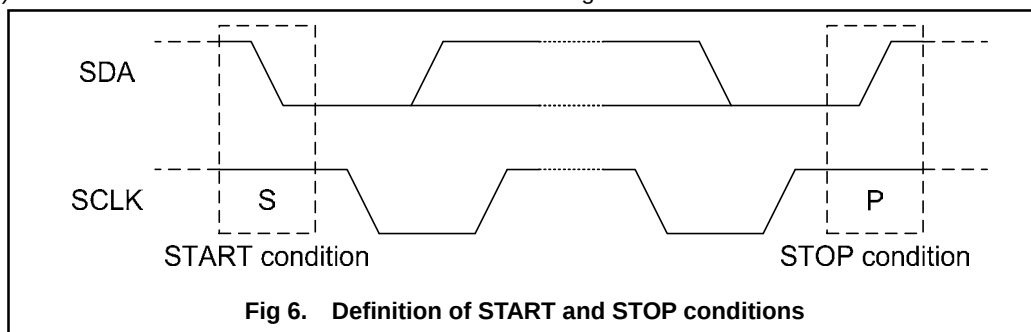
BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig 5.



START AND STOP CONDITIONS

Both SDA and SCLK lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCLK is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCLK is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig 6.



SYSTEM CONFIGURATION

The system configuration is illustrated in Fig 7 and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

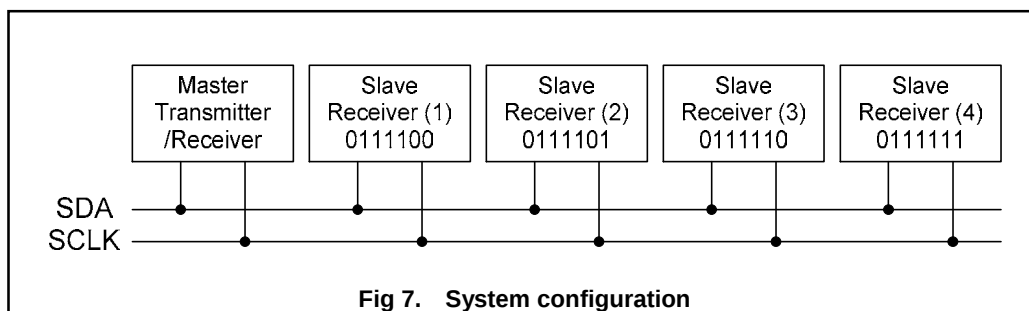


Fig 7. System configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating a acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated in Fig 8.

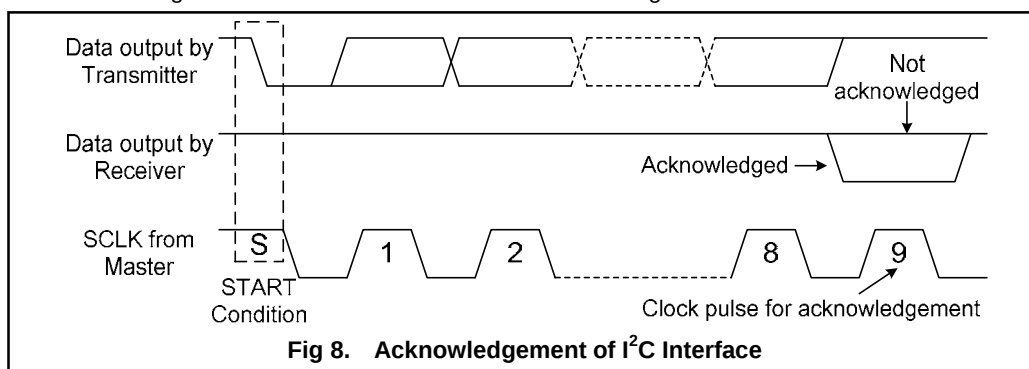


Fig 8. Acknowledgement of I²C Interface

I²C INTERFACE PROTOCOL

ST7571 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for ST7571. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1).

The I²C Interface protocol is illustrated in Fig 9.

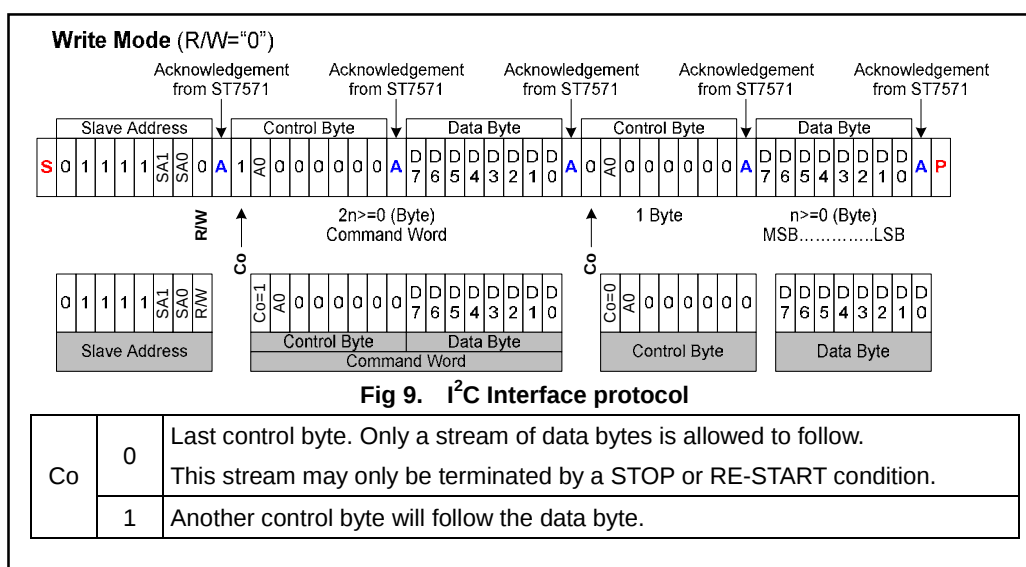
The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command words are followed and define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7571 device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7571 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.



Data Transfer

The ST7571 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig. 10, Fig. 11.

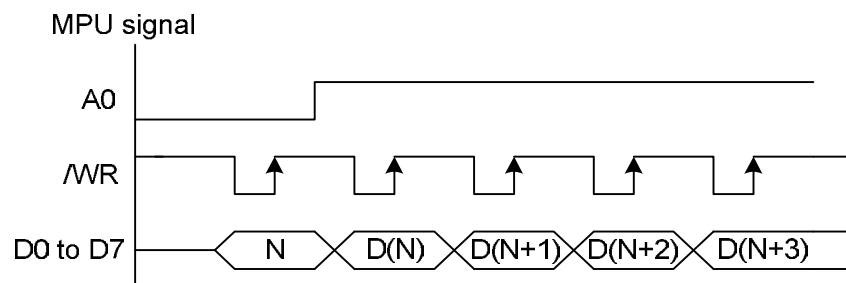


Fig. 10 Timing of MPU

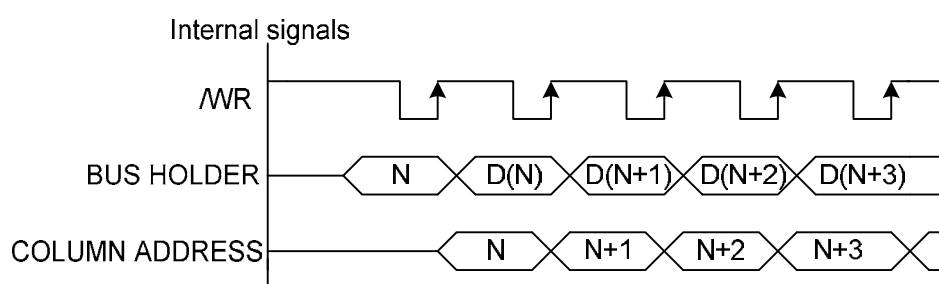


Fig. 11 Timing of driver IC

7.2 DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 129-row (17 pages by 8 bits) by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only). Data is written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 15, and Page 16 is for Icon page.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

When set Column Address MSB / LSB instruction is issued, 7-bit (Y[7:1]) are set and lowest bit (Y0) is set to "0". The internal column address (Y[7:0]) is increased by 1 automatically after each byte of data access (write data). After sequential access twice, the column address (Y[7:1]) will point to the next column address. Please refer to Fig. 12.

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the Display Data RAM.

SEG Output	SEG 0		SEG 1		SEG 2		SEG 3		...	SEG 124		SEG 125		SEG 126		SEG 127	
Column Address [Y7:Y1]	00H		01H		02H		03H		...	7CH		7DH		7EH		7FH	
Internal column address [Y7:Y0]	00	01	02	03	04	05	06	07	...	F8	F9	FA	FB	FC	FD	FE	FF
Display Data (MX=0)	1	1	1	0	0	1	0	0	...	1	1	1	0	0	1	0	0
LCD panel display									...								
Display data (MX=1)	0	0	0	1	1	0	1	1	...	0	0	0	1	1	0	1	1
LCD panel display									...								

Fig. 12 The Relationship between the Column Address and The Segment Outputs

7.3 LCD DISPLAY CIRCUITS

Oscillator

This is on-chip Oscillator without external resistor. When the internal oscillator is used, this pin must connect to VDD1; when the external oscillator is used, this pin could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (FR) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Fig. 13.

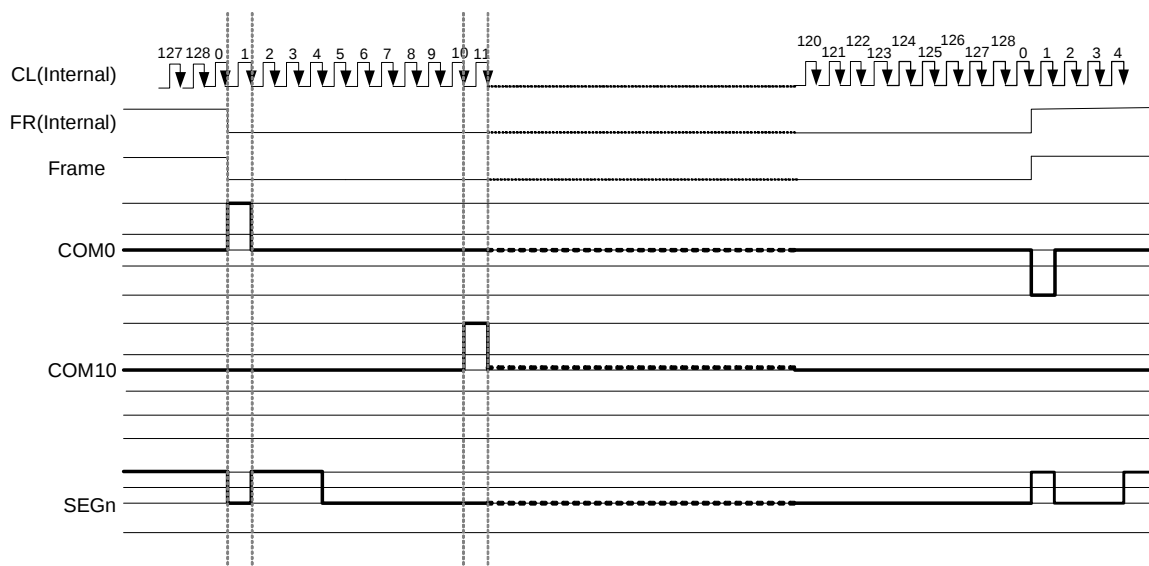


Fig. 13 frame AC Driving Waveform (Duty Ratio: 1/129)

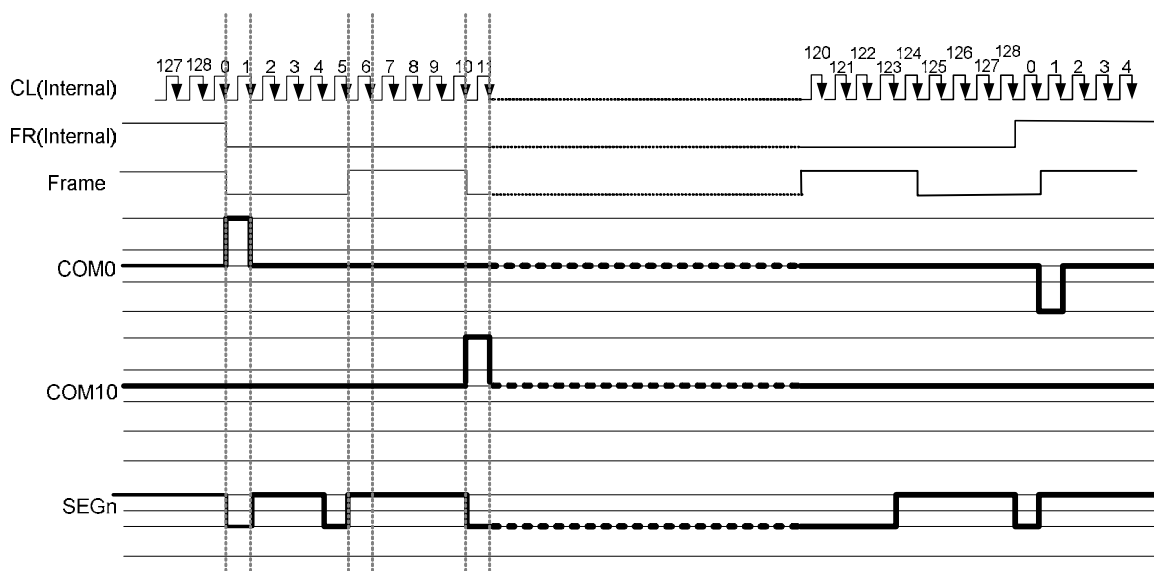


Fig. 14 N-Line Inversion Driving Waveform (N=5, Duty Ratio=1/129)

Partial Display on LCD

The ST7571 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages. The partial display duty ratio could be set from 16 ~ 128.

If the partial display region is out of the Max. Display range, it would be no operation.

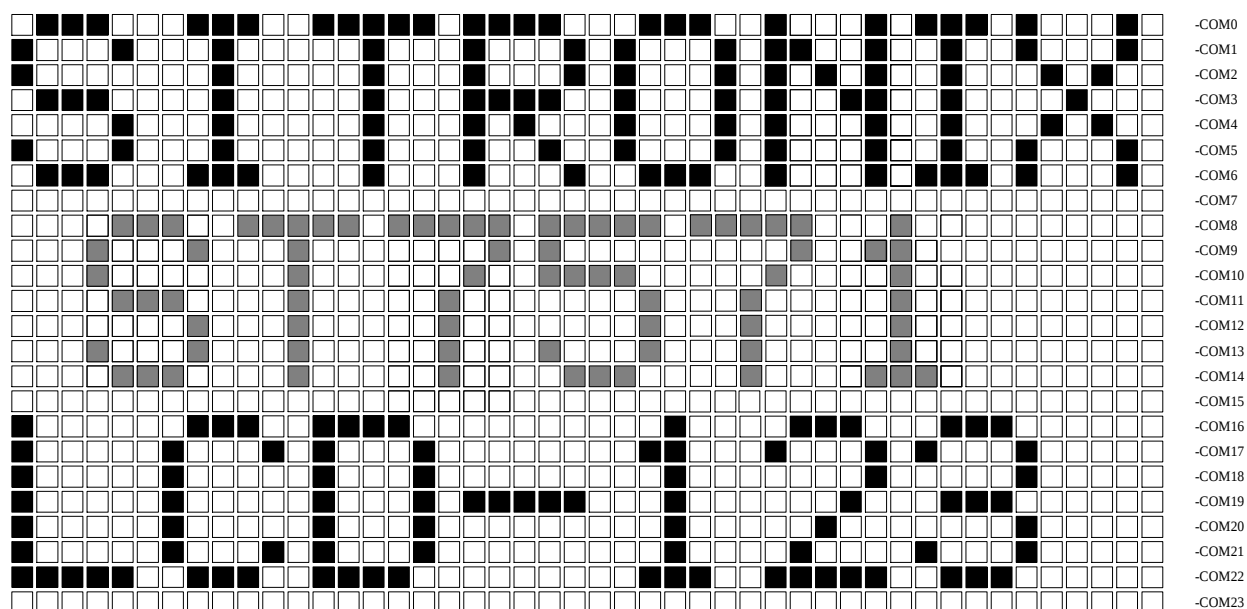


Fig. 15 Reference Example for Partial Display

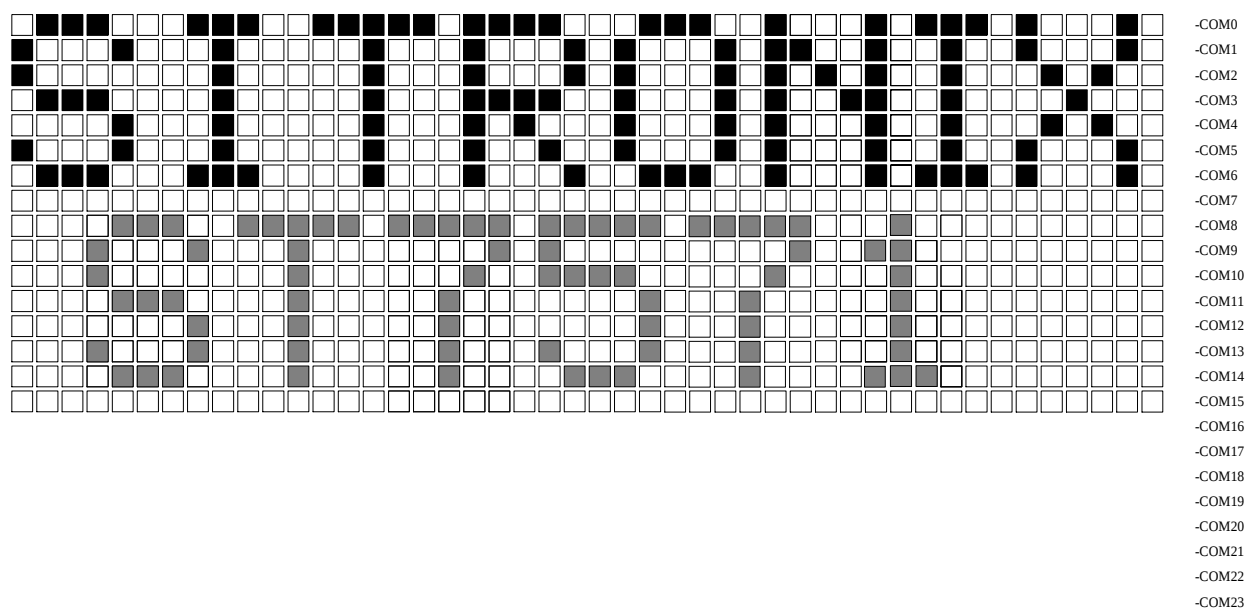


Fig. 16 Partial Display (Partial Display Duty=16, initial COM0=0)

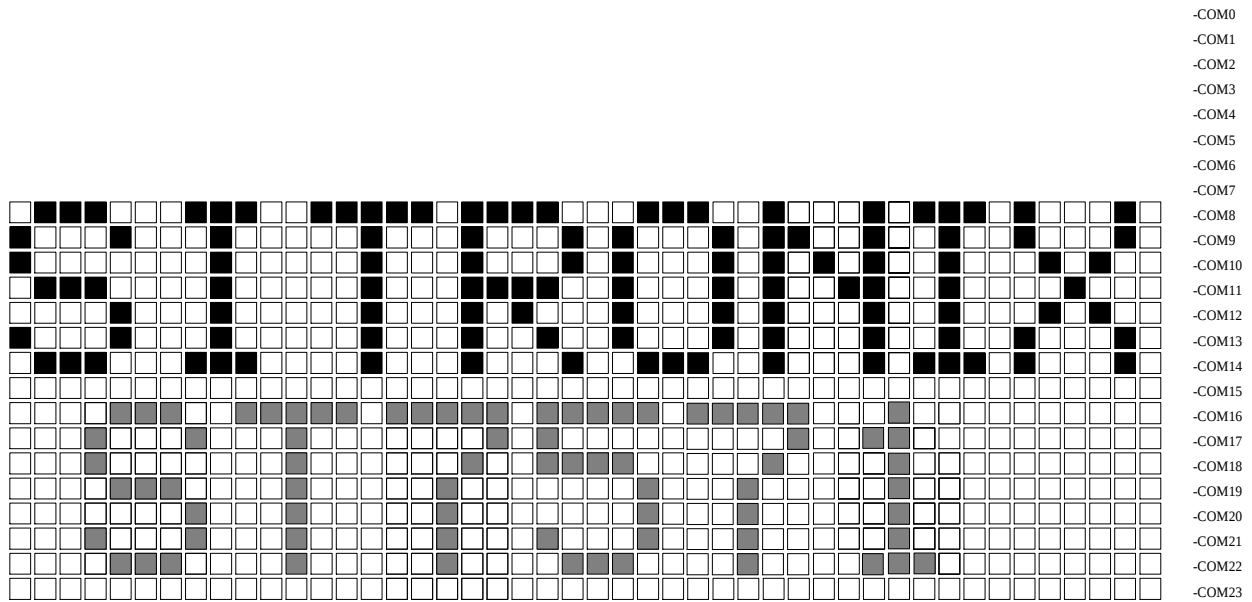


Fig. 17 Moving Display (Partial Display Duty=16,Initial COM0=8)

7.4 POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

Voltage Regulator Circuits

The internal Voltage Regulator circuit provides the liquid crystal operating voltage (V0) by adjusting resistors (SRR and EV). The parameter “SRR” can be set by “Select Regulator Register”.

The parameter “EV” can be set by “Set Electronic Volume Register”, and the range of EV is 0~63.

$$V0 = SRR \times \left(1 - \frac{(63 - EV)}{210}\right) \times 2.1$$

Table 5 Internal Regulator Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
SRR (Select Regulator Ratio)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Fig. 18 shows V0 voltage measured by adjusting regulator register ratio and 6-bit electronic registers for each temperature coefficient at Ta = 25°C. **The recommended range of EV setting is level 16 ~ 47.**

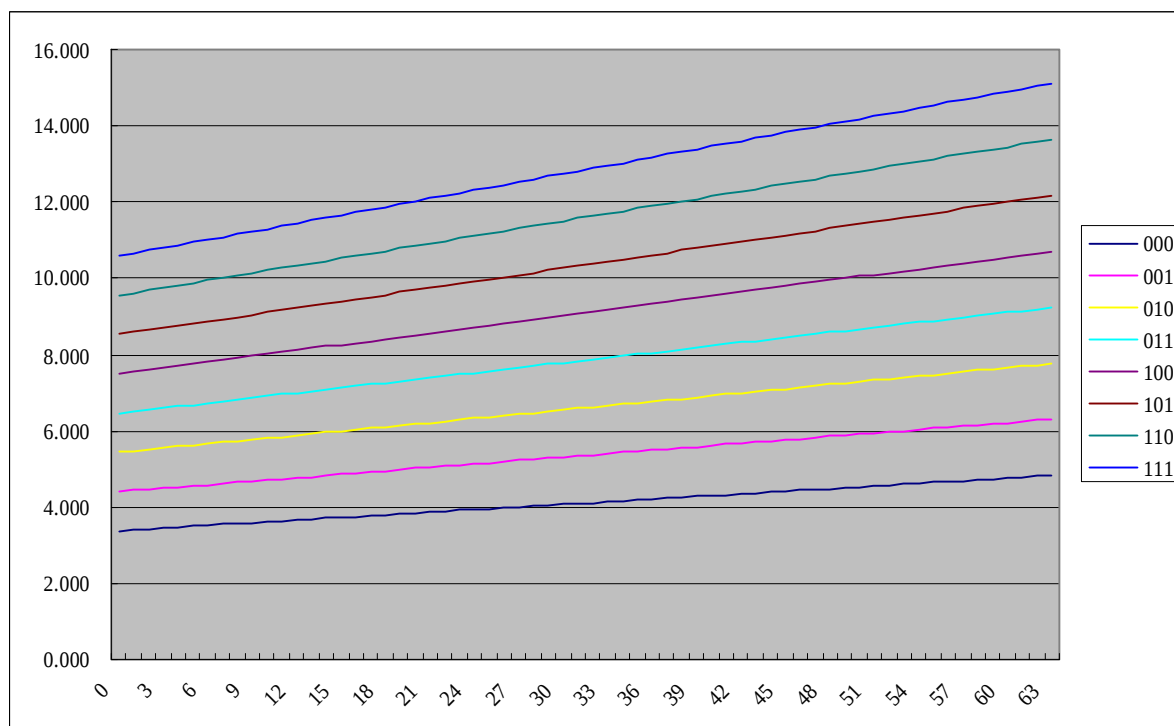


Fig. 18 Electronic Volume Level (25°C)

Voltage Follower Circuits

V0 is resistively divided into two voltage levels (VG, VM), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 6 shows the relationship between VG to VM level and each duty ratio.

Table 6 The Relationship between V1 to V4 Level and Each Duty Ratio

LCD Bias	VG	VM	Remarks
1/N	$2/N \times V0$	$1/N \times V0$	N = 5 to 12

Booster Efficiency

Booster Efficiency (Level1~4) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level2 is higher than level1), The Boost Efficiency is better than lower level, and it just need few more power consumption current. It could be applied to each multiple voltage Condition. When the LCD Panel loading is heavier, then the Performance of Booster will be not in a good working condition. We could set the BE level to be higher. We do not need to change to higher Booster Stage, and just need few more current. The Booster Efficiency Command could be used together with Booster Stage Command to choose one best Boost output condition. We could see the Boost Stage Command as a large scale operation, and see the Booster Efficiency Command as a small scale operation. These commands are very convenient for using.

7.5 RESET CIRCUITS

Setting RST to “L” or Reset instruction can initialize internal function.

When RST becomes “L”, following procedure is occurred.

Page address: 0

Column address: 0

Display ON / OFF: OFF

Initial display line: 0 (first)

Initial COM0 register: 0 (COM0)

Partial display duty ratio: 1/128

Reverse display ON / OFF: OFF (normal)

N-line inversion register: 0 (disable)

Entire Display ON/OFF: OFF

ICON Control register ON/OFF: OFF (ICON disable)

Power control register (VC, VR, VF) = (0, 0, 0)

Booster Efficiency BE = (1)

Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)

Contrast Level: 32

LCD bias ratio: 1/12

COM Scan Direction: 0

ADC Select: 0

Oscillator: OFF

Power Save Mode: Release

Display Data Length register: 0 (for SPI mode)

When RST instruction is issued, following procedure is occurred.

Page address: 0

Column address: 0

Initial display line: 0 (First)

Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)

Contrast Level: 32

Display Data Length register: 0 (for SPI mode)

8. INSTRUCTIONS

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	
Mode Set	0	0	0	0	1	1	1	0	0	0	2-byte instruction to set Mode and FR(Frame frequency control) BE(Booster efficiency control)	9.1.1
	0	0	FR3	FR2	FR1	FR0	BE1	BE0	x'	0		
Write display data	1	0	Write data								Write data into DDRAM	9.1.2
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable(default) ICON=1: ICON enable & set the page address to 16	9.1.3
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address	9.1.4
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB	9.1.5
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB	9.1.6
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON	9.1.7
Set initial display line register	0	0	0	1	0	0	0	0	x'	x'	2-byte instruction to specify the initial display line to realize vertical scrolling	9.1.8
	0	0	x'	S6	S5	S4	S3	S2	S1	S0		
Set initial COM0 register	0	0	0	1	0	0	0	1	x'	x'	2-byte instruction to specify the initial COM0 to realize window scrolling	9.1.9
	0	0	x'	C6	C5	C4	C3	C2	C1	C0		
Set partial display duty ration	0	0	0	1	0	0	1	0	x'	x'	2-byte instruction to set partial display duty ratio	9.1.10
	0	0	D7	D6	D5	D4	D3	D2	D1	D0		
Set N-line inversion	0	0	0	1	0	0	1	1	x'	x'	2-byte instruction to set N-line inversion register	9.1.11
	0	0	x'	x'	x'	N4	N3	N2	N1	N0		
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line inversion mode	9.1.12
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display REV=1: reverse display	9.1.13
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display EON=1: entire display ON	9.1.14

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation	9.1.15
Select regulator register	0	0	0	0	1	0	0	R2	R1	R0	Select the internal resistance ratio of the regulator resistor	9.1.16
Select electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the reference voltage	9.1.17
	0	0	x'	x'	EV5	EV4	EV3	EV2	EV1	EV0		
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias	9.1.18
SHL select	0	0	1	1	0	0	SHL	x'	x'	x'	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction	9.1.19
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-direction selection ADC=0: normal direction ADC=1: reverse direction	9.1.20
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator	9.1.21
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode	9.1.22
Release power save mode	0	0	1	1	1	0	0	0	0	1	release power save mode	9.1.23
Reset	0	0	1	1	1	0	0	0	1	0	initial the internal function	9.1.24
Display data length	x'	x'	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes. (SPI mode)	9.1.25
	x'	x'	D7	D6	D5	D4	D3	D2	D1	D0		
NOP	0	0	1	1	1	0	0	0	1	1	No operation	9.1.26
Test Command set 1	0	0	1	1	1	1	x'	x'	x'	x'	Enter test command set 1 Use for Burning EE	9.1.27
Test Command set 2	0	0	1	1	0	1	0	0	0	1	Enter test command set 2 Use for Burning EE	9.1.28
Test Command set 3	0	0	0	1	1	1	1	0	1	1	Don't use this instruction	9.1.29

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
COMMAND SET 1											
Disable autoread	0	0	1	0	1	0	1	0	1	0	Disable autoread
Enter EEPROM mode	0	0	0	0	0	1	0	0	1	1	Enter EEPROM mode
Enable read mode	0	0	0	0	1	0	0	0	0	0	Enable read mode
Set read pulse	0	0	0	1	1	1	0	0	0	1	Set read pulse width (Do not modify this value)
Exit EEPROM mode	0	0	1	0	0	0	0	0	1	1	Exit EEPROM mode
Enable erase mode	0	0	0	1	0	0	1	0	1	0	Enable erase mode
Set erase pulse	0	0	0	1	0	1	0	1	0	1	Set erase pulse width (Do not modify this value)
Enable write mode	0	0	0	0	1	1	0	1	0	1	Enable write mode
Set write pulse	0	0	0	1	1	0	1	0	1	0	Set write pulse width (Do not modify this value)
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode
COMMAND SET 2											
Increase vop offset	0	0	0	1	0	1	0	0	0	1	Increase vop offset 1 level
Decrease vop offset	0	0	0	1	0	1	0	0	1	0	Decrease vop offset 1 level
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode

EE Burning Flow

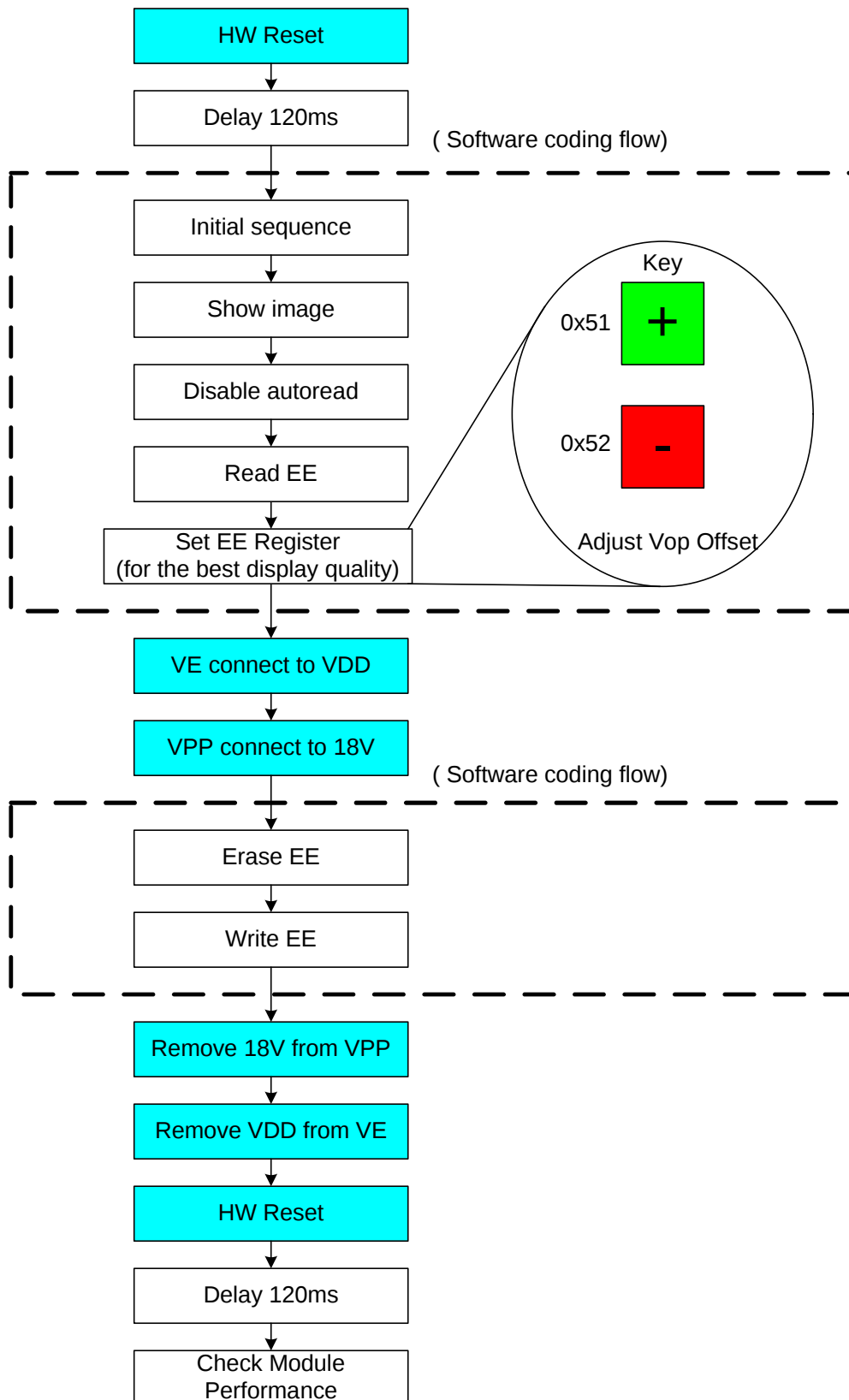


Fig. 19 EE Burning flow chart

Software Function

void Disable_autoread(void)			
{			
	Write(COMMAND, 0x00D1);		//Enter test command set 2
	Write(COMMAND, 0x00AA);		//Disable autoread
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

void Read_EE (void)			
{			
	Write(COMMAND, 0x00D1);		//Enter test command set 2
	Write(COMMAND, 0x00AA);		//Autoread disable
	Write(COMMAND, 0x0013);		//Enter EEPROM mode
	Write(COMMAND, 0x0020);		//Enable read mode
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0071);		//Set read pulse
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0083);		//Exit EEPROM mode
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

void Set_EE_Register (void)			
{ // Adjust Vop offset here			
//command 0x51 and 0x52 can be set many times for adjusting a suitable Vop			
//Maximum adjusting ranges are +/-16 levels.			
	Write(COMMAND, 0x00FD);		//Enter test command set 1
	Write(COMMAND, 0x0051);		//0x0051 for increase Vop offset
	or		
	Write(COMMAND, 0x0052);		//0x0052 for decrease Vop offset
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

void Erase_EE (void)			
{			
	Write(COMMAND, 0x00D1);		//Enter test command set 2
	Write(COMMAND, 0x0013);		//Enter EEPROM mode
	Write(COMMAND, 0x004A);		//Enable erase mode
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0055);		//Set erase pulse
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0083);		//Exit EEPROM mode
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

void Write_EE (void)			
{			
	Write(COMMAND, 0x00D1);		//Enter test command set 2
	Write(COMMAND, 0x0013);		//Enter EEPROM mode
	Write(COMMAND, 0x0035);		//Enable write mode
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x006A);		//Set write pulse
	Delay(200);		//Delay 200ms
	Write(COMMAND, 0x0083);		//Exit EEPROM mode
	Write(COMMAND, 0x0000);		//Enter normal mode
}			

9.1.1 Set Mode Register

2-byte instruction to set FR (Frame frequency control) and BE (Booster efficiency control)

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	FR3	FR2	FR1	FR0	BE1	BE0	x'	0

Frame frequency

This command is used to set the frame frequency.

FR ₃	FR ₂	FR ₁	FR ₀	FR frequency
0	0	0	0	77 Hz $\pm 10\%$
0	0	0	1	51 Hz $\pm 20\%$
0	0	1	0	55 Hz $\pm 20\%$
0	0	1	1	58 Hz $\pm 20\%$
0	1	0	0	63 Hz $\pm 20\%$
0	1	0	1	67 Hz $\pm 20\%$
0	1	1	0	68 Hz $\pm 20\%$
0	1	1	1	70 Hz $\pm 20\%$
1	0	0	0	73 Hz $\pm 20\%$
1	0	0	1	75 Hz $\pm 20\%$
1	0	1	0	80 Hz $\pm 20\%$
1	0	1	1	85 Hz $\pm 20\%$
1	1	0	0	91 Hz $\pm 20\%$
1	1	0	1	102 Hz $\pm 20\%$
1	1	1	0	113 Hz $\pm 20\%$
1	1	1	1	123 Hz $\pm 20\%$

Booster Efficiency

The ST7571 incorporates software configurable Booster Efficiency Command. It could be used with Voltage multiplier to get the suitable Vop and Power consumption. **(Recommend setting is Level 3)**

BE1	BE0	Description
0	0	Booster Efficiency Level 1
0	1	Booster Efficiency Level 2
1	0	Booster Efficiency Level 3
1	1	Booster Efficiency Level 4

9.1.2 Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

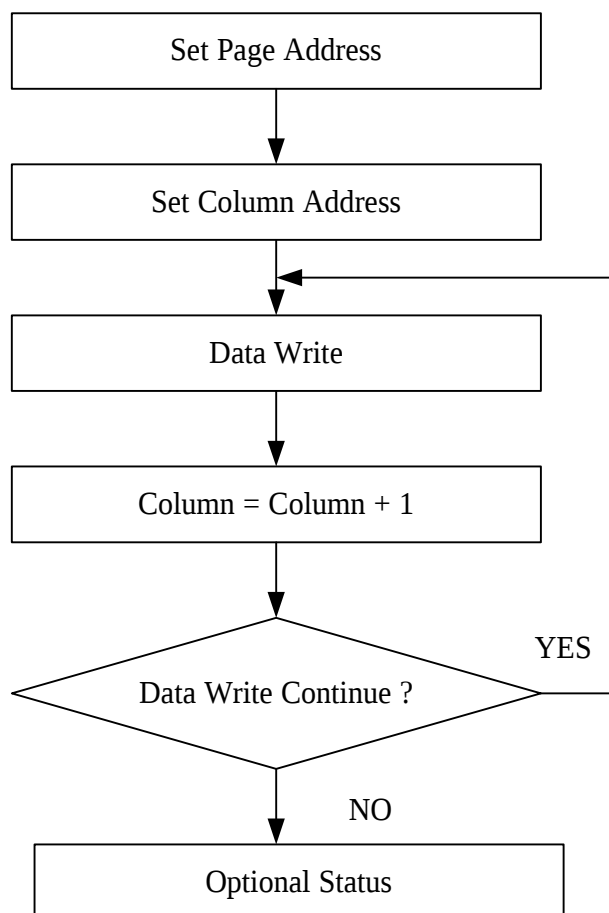


Fig. 20 Sequence for Writing Display Data

9.1.3 ICON Control Register ON/OFF

This instruction makes ICON enable or disable. By default, ICON display is disabled (ICON= 0). When ICON control register is set to “1”, ICON display is enabled and page address is set to “16”. Then user can write data for icons. It is impossible to set the page address to “16” by Set Page Address instruction. Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to “16”. When ICON control register is set to “0”, ICON display is disabled.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	ICON

ICON=0: ICON disable (default)

ICON=1: ICON enable & set the page address to 16

9.1.4 Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write display data. Changing the Page Address doesn't affect the display status. Set Page Address instruction can not be used to set the page address to “16”. Use ICON control register ON/OFF instruction to set the page address to “16”.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

9.1.5 & 9.1.6 Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write display data.

When the microprocessor writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y7	Y6	Y5

Set Column Address LSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y4	Y3	Y2	Y1

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Column address [Y7:Y1]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

9.1.7 Display ON / OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON

DON = 0: display OFF

9.1.8 Set Initial Display Line Register

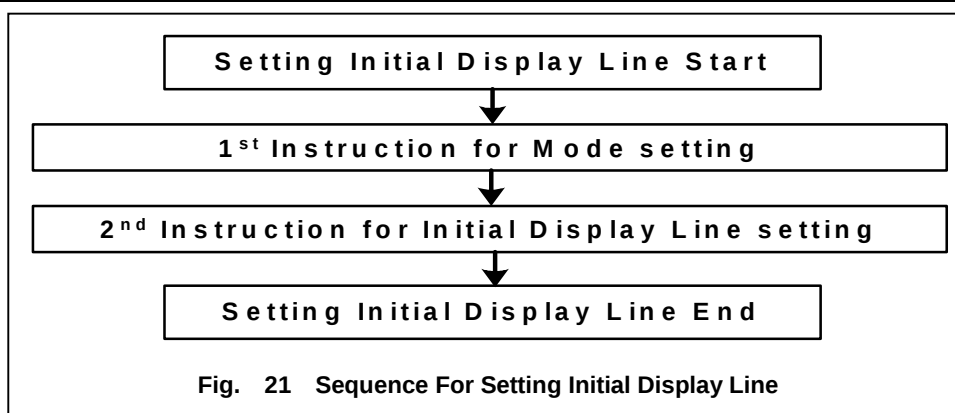
Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row(COM0) of LCD panel.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	S6	S5	S4	S3	S2	S1	S0
S6	S5	S4	S3	S2	S1	S0	Line address		
0	0	0	0	0	0	0	0		
0	0	0	0	0	0	1	1		
0	0	0	0	0	1	0	2		
0	0	0	0	0	1	1	3		
:	:	:	:	:	:	:	:		
1	1	1	1	1	0	0	124		
1	1	1	1	1	0	1	125		
1	1	1	1	1	1	0	126		
1	1	1	1	1	1	1	127		



9.1.9 Set Initial COM0 Register

Set the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

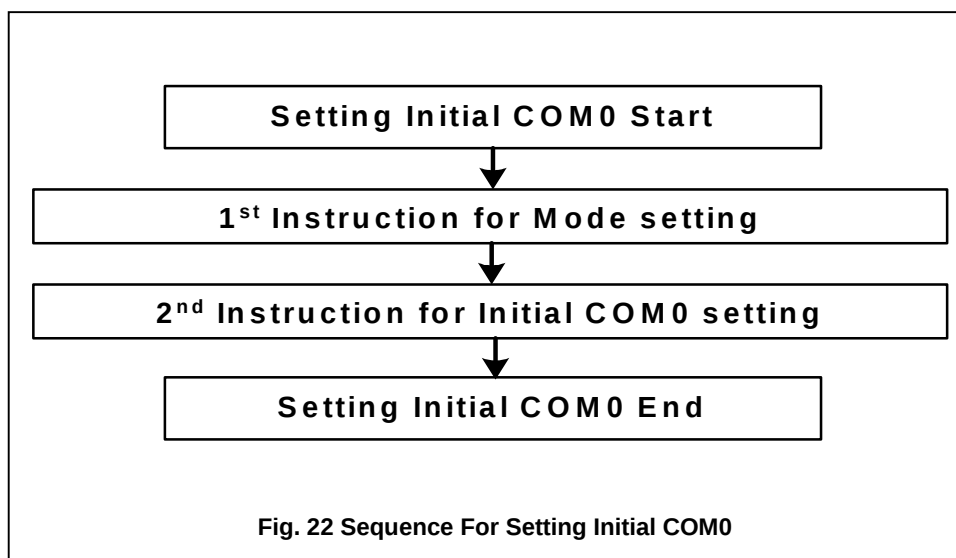
The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM124
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127



9.1.10 Set Partial Display Duty Ratio

Sets the duty ratio within range of 16 to 128 (ICON is not included) or 17 to 129 (including ICON) to realize partial display by using the 2-byte instruction.

The 1st Instruction

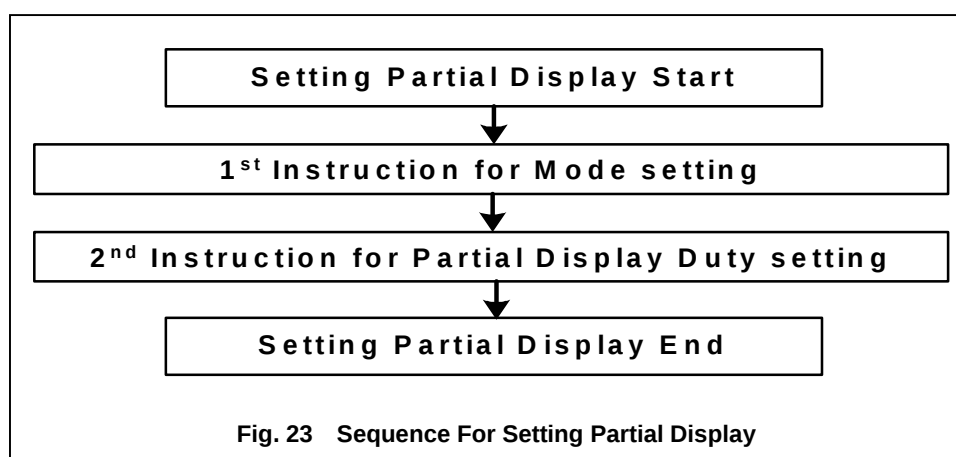
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected Partial Duty Ratio
0	0	0	0	0	0	0	0	No Operation
:	:	:	:	:	:	:	:	
0	0	0	0	1	1	1	1	
0	0	0	1	0	0	0	0	1/(16+1)
0	0	0	1	0	0	0	1	1/(17+1)
:	:	:	:	:	:	:	:	:
0	1	1	0	0	1	0	0	1/(100+1)
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1/(127+1)
1	0	0	0	0	0	0	0	1/(128+1)
1	0	0	0	0	0	0	1	No Operation
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	

NOTE: The duty includes the duty for ICON.



9.1.11 Set N-line Inversion Register (For 128 duty condition, recommended 12-line inversion)

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K : D/N

D: The number of display duty ratio (D is selectable by customers)

N: N for N-line inversion (N is selectable by customers).

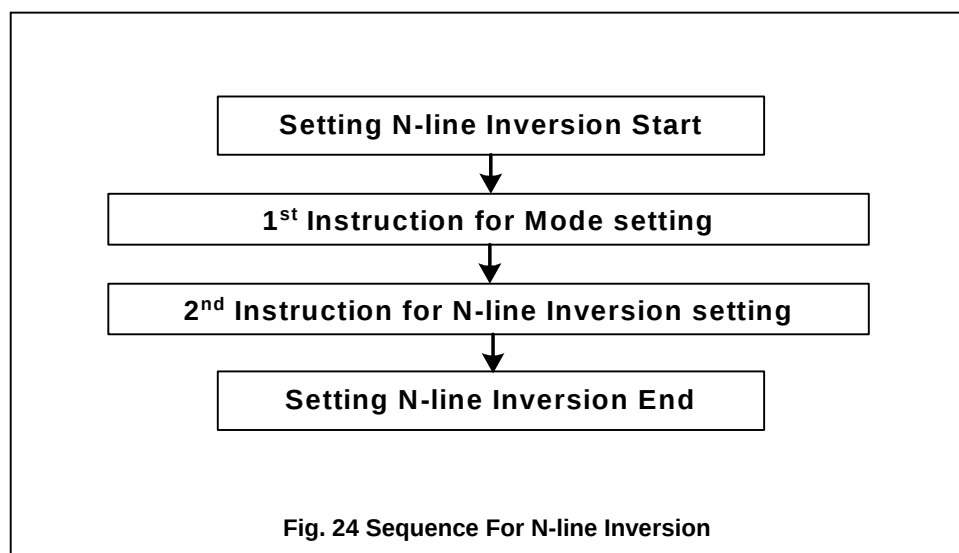
The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
0	1	0	1	0	12-line inversion (Recommend)
					:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion



9.1.12 Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

9.1.13 Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	DDRAM data = "00" – White	DDRAM data = "01" – Light gray	DDRAM data = "10" – Dark gray	DDRAM data = "11" – Black
0 (normal)	White	Light gray	Dark gray	Black
1 (reverse)	Black	Dark gray	Light gray	White

9.1.14 Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

Entire	DDRAM data = "00" – White	DDRAM data = "01" – Light gray	DDRAM data = "10" – Dark gray	DDRAM data = "11" – Black
0 (normal)	White	Light gray	Dark gray	Black
1 (Entire)	Black	Black	Black	Black

9.1.15 Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0			Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
	0		Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
		0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

9.1.16 Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0
R2		R1		R0		1+ (Rb / Ra)			
0		0		0		2.3			
0		0		1		3.0			
0		1		0		3.7			
0		1		1		4.4			
1		0		0		5.1			
1		0		1		5.8			
1		1		0		6.5			
1		1		1		7.2			

9.1.17 Set Electronic Volume Register

Consist of 2-byte Instructions

The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register.

After second instruction, Reference Voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

9.1.18 Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

9.1.19 SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	x	x	x

SHL = 0: normal direction (COM0 → COM127)

SHL = 1: reverse direction (COM127 → COM0)

9.1.20 ADC Select

Change the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG127)

ADC = 1: reverse direction (SEG127 → SEG0)

9.1.21 Oscillator ON Start

This instruction enables the built-in oscillator circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

9.1.22 & 9.1.23 Power Save

The ST7571 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

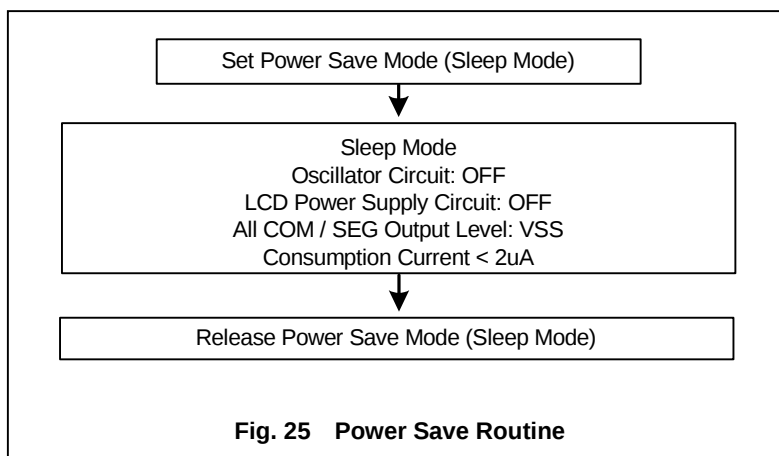
Set Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode , P = 1: sleep mode

Release Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1



9.1.24 Reset

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

9.1.25 Display Data Length (8 bits 3-Line SPI Mode)

This command is used in 3-Line SPI mode only. It concludes two continuous commands, the first byte is command code, the second byte will indicate how many data bytes will be written. When A0 is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command.

The 1st Instruction: Set Data Length Command (Only Write Mode)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

9.1.26 NOP

No operation

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

9.1.27 Test Command set 1

This instruction is for testing IC. Use for burning EE.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	x	1

9.1.28 Test Command set 2

This instruction is for testing Use for burning EE.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	1	0	0	0	1

9.1.29 Test Command set 3

This instruction is for testing IC. Please do not use it.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	1	0	1	1

10. COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

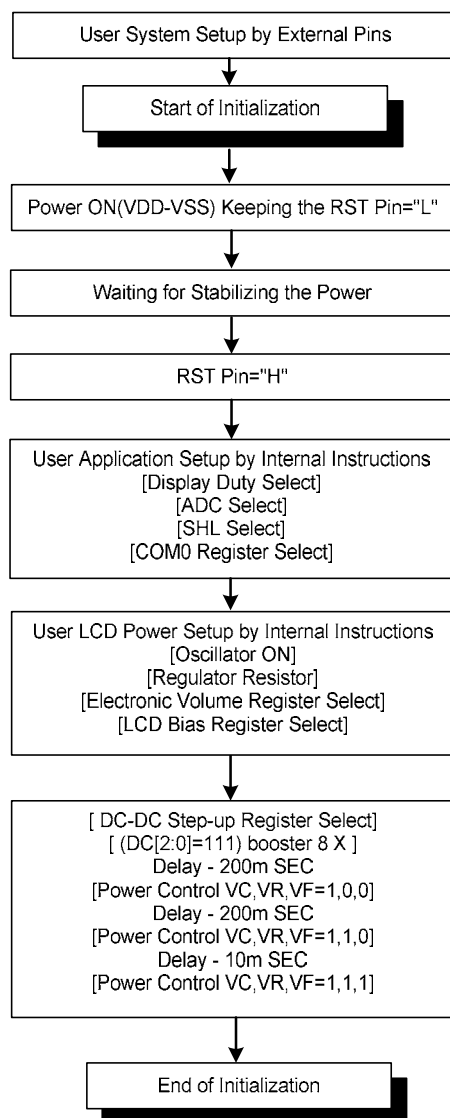
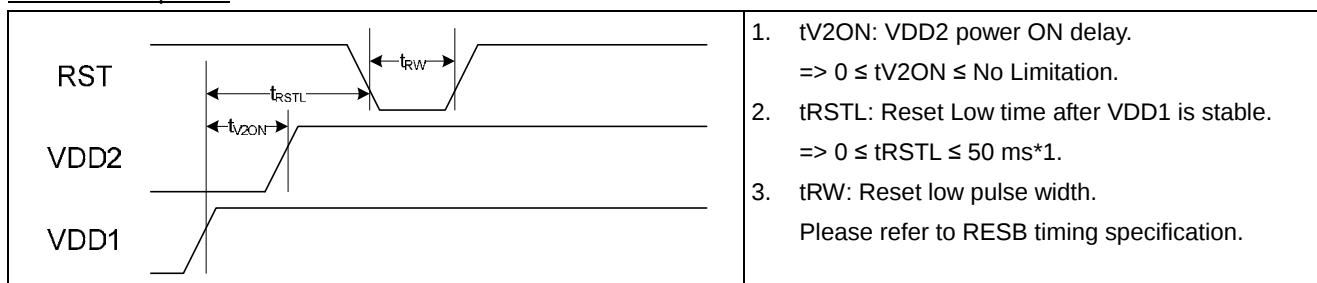


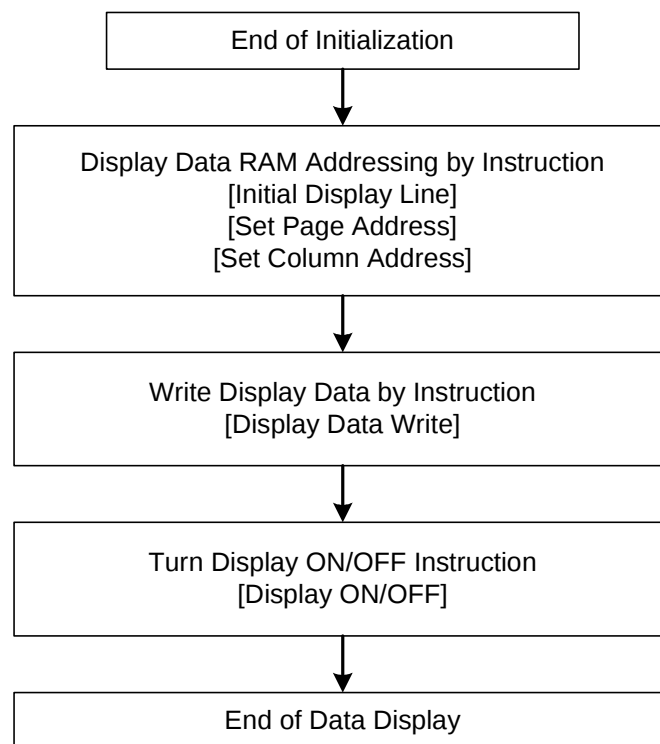
Fig. 26 Initializing with the Built-in Power Supply Circuits

Power On Sequence



Note:

1. IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON. The specification listed here is to prevent abnormal display on LCD module.
2. Be sure the power is stable and the internal reset is finished (refer to RST timing specification).

Referential Instruction Setup Flow: Data Displaying**Fig. 27 Data Displaying**

Referential Instruction Setup Flow: Power OFF

By setting 0xA9, ST7571 will go into power save mode. The LCD driving outputs are fixed to VSS, built-in power circuits are turned OFF and a discharge process starts.

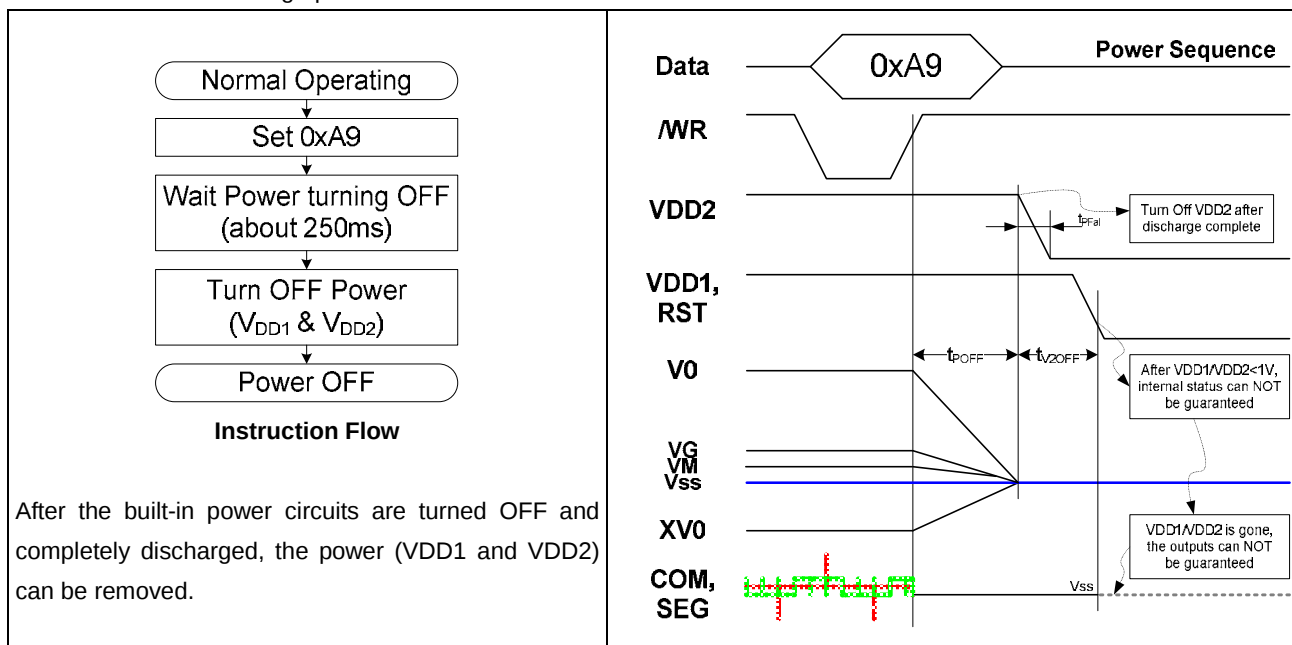


Fig. 28 Power off instruction flow

Note:

1. t_{POFF} : Internal Power discharge time. => 250ms (max).
2. t_{V2OFF} : Period between VDD1 and VDD2 OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDD1 OFF before VDD2. Without VDD1, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.8".
7. When turning VDD2 OFF, the falling time should follow the specification:
 $300\text{ms} \leq t_{PFall} \leq 1\text{sec}$

void Initial_ST7571(void)

```
{
    Reset( );
    Delay (1000);
    Write(COMMAND,0xAE);           // Display OFF
    Write(COMMAND,0x38);           // MODE SET
    Write(COMMAND,0xB4);           // FR=1011 => 85Hz
                                   // BE1=0,BE0=1 => booster efficiency level 2
    Write(COMMAND,0xA1);           // ADC select, ADC=1 =>reverse direction
    Write(COMMAND,0xC8);           // SHL select, SHL=1 => reverse direction
    Write(COMMAND,0x44);           // Set initial COM0 register
    Write(COMMAND,0x00);           //

    Write(COMMAND, 0xAB );         // OSC. On
    Write(COMMAND, 0x67 );         // DC-DC step up, 8 times boosting circuit
    Write(COMMAND,0x25);           // Select regulator register(1+(ra+rb))
    Write(COMMAND,0x81);           // Set Reference Voltage
    Write(COMMAND,0x23);           // EV=35 => Vop =10.556V
    Write(COMMAND,0x54);           // Set LCD Bias=1/9 V0
    Write(COMMAND,0xF3);           // Release Bias Power Save Mode

    Write(COMMAND,0x04);           //
    Write(COMMAND,0x40);           // Set initial display line register
    Write(COMMAND,0x00);           //
    Write(COMMAND,0x93);           // Select FRC and PWM mode( 4FRC,15PWM )
    Write(COMMAND,0x2C);           // Power Control, Vc: On  Vr: Off  Vf: Off
    Delay (2000);                 // Delay 200ms
    Write(COMMAND,0x2E);           // Power Control, Vc: On  Vr: On  Vf: Off
    Delay (2000);                 // Delay 200ms
    Write(COMMAND,0x2F);           // Power Control, Vc: On  Vr: On  Vf: On
    Delay (2000);                 // Delay 200ms
    Write(COMMAND,0xAF);           // Display ON
}
```

* The initial code is for reference only. An optimized initial code should be checked on customer's system and LCD module.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1	-0.3 ~ 3.3	V
Analog Power supply voltage	VDD2	-0.3 ~ 3.3	V
Analog Power supply voltage	VDD3	-0.3 ~ 3.3	V
LCD Power supply voltage	V0-XV0	-0.3 ~ 15	V
LCD Power supply voltage	VG, VM	-0.3 ~ VDD2	
Operating temperature	TOPR	-30 to +85	°C
Storage temperature	TSTR	-40 to +125	°C

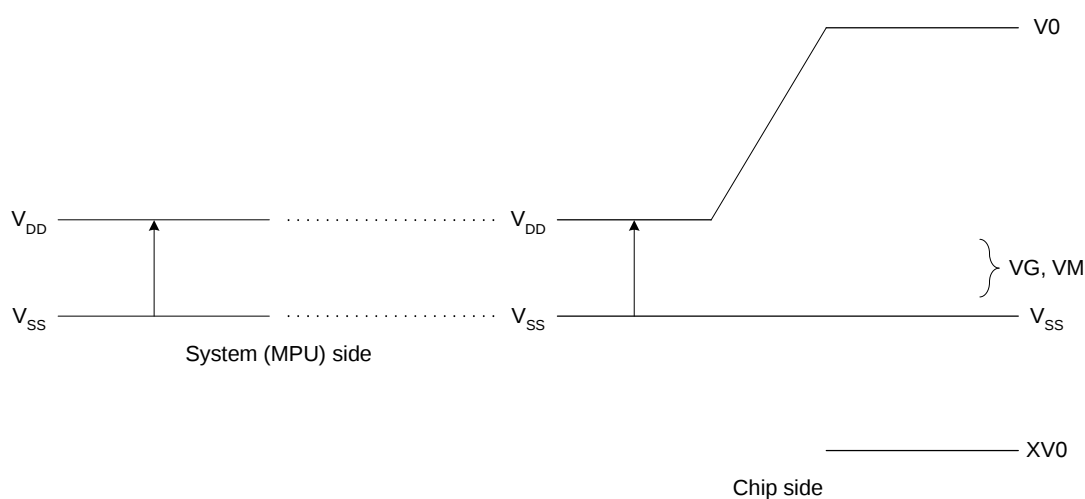


Fig. 30

Notes

- Stresses above those listed under Limiting Values may cause permanent damage to the device.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
- Insure the voltage levels of V_0 , V_{DD2} , V_G , V_M , V_{SS} and XV_0 always match the correct relation:
 $V_0 \geq V_{DD2} > V_G > V_M > V_{SS} \geq XV_0$

DC CHARACTERISTICS

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Digital Operating Voltage	VDD1		1.8	—	3.3	V	VDD1
Analog Operating Voltage	VDD2		2.4	—	3.3	V	*2
Analog Operating Voltage	VDD3		2.4	—	3.3	V	*2
High-level Input Voltage	VIHC		0.7 x VDD1	—	VDD1	V	*1
Low-level Input Voltage	VILC		VSS	—	0.3 x VDD1	V	*1
Input leakage current	ILI	VIN = VDD1 or VSS	−1.0	—	1.0	μA	*3
Output leakage current	ILO	VIN = VDD1 or VSS	−3.0	—	3.0	μA	*4
LCD Driver ON Resistance	RON	Ta = 25°C	Vop=12V ΔV=1.2V	—	0.7	KΩ	SEGn COMn *5
			VG=2V ΔV=0.2V	—	0.7		
Frame Frequency	fFR	1/129 duty, Ta = 25°C FR[3:0]=0000(77Hz)	70	77	84	Hz	

* VSS1 = VSS2 = VSS3 = 0 V unless otherwise specified.

Bare Dice Current Consumption

Using Internal Power Circuits and applying external operating voltage (VDD1, VDD2 & VDD3).

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display ON Pattern: SNOW	ISS	VDD1=1.8V, VDD2=VDD3=2.8V Ta = 25°C, Vop=10.5V, 8X booster, 1/9 Bias, N-Line=0x01, 1/129 duty, FR[3:0]=0000(77Hz)	—	450	600	μA	*6
Power Save	ISS	VDD1=1.8V, VDD2=VDD3=2.8V , Ta = 25°C	—	5	10	μA	*6

Note:

- The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR (R/W), CSB, IMS, OSC, P/S, /DOF, RESB, and MODE terminals.
- Used by internal analog circuits.
- The A0, /RD (E), /WR, /R(W), CSB, IMS, OSC, P/S, /DOF, RESB and MODE terminals.
- Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.
- These are the resistance values for when a specified voltage difference is applied between the output terminals (SEGn/COMn) and the various power supply terminals (V0, XV0, VG & VM).
 $R_{ON} = \Delta V / \Delta I$ (ΔV is the specified voltage difference; ΔI is the current when applying ΔV between output and power)
- It indicates the current consumed by Bare Chip alone.

Internal Power Circuits

The operation ranges of the internal power circuits are shown below:

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Vop	V0-XV0		—	—	15	V	
Voltage follower output voltage	VM		0.7	VG/2	VDD2-0.7	V	
VG output voltage range	VG		1.8	—	VDD2	V	

Internal Power Application Notes

- I Positive Booster: $(VDD2 \times 8 \times BE) \geq V0$ or $(VDD2 \times 8 \times BE) \geq Vop$;
- I Negative Booster: $[-VDD2 \times (8 - 1) \times BE] \leq XV0$ or $[VDD2 \times (8 - 1) \times BE] \geq (Vop - VG)$,.....where $VG = Vop \times 2 / N$;
- I Vop requirement: $[VDD2 \times (8 - 1) \times BE] \geq [Vop \times (N - 2) / N]$ or $[Vop \leq VDD2 \times (8 - 1) \times BE \times N / (N - 2)]$.
- I “8” is the booster stage and BE is the booster efficiency. Actual BE should be determined by module loading and ITO resistance value.
- I $1.8V \leq VG < VDD2$. Recommend VG setting is: $(VDD2 - VG) = 0.5 \sim 0.8V$.
- I $VM = VG/2$ and $0.7V \leq VM < VDD2$.
- I The worse condition should be considered. Furthermore, it should reserve some range for the temperature compensation and the contrast control (for end-customer).

Internal Power Application Summary (Recommend LCD Module Setting)

For quick reference, the following table lists some recommended settings for LCD module.

VDD1=1.8V, VDD2=2.8V, N-Line=0, Panel Size=1.5”

Duty	Vop	Bias
1/129	10V ~ 12V	1/9,
1/81	9V ~ 11V	1/9
1/65	8.5V ~ 10.5V	1/9

Note:

1. It is recommended to reserve some range for user adjustment and temperature effect.
2. The value listed above is in the IC point of view. The liquid crystal display status should be checked by customer.

TIMING CHARACTERISTICS

System Bus Write Characteristics 1 (For the 8080 Series MPU)

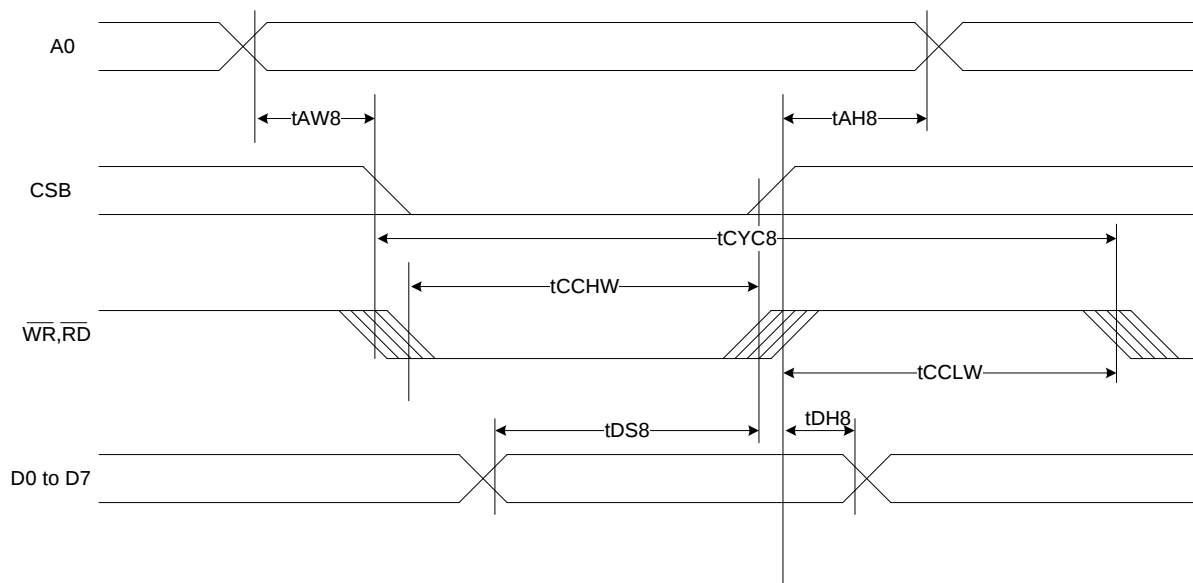


Fig. 31

(VDD1 = 1.8~3.3V, $T_a = -30 \sim 85^\circ\text{C}$)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Write L pulse width	WR	tCCLW		360	—	
Write H pulse width		tCCHW		280	—	
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Data hold time		tDH8		30	—	

*1 The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ is specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tCCLW is specified as the overlap between CSB being “L” and WR being at the “L” level.

System Bus Write Characteristics 1 (For the 6800 Series MPU)

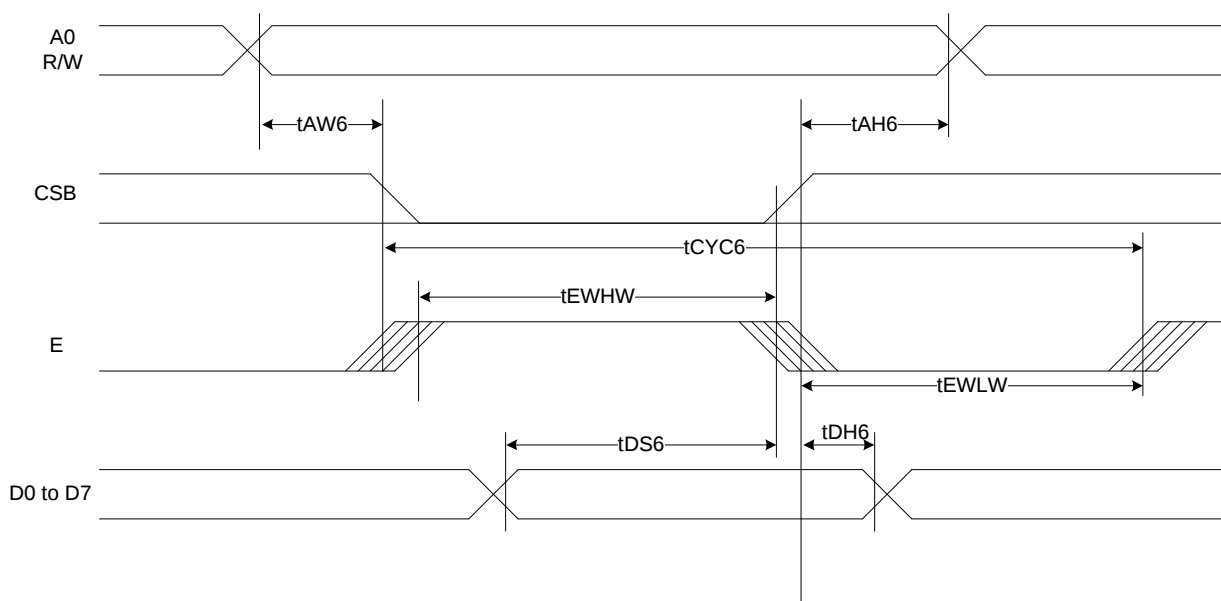


Fig. 32

(VDD1 = 1.8V~3.3V , Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEHLW		360	—	
Enable H pulse width (WRITE)		tEHWLW		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Data hold time		tDH6		30	—	

*1 The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYC6} - t_{EHLW} - t_{EHWLW})$ is specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEHLW is specified as the overlap between CSB being "H" and E being "L".

SERIAL INTERFACE(4-Line Interface)

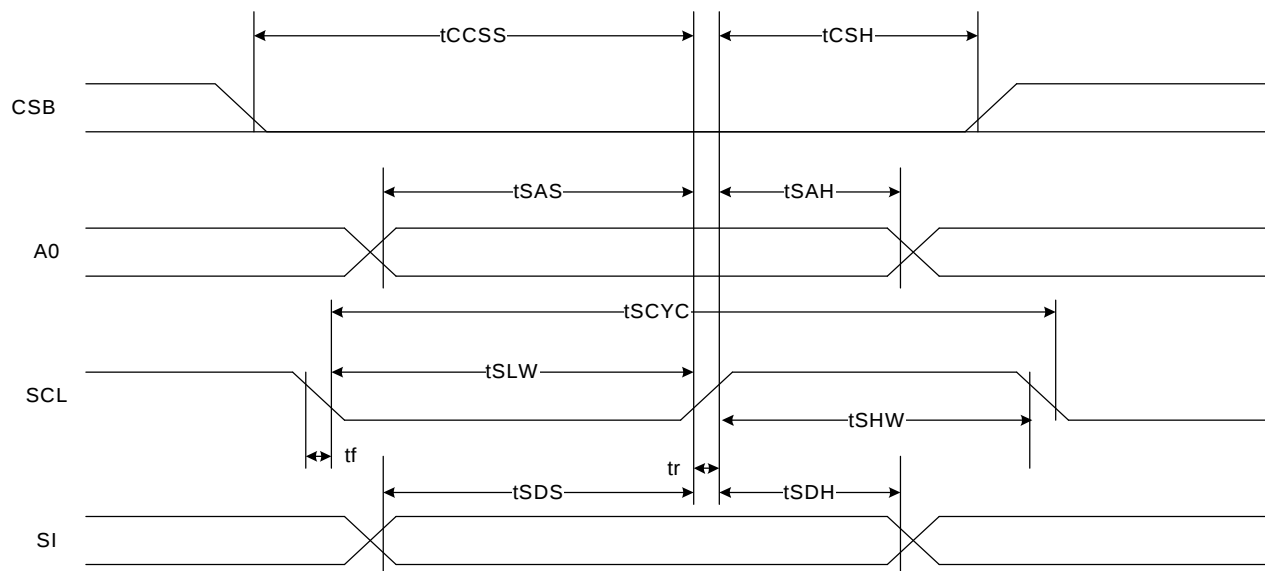


Fig. 33

(VDD1=1.8V~3.3V, Ta=-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

SERIAL INTERFACE(3-Line Interface)

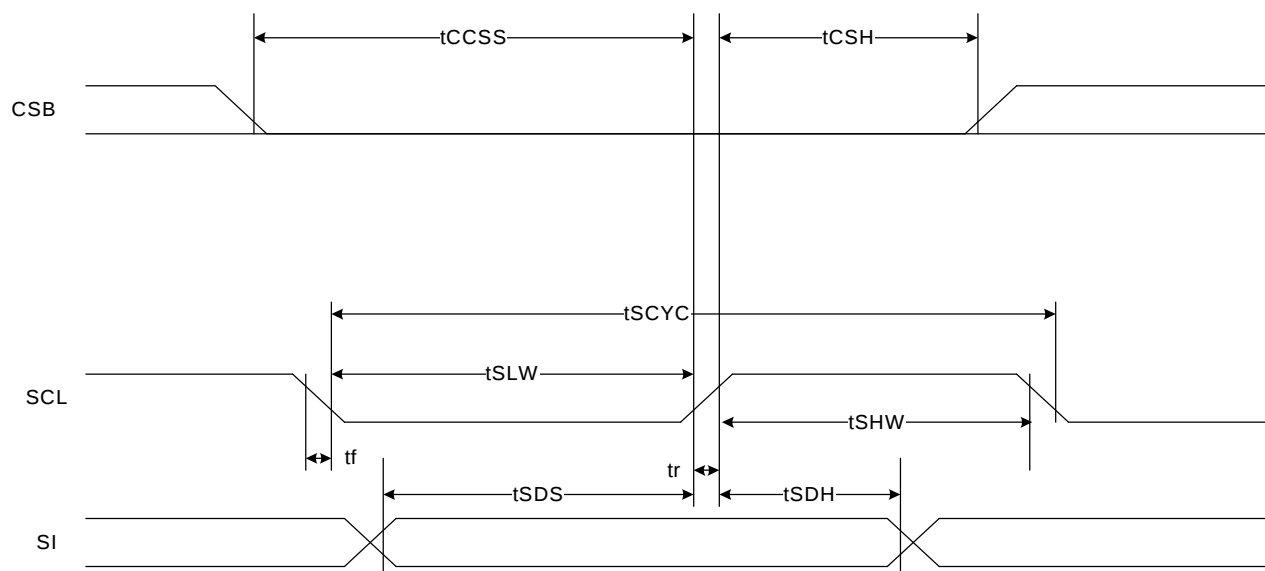


Fig. 34

(VDD1=1.8V~3.3V, Ta=-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

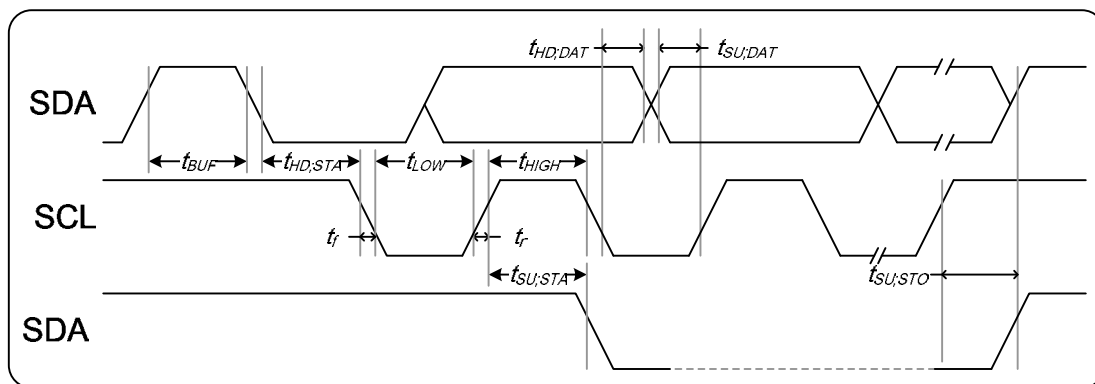


Fig. 35

(VDD1=3.3V, Ta=-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SDA	TSU;Data		100	-	ns
Data hold time	SDA	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SDA	TSU;SUA		0.6	-	us
Start condition hold time	SDA	THD;STA		0.6	-	us
Setup time for STOP condition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and START condition	SCL	TBUF		1.3		us

RESET TIMING

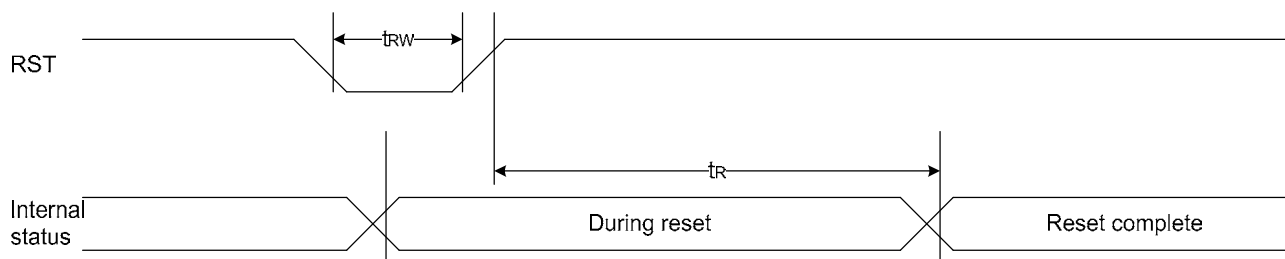


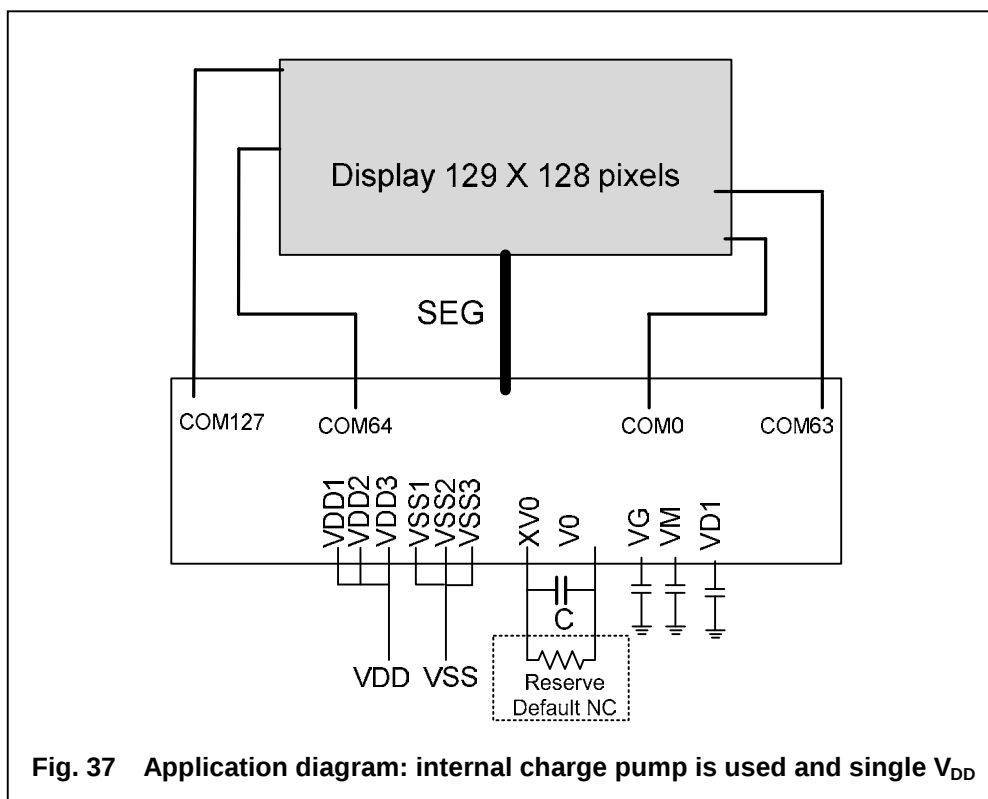
Fig. 36

(VDD1 = 1.8V~3.3V , Ta = -30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		120	—	—	ms
Reset “L” pulse width	RST	tRW		2.0	—	—	us

POWER PAD CONNECT

The pinning of the ST7571 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 129 X 128 pixels.

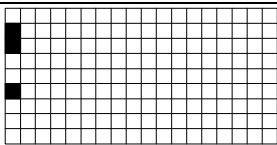
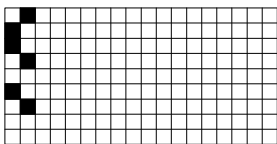
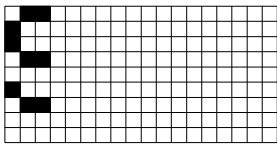


The required minimum value for the external capacitors in an application with the ST7571 are: $C = 1\mu F$.

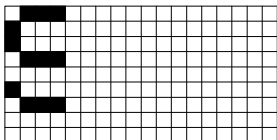
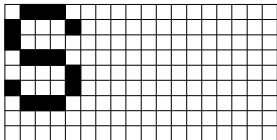
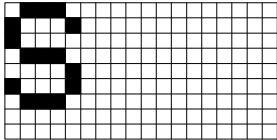
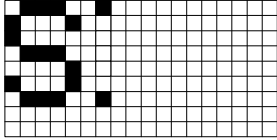
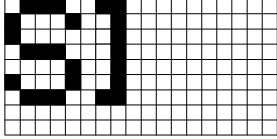
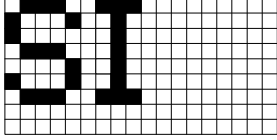
Higher capacitor values are recommended for ripple reduction.

APPLICATION Program Example

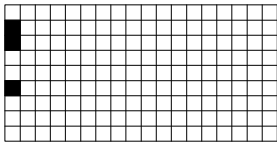
4-Gray programming example for ST7571

SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
0	Start		CSB IS going low.
1	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 x' 0		Mode Set. FR[3:0] = 0000 BE= 1
2	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 1 0 1 1		OSC ON
3.a	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 R2 R1 R0		Set Ra/Rb Set R[2:0]
3.b	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0 1 0 x' x' Ev5 Ev4 Ev3 Ev2 Ev1 Ev0		Set EV Set Ev[5:0]
3.c	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 1 0 B2 B1 B0		Set Bias Set B[2:0]
4	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 1 x' 0		Mode Set.
5.a	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 1 1 1 1		SET Power Control Booster ON Regulator ON Follower ON
5.b	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 1 1 1 1		Display control. Display on
6	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here...
7	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
8	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.

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9	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1		Data Write.
10	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 1 1 0 0 1 0 1 0 0 1 1 0 0 1 0		Data Write.
11	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.
12	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
13	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1		Data Write.
14	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 1		Data Write.
15	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 0 1 1 1		Display Control. Set Reverse display mode REV=1
16	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0		Set column address of RAM. Set address to "00000000". Y[7:0]=00000000 (Y0 default is 0)
17	A0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0		Data Write.

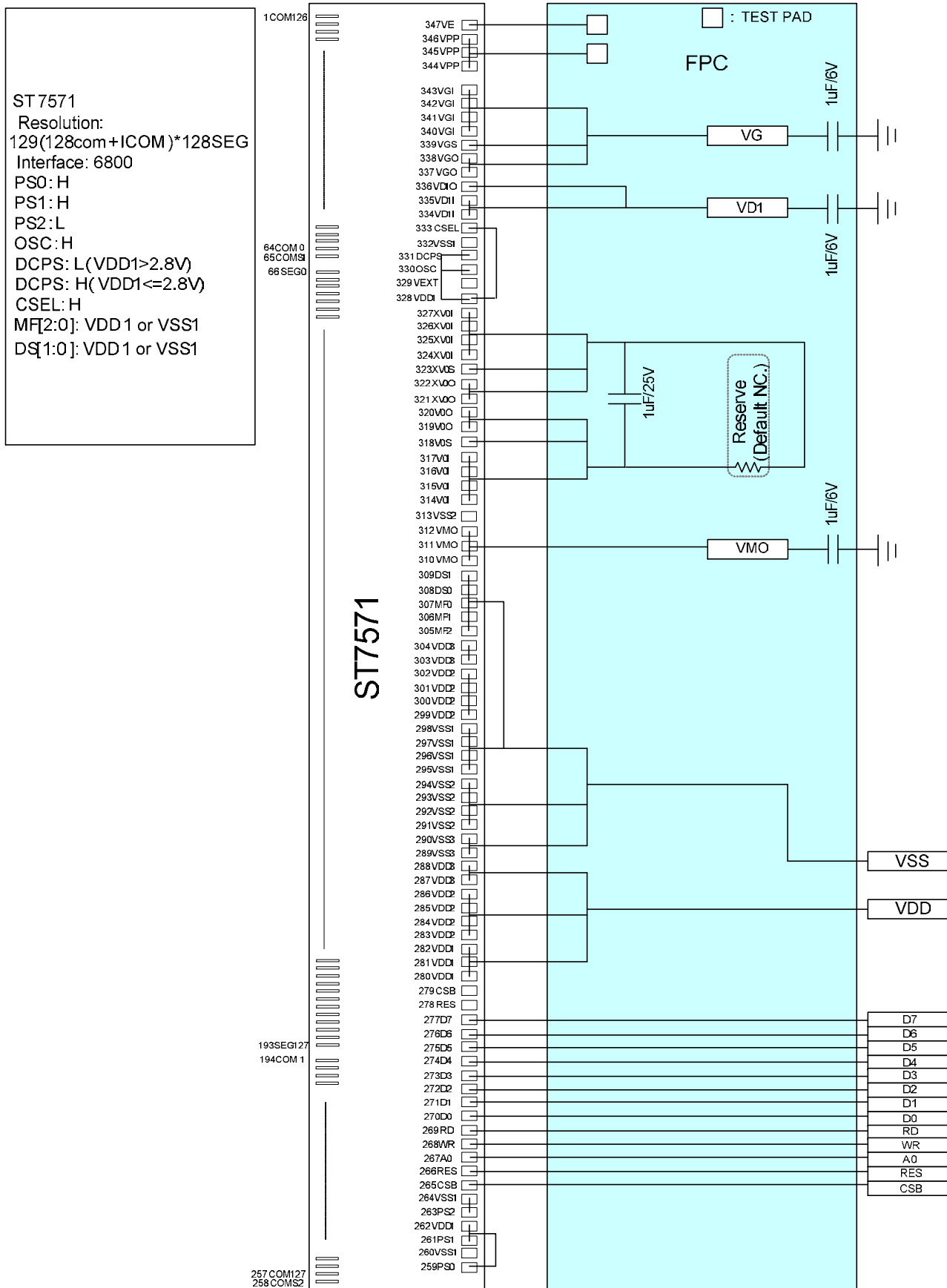
Programming example for ST7571(Use I²C Interface)

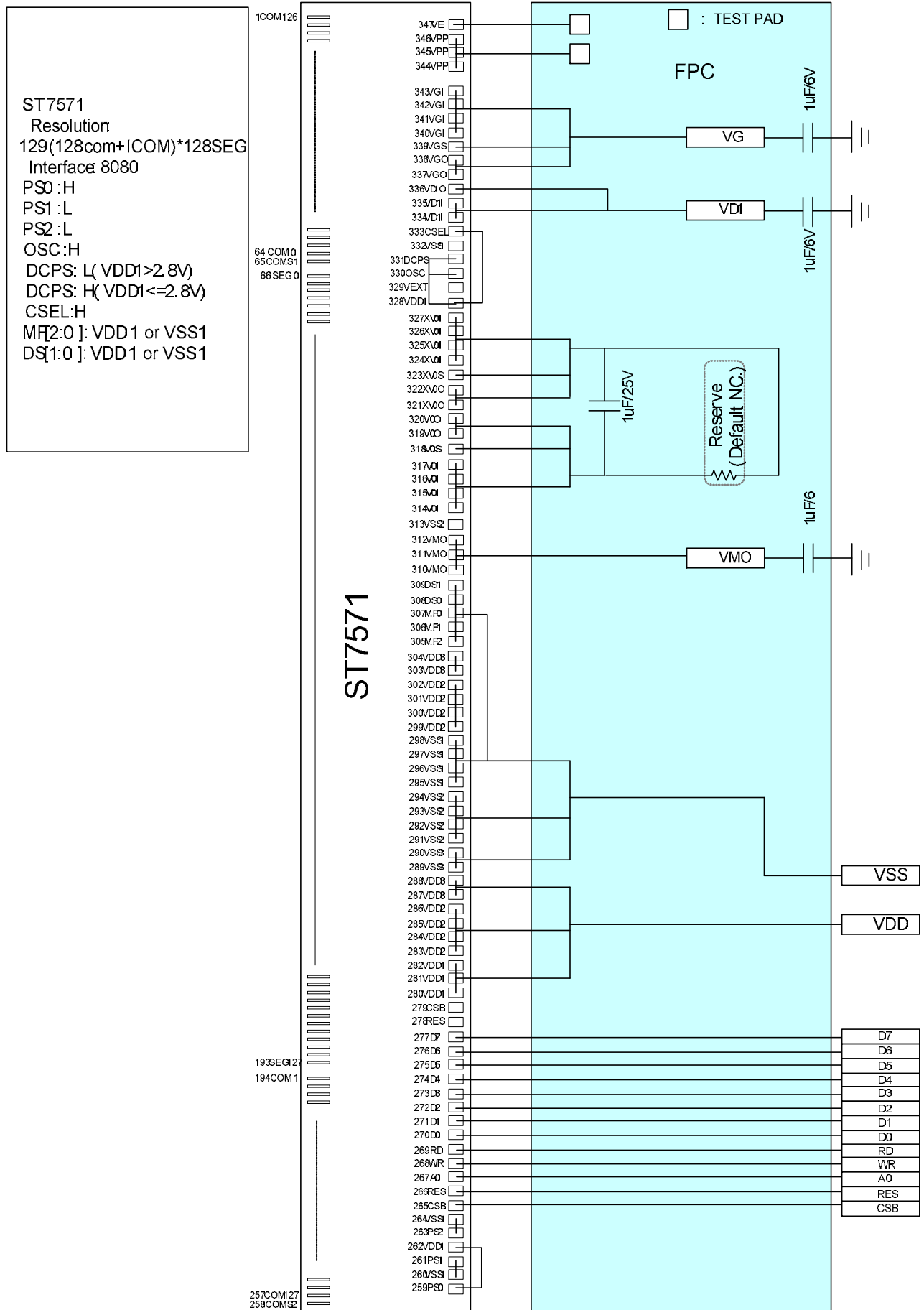
SETP	SERIAL BUS BYTE	DISPLAY	OPERATION
1	I ² C INTERFACE Start		
2	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
3	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0
4	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 0 0 0 0 0 0 0 1 0 x' 0		Mode Set. FR[3:0] = 0000 BE= 1
5	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 1 0 1 1		OSC ON
6.a	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 R2 R1 R0		Set Ra/Rb Set R[2:0]
6.b	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 1 x' x' Ev5 Ev4 Ev3 Ev2 Ev1 Ev0		Set EV Set Ev[5:0]
6.c	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 1 0 B2 B1 B0		Set Bias Set B[2:0]
7	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 0 0 0 0 0 0 0 0 1 x' 0		Mode Set.
8.a	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 1 1 1 1		SET Power Control Booster ON Regulator ON Follower ON
8.b	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 1 1 1 1		Display control. Display on
9	I ² C INTERFACE Start		restart
10	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
11	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 0		Control byte with clear Co bit and A0 set to logic 1
12	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 1 1 0 0 0 1 0 0 1 1 0		Data Write. Y,X are initialized to 0 by default, so they aren't set here...

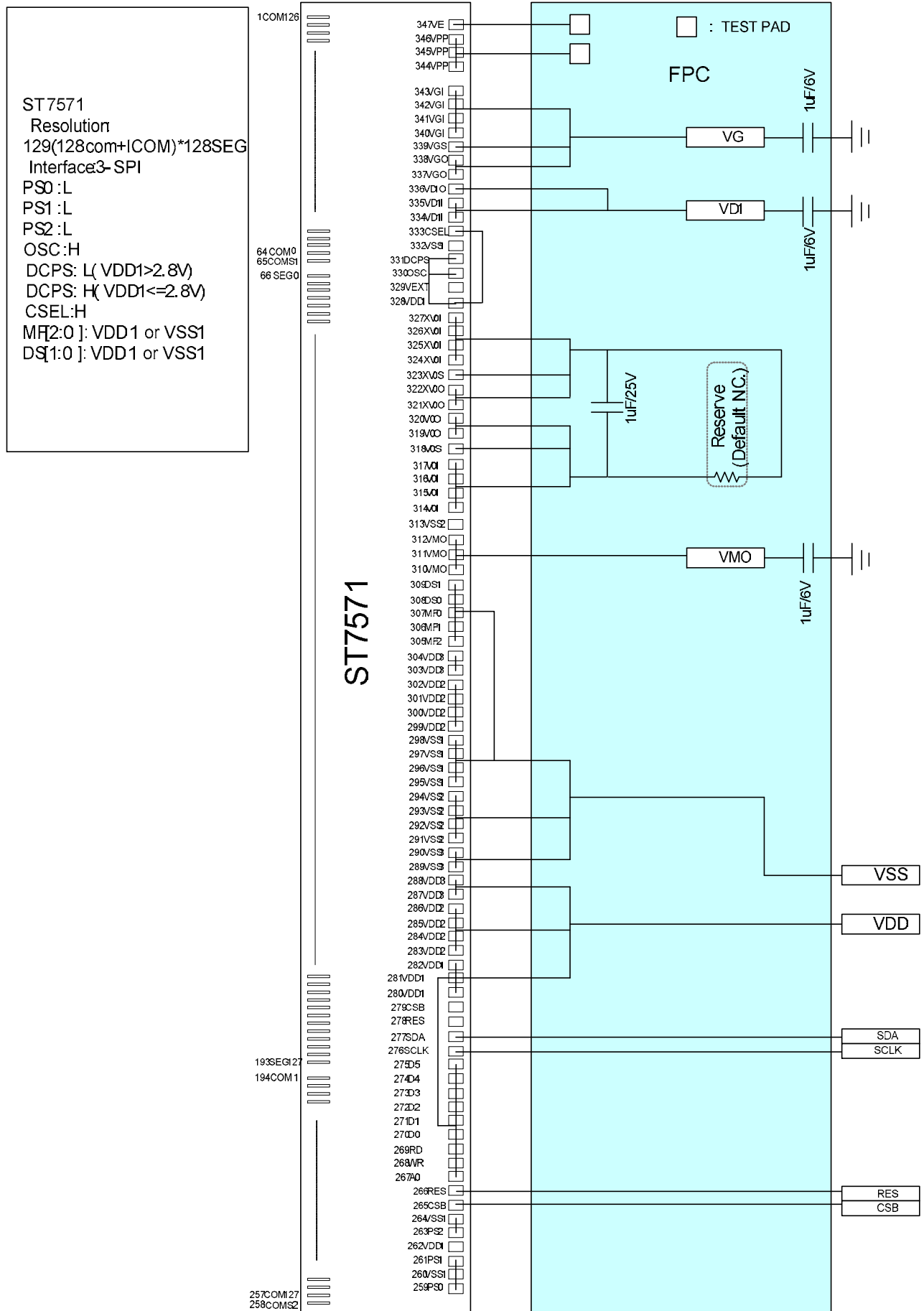
13	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
14	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
15	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1		Data Write.
16	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 0 0 1 0 0 0 1 1 0 0 1 0		Data Write.
17	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Data Write.
18	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1		Data Write.
19	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1		Data Write.
20	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1		Data Write.
21	I ² C INTERFACE start		restart
22	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
23	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0

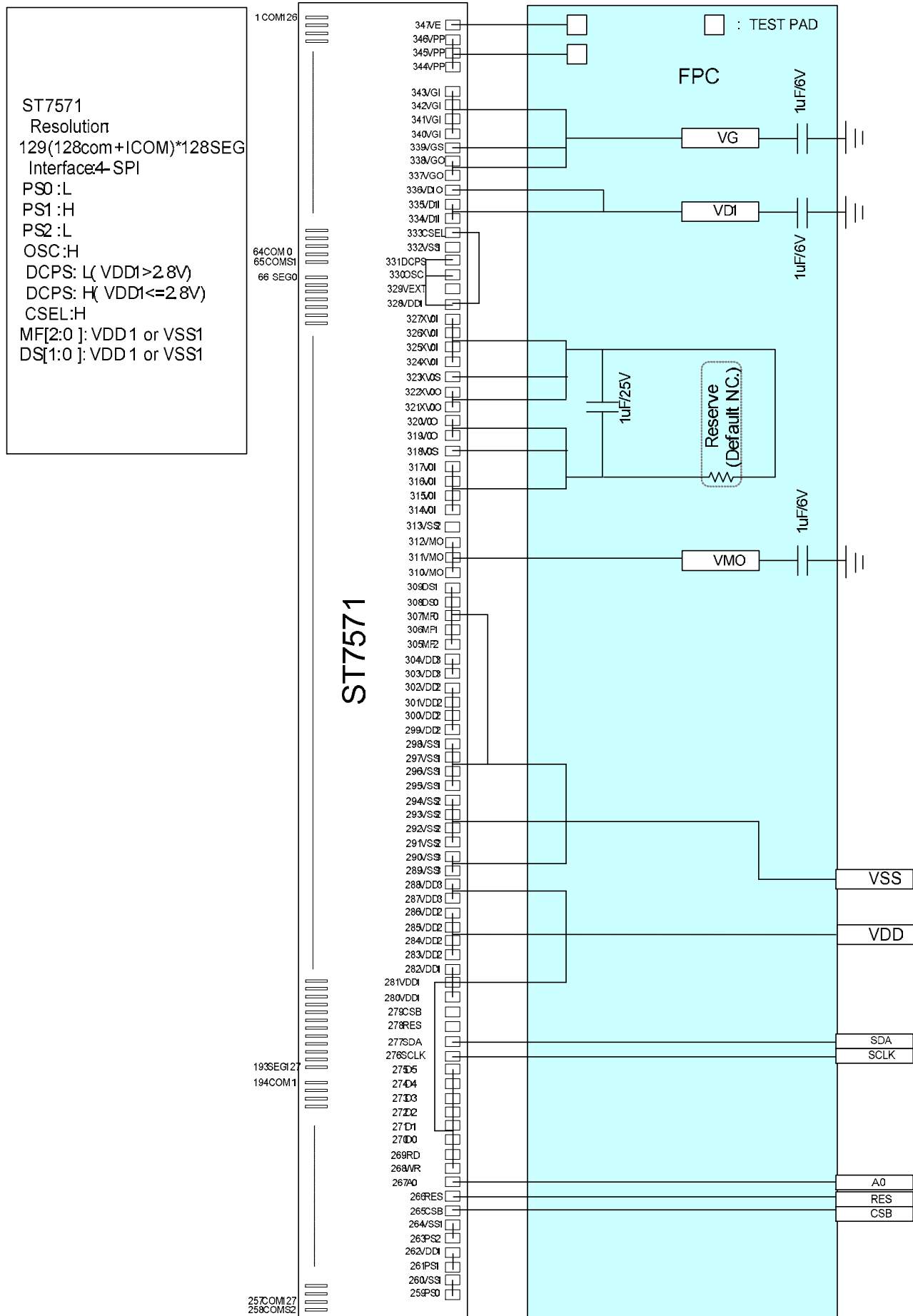
24	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 1 0 0 1 1 1		Display Control. Set Reverse display mode REV=1
25	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0
26	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0		Set column address of RAM. Set address to "00000000". Y[7:0]=00000000 (Y0 default is 00)
27	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 1 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 1
28	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Data Write.
29	I ² C INTERFACE start		restart
30	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		Slave address for write
31	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with set Co bit and A0 set to logic 0
32	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Set X address of RAM. Set address to "00000000".
33	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 1 0 0 0 0 0 0 0		Control byte with cleared Co bit and A0 set to logic 0

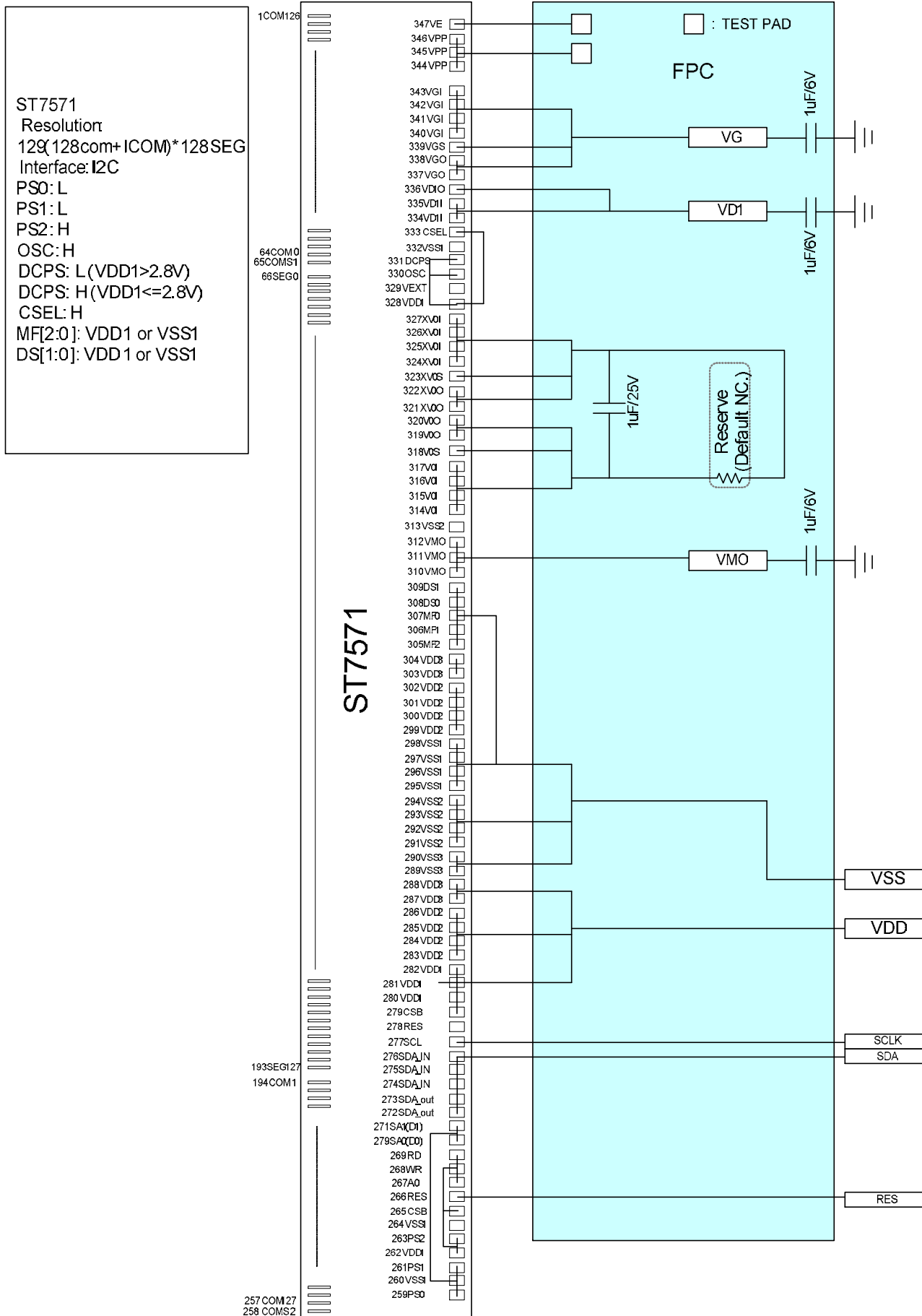
APPLICATION NOTES :











ST7571 Specification Revision History		
Version	Date	Description
0.1	2007/02/08	1. Added Pad Arrangement 2. Added Pad Center Coordinates 3. Added Application notes
0.2	2007/3/15	1. Modified Pad Center Coordinates PAD No.351~354
0.3	2007/8/2	1. Modify the description about un-used pins of serial interface 2. Correct the VE pin status, when writing the EE. 3. Add EE writing flow.
0.4	2007/10/30	1. Remove some dummy commands 2. Add 2 test commands 3. Correct description for CSEL
1.0	2008/01/29	1. Remove TBD. 2. Add DCPS and COMMON reference circuit 3. Add some commands for burning EE in command table. 4. Modify the power consumption current for N-Line=1 condition. 5. Reserve read function
1.1	2008/04/02	1. Remove CSL=L setting. 2. Modify Application note 3. Add Initial code 4. Modify ITO layout reference 5. Modify 9.1.14 entire display
1.2	2008/08/08	1. Re-arrange sections for document format issue. 2. Remove one of the Power OFF flow (not easy control by customer). 3. Update recommend N-Line setting as 12-line (0x0A). 4. Rewrite some description for easy understanding and grammar issue. 5. Fix wrong Limiting Values. 6. Rewrite DC Characteristics section. Separate Internal Power Application Note for detailed description. 7. Modify Recommend LCD Vop Setting: use same bias for easy use.