ER-OLED0.83-1Series

OLED Display Datasheet

EastRising Technology Co., Limited

Attention:

A. Some specifications of IC are not listed in this datasheet. Please refer to the IC datasheet for more details.

B. The related documents for interfacing, demo code, ic datasheet are all available, please download from www.buydisplay.com.

C. Please pay more attention to “Quality Control” in this Datasheet. We assume you already agree with these criterions when you place an order with us. No more recommendations.

REV	DESCRIPTION	RELEASE DATE
1.0	Preliminary Release	May-02-2010

ORDERING INFORMATION

Order Number

Part Number(Order Number)	Description
ER-OLED0.83-1W	0.83”OLED Display Module in White Color
ER-OLED0.83-1B	0.83”OLED Display Module in Blue Color
ER-DBO0.83-1	Testing or Demo Board for ER-OLED0.83-1 Series Products

Image

↑ ER-OLED0.83-1W

↑ ER-OLED0.83-1B

Contents

1. Basic Specifications

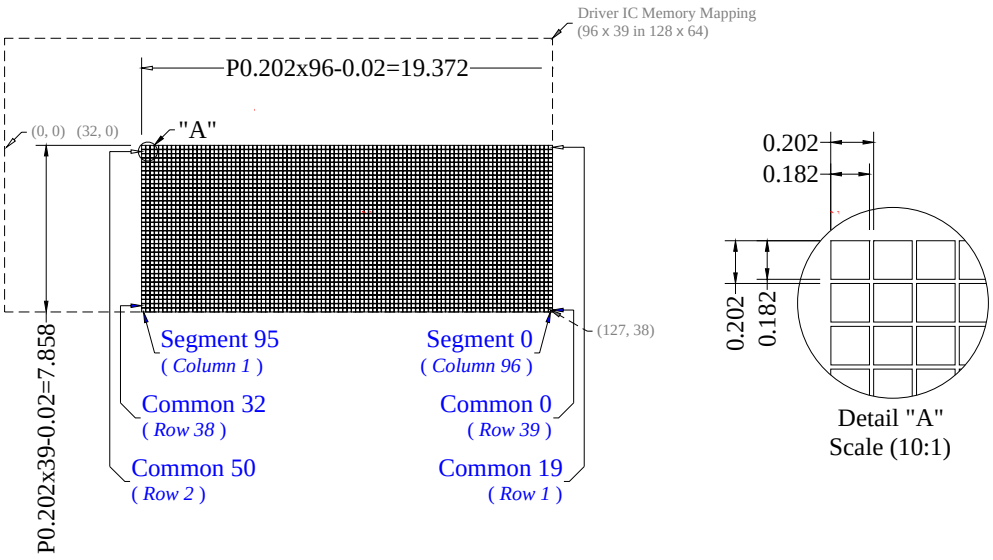
1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: Monochrome (Blue and White)
3) Drive Duty: 1/39 Duty

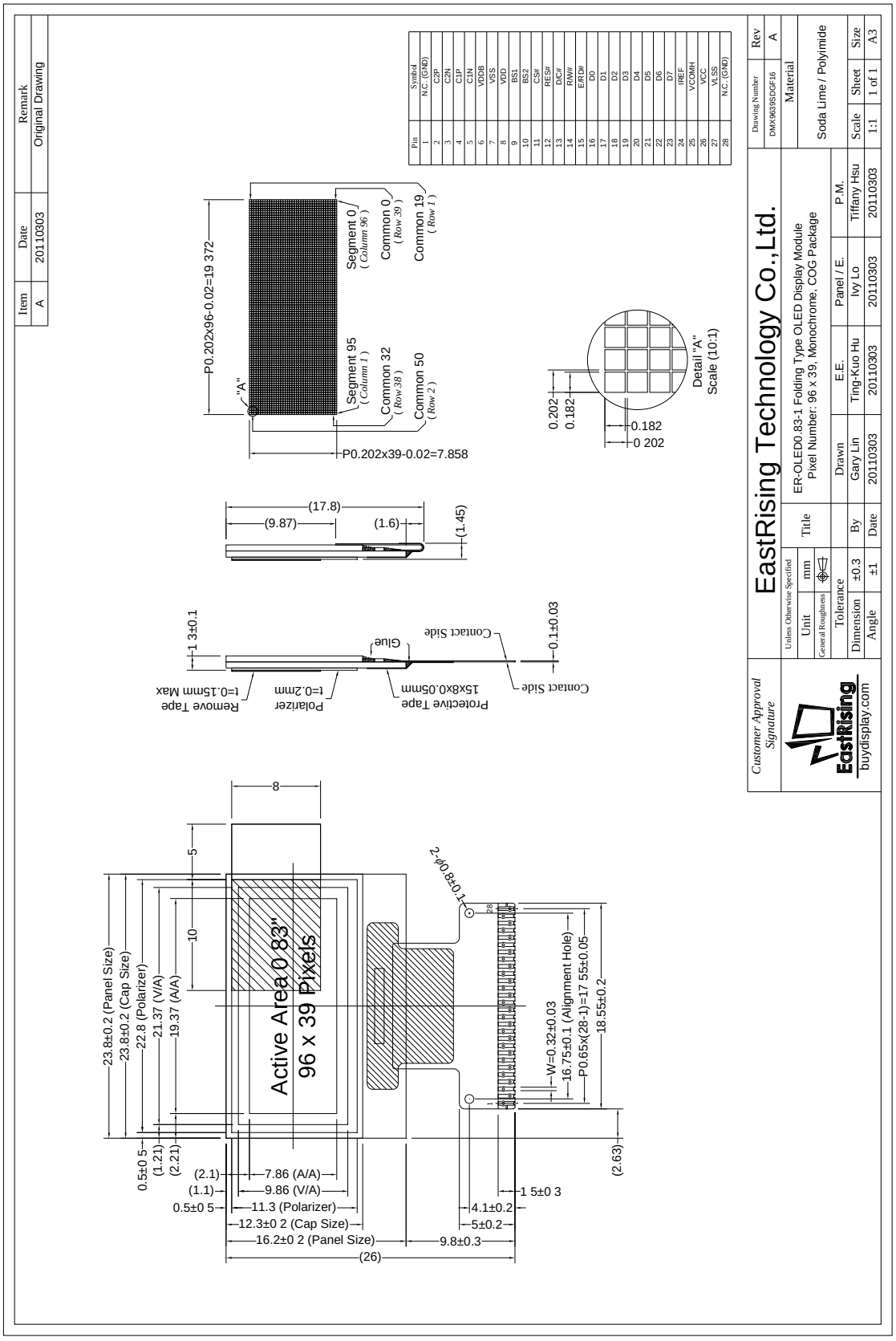
1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 96 × 39
3) Panel Size: 23.80 × 16.20 × 1.30 (mm)
4) Active Area: 19.372 × 7.858 (mm)
5) Pixel Pitch: 0.202 × 0.202 (mm)
6) Pixel Size: 0.182 × 0.182 (mm)
7) Weight: 0.99 (g)

1.3 Active Area / Memory Mapping & Pixel Construction



1.4 Mechanical Drawing



1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
8	VDD	P	**Power Supply for Logic** This is a voltage supply pin. It must be connected to external source.
7	VSS	P	**Ground of Logic Circuit** This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
26	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V_{SS} when the converter is used. It must be connected to external source when the converter is not used.
27	VLSS	P	**Ground of Analog Circuit** This is an analog ground pin. It should be connected to V_{SS} externally.
Driver			
24	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 12.5μA maximum.
25	VCOMH	O	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.
DC/DC Converter			
6	VDDB	P	**Power Supply for DC/DC Converter Circuit** his is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to V_{DD} when the converter is not used.
4 / 5 2 / 3	C1P / C1N C2P / C2N	I	**Positiv Terminal of the Flying Inverting Capacitor** **Negative Terminal of the Flying Boost Capacitor** The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
Interface			
9 10	BS1 BS2	I	**Communicating Protocol Select** These pins are MCU interface selection input. See the following table:

	BS1	BS2
I^2C	1	0
4-wire SPI	0	0
8-bit 68XX Parallel	0	1
8-bit 80XX Parallel	1	1

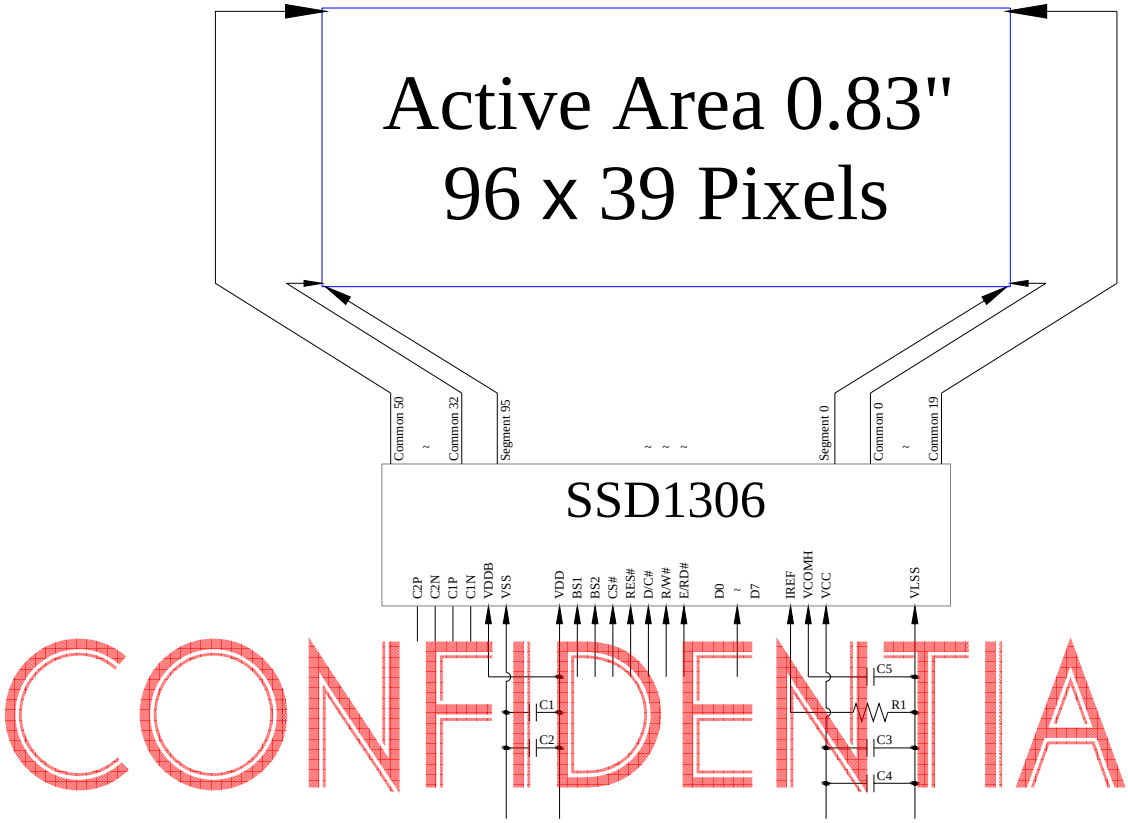
12	RES#	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed.
11	CS#	I	**Chip Select** This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
13	D/C#	I	**Data/Command Control** This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection.
15	E/RD#	I	**Read/Write Enable or Read** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
14	R/W#	I	**Read/Write Select or Write** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
16~23	D0~D7	I/O	**Host Data Input/Output Bus** These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I^2C mode is selected, D2 & D1 should be tired together and serve as SDA_{out} & SDA_{in} in application and D0 is the serial clock input SCL.
Reserve			
1, 28	N.C. (GND)	-	**Reserved Pin (Supporting Pin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

1.6 Block Diagram

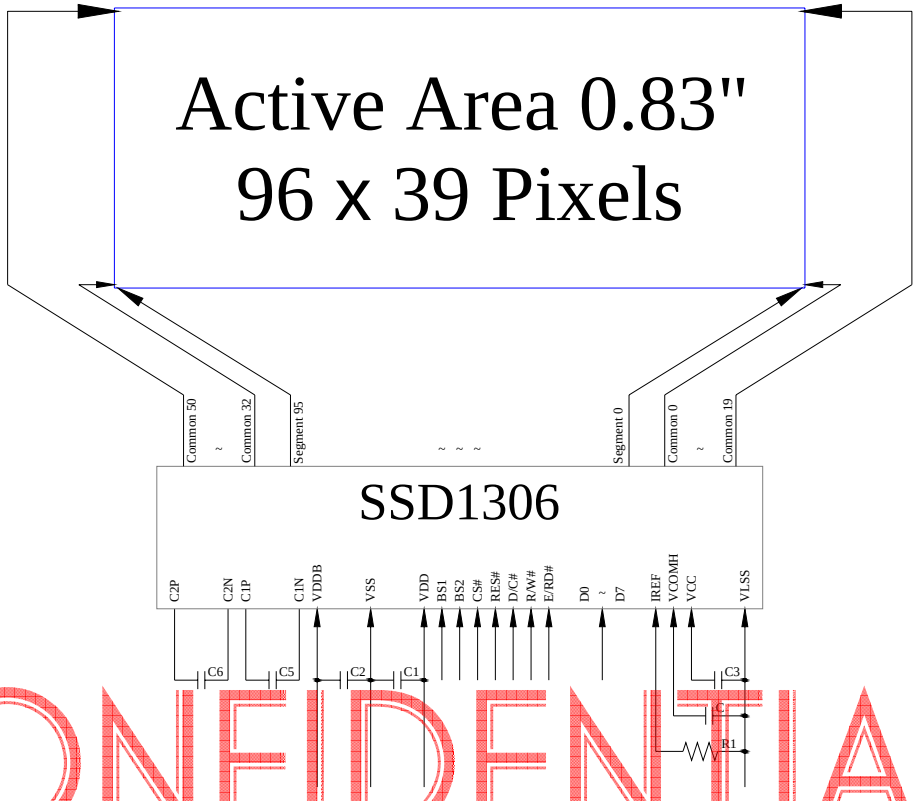
1.6.1 V_{CC} Supplied Externally



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C3: 0.1μF
C2: 2.2μF
C4, C5: 4.7μF / 16V, X7R
R1: 390kΩ, R1 = (Voltage at IREF - VSS) / IREF

1.6.2 V_{CC} Generated by Internal DC/DC Circuit



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C2: 1µF
C3: 2.2µF
C4: 4.7µF / 16V X7R
C5, C6: 1µF / 16V X5R
R1: 390kΩ, R1 = (Voltage at IREF - VSS) / IREF

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	11	V	1, 2
Supply Voltage for DC/DC	*V_{DDB}*	*-0.3*	*5*	*V*	*1, 2*
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	80	°C	
Life Time (100 cd/m^2)		10,000	-	hour	3

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: V_{CC} = 7.25V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 4	80	100	-	cd/m^2
C.I.E. (Blue)	(x) (y)	C.I.E. 1931	0.12 0.22	0.16 0.26	0.20 0.30	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 7.25V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 4 (Internal DC/DC Disable)	7.0	7.25	7.5	V
Supply Voltage for DC/DC	*V_{DDB}*	*Internal DC/DC Enable*	*3.3*	-	*4.2*	*V*
Supply Voltage for Display (Generated by Internal DC/DC)	*V_{CC}*	*Note 4 (Internal DC/DC Enable)*	*7.0*	-	*7.5*	*V*
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 5	-	2.3	2.9	mA
		Note 6	-	3.6	4.5	mA
		Note 7	-	7.2	9.0	mA
Operating Current for V_{DDB} (V_{CC} Generated by Internal DC/DC)	*I_{DDB}*	*Note 5*	*-*	*6.9*	*8.6*	*mA*
		Note 6	*-*	*10.9*	*13.6*	*mA*
		Note 7	*-*	*20.8*	*26.0*	*mA*
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

Note 4: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 5: V_{DD} = 2.8V, V_{CC} = 7.25V, 30% Display Area Turn on.
Note 6: V_{DD} = 2.8V, V_{CC} = 7.25V, 50% Display Area Turn on.
Note 7: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.

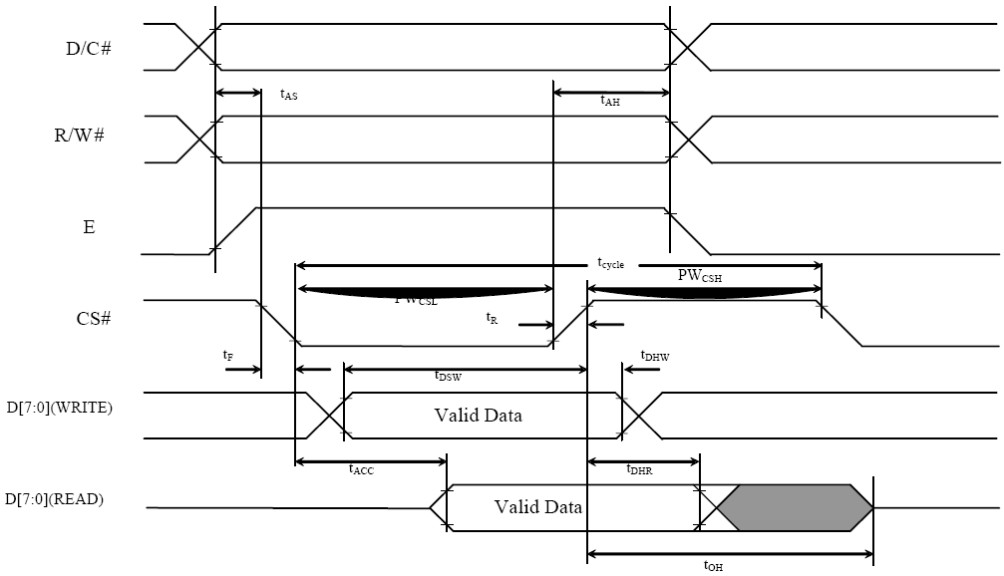
* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

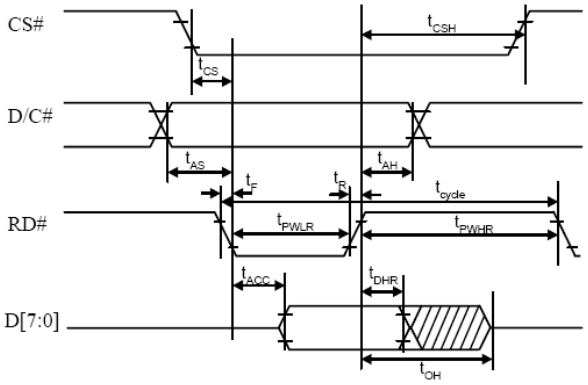
* (V_{DD} - V_{SS} = 1.65V to 3.3V T_a = 25°C)



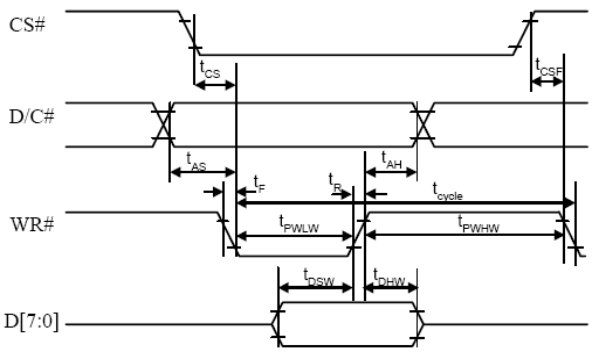
3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



(***Read Timing***)

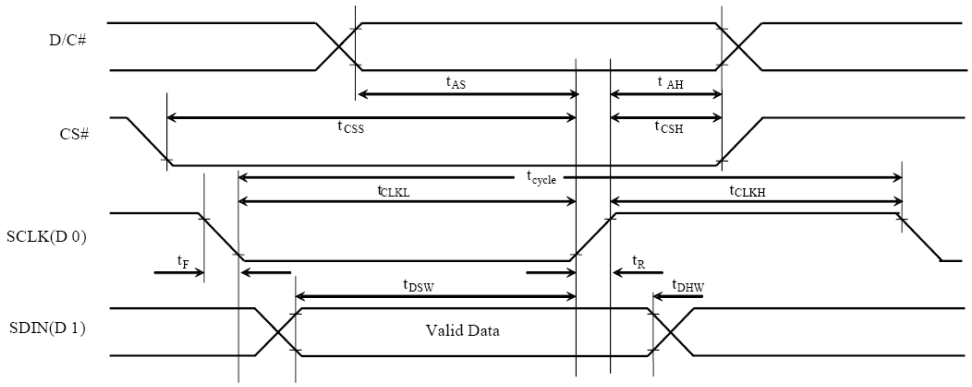


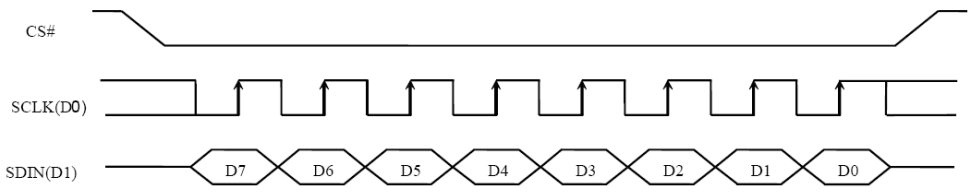
(***Write Timing***)

3.3.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

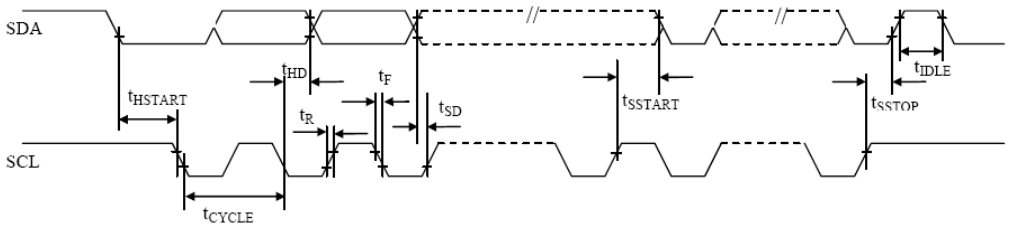




3.3.4 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	µs
t_{HSTART}	Start Condition Hold Time	0.6	-	µs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	µs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	µs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	µs

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



4. Functional Specification

4.1 Commands

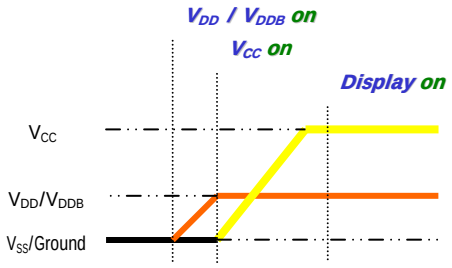
Refer to the Technical Manual for the SSD1306

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

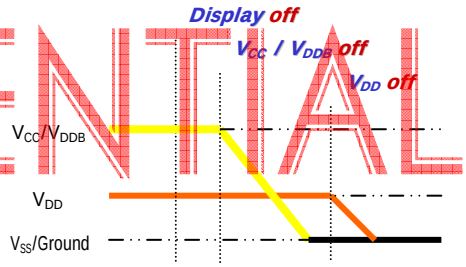
4.2.1 Power up Sequence:

1. Power up V_{DD} / V_{DDB}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC} / V_{DD}
3. Delay 100ms
   (When V_{CC} / V_{DDB} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 8:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} / V_{DDB} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}, V_{DDB}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} / V_{DDB} power down.

4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

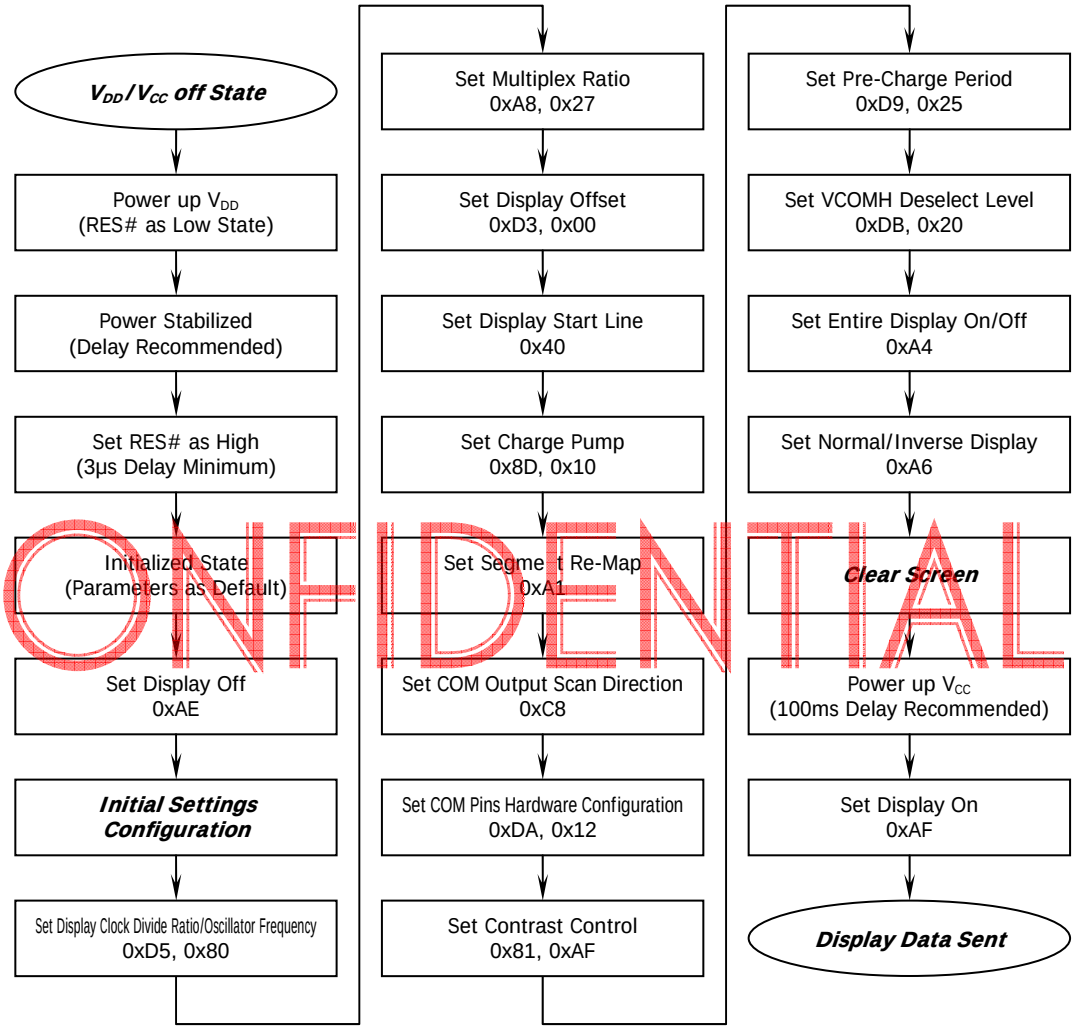
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

4.4 Actual Application Example

Command usage and explanation of an actual example

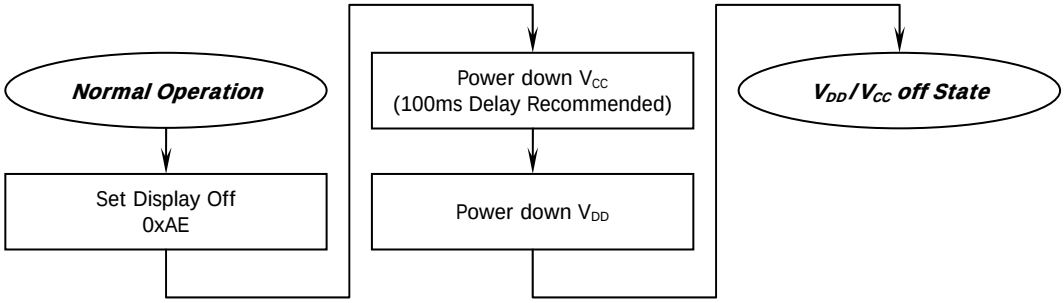
4.4.1 V_{CC} Supplied Externally

<Power up Sequence>

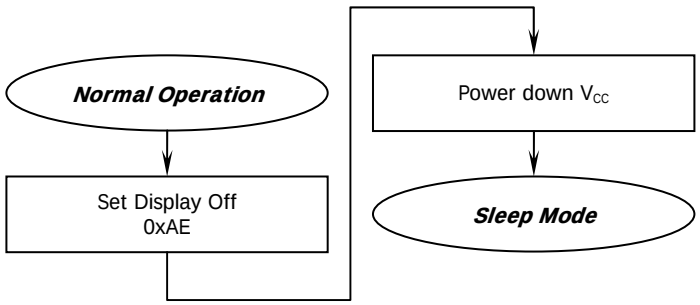


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

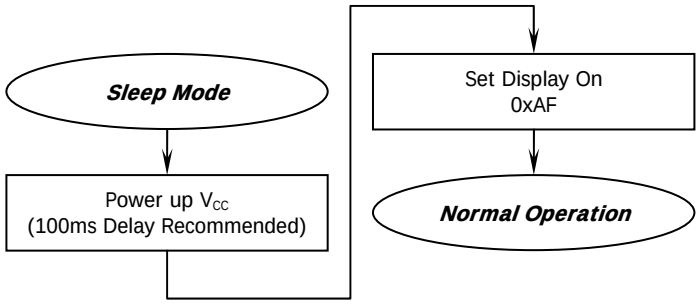
<Power down Sequence>



<Entering Sleep Mode>

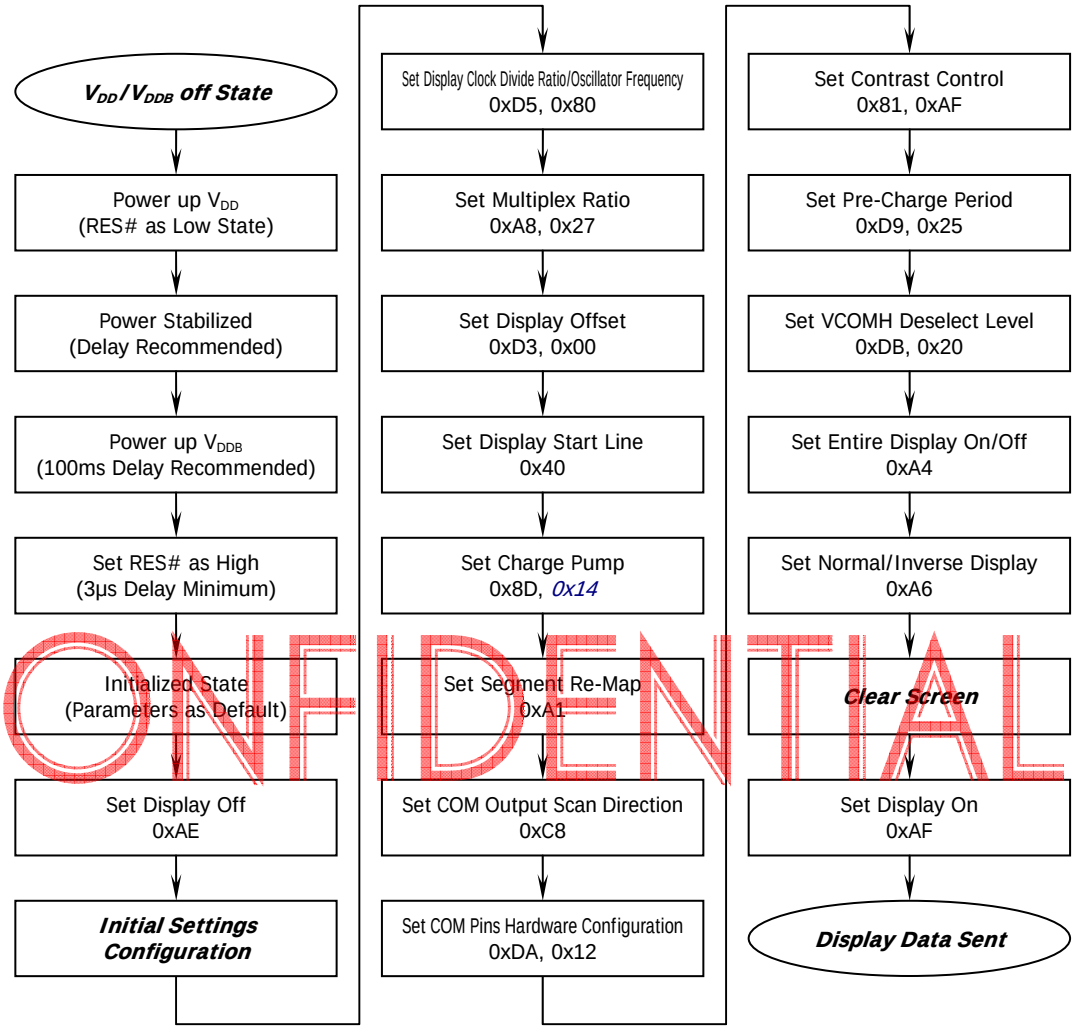


<Exiting Sleep Mode>



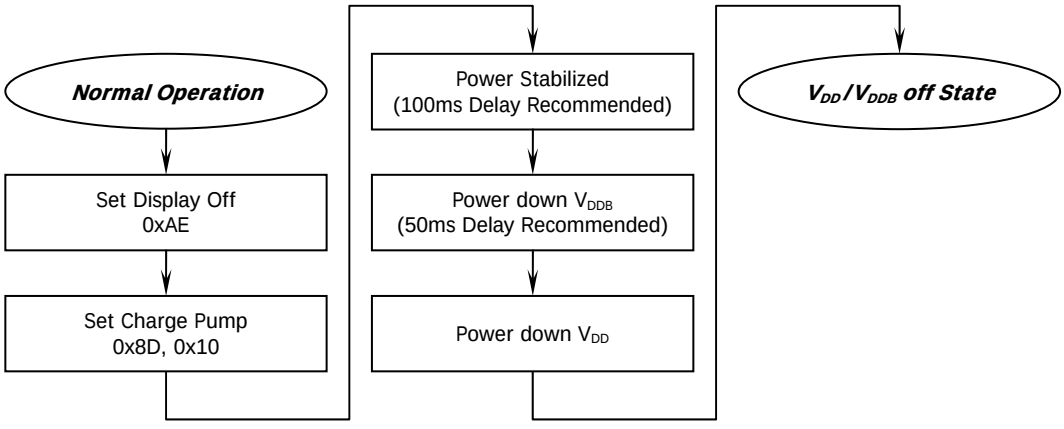
4.4.2 V_{CC} Generated by Internal DC/DC Circuit

<Power up Sequence>

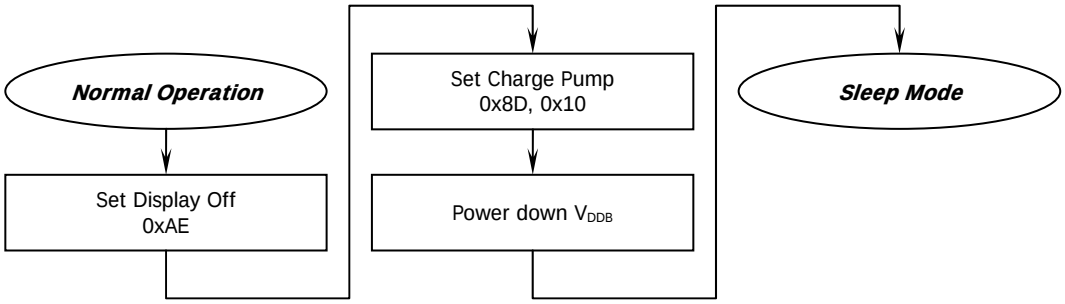


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

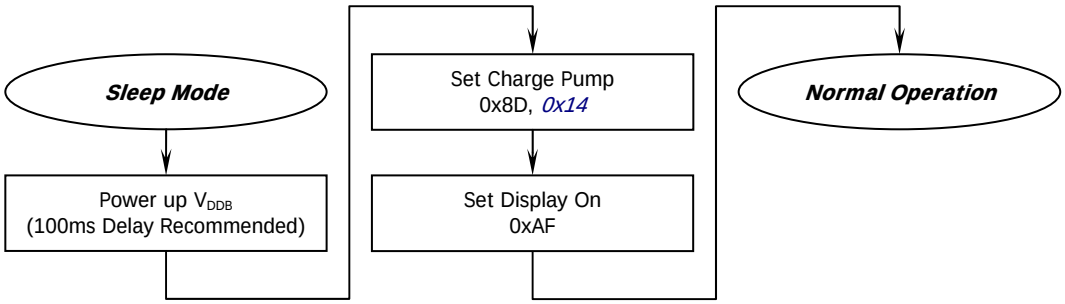
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



5. QUALITY CONTROL

5.1 EastRising Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature: 23±5℃

Humidity: 55±15% RH

Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥50cm

Distance between the Panel & Eyes of the Inspector: ≥30cm

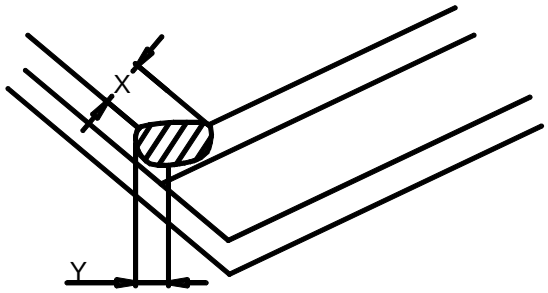
Finger glove (or finger cover) must be worn by the inspector.

Inspection table of jig must be anti-electrostatic.

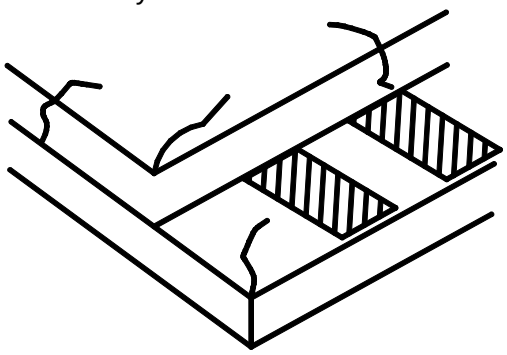
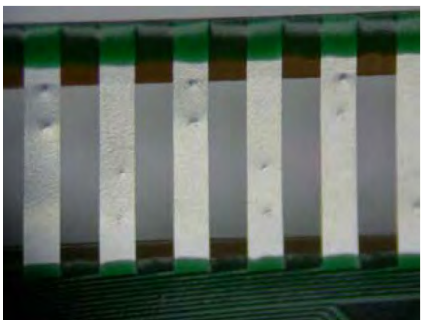
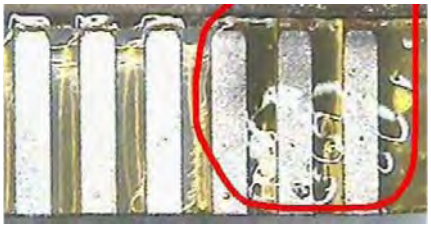
5.2 EastRising OLED Display Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

5.2.1 EastRising Cosmetic Check (Display Off) in Non-Active Area

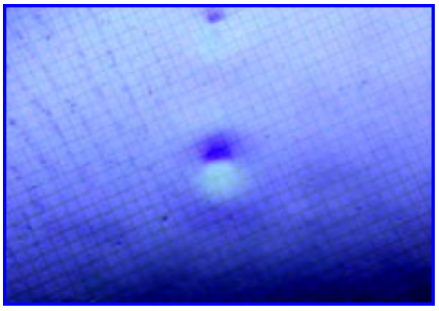
Check Item	Classification	Criteria
Panel General Chipping	Minor	X>6mm (Along with Edge) Y>1mm (Perpendicular to edge) 

5.2.2 EastRising Cosmetic Check (Display Off)in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Termial Lead Prober Mark	Acceptable	
Glue or Contamination on Pin	Minor	
Ink marking on Back Side of Panel (Exclude on Film)	Acceptable	Ignore for Any

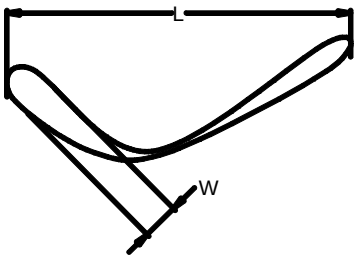
5.2.3 EastRising Cosmetic Check (Display Off) in Active Area

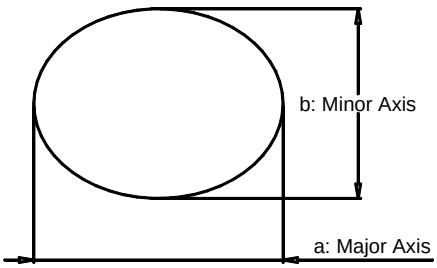
EastRising recommends to execute in clear environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches,Fiber,Line-Shape Defect (On Polarizer)	Minor	W≤0.1 Ignore W>0.1 L≤2 n≤1 L>2 n=0
Dirt, Black Spot, Foreign Material (On Polarizer)	Minor	Φ≤0.1 Ignore 0.1<Φ≤0.25 n≤1 0.25<Φ n=0
Dent,Bubbles,White Spot (Any Transparent Spot on Polarizer)	Minor	Φ≤0.5 Ignore if no Influence on Display 0.5<Φ n=0 
Fingerpint ,Flow Mark (On Polarizer)	Minor	Not Allowable

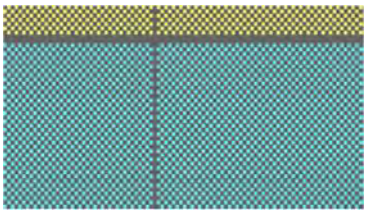
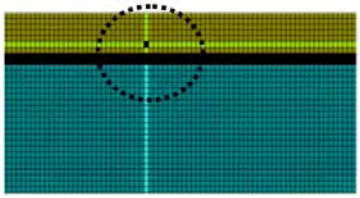
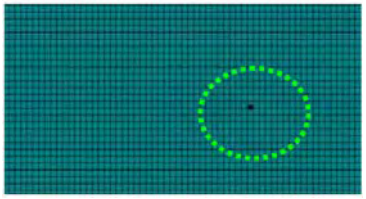
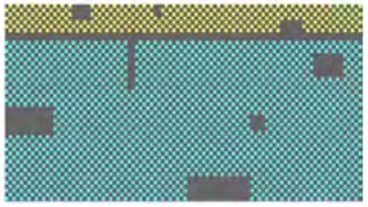
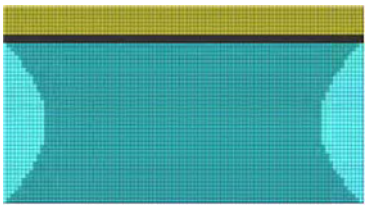
* Protective film should not be tear off when cosmetic check.

* Definition of W & L &Φ(Unit:mm): Φ=(a+b)/2





5.2.4 EastRising Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

6.PRECAUTIONS for USING

6.1 Handling Precautions

1) Since the EastRiisng OLED display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.

2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.

3) If pressure is applied to the display surface or its neighborhood of the EastRising OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.

4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.

5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
* Scotch Mending Tape No. 810 or an equivalent
Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy. Also, pay attention that the following liquid and solvent may spoil the polarizer:
* Water
* Ketone
* Aromatic Solvents

6) Hold EastRising OLED display module very carefully when placing OLED display module into the system housing. Do not apply excessive stress or pressure to OLED display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.

7) Do not apply stress to the driver IC and the surrounding molded sections.

8) Do not disassemble nor modify the OLED display module.

9) Do not apply input signals while the logic power is off.

10) Pay sufficient attention to the working environments when handing EastRising OLED display modules to prevent occurrence of element breakage accidents by static electricity.
* Be sure to make human body grounding when handling OLED display modules.
* Be sure to ground tools to use or assembly such as soldering irons.
* To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

* Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the EastRising OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

6.2 Storage Precautions

1) When storing EastRising OLED display modules, put them in static electricity preventive bags avoiding exposure neither to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high
humidity environment or low temperature (less than 0℃) environments. (We recommend you to store these modules in the packaged state when they were shipped from EastRising.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

6.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.

2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.

3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)

4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.

5) As for EMI, take necessary measures on the equipment side basically.

6) When fastening the OLED display module, fasten the external plastic housing section.

7) If power supply to the EastRising OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.

6.4 Precautions when disposing of the EastRising OLED display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

6.5 Other Precautions

1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC

3) With this OLED display module, the OLED driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.

4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

That's the end of the datasheet.